

## 5 VOLT FlashFile™ MEMORY

28F160S5 and 28F320S5 (x8/x16)

- **Two 32-Byte Write Buffers**
  - 2  $\mu$ s per Byte Effective Programming Time
- **Operating Voltage**
  - 5 V  $V_{CC}$
  - 5 V  $V_{PP}$
- **70 ns Read Access Time (16 Mbit)**  
**90 ns Read Access Time (32 Mbit)**
- **High-Density Symmetrically-Blocked Architecture**
  - 32 64-Kbyte Erase Blocks (16 Mbit)
  - 64 64-Kbyte Erase Blocks (32 Mbit)
- **System Performance Enhancements**
  - STS Status Output
- **Industry-Standard Packaging**
  - SSOP and TSOP (16 and 32 Mbit)
  - SSOP (32 Mbit)
- **Cross-Compatible Command Support**
  - Intel Standard Command Set
  - Common Flash Interface (CFI)
  - Scaleable Command Set (SCS)
- **Block Erase Cycles**
  - 100,000 at 0 °C to +70 °C (Commercial)
  - 10,000 at -40 °C to +85 °C (Extended)
- **Enhanced Data Protection Features**
  - Absolute Protection with  $V_{PP} = GND$
  - Flexible Block Locking
  - Block Erase/Program Lockout during Power Transitions
- **Configurable x8 or x16 I/O**
- **Automation Suspend Options**
  - Program Suspend to Read
  - Block Erase Suspend to Program
  - Block Erase Suspend to Read
- **ETOX™ V Nonvolatile Flash Technology**

Intel® 5 Volt FlashFile™ memory provides high-density, low-cost, nonvolatile, read/write storage solutions for a wide range of applications. The 5 Volt FlashFile memories are available at various densities in the same package type. Their symmetrically-blocked architecture, voltage, and extended cycling provide highly flexible components suitable for resident flash arrays, SIMMs, and memory cards. Enhanced suspend capabilities provide an ideal solution for code or data storage applications. For secure code storage applications, such as networking, where code is either directly executed out of flash or downloaded to DRAM, the 5 Volt FlashFile memory offers three levels of protection: absolute protection with  $V_{PP}$  at GND, selective block locking, and program/erase lockout during power transitions. These alternatives give designers ultimate control of their code security needs.

This family of products is manufactured on Intel® 0.4  $\mu$ m ETOX™ V process technology. It comes in the industry-standard 56-lead SSOP. In addition, the 16-Mb device is available in the industry-standard 56-lead TSOP package.

**NOTE:** This document formerly known as *Word-Wide FlashFile™ Memory Family 28F160S5, 28F320S5*.

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# CONTENTS

PAGE	PAGE
<b>1.0 INTRODUCTION .....</b>	<b>5</b>
1.1 New Features.....	5
1.2 Product Overview.....	5
1.3 Pinout and Pin Description.....	6
<b>2.0 PRINCIPLES OF OPERATION .....</b>	<b>9</b>
2.1 Data Protection .....	10
<b>3.0 BUS OPERATION.....</b>	<b>10</b>
3.1 Read .....	10
3.2 Output Disable .....	11
3.3 Standby.....	11
3.4 Deep Power-Down .....	11
3.5 Read Query Operation .....	11
3.6 Read Identifier Codes Operation .....	11
3.7 Write .....	12
<b>4.0 COMMAND DEFINITIONS .....</b>	<b>12</b>
4.1 Read Array Command.....	16
4.2 Read Query Mode Command.....	16
4.2.1 Query Structure Output .....	16
4.2.2 Query Structure Overview .....	18
4.2.3 Block Status Register .....	19
4.2.4 CFI Query Identification String.....	20
4.2.5 System Interface Information.....	21
4.2.6 Device Geometry Definition.....	22
4.2.7 Intel-Specific Extended Query Table .....	23
4.3 Read Identifier Codes Command .....	24
4.4 Read Status Register Command.....	24
4.5 Clear Status Register Command.....	25
4.6 Block Erase Command .....	25
4.7 Full Chip Erase Command .....	25
4.8 Write to Buffer Command.....	26
4.9 Byte/Word Program Command.....	26
4.10 STS Configuration Command.....	27
4.11 Block Erase Suspend Command.....	27
4.12 Program Suspend Command .....	27
4.13 Set Block Lock-Bit Command .....	28
4.14 Clear Block Lock-Bits Command .....	28
<b>5.0 DESIGN CONSIDERATIONS .....</b>	<b>38</b>
5.1 Three-Line Output Control.....	38
5.2 STS and WSM Polling.....	38
5.3 Power Supply Decoupling .....	38
5.4 V <sub>PP</sub> Trace on Printed Circuit Boards.....	38
5.5 V <sub>CC</sub> , V <sub>PP</sub> , RP# Transitions.....	38
5.6 Power-Up/Down Protection .....	38
<b>6.0 ELECTRICAL SPECIFICATIONS.....</b>	<b>39</b>
6.1 Absolute Maximum Ratings.....	39
6.2 Operating Conditions.....	39
6.3 Capacitance .....	40
6.4 DC Characteristics .....	40
6.5 AC Characteristics—Read-Only Operations.....	44
6.6 AC Characteristics—Write Operations.....	46
6.7 Erase, Write, and Lock-Bit Configuration Performance.....	49
<b>7.0 ORDERING INFORMATION.....</b>	<b>50</b>
<b>8.0 ADDITIONAL INFORMATION .....</b>	<b>51</b>

## REVISION HISTORY

Number	Description
-001	Original version
-002	<p>Added commercial temperature information throughout the document.</p> <p>Updated address in Figure 5.</p> <p>Added descriptive information for CFI query to Section 4.2.5, <i>System Interface Information</i></p> <p>Updated addresses and added descriptive information in Table 9 and Table 10.</p> <p>Corrected documentation errors in Table 15 and Table 16.</p> <p>Updated Figure 6. Modified decision diamond for checking counter.</p> <p>Corrected documentation errors in Figure 11 and Figure 12.</p> <p>Updated Table 19 to include commercial and extended temperature range specifications.</p> <p>Updated note 4 in Table 19 for clarification.</p> <p>Updated Table 20 to show 16 Mb/32 Mb specifications more clear and corrected documentation error.</p> <p>Corrected documentation error in Figure 17 and Table 23.</p> <p>Updated package designators and order codes in Appendix A.</p>
-003	Corrected error in datasheet designator
-004	<p>Added Max values for Erase, Write, and Lock-Bit performance, Section 6.7.</p> <p>Corrected Figure 11, Comments section from "Data = D0H" to "Data = 01H."</p> <p>Added Table 18 to reflect de-rated read performance specifications.</p> <p>Name of document changed from <i>Word-Wide FlashFile™ Memory Family 28F160S5, 28F320S5</i>.</p>

## 1.0 INTRODUCTION

This datasheet contains 5 Volt FlashFile™ memory (28F160S5, 28F320S5) specifications. Section 1.0 provides a flash memory overview. Sections 2.0 through 5.0 describe the memory organization and functionality. Section 6.0 covers electrical specifications for extended temperature product offerings. Finally, Section 7.0 provides ordering and reference information.

### 1.1 New Features

The 5 Volt FlashFile memory family maintains basic compatibility with Intel's 28F016SA and 28F016SV. Key enhancements include:

- Common Flash Interface (CFI) Support
- Scaleable Command Set (SCS) Support
- Enhanced Suspend Capabilities

They share a compatible status register, basic software commands, and pinout. These similarities enable a clean migration from the 28F016SA or 28F016SV. When upgrading, it is important to note the following differences:

- Because of new feature and density options, the devices have different device identifier codes. This allows for software optimization.
- New software commands.
- To take advantage of the 5 V technology on the 28F160S5 and 28F320S5, allow  $V_{PP}$  connection to  $V_{CC}$ . The 28F160S5 and 28F320S5 FlashFile memories do not support a 12 V  $V_{PP}$  option.

### 1.2 Product Overview

The 5 Volt FlashFile memory family provides density upgrades with pinout compatibility for the 16- and 32-Mbit densities. They are high-performance memories arranged as 1 Mword and 2 Mwords of 16 bits or 2 Mbyte and 4 Mbyte of 8 bits. This data is grouped in thirty-two and sixty-four 64-Kbyte blocks that can be erased, locked, and unlocked in-system. Figure 1 shows the block diagram, and Figure 4 illustrates the memory organization.

Specifically designed for 5 V systems, the 28F160S5 and 28F320S5 support read and write operation with  $V_{CC}$  equal to  $V_{PP}$ . Coupled with this capability, high programming performance is achieved through small, highly-optimized write buffer operations. Additionally, the dedicated  $V_{PP}$  pin gives complete data protection when  $V_{PP} \leq V_{PPLK}$ .

A Common Flash Interface (CFI) permits OEM-specified software algorithms to be used for entire families of devices. This allows device-independent, JEDEC ID-independent, and forward- and backward-compatible software support for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

Scaleable Command Set (SCS) allows a single, simple software driver in all host systems to work with all SCS-compliant flash memory devices, independent of system-level packaging (e.g., memory card, SIMM, or direct-to-board placement). Additionally, SCS provides the highest system/device data transfer rates and minimizes device and system-level implementation costs.

A Command User Interface (CUI) serves as the interface between the system processor and internal device operation. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, program, and lock-bit configuration operations.

A block erase operation erases one of the device's 64-Kbyte blocks typically within  $t_{WHQV2/EHQV2}$  independent of other blocks. Each block can be independently erased 100,000 times in the commercial temperature range (0 °C to +70 °C) and 10,000 times in the extended temperature range (-40 °C to +85 °C). Block erase suspend allows system software to suspend block erase to read or write data from any other block.

Data is programmed in byte, word or page increments. Program suspend mode enables the system to read data or execute code from any other flash memory array location.

The device incorporates two Write Buffers of 32 bytes (16 words) to allow optimum-performance data programming. This feature can improve system program performance by up to eight times over non-buffer programming.

Individual block locking uses a combination of block lock-bits to lock and unlock blocks. Block lock-bits gate block erase, full chip erase, program and write to buffer operations. Lock-bit configuration operations (Set Block Lock-Bit and Clear Block Lock-Bits commands) set and clear lock-bits.

The status register and the STS pin in RY/BY# mode indicate whether or not the device is busy executing an operation or ready for a new command. Polling the status register, system software retrieves WSM feedback. STS in RY/BY# mode gives an additional indicator of WSM activity by providing a hardware status signal. Like the status register, RY/BY#-low indicates that the WSM is performing a block erase, program, or lock-bit operation. RY/BY#-high indicates that the WSM is ready for a new command, block erase is suspended (and program is inactive), program is suspended, or the device is in deep power-down mode.

The Automatic Power Savings (APS) feature substantially reduces active current when the device is in static mode (addresses not switching).

The BYTE# pin allows either x8 or x16 read/writes to the device. BYTE# at logic low selects 8-bit mode with address A<sub>0</sub> selecting between the low byte and high byte. BYTE# at logic high enables 16-bit operation with address A<sub>1</sub> becoming the lowest order address. Address A<sub>0</sub> is not used in 16-bit mode.

When one of the CE<sub>x</sub># pins (CE<sub>0</sub>#, CE<sub>1</sub>#) and RP# pins are at V<sub>CC</sub>, the component enters a CMOS standby mode. Driving RP# to GND enables a deep power-down mode which significantly reduces power consumption, provides write protection, resets the device, and clears the status register. A reset time (t<sub>PHQV</sub>) is required from RP# switching high until outputs are valid. Likewise, the device has a wake time (t<sub>PHL</sub>) from RP#-high until writes to the CUI are recognized.

### 1.3 Pinout and Pin Description

The 16-Mbit device is available in the 56-lead TSOP and 56-lead SSOP. The 32-Mb device is available in the 56-lead SSOP. The pinouts are shown in Figures 2 and 3.

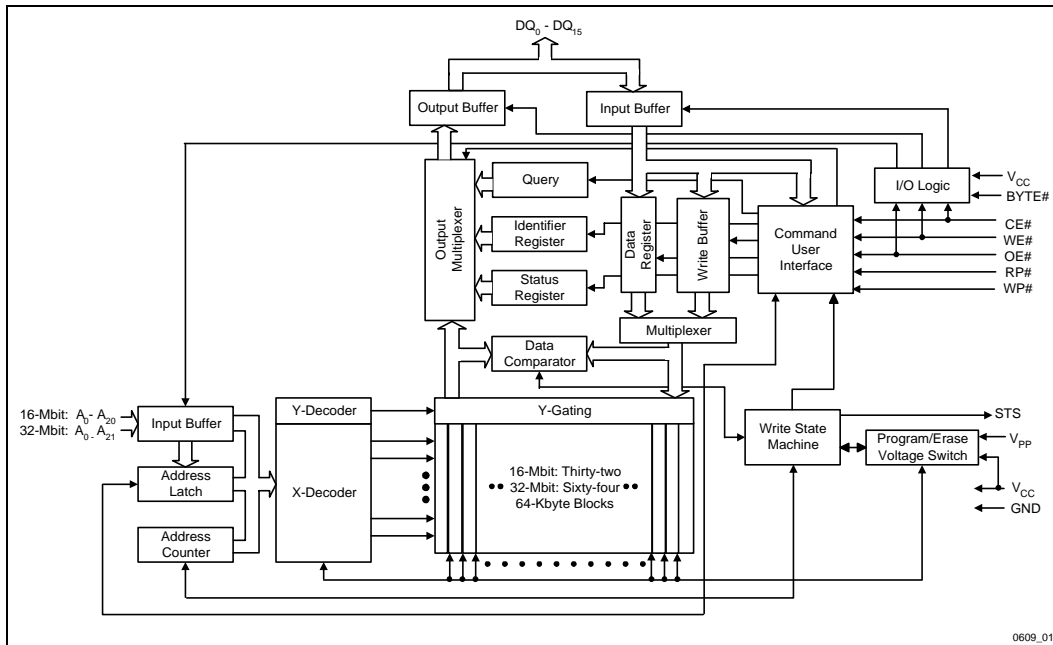


Figure 1. 28F320S5 and 28F160S5 Block Diagram

Table 1. Pin Descriptions

Sym	Type	Name and Function
A <sub>0</sub> –A <sub>21</sub>	INPUT	<b>ADDRESS INPUTS:</b> Address inputs for read and write operations are internally latched during a write cycle. A <sub>0</sub> selects high or low byte when operating in x8 mode. In x16 mode, A <sub>0</sub> is not used; input buffer is off. 16-Mbit → A <sub>0</sub> –A <sub>20</sub> 32-Mbit → A <sub>0</sub> –A <sub>21</sub>
DQ <sub>0</sub> – DQ <sub>15</sub>	INPUT/ OUTPUT	<b>DATA INPUT/OUTPUTS:</b> Inputs data and commands during CUI write cycles; outputs data during memory array, status register, query and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle.
CE <sub>0</sub> #, CE <sub>1</sub> #	INPUT	<b>CHIP ENABLE:</b> Activates the device's control logic, input buffers, decoders, and sense amplifiers. With CE <sub>0</sub> # or CE <sub>1</sub> # high, the device is deselected and power consumption reduces to standby levels. Both CE <sub>0</sub> # and CE <sub>1</sub> # must be low to select the device. Device selection occurs with the latter falling edge of CE <sub>0</sub> # or CE <sub>1</sub> #. The first rising edge of CE <sub>0</sub> # or CE <sub>1</sub> # disables the device.
RP#	INPUT	<b>RESET/DEEP POWER-DOWN:</b> When driven low, RP# inhibits write operations which provides data protection during system power transitions, puts the device in deep power-down mode, and resets internal automation. RP#-high enables normal operation. Exit from deep power-down sets the device to read array mode.
OE#	INPUT	<b>OUTPUT ENABLE:</b> Gates the device's outputs during a read cycle.
WE#	INPUT	<b>WRITE ENABLE:</b> Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of the WE# pulse.
STS	OPEN DRAIN OUTPUT	<b>STATUS:</b> Indicates the status of the internal state machine. When configured in level mode (default), it acts as a RY/BY# pin. For this and alternate configurations of the STATUS pin, see the Configuration command. Tie STS to V <sub>CC</sub> with a pull-up resistor.
WP#	INPUT	<b>WRITE PROTECT:</b> Master control for block locking. When V <sub>IL</sub> , locked blocks cannot be erased or programmed, and block lock-bits cannot be set or cleared.
BYTE#	INPUT	<b>BYTE ENABLE:</b> Configures x8 mode (low) or x16 mode (high).
V <sub>PP</sub>	SUPPLY	<b>BLOCK ERASE, PROGRAM, LOCK-BIT CONFIGURATION POWER SUPPLY:</b> Necessary voltage to perform block erase, program, and lock-bit configuration operations. Do not float any power pins.
V <sub>CC</sub>	SUPPLY	<b>DEVICE POWER SUPPLY:</b> Do not float any power pins.
GND	SUPPLY	<b>GROUND:</b> Do not float any ground pins.
NC		<b>NO CONNECT:</b> Lead is not internally connected; it may be driven or floated.

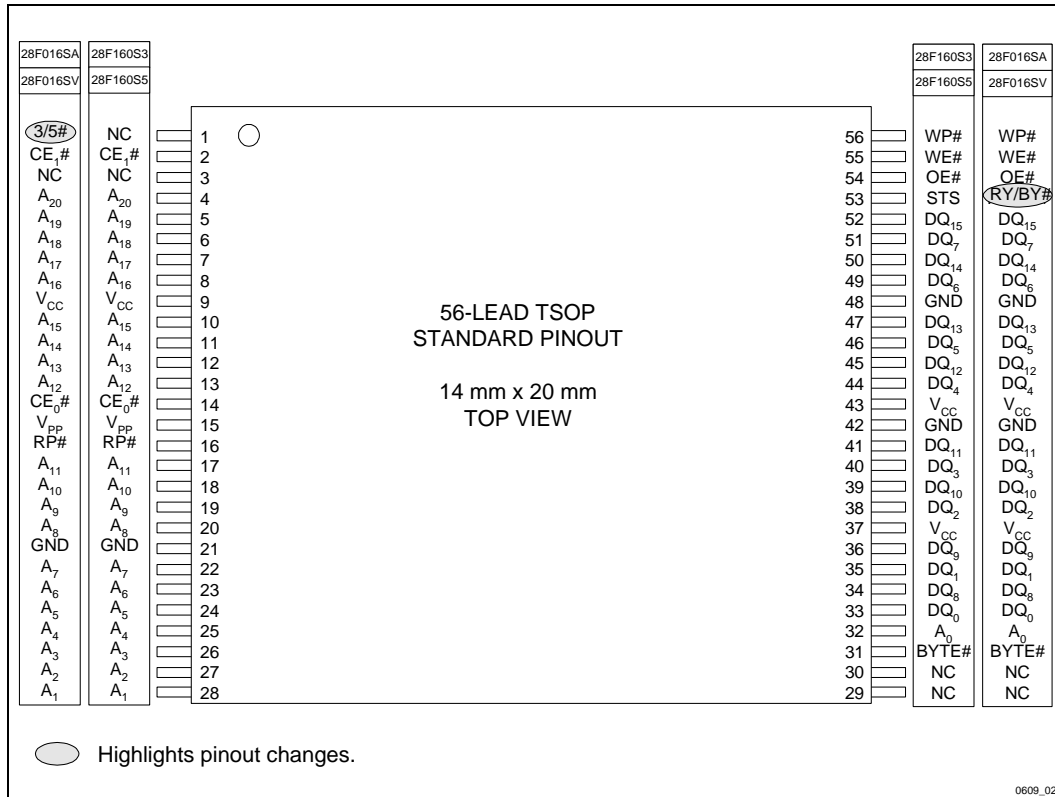
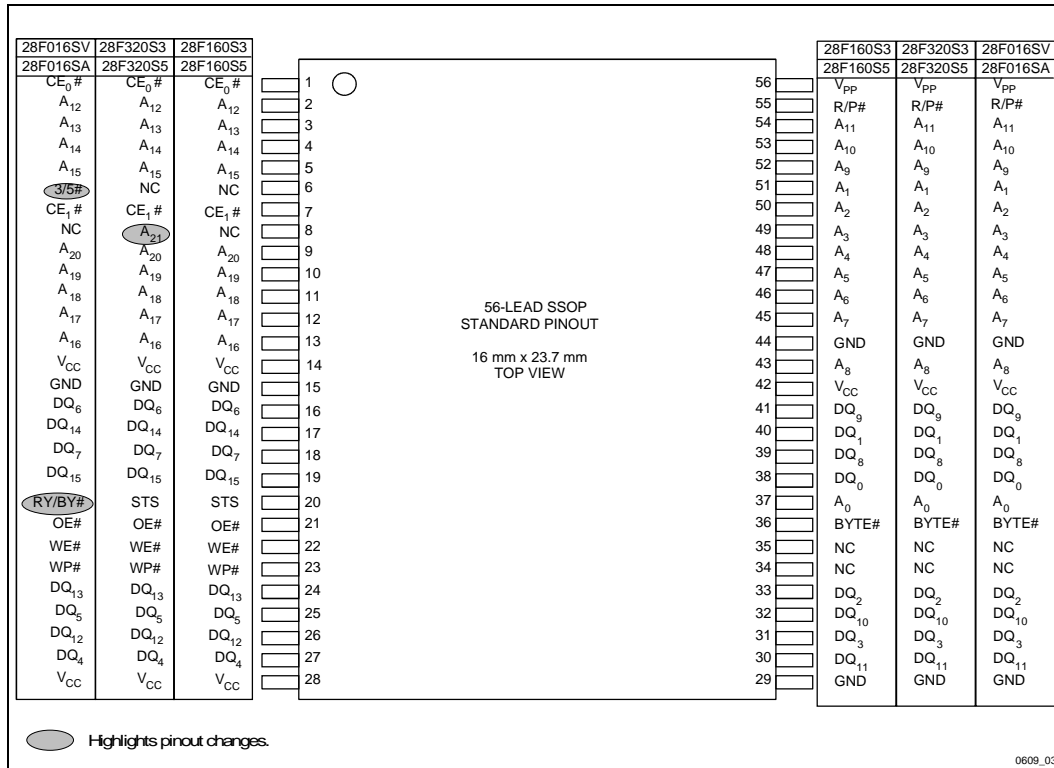


Figure 2. 28F160S5 TSOP 56-Lead Pinout




**Figure 3. 28F320S5 and 28F160S5 SSOP 56-Lead Pinout**

## 2.0 PRINCIPLES OF OPERATION

The 5 Volt FlashFile memories include an on-chip Write State Machine (WSM) to manage block erase, program, and lock-bit configuration functions. It allows for: 100% TTL-level control inputs, fixed power supplies during block erase, programming, lock-bit configuration, and minimal processor overhead with RAM-like interface timings.

After initial device power-up or return from deep power-down mode (see *Bus Operations*), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby, and output disable operations.

Read Array, status register, query, and identifier codes can be accessed through the CUI independent of the V<sub>PP</sub> voltage. Proper programming voltage on V<sub>PP</sub> enables successful

block erase, program, and lock-bit configuration. All functions associated with altering memory contents—block erase, program, lock-bit configuration, status, and identifier codes—are accessed via the CUI and verified through the status register.

Commands are written using standard micro-processor write timings. The CUI contents serve as input to the WSM that controls the block erase, programming, and lock-bit configuration. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification, and margining of data. Addresses and data are internally latched during write cycles. Writing the appropriate command outputs array data, identifier codes, or status register data.

Interface software that initiates and polls progress of block erase, programming, and lock-

bit configuration can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system software to suspend a block erase to read or write data from any other block. Program suspend allows system software to suspend a program to read data from any other flash memory array location.

### 2.1 Data Protection

Depending on the application, the system designer may choose to make the V<sub>PP</sub> power supply switchable or hardwired to V<sub>PPH</sub>. The device supports either design practice, and encourages optimization of the processor-memory interface.

When  $V_{PP} \leq V_{PPLK}$ , memory contents cannot be altered. When high voltage is applied to V<sub>PP</sub>, the two-step block erase, program, or lock-bit configuration command sequences provide protection from unwanted operations. All write functions are disabled when V<sub>CC</sub> voltage is below the write lockout voltage V<sub>LKO</sub> or when RP# is at V<sub>IL</sub>. The device's block locking capability provides additional protection from inadvertent code or data alteration.

### 3.0 BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

#### 3.1 Read

Block information, query information, identifier codes and status registers can be read independent of the V<sub>PP</sub> voltage.

The first task is to place the device into the desired read mode by writing the appropriate read-mode command (Read Array, Query, Read Identifier Codes, or Read Status Register) to the CUI. Upon initial device power-up or after exit from deep power-down mode, the device automatically resets to read array mode. Control pins dictate the data flow in and out of the component. CE<sub>0</sub>#, CE<sub>1</sub># and OE# must be driven active to obtain data at the outputs. CE<sub>0</sub># and CE<sub>1</sub># are the device selection controls, and, when both are active, enable the selected memory device. OE# is the data output (DQ<sub>0</sub>–DQ<sub>15</sub>) control: When active it drives the selected memory data onto the I/O bus. WE# must be at V<sub>IH</sub> and RP# must be at V<sub>IH</sub>. Figure 16 illustrates a read cycle.

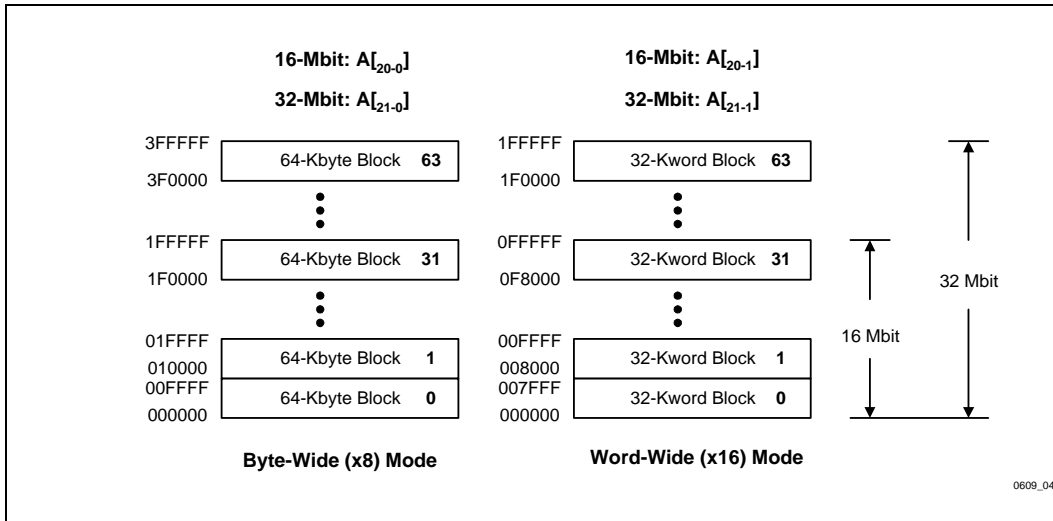


Figure 4. Memory Map

### 3.2 Output Disable

With OE# at a logic-high level ( $V_{IH}$ ), the device outputs are disabled. Output pins DQ<sub>0</sub>–DQ<sub>15</sub> are placed in a high-impedance state.

### 3.3 Standby

CE<sub>0</sub># or CE<sub>1</sub># at a logic-high level ( $V_{IH}$ ) places the device in standby mode, substantially reducing device power consumption. DQ<sub>0</sub>–DQ<sub>15</sub> (or DQ<sub>0</sub>–DQ<sub>7</sub> in x8 mode) outputs are placed in a high-impedance state independent of OE#. If deselected during block erase, programming, or lock-bit configuration, the device continues functioning and consuming active power until the operation completes.

### 3.4 Deep Power-Down

RP# at  $V_{IL}$  initiates the deep power-down mode.

In read mode, RP#-low deselects the memory, places output drivers in a high-impedance state, and turns off all internal circuits. RP# must be held low for time  $t_{PLPH}$ . Time  $t_{PHQV}$  is required after return from power-down until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI resets to read array mode, and the status register is set to 80H.

During block erase, programming, or lock-bit configuration modes, RP#-low will abort the operation. STS in RY/BY# mode remains low until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially corrupted after programming or partially altered after an erase or lock-bit configuration. Time  $t_{PHWL}$  is required after RP# goes to logic-high ( $V_{IH}$ ) before another command can be written.

It is important in any automated system to assert RP# during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase, programming, or lock-bit configuration modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. Intel's Flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

### 3.5 Read Query Operation

The read query operation outputs block status, Common Flash Interface (CFI) ID string, system interface, device geometry, and Intel-specific extended query information.

### 3.6 Read Identifier Codes Operation

The read-identifier codes operation outputs the manufacturer code, device code, and block lock configuration codes for each block configuration (see Figure 5). Using the manufacturer and device codes, the system software can automatically match the device with its proper algorithms. The block-lock configuration codes identify each block's lock-bit setting.

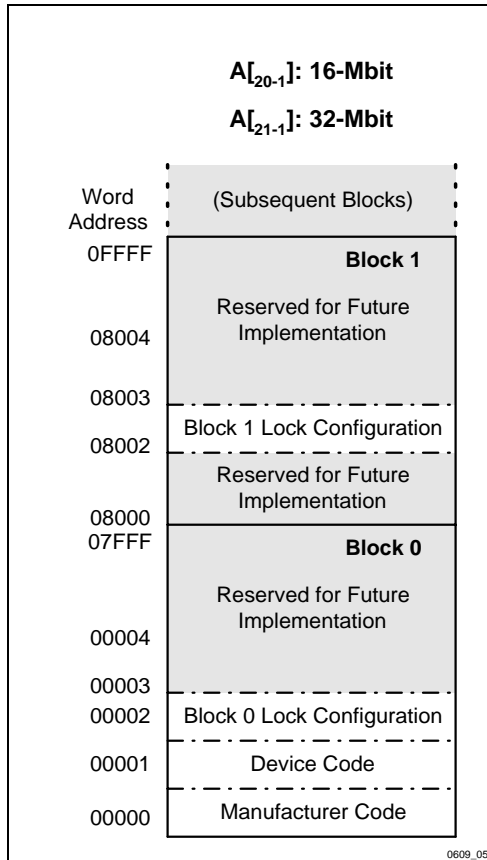


Figure 5. Device Identifier Code Memory Map

### 3.7 Write

Writing commands to the CUI enables reading of device data, query, identifier codes, inspection and clearing of the status register. Additionally, when  $V_{PP} = V_{PPH}$ , block erasure, programming, and lock-bit configuration can also be performed.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Byte/Word Write command requires the command and address of the location to be written. Set Block Lock-Bit commands require the command and address within the block to be locked. The Clear Block Lock-Bits command requires the command and an address within the device.

The CUI does not occupy an addressable memory location. It is written when  $WE\#$ ,  $CE_0\#$ , and  $CE_1\#$  are active and  $OE\# = V_{IH}$ . The address and data needed to execute a command are latched on the rising edge of  $WE\#$  or  $CE_x\#$  ( $CE_0\#$ ,  $CE_1\#$ ), whichever goes high first. Standard microprocessor write timings are used. Figure 17 illustrates a write operation.

### 4.0 COMMAND DEFINITIONS

$V_{PP}$  voltage  $\leq V_{PPLK}$  enables read operations from the status register, identifier codes, or memory blocks. Placing  $V_{PPH}$  on  $V_{PP}$  enables successful block erase, programming, and lock-bit configuration operations.

Device operations are selected by writing specific commands into the CUI. Table 2 and Table 3 define these commands.

**Table 2. Bus Operations**

Mode	Notes	RP#	CE <sub>0</sub> #	CE <sub>1</sub> #	OE# <sup>(11)</sup>	WE# <sup>(11)</sup>	Address	V <sub>PP</sub>	DQ <sup>(8)</sup>	STS <sup>(3)</sup>
Read	1,2	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	X	X	D <sub>OUT</sub>	X
Output Disable		V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	X	X	High Z	X
Standby		V <sub>IH</sub>	V <sub>IL</sub> V <sub>IH</sub> V <sub>IH</sub>	V <sub>IH</sub> V <sub>IL</sub> V <sub>IH</sub>	X	X	X	X	High Z	X
Reset/Power-Down Mode	10	V <sub>IL</sub>	X	X	X	X	X	X	High Z	High Z <sup>(9)</sup>
Read Identifier Codes	4	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	See Figure 5	X	D <sub>OUT</sub>	High Z <sup>(9)</sup>
Read Query	5	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	See Table 6	X	D <sub>OUT</sub>	High Z <sup>(9)</sup>
Write	3,6,7	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	X	V <sub>PPH</sub>	D <sub>IN</sub>	X

**NOTES:**

1. Refer to *DC Characteristics*. When  $V_{PP} \leq V_{PPLK}$ , memory contents can be read, but not altered.
2. X can be V<sub>IL</sub> or V<sub>IH</sub> for control and address input pins and V<sub>PPLK</sub> or V<sub>PPH</sub> for V<sub>PP</sub>. See *DC Characteristics*, for V<sub>PPLK</sub> and V<sub>PPH</sub> voltages.
3. STS in RY/BY# mode (default) is V<sub>OL</sub> when the WSM is executing internal block erase, programming, or lock-bit configuration algorithms. It is V<sub>OH</sub> when the WSM is not busy, in block erase suspend mode (with programming inactive), program suspend mode, or deep power-down mode.
4. See Section 4.3 for read identifier code data.
5. See Section 4.2 for read query data.
6. Command writes involving block erase, write, or lock-bit configuration are reliably executed when V<sub>PP</sub> = V<sub>PPH</sub> and V<sub>CC</sub> = V<sub>CC1/2</sub> (see Section 6.2).
7. Refer to Table 3 for valid D<sub>IN</sub> during a write operation.
8. DQ refers to DQ<sub>0-7</sub> if BYTE# is low and DQ<sub>0-15</sub> if BYTE# is high.
9. High Z will be V<sub>OH</sub> with an external pull-up resistor.
10. RP# at GND ± 0.2 V ensures the lowest deep power-down current.
11. OE# = V<sub>IL</sub> and WE# = V<sub>IL</sub> concurrently is an undefined state and should not be attempted.

Table 3. 5 Volt FlashFile™ Memory (28F160S5, 28F320S5) Command Set Definitions<sup>(13)</sup>

Command	Scaleable or Basic Command Set <sup>(14)</sup>	Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
				Oper <sup>(1)</sup>	Addr <sup>(2)</sup>	Data <sup>(3,4)</sup>	Oper <sup>(1)</sup>	Addr <sup>(2)</sup>	Data <sup>(3,4)</sup>
Read Array	SCS/BCS	1		Write	X	FFH			
Read Identifier Codes	SCS/BCS	≥2	5	Write	X	90H	Read	IA	ID
Read Query	SCS	≥2		Write	X	98H	Read	QA	QD
Read Status Register	SCS/BCS	2		Write	X	70H	Read	X	SRD
Clear Status Register	SCS/BCS	1		Write	X	50H			
Write to Buffer	SCS	> 2	8, 9, 10	Write	BA	E8H	Write	BA	N
Word/Byte Program	SCS/BCS	2	6,7	Write	X	40H or 10H	Write	PA	PD
Block Erase	SCS/BCS	2	6,10	Write	X	20H	Write	BA	D0H
Block Erase, Word/Byte Program Suspend	SCS/BCS	1	6	Write	X	B0H			
Block Erase, Word/Byte Program Resume	SCS/BCS	1	6	Write	X	D0H			
STS pin Configuration	SCS	2		Write	X	B8H	Write	X	CC
Set Block Lock-Bit	SCS	2	11	Write	X	60H	Write	BA	01H
Clear Block Lock-Bits	SCS	2	12	Write	X	60H	Write	X	D0H
Full Chip Erase	SCS	2	10	Write	X	30H	Write	X	D0H

**NOTES:**

1. Bus operations are defined in Table 2.
2. X = Any valid address within the device.  
BA = Address within the block being erased or locked.  
IA = Identifier Code Address: see Table 12.  
QA = Query database Address.  
PA = Address of memory location to be programmed.
3. ID = Data read from Identifier Codes.  
QD = Data read from Query database.  
SRD = Data read from status register. See Table 15 for a description of the status register bits.  
PD = Data to be programmed at location PA. Data is latched on the rising edge of WE#.  
CC = Configuration Code. (See Table 14.)
4. The upper byte of the data bus (DQ<sub>8-15</sub>) during command writes is a "Don't Care" in x16 operation.
5. Following the Read Identifier Codes command, read operations access manufacturer, device, and block-lock codes. See Section 4.3 for read identifier code data.
6. If a block is locked (i.e., the block's lock-bit is set to 0), WP# must be at V<sub>IH</sub> in order to perform block erase, program and suspend operations. Attempts to issue a block erase, program and suspend operation to a locked block while WP# is V<sub>IL</sub> will fail.
7. Either 40H or 10H are recognized by the WSM as the byte/word program setup.
8. After the Write to Buffer command is issued, check the XSR to make sure a Write Buffer is available.
9. N = byte/word count argument such that the number of bytes/words to be written to the input buffer = N + 1. N = 0 is 1 byte/word length, and so on. Write to Buffer is a multi-cycle operation, where a byte/word count of N + 1 is written to the correct memory address (WA) with the proper data (WD). The Confirm command (D0h) is expected after exactly N + 1 write cycles; any other command at that point in the sequence aborts the buffered write. Writing a byte/word count outside the buffer boundary causes unexpected results and should be avoided.
10. The write to buffer, block erase, or full chip erase operation does not begin until a Confirm command (D0h) is issued. Confirm also reactivates suspended operations.
11. A block lock-bit can be set only while WP# is V<sub>IH</sub>.
12. WP# must be at V<sub>IH</sub> to clear block lock-bits. The clear block lock-bits operation simultaneously clears all block lock-bits.
13. Commands other than those shown above are reserved for future use and should not be used.
14. The Basic Command Set (BCS) is the same as the 28F008SA Command Set or Intel Standard Command Set. The Scaleable Command Set (SCS) is also referred to as the Intel Extended Command Set.

## 4.1 Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started block erase, program, or lock-bit configuration, the device will not recognize the Read Array command until the WSM completes its operation—unless the WSM is suspended via an Erase-Suspend or Program-Suspend command. The Read Array command functions independently of the  $V_{PP}$  voltage.

## 4.2 Read Query Mode Command

This section defines the data structure or “database” returned by the Common Flash Interface (CFI) Query command. System software should parse this structure to gain critical information such as block size, density, x8/x16, and electrical specifications. Once this information has been obtained, the software will know which command sets to use to enable flash writes, block erases, and otherwise control the flash component. The Query is part of an overall specification for multiple command set and control interface descriptions called Common Flash Interface, or CFI.

### 4.2.1 QUERY STRUCTURE OUTPUT

The Query “database” allows system software to gain critical information for controlling the flash component. This section describes the device’s CFI-compliant interface that allows the host system to access Query data.

Query data are always presented on the lowest-order data outputs (DQ<sub>0-7</sub>) only. The numerical offset value is the address relative to the maximum bus width supported by the device. On this device, the Query table device starting address is a 10h word address, since the maximum bus width is x16.

For this word-wide (x16) device, the first two bytes of the Query structure, “Q” and “R” in ASCII, appear on the low byte at word addresses 10h and 11h. This CFI-compliant device outputs 00H data on upper bytes. Thus, the device outputs ASCII “Q” in the low byte (DQ<sub>0-7</sub>) and 00h in the high byte (DQ<sub>8-15</sub>).

Since the device is x8/x16 capable, the x8 data is still presented in word-relative (16-bit) addresses. However, the “fill data” (00h) is not the same as driven by the upper bytes in the x16 mode. As in x16 mode, the byte address (A<sub>0</sub>) is ignored for Query output so that the “odd byte address” (A<sub>0</sub> high) repeats the “even byte address” data (A<sub>0</sub> low). Therefore, in x8 mode using byte addressing, the device will output the sequence “Q”, “Q”, “R”, “R”, “Y”, “Y”, and so on, beginning at byte-relative address 20h (which is equivalent to word offset 10h in x16 mode).

At Query addresses containing two or more bytes of information, the least significant data byte is presented at the lower address, and the most significant data byte is presented at the higher address.



**Table 4. Summary of Query Structure Output as a Function of Device and Mode**

Device Type/Mode	Word Addressing		Byte Addressing	
	Location	Query Data Hex, ASCII	Location	Query Data Hex, ASCII
x16 device/ x16 mode	10h 11h 12h	0051h "Q" 0052h "R" 0059h "Y"	20h 21h 22h	51h "Q" 00h null 52h "R"
x16 device/ x8 mode	N/A <sup>(1)</sup>	N/A	20h 21h 22h	51h "Q" 51h "Q" 52h "R"

**NOTE:**

1. The system must drive the lowest order addresses to access all the device's array data when the device is configured in x8 mode. Therefore, word addressing where lower addresses are not toggled by the system is "Not Applicable" for x8-configured devices.

**Table 5. Example of Query Structure Output of a x16- and x8-Capable Device**

Device Address	Word Addressing: Query Data	Byte Address	Byte Addressing: Query Data
A <sub>16</sub> -A <sub>1</sub>	D <sub>15</sub> -D <sub>0</sub>	A <sub>7</sub> -A <sub>0</sub>	D <sub>7</sub> -D <sub>0</sub>
0010h	0051h "Q"	20h	51h "Q"
0011h	0052h "R"	21h	51h "Q"
0012h	0059h "Y"	22h	52h "R"
0013h	P_ID <sub>LO</sub> PrVendor	23h	52h "R"
0014h	P_ID <sub>HI</sub> ID #	24h	59h "Y"
0015h	P <sub>LO</sub> PrVendor	25h	59h "Y"
0016h	P <sub>HI</sub> TblAdr	26h	P_ID <sub>LO</sub> PrVendor
0017h	A_ID <sub>LO</sub> AltVendor	27h	P_ID <sub>LO</sub> ID #
0018h	A_ID <sub>HI</sub> ID #	28h	P_ID <sub>HI</sub> "
...	...	...	...

#### 4.2.2 QUERY STRUCTURE OVERVIEW

The Query command causes the flash component to display the Common Flash Interface (CFI) Query structure or “database.” The structure sub-sections and address locations are summarized in Table 8.

The following sections describe the Query structure sub-sections in detail.

**Table 6. Query Structure<sup>(1)</sup>**

Offset	Sub-Section Name	Description
00h		Manufacturer Code
01h		Device Code
(BA+2)h <sup>(2)</sup>	Block Status Register	Block-specific information
04-0Fh	<i>Reserved</i>	<i>Reserved for vendor-specific information</i>
10h	CFI Query Identification String	Command set ID and vendor data offset
1Bh	System Interface Information	Device timing and voltage information
27h	Device Geometry Definition	Flash device layout
P <sup>(3)</sup>	Primary Intel-specific Extended Query table	Vendor-defined additional information specific to the Primary Vendor Algorithm

**NOTES:**

1. Refer to Section 4.2.1 and Table 4 for the detailed definition of offset address as a function of device word width and mode.
2. BA = The beginning location of a Block Address (i.e., 08000h is the beginning location of block 1 when the block size is 32 Kword).
3. Offset 15 defines “P” which points to the Primary Intel-specific Extended Query Table.

**4.2.3 BLOCK STATUS REGISTER**

The block status register indicates whether an erase operation completed successfully or whether a given block is locked or can be accessed for flash program/erase operations.

Block Erase Status (BSR.1) allows system software to determine the success of the last block erase operation. BSR.1 can be used just after power-up to verify that the V<sub>CC</sub> supply was not accidentally removed during an erase operation. This bit is only reset by issuing another erase operation to the block. The block status register is accessed from word address 02h within each block.

**Table 7. Block Status Register**

Offset	Length (bytes)	Description	28F32/160S5 x16 Device/Mode
(BA+2)h <sup>(1)</sup>	01h	Block Status Register	BA+2: 0000h or 0001h
		BSR.0 = Block Lock Status 1 = Locked 0 = Unlocked	BA+2 (bit 0): 0 or 1
		BSR.1 = Block Erase Status 1 = Last erase operation did not complete successfully 0 = Last erase operation completed successfully	BA+2 (bit 1): 0 or 1
		<i>BSR 2-7 Reserved for future use</i>	BA+2 (bits 2-7): 0

**NOTE:**

1. BA = The beginning location of a Block Address (i.e., 008000h is the beginning location of block 1 in word mode.)

#### 4.2.4 CFI QUERY IDENTIFICATION STRING

The Identification String provides verification that the component supports the Common Flash Interface specification. Additionally, it indicates which version of the spec and which vendor-specified command set(s) is (are) supported.

**Table 8. CFI Identification**

Offset	Length (Bytes)	Description	28F320/160S5
10h	03h	Query-Unique ASCII string "QRY"	10: 0051h 11: 0052h 12: 0059h
13h	02h	Primary Vendor Command Set and Control Interface ID Code 16-bit ID Code for Vendor-Specified Algorithms	13: 0001h 14: 0000h
15h	02h	Address for Primary Algorithm Extended Query Table Offset value = $P = 31h$	15: 0031h 16: 0000h
17h	02h	Alternate Vendor Command Set and Control Interface ID Code Second Vendor-Specified Algorithm Supported <b>Note: 0000h means none exists</b>	17: 0000h 18: 0000h
19h	02h	Address for Secondary Algorithm Extended Query Table <b>Note: 0000h means none exists</b>	19: 0000h 1A: 0000h

**4.2.5 SYSTEM INTERFACE INFORMATION**

Note that a query on the 28F160S5/28F320S5 will return system interface information of the S3 device.

The following device information can be useful in optimizing system interface software.

**Table 9. System Interface Information**

Offset	Length (bytes)	Description	28F160S5	28F320S5
1Bh	01h	V <sub>CC</sub> Logic Supply Minimum Program/Erase Voltage bits 7–4 BCD volts bits 3–0 BCD 100 mv	1B: 0027h	1B: 0027h
1Ch	01h	V <sub>CC</sub> Logic Supply Maximum Program/Erase Voltage bits 7–4 BCD volts bits 3–0 BCD 100 mv	1C: 0055h	1C: 0055h
1Dh	01h	V <sub>PP</sub> [Programming] Supply Minimum Program/Erase Voltage bits 7–4 HEX volts bits 3–0 BCD 100 mv	1D: 0027h	1D: 0027h
1Eh	01h	V <sub>PP</sub> [Programming] Supply Maximum Program/Erase Voltage bits 7–4 HEX volts bits 3–0 BCD 100 mv	1E: 0055h	1E: 0055h
1Fh	01h	Typical Time-Out per Single Byte/Word Program, 2 <sup>N</sup> μsec	1F: 0003h (2 <sup>3</sup> = 8)	1F: 0003h (2 <sup>3</sup> = 8)
20h	01h	Typical Time-Out for Max. Buffer Write, 2 <sup>N</sup> μsec	20: 0006h (2 <sup>6</sup> = 64)	20: 0006h (2 <sup>6</sup> = 64)
21h	01h	Typical Time-Out per Individual Block Erase, 2 <sup>N</sup> msec	21: 000Ah (0Ah = 10d, 2 <sup>10</sup> = 1024)	21: 000Ah (0Ah = 10d, 2 <sup>10</sup> = 1024)
22h	01h	Typical Time-Out for Full Chip Erase, 2 <sup>N</sup> msec	22: 000Fh (0Fh = 15d, 2 <sup>15</sup> = 32768)	22: 000Fh (0Fh = 15d, 2 <sup>15</sup> = 32768)
23h	01h	Maximum Time-Out for Byte/Word Program, 2 <sup>N</sup> Times Typical	23: 0004h 2 <sup>4</sup> = 16, 16xTypical)	23: 0004h 2 <sup>4</sup> = 16, 16xTypical)
24h	01h	Maximum Time-Out for Buffer Write, 2 <sup>N</sup> Times Typical 2 <sup>4</sup> = 16, 16 x Typical)	24: 0004h 2 <sup>4</sup> = 16, 16xTypical)	24: 0004h 2 <sup>4</sup> = 16, 16xTypical)
25h	01h	Maximum Time-Out per Individual Block Erase, 2 <sup>N</sup> Times Typical 2 <sup>4</sup> = 16, 16 x Typical)	25: 0004h 2 <sup>4</sup> = 16, 16xTypical)	25: 0004h 2 <sup>4</sup> = 16, 16xTypical)
26h	01h	Maximum Time-Out for Full Chip Erase, 2 <sup>N</sup> Times Typical 2 <sup>4</sup> = 16, 16 x Typical)	26: 0004h 2 <sup>4</sup> = 16, 16xTypical)	26: 0004h 2 <sup>4</sup> = 16, 16xTypical)

## 4.2.6 DEVICE GEOMETRY DEFINITION

This field provides critical details of the flash device geometry.

Table 10. Device Geometry Definition

Offset	Length (bytes)	Description	28F160S5	28F320S5
27h	01h	Device Size = $2^N$ in Number of Bytes	27: 0015h (15h = 21d, $2^{21}$ = 2097152 bytes = 2 MB = 16 Mb)	27: 0016h (16h = 22d, $2^{22}$ = 4194304 bytes = 4 MB = 32 Mb)
28h	02h	Flash Device Interface Description  <u>value</u> <u>meaning</u>  0002h    x8/x16 asynchronous	28: 0002h 29: 0000h	28: 0002h 29: 0000h
2Ah	02h	Maximum Number of Bytes in Write Buffer = $2^N$	2A: 0005h 2B: 0000h ( $2^5$ = 32)	2A: 0005h 2B: 0000h ( $2^5$ = 32)
2Ch	01h	Number of Erase Block Regions within Device:  <b>bits 7–0 = x = # of regions within the device containing one or more contiguous Erase Blocks of the same size.</b>	2C: 0001h	2C: 0001h
2Dh	04h	Erase Block Region Information  <b>bits 15–0 = y</b> , where $y+1$ = number of erase blocks of identical size within region.  <b>bits 31–16 = z</b> , where the erase block(s) within this region are $z \times 256$ Bytes. $z$ is the number of “256-Byte” clusters in an erase block.	y: 2D: 001Fh 2E: 0000h (1Fh+1=32 blocks)  z: 2F: 0000h 30: 0001h (100h = 256, 256 x 256 = 64 KB)	y: 2D: 003Fh 2E: 0000h (3Fh+1=64 blocks)  z: 2F: 0000h 30: 0001h (100h = 256, 256 x 256= 64 KB)

**4.2.7 INTEL-SPECIFIC EXTENDED QUERY TABLE**

Certain flash features and commands are optional. The Intel-Specific Extended Query table specifies this and other similar types of information.

**Table 11. Primary-Vendor Specific Extended Query**

Offset <sup>(1)</sup>	Length (bytes)	Description	Data
(P)h	03h	Primary Extended Query Table Unique ASCII String "PRI"	31: 0050h 32: 0052h 33: 0049h
(P+3)h	01h	Major Version Number, ASCII	34: 0031h
(P+4)h	01h	Minor Version Number, ASCII	35: 0030h
(P+5)h	04h	Optional Feature & Command Support  bit 0 Chip Erase Supported (1=yes, 0=no) bit 1 Suspend Erase Supported (1=yes, 0=no) bit 2 Suspend Program Supported (1=yes, 0=no) bit 3 Lock/Unlock Supported (1=yes, 0=no) bit 4 Queued Erase Supported (1=yes, 0=no)  <i>bits 5-31 Reserved for future use; undefined bits are "0"</i>	36: 000Fh 37: 0000h 38: 0000h 39: 0000h
(P+9)h	01h	Supported Functions after Suspend  Read Array, Status, and Query are always supported during suspended Erase or Program operation. This field defines other operations supported.  bit 0 Program Supported after Erase Suspend (1=yes, 0=no)  <i>bits 1-7 Reserved for future use; undefined bits are "0"</i>	3A: 0001h
(P+A)h	02h	Block Status Register Mask  Defines which bits in the Block Status Register section of Query are implemented.  bit 0 Block Status Register Lock-Bit [BSR.0] active (1=yes, 0=no) bit 1 Block Erase Status Bit [BSR.1] active (1=yes, 0=no)  <i>bits 2-15 Reserved for future use; undefined bits are "0"</i>	3B: 0003h 3C: 0000h

**NOTES:**

- The variable P is a pointer which is defined at offset 15h in Table 8.

Table 11. Primary-Vendor Specific Extended Query (Continued)

Offset	Length (bytes)	Description	Data
(P+C)h	01h	V <sub>CC</sub> Logic Supply Optimum Program/Erase voltage (highest performance) bits 7–4 BCD value in volts bits 3–0 BCD value in 100 mv	3D: 0050h
(P+D)h	01h	V <sub>PP</sub> [Programming] Supply Optimum Program/Erase voltage bits 7–4 HEX value in volts bits 3–0 BCD value in 100 mv	3E: 0050h
(P+E)h	reserved	Reserved for future use	

Table 12. Identifier Codes

Code	Address <sup>(2)</sup>	Data
Manufacturer Code	000000	B0
Device Code	16 Mbit	000001
	32 Mbit	000001
Block Lock Configuration • Block Is Unlocked • Block Is Locked • Reserved for Future Use	x0002 <sup>(1)</sup>	DQ <sub>0</sub> = 0
		DQ <sub>0</sub> = 1
		DQ <sub>2-7</sub>
Block Erase Status • Last erase completed successfully • Last erase did not complete successfully • Reserved for Future Use	x0002 <sup>(1)</sup>	DQ <sub>1</sub> = 0
		DQ <sub>1</sub> = 1
		DQ <sub>2-7</sub>

**NOTES:**

- X selects the specific block lock configuration code. See Figure 5 for the device identifier code memory map.
- A<sub>0</sub> should be ignored in this address. The lowest order address line is A<sub>1</sub> in both word and byte mode.

### 4.3 Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 5 retrieve the manufacturer, device, block lock configuration, and block erase status codes (see Table 12 for identifier code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the V<sub>PP</sub> voltage. Following the Read Identifier Codes command, the information in Table 12 can be read.

### 4.4 Read Status Register Command

The status register may be read to determine when programming, block erasure, or lock-bit configuration is complete and whether the operation completed successfully. It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of OE#, CE<sub>0</sub>#, or CE<sub>1</sub># whichever occurs last. OE# or CE<sub>X</sub># must toggle to V<sub>IH</sub> to update the status register latch. The Read Status Register command functions independently of the V<sub>PP</sub> voltage.



Following a program, block erase, set block lock-bit, or clear block lock-bits command sequence, only SR.7 is valid until the Write State Machine completes or suspends the operation. Device I/O pins DQ<sub>0-6</sub> and DQ<sub>8-15</sub> are invalid. When the operation completes or suspends (SR.7 = 1), all contents of the status register are valid when read.

The eXtended Status Register (XSR) may be read to determine Write Buffer availability (see Table 16). The XSR may be read at any time by writing the Write to Buffer command. After writing this command, all subsequent read operations output data from the XSR, until another valid command is written. The contents of the XSR are latched on the falling edge of OE# or CE<sub>x</sub># whichever occurs last in the read cycle. Write to buffer command must be re-issued to update the XSR latch.

#### 4.5 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3, and SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 15). By allowing system software to reset these bits, several operations (such as cumulatively erasing or locking multiple blocks or programming several bytes/words in sequence) may be performed. The status register may be polled to determine if an error occurred during the sequence.

To clear the status register, the Clear Status Register command is written. It functions independently of the applied V<sub>PP</sub> voltage. This command is not functional during block erase or program suspend modes.

#### 4.6 Block Erase Command

Block Erase is executed one block at a time and initiated by a two-cycle command. A Block Erase Setup command is written first, followed by a Confirm command. This command sequence requires appropriate sequencing and an address within the block to be erased (erase changes all block data to FFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 9). The CPU can detect block erase completion by

analyzing STS in level RY/BY# mode or status register bit SR.7. Toggle OE#, CE<sub>0</sub>#, or CE<sub>1</sub># to update the status register.

When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1." Also, reliable block erasure can only occur when V<sub>CC</sub> = V<sub>CC1/2</sub> and V<sub>PP</sub> = V<sub>PPH</sub>. In the absence of these voltages, block contents are protected against erasure. If block erase is attempted while V<sub>PP</sub> ≤ V<sub>PPLK</sub>, SR.3 and SR.5 will be set to "1." Successful block erase requires that the corresponding block lock-bit be cleared, or WP# = V<sub>IH</sub>. If block erase is attempted when the corresponding block lock-bit is set and WP# = V<sub>IL</sub>, the block erase will fail and SR.1 and SR.5 will be set to "1."

#### 4.7 Full Chip Erase Command

The Full Chip Erase command followed by a Confirm command erases all unlocked blocks. After the Confirm command is written, the device erases all unlocked blocks from block 0 to block 31 (or 63) sequentially. Block preconditioning, erase, and verify are handled internally by the WSM. After the Full Chip Erase command sequence is written to the CUI, the device automatically outputs the status register data when read. The CPU can detect full chip erase completion by polling the STS pin in level RY/BY# mode or status register bit SR.7.

When the full chip erase is complete, status register bit SR.5 should be checked to see if the operation completed successfully. If an erase error occurred, the status register should be cleared before issuing the next command. The CUI remains in read status register mode until a new command is issued. If an error is detected while erasing a block during a full chip erase operation, the WSM skips the remaining cells in that block and proceeds to erase the next block. Reading the block valid status code by issuing the Read Identifier Codes command or Query command informs the user of which block(s) failed to erase.

This two-step command sequence of setup followed by execution ensures that block contents are not accidentally erased. An invalid Full Chip Erase command sequence will result in both status register bits SR.4 and SR.5 being set to 1. Also, reliable full chip erasure can only occur when  $V_{CC} = V_{CC1/2}$  and  $V_{PP} = V_{PPH}$ . In the absence these voltages, block contents are protected against erasure. If full chip erase is attempted while  $V_{PP} \leq V_{PPLK}$ , SR.3 and SR.5 will be set to 1. When  $WP\# = V_{IL}$ , only unlocked blocks are erased. Full chip erase cannot be suspended.

#### 4.8 Write to Buffer Command

To program the flash device via the write buffers, a Write to Buffer command sequence is initiated. A variable number of bytes or words, up to the buffer size, can be written into the buffer and programmed to the flash device. First, the Write to Buffer Setup command is issued along with the Block Address. At this point, the XSR information is loaded and XSR.7 indicates that another Write to Buffer command is possible. If XSR.7 = 0, no write buffer is available. To retry, continue monitoring XSR.7 by issuing the Write to Buffer Setup command with the Block Address until XSR.7 = 1. When XSR.7 transitions to a "1," the buffer is ready for loading.

Next, a word or byte count is issued at a valid address within the block. On the next write, a device start address is given along with the write buffer data. For maximum programming performance and lower power, align the start address at the beginning of a write buffer boundary. Subsequent writes must supply additional device addresses and data, depending on the count. All subsequent addresses must lie within the start address plus the count.

After the final buffer data is given, a Write Confirm command is issued. This initiates the WSM to begin copying the buffer data to the flash memory. If a command other than Write Confirm is written to the device, an "Invalid Command/Sequence" error will be generated and status register bits SR.5 and SR.4 will be set to "1." For additional buffer writes, issue another Write to Buffer Setup command and check XSR.7. The write buffers can be loaded while the WSM is busy as long as XSR.7 indicates that a buffer is available. Refer to Figure 6 for the *Write to Buffer Flowchart*.

If an error occurs while writing, the device will stop programming, and status register bit SR.4 will be set to a "1" to indicate a program failure. Any time a media failure occurs during a program or an erase (SR.4 or SR.5 is set), the device will not accept any more Write to Buffer commands. Additionally, if the user attempts to write past an erase block boundary with a Write to Buffer command, the device will abort programming. This will generate an "Invalid Command/Sequence" error and status register bits SR.5 and SR.4 will be set to "1." To clear SR.4 and/or SR.5, issue a Clear Status Register command.

Reliable buffered programming can only occur when  $V_{CC} = V_{CC1/2}$  and  $V_{PP} = V_{PPH}$ . If programming is attempted while  $V_{PP} \leq V_{PPLK}$ , status register bits SR.4 and SR.5 will be set to "1." Programming attempts with invalid  $V_{CC}$  and  $V_{PP}$  voltages produce spurious results and should not be attempted. Finally, successful programming requires that the corresponding Block Lock-Bit be cleared, or  $WP\# = V_{IH}$ . If a buffered write is attempted when the corresponding Block Lock-Bit is set and  $WP\# = V_{IL}$ , SR.1 and SR.4 will be set to "1."

#### 4.9 Byte/Word Program Command

Byte/Word programming is executed by a two-cycle command sequence. Byte/Word Program setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the program and verify algorithms internally. After the write sequence is written, the device automatically outputs status register data when read. The CPU can detect the completion of the program event by analyzing STS in level RY/BY# mode or status register bit SR.7.

When programming is complete, status register bit SR.4 should be checked. If a programming error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully program to "0"s. The CUI remains in read status register mode until it receives another command. Refer to Figure 7 for the *Single Word/Byte Program Flowchart*.

Also, Reliable byte/word programming can only occur when  $V_{CC} = V_{CC1/2}$  and  $V_{PP} = V_{PPH}$ . In the absence of this high voltage, contents are protected against programming. If a byte/word program is

attempted while  $V_{PP} \leq V_{PPLK}$ , status register bits SR.4 and SR.3 will be set to “1.” Successful byte/word programming requires that the corresponding block lock-bit be cleared. If a byte/word program is attempted when the corresponding block lock-bit is set and  $WP\# = V_{IL}$ , SR.1 and SR.4 will be set to “1.”

#### 4.10 STS Configuration Command

The Status (STS) pin can be configured to different states using the STS pin Configuration command. Once the STS pin has been configured, it remains in that configuration until another configuration command is issued or  $RP\#$  is low. Initially, the STS pin defaults to level RY/BY# operation where STS low indicates that the state machine is busy. STS high indicates that the state machine is ready for a new operation or suspended.

To reconfigure the Status (STS) pin to other modes, the STS pin Configuration command is issued followed by the desired configuration code. The three alternate configurations are all pulse mode for use as a system interrupt as described in Table 14. For these configurations, bit 0 controls Erase Complete interrupt pulse, and bit 1 controls Write Complete interrupt pulse. When the device is configured in one of the pulse modes, the STS pin pulses low with a typical pulse width of 250 ns. Supplying the 00h configuration code with the Configuration command resets the STS pin to the default RY/BY# level mode. Refer to Table 14 for configuration coding definitions. The Configuration command may only be given when the device is not busy or suspended. Check SR.7 for device status. An invalid configuration code will result in both status register bits SR.4 and SR.5 being set to “1.”

#### 4.11 Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or program data in another block of memory. Once the block erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bits SR.7 can determine when the block erase operation has been suspended. When  $SR.7 = 1$ , SR.6 should

also be set to “1”, indicating that the device is in the erase suspend mode. STS in level RY/BY# mode will also transition to  $V_{OH}$ . Specification  $t_{WHRH2}$  defines the block erase suspend latency.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A Program command sequence can also be issued during erase suspend to program data in other blocks. Using the Program Suspend command (see Section 4.12), a program operation can also be suspended. During a program operation with block erase suspended, status register bit SR.7 will return to “0” and STS in RY/BY# mode will transition to  $V_{OL}$ . However, SR.6 will remain “1” to indicate block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and STS in RY/BY# mode will return to  $V_{OL}$ . After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 10).  $V_{PP}$  must remain at  $V_{PPH}$  and  $V_{CC}$  must remain at  $V_{CC1/2}$  (the same  $V_{PP}$  and  $V_{CC}$  levels used for block erase) while block erase is suspended.  $RP\#$  must also remain at  $V_{IH}$  (the same  $RP\#$  level used for block erase). Block erase cannot resume until program operations initiated during block erase suspend have completed.

#### 4.12 Program Suspend Command

The Program Suspend command allows program interruption to read data in other flash memory locations. Once the programming process starts, writing the Program Suspend command requests that the WSM suspend the program sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the Program Suspend command is written. Polling status register bits SR.7 can determine when the programming operation has been suspended. When  $SR.7 = 1$ , SR.2 should also be set to “1”, indicating that the device is in the program suspend mode. STS in level RY/BY# mode will also transition to  $V_{OH}$ . Specification  $t_{WHRH1}$  defines the program suspend latency.

At this point, a Read Array command can be written to read data from locations other than that which is

suspended. The only other valid commands while programming is suspended are Read Status Register and Program Resume. After a Program Resume command is written, the WSM will continue the programming process. Status register bits SR.2 and SR.7 will automatically clear and STS in RY/BY# mode will return to  $V_{OL}$ . After the Program Resume command is written, the device automatically outputs status register data when read.  $V_{PP}$  must remain at  $V_{PPH}$  and  $V_{CC}$  must remain at  $V_{CC1/2}$  (the same  $V_{PP}$  and  $V_{CC}$  levels used for programming) while in program suspend mode. RP# must also remain at  $V_{IH}$  (the same RP# level used for programming). Refer to Figure 8 for the *Program Suspend/Resume Flowchart*.

#### 4.13 Set Block Lock-Bit Command

A flexible block locking and unlocking scheme is enabled via a combination of block lock-bits. The block lock-bits gate program and erase operations. With  $WP\# = V_{IH}$ , individual block lock-bits can be set using the Set Block Lock-Bit command.

Set block lock-bit is initiated using a two-cycle command sequence. The Set Block Lock-Bit setup along with appropriate block or device address is written followed by the Set Block Lock-Bit Confirm and an address within the block to be locked. The WSM then controls the set lock-bit algorithm. After the sequence is written, the device automatically outputs status register data when read. The CPU can detect the completion of the set lock-bit event by analyzing STS in level RY/BY# mode or status register bit SR.7.

When the set lock-bit operation is complete, status register bit SR.4 should be checked. If an error is detected, the status register should be cleared. The CUI will remain in read status register mode until a new command is issued.

This two-step sequence of setup followed by execution ensures that lock-bits are not accidentally set. An invalid Set Block Lock-Bit command will result in status register bits SR.4 and SR.5 being set to "1." Also, reliable operations occur only when  $V_{CC} = V_{CC1/2}$  and  $V_{PP} = V_{PPH}$ . In the absence these voltages, lock-bit contents are protected against alteration.

A successful set block lock-bit operation requires that  $WP\# = V_{IH}$ . If it is attempted with  $WP\# = V_{IL}$ , the operation will fail and SR.1 and SR.4 will be set to "1." See Table 13 for write protection alternatives. Refer to Figure 11 for the *Set Block Lock-Bit Flowchart*.

#### 4.14 Clear Block Lock-Bits Command

All set block lock-bits are cleared in parallel via the Clear Block Lock-Bits command. This command is valid only when  $WP\# = V_{IH}$ .

The clear block lock-bits operation is initiated using a two-cycle command sequence. A Clear Block Lock-Bits setup command is written followed by a Confirm command. Then, the device automatically outputs status register data when read (see Figure 12). The CPU can detect completion of the clear block lock-bits event by analyzing STS in level RY/BY# mode or status register bit SR.7.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally cleared. An invalid Clear Block Lock-Bits command sequence will result in status register bits SR.4 and SR.5 being set to "1." Also, a reliable clear block lock-bits operation can only occur when  $V_{CC} = V_{CC1/2}$  and  $V_{PP} = V_{PPH}$ . If a clear block lock-bits operation is attempted while  $V_{PP} \leq V_{PPLK}$ , SR.3 and SR.5 will be set to "1." In the absence of these voltages, the block lock-bits contents are protected against alteration. A successful clear block lock-bits operation requires that  $WP\# = V_{IH}$ .

If a clear block lock-bits operation is aborted due to  $V_{PP}$  or  $V_{CC}$  transitioning out of valid range or RP# or WP# active transition, block lock-bit values are left in an undetermined state. A repeat of clear block lock-bits is required to initialize block lock-bit contents to known values.

When the operation is complete, status register bit SR.5 should be checked. If a clear block lock-bit error is detected, the status register should be cleared. The CUI will remain in read status register mode until another command is issued.

**Table 13. Write Protection Alternatives**

Operation	Block Lock-Bit	WP#	Effect
Program and Block Erase	0	$V_{IL}$ or $V_{IH}$	Block erase and programming enabled
	1	$V_{IL}$	Block is locked. Block erase and programming disabled
		$V_{IH}$	Block Lock-Bit override. Block erase and programming enabled
Full Chip Erase	0,1	$V_{IL}$	All unlocked blocks are erased
	X	$V_{IH}$	Block Lock-Bit override. All blocks are erased
Set or Clear Block Lock-Bit	X	$V_{IL}$	Set or clear block lock-bit disabled
		$V_{IH}$	Set or clear block lock-bit enabled

**Table 14. Configuration Coding Definitions**

Reserved	Pulse on Write Complete	Pulse on Erase Complete							
bits 7–2	bit 1	bit 0							
<p>DQ7–DQ2 = Reserved</p> <p>DQ1/DQ0 = STS Pin Configuration Codes</p> <ul style="list-style-type: none"> <li>00 = default, level mode RY/BY# (device ready) indication</li> <li>01 = pulse on Erase complete</li> <li>10 = pulse on Flash Program complete</li> <li>11 = pulse on Erase or Program Complete</li> </ul> <p>Configuration Codes 01b, 10b, and 11b are all pulse mode such that the STS pin pulses low then high when the operation indicated by the given configuration is completed.</p> <p>Configuration Command Sequences for STS pin configuration (masking bits D7–D2 to 00h) are as follows:</p> <table style="width: 100%; border: none;"> <tr> <td>Default RY/BY# level mode</td> <td style="text-align: right;">B8h, 00h</td> </tr> <tr> <td>ER INT (Erase Interrupt): Pulse-on-Erase Complete</td> <td style="text-align: right;">B8h, 01h</td> </tr> <tr> <td>PR INT (Program Interrupt): Pulse-on-Flash-Program Complete</td> <td style="text-align: right;">B8h, 02h</td> </tr> <tr> <td>ER/PR INT (Erase or Program Interrupt): Pulse-on-Erase or Program Complete</td> <td style="text-align: right;">B8h, 03h</td> </tr> </table>	Default RY/BY# level mode	B8h, 00h	ER INT (Erase Interrupt): Pulse-on-Erase Complete	B8h, 01h	PR INT (Program Interrupt): Pulse-on-Flash-Program Complete	B8h, 02h	ER/PR INT (Erase or Program Interrupt): Pulse-on-Erase or Program Complete	B8h, 03h	<p>DQ7–DQ2 are reserved for future use.</p> <p>default (DQ1/DQ0 = 00) RY/BY#, level mode —used to control HOLD to a memory controller to prevent accessing a flash memory subsystem while any flash device's WSM is busy.</p> <p>configuration 01 ER INT, pulse mode<sup>(1)</sup> —used to generate a system interrupt pulse when any flash device in an array has completed a block erase or sequence of queued block erases. Helpful for reformatting blocks after file system free space reclamation or 'cleanup'</p> <p>configuration 10 PR INT, pulse mode<sup>(1)</sup> —used to generate a system interrupt pulse when any flash device in an array has complete a program operation. Provides highest performance for servicing continuous buffer write operations.</p> <p>configuration ER/PR INT, pulse mode<sup>(1)</sup> —used to generate system interrupts to trigger servicing of flash arrays when either erase or flash program operations are completed when a common interrupt service routine is desired.</p>
Default RY/BY# level mode	B8h, 00h								
ER INT (Erase Interrupt): Pulse-on-Erase Complete	B8h, 01h								
PR INT (Program Interrupt): Pulse-on-Flash-Program Complete	B8h, 02h								
ER/PR INT (Erase or Program Interrupt): Pulse-on-Erase or Program Complete	B8h, 03h								

**NOTE:**

1. When the device is configured in one of the pulse modes, the STS pin pulses low with a typical pulse width of 250 ns.

Table 15. Status Register Definition

WSMS	ESS	ECLBS	BWSLBS	VPPS	BWSS	DPS	R
7	6	5	4	3	2	1	0
SR.7 = WRITE STATE MACHINE STATUS 1 = Ready 0 = Busy  SR.6 = ERASE SUSPEND STATUS 1 = Block erase suspended 0 = Block erase in progress/completed  SR.5 = ERASE AND CLEAR LOCK-BITS STATUS 1 = Error in block erasure or clear lock-bits 0 = Successful block erase or clear lock-bits  SR.4 = PROGRAM AND SET LOCK-BIT STATUS 1 = Error in program or block lock-bit 0 = Successful program or set block lock-bit  SR.3 = V <sub>PP</sub> STATUS 1 = V <sub>PP</sub> low detect, operation abort 0 = V <sub>PP</sub> OK  SR.2 = PROGRAM SUSPEND STATUS 1 = Program suspended 0 = Program in progress/completed  SR.1 = DEVICE PROTECT STATUS 1 = Block Lock-Bit and/or WP# lock detected, operation abort 0 = Unlock  SR.0 = RESERVED FOR FUTURE ENHANCEMENTS				<b>NOTES:</b>  Check STS in RY/BY# mode or SR.7 to determine block erase, programming, or lock-bit configuration completion. SR.6-0 are invalid while SR.7 = "0."  If both SR.5 and SR.4 are "1"s after a block erase or lock-bit configuration attempt, an improper command sequence was entered.  SR.3 does not provide a continuous indication of V <sub>PP</sub> level. The WSM interrogates and indicates the V <sub>PP</sub> level only after a block erase, program, or lock-bit configuration operation. SR.3 reports accurate feedback only when V <sub>PP</sub> = V <sub>PPH</sub> .  SR.1 does not provide a continuous indication of block lock-bit values. The WSM interrogates the block lock-bit, and WP# only after a block erase, program, or lock-bit configuration operation. It informs the system, depending on the attempted operation, if the block lock-bit is set.  SR.0 is reserved for future use and should be masked when polling the status register.			

Table 16. Extended Status Register Definition

WBS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
XSR.7 = WRITE BUFFER STATUS 1 = Write to buffer available 0 = Write to buffer not available  XSR.6-0 = RESERVED FOR FUTURE ENHANCEMENTS				<b>NOTES:</b>  After a Write to buffer command, XSR.7 indicates that another Write to buffer command is possible.  SR.6-0 are reserved for future use and should be masked when polling the status register			

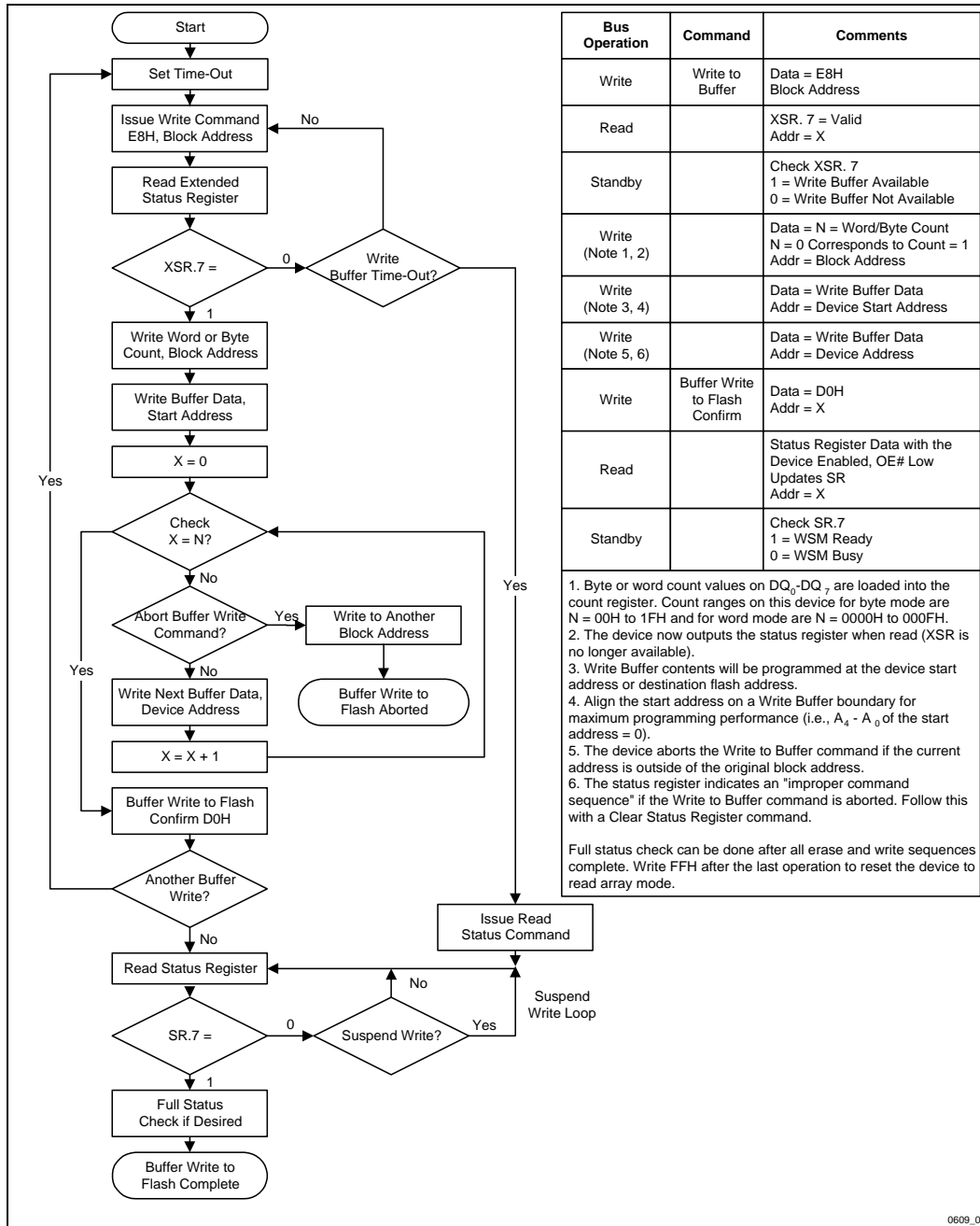


Figure 6. Write to Buffer Flowchart

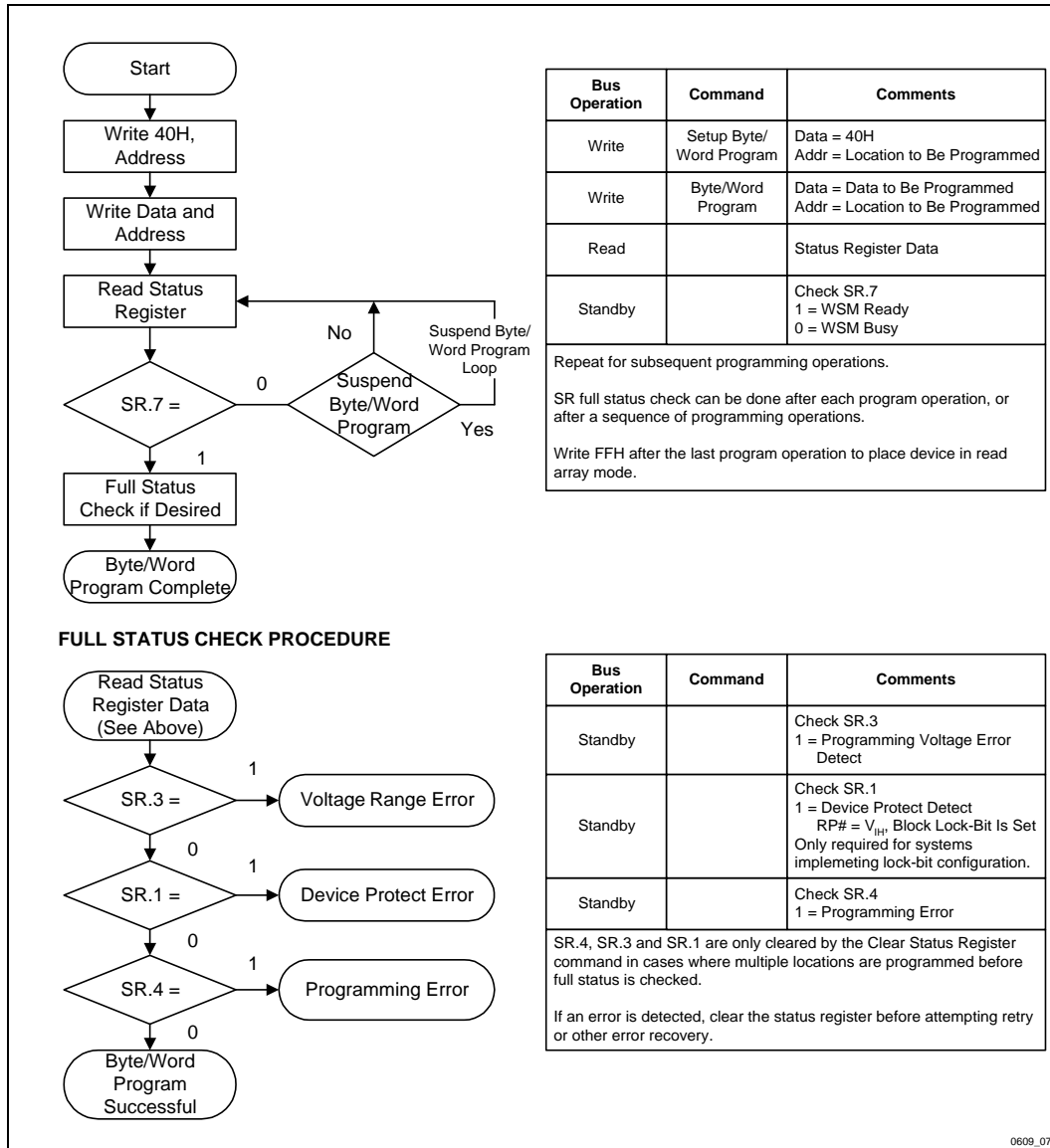


Figure 7. Single Byte/Word Program Flowchart



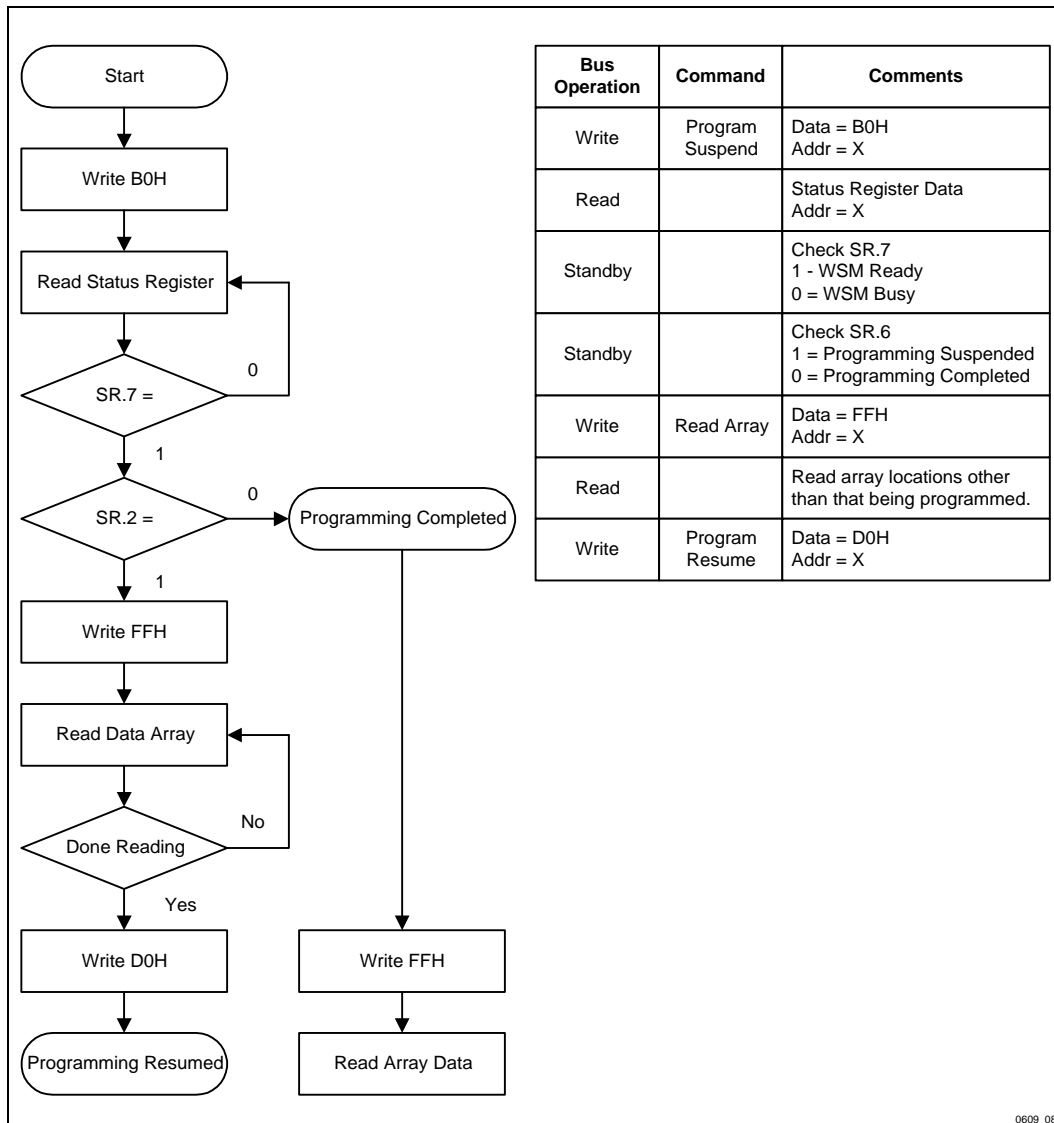


Figure 8. Program Suspend/Resume Flowchart

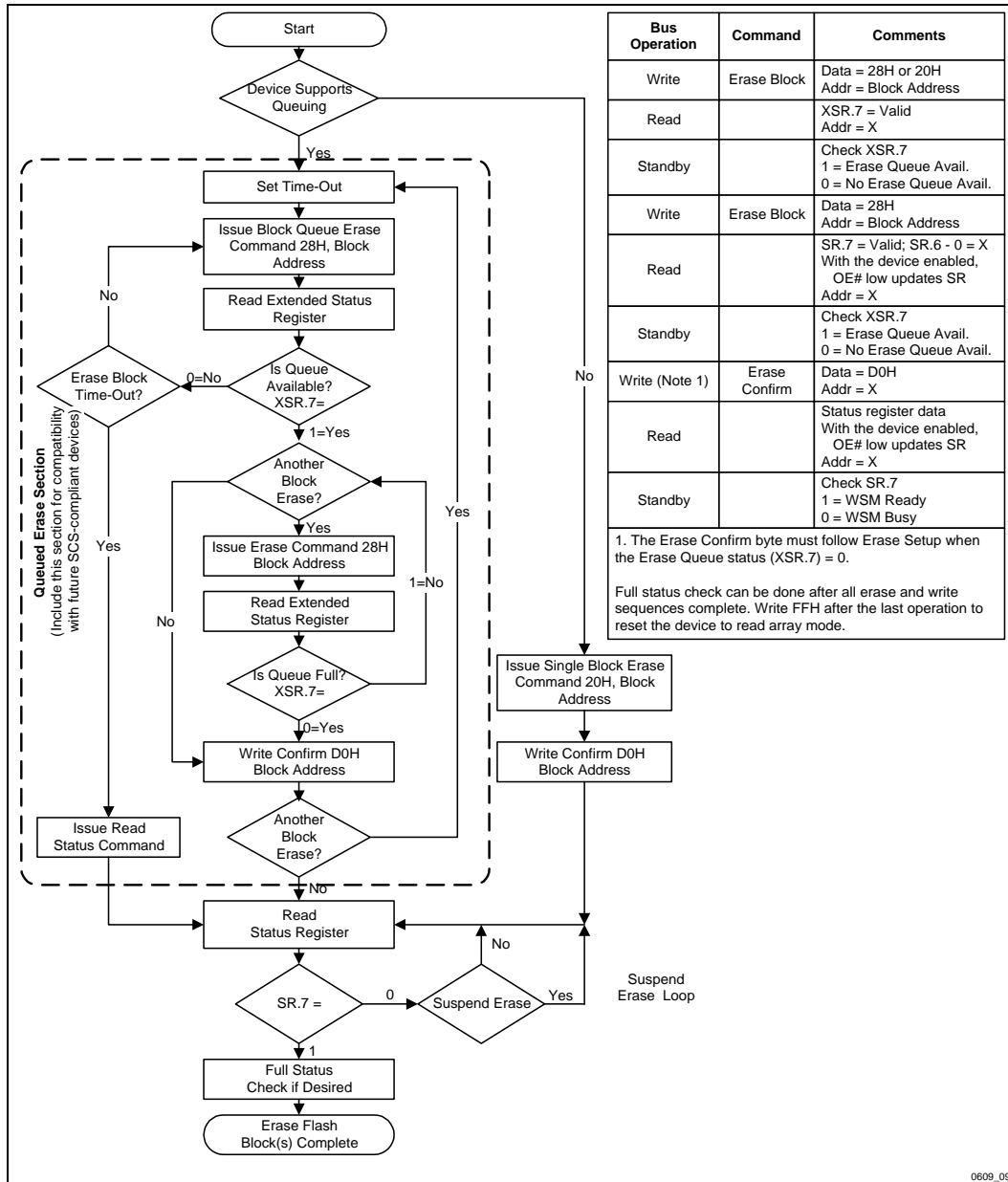


Figure 9. Block Erase Flowchart

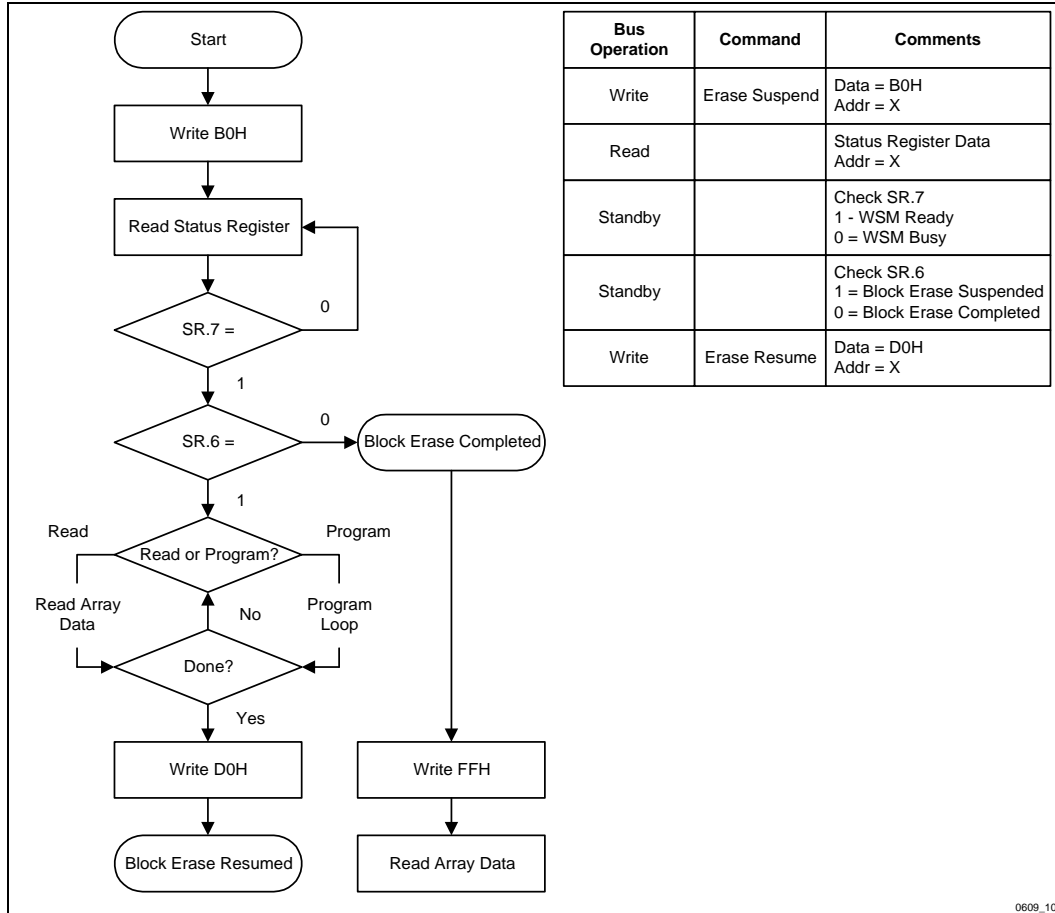


Figure 10. Block Erase Suspend/Resume Flowchart

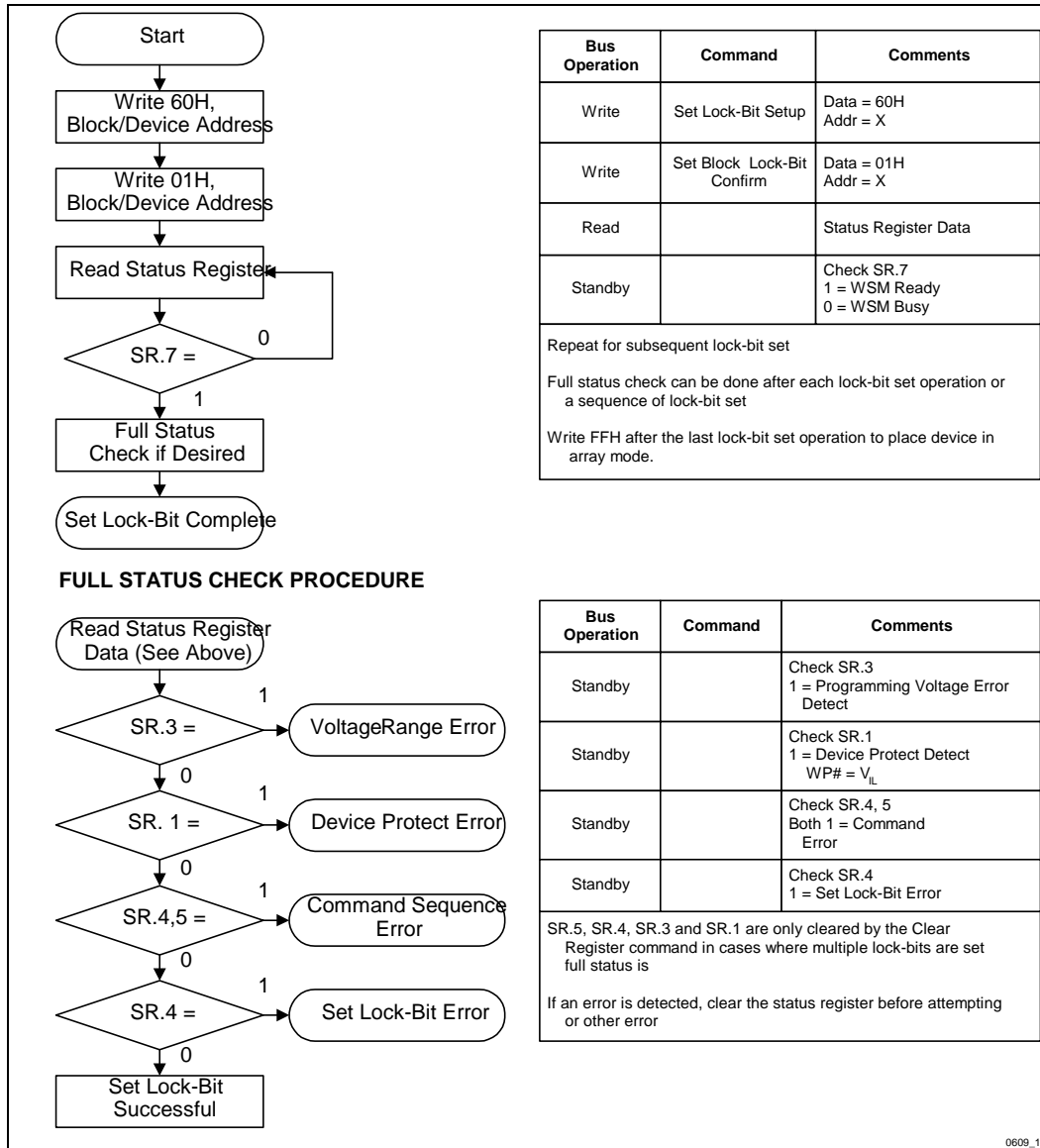


Figure 11. Set Block Lock-Bit Flowchart

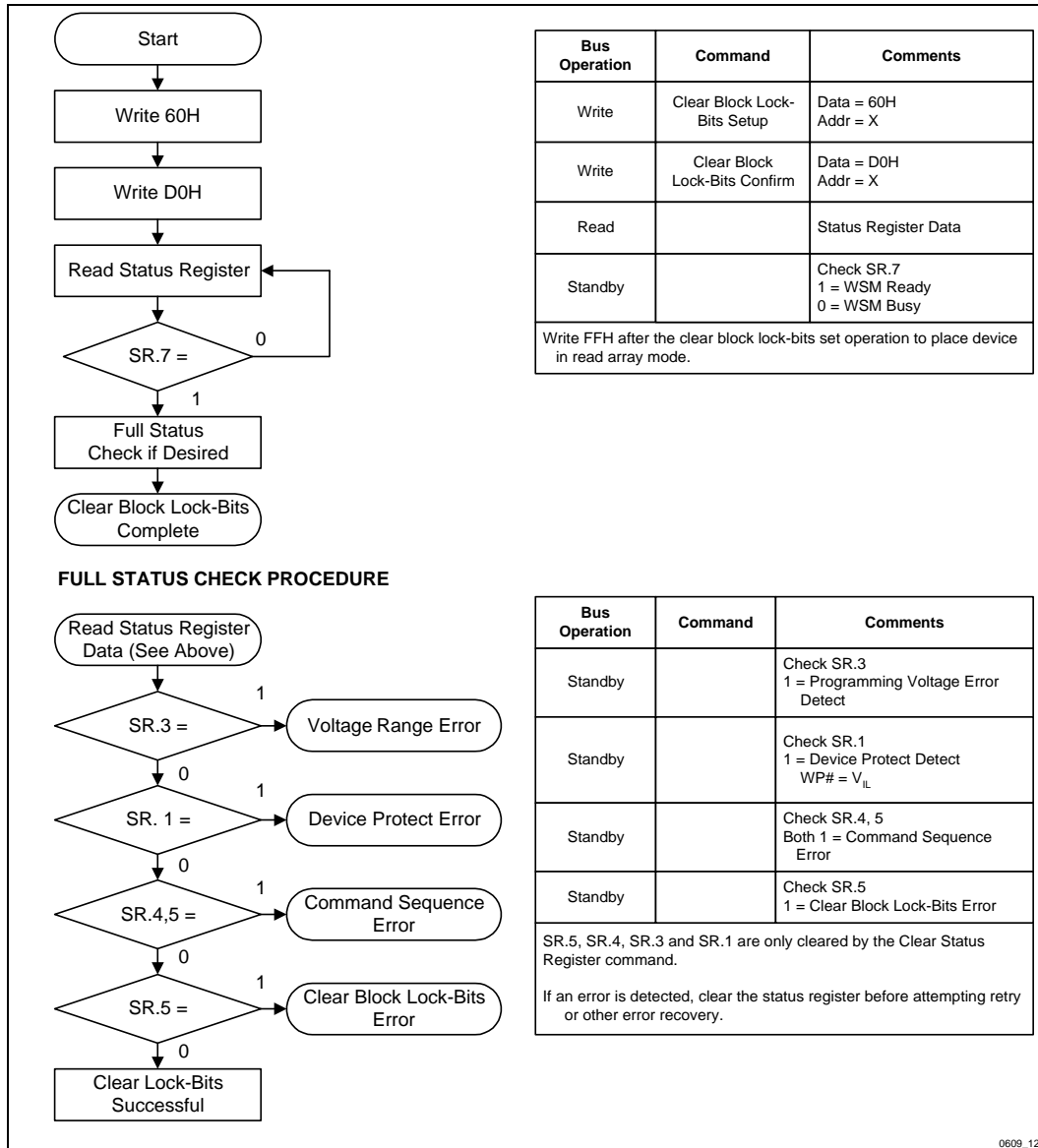


Figure 12. Clear Block Lock-Bits Flowchart

## 5.0 DESIGN CONSIDERATIONS

### 5.1 Three-Line Output Control

Intel provides three control inputs to accommodate multiple memory connections:  $CE_X\#$  ( $CE_0\#$ ,  $CE_1\#$ ),  $OE\#$ , and  $RP\#$ . Three-line control provides for:

- a. Lowest possible memory power dissipation;
- b. Data bus contention avoidance.

To use these control inputs efficiently, an address decoder should enable  $CE_X\#$  while  $OE\#$  should be connected to all memory devices and the system's  $READ\#$  control line. This assures that only selected memory devices have active outputs, while deselected memory devices are in standby mode.  $RP\#$  should be connected to the system  $POWERGOOD$  signal to prevent unintended writes during system power transitions.  $POWERGOOD$  should also toggle during system reset.

### 5.2 STS and WSM Polling

STS is an open drain output that should be connected to  $V_{CC}$  by a pull-up resistor to provide a hardware form of detecting block erase, program, and lock-bit configuration completion. In default mode, it transitions low during execution of these commands and returns to  $V_{OH}$  when the WSM has finished executing the internal algorithm. For alternate STS pin configurations, see Section 4.10. STS can be connected to an interrupt input of the system CPU or controller. It is active at all times. STS, in default mode, is also  $V_{OH}$  when the device is in block erase suspend (with programming inactive) or in reset/power-down mode.

### 5.3 Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. Standby current levels, active current levels and transient peaks produced by falling and rising edges of  $CE_X\#$  and  $OE\#$  are areas of interest. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1  $\mu F$  ceramic capacitor connected between its  $V_{CC}$  and GND and  $V_{PP}$  and GND. These high-frequency, low-inductance capacitors should be placed as close as possible to package leads.

Additionally, for every eight devices, a 4.7  $\mu F$  electrolytic capacitor should be placed at the array's power supply connection between  $V_{CC}$  and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

### 5.4 $V_{PP}$ Trace on Printed Circuit Boards

Updating target-system resident flash memories requires that the printed circuit board designer pay attention to  $V_{PP}$  power supply traces. The  $V_{PP}$  pin supplies the memory cell current for programming and block erasing. Use similar trace widths and layout considerations given to the  $V_{CC}$  power bus. Adequate  $V_{PP}$  supply traces and decoupling will decrease  $V_{PP}$  voltage spikes and overshoots.

### 5.5 $V_{CC}$ , $V_{PP}$ , $RP\#$ Transitions

Block erase, program, and lock-bit configuration are not guaranteed if  $RP\# \neq V_{IH}$ , or if  $V_{PP}$  or  $V_{CC}$  fall outside of a valid voltage range ( $V_{CC1/2}$  and  $V_{PPH}$ ). If  $V_{PP}$  error is detected, status register bit SR.3 and SR.4 or SR.5 are set to "1." If  $RP\#$  transitions to  $V_{IL}$  during block erase, program, or lock-bit configuration, STS in level RY/BY# mode will remain low until the reset operation is complete. Then, the operation will abort and the device will enter deep power-down. Because the aborted operation may leave data partially altered, the command sequence must be repeated after normal operation is restored.

### 5.6 Power-Up/Down Protection

The device offers protection against accidental block erase, programming, or lock-bit configuration during power transitions.

A system designer must guard against spurious writes for  $V_{CC}$  voltages above  $V_{LKO}$  when  $V_{PP}$  is active. Since both  $WE\#$  and  $CE_X\#$  must be low for a command write, driving either input signal to  $V_{IH}$  will inhibit writes. The CUI's two-step command sequence architecture provides an added level of protection against data alteration.

In-system block lock and unlock renders additional protection during power-up by prohibiting block erase and program operations.  $RP\# = V_{IL}$  disables the device regardless of its control inputs states.

## 6.0 ELECTRICAL SPECIFICATIONS

### 6.1 Absolute Maximum Ratings

Temperature under Bias	
Commercial .....	0 °C to +70 °C
Extended .....	-40 °C to +85 °C
Storage Temperature.....	-65 °C to +125 °C
Voltage On Any Pin (except V <sub>CC</sub> and V <sub>PP</sub> )	
.....	-0.5 V to + V <sub>CC</sub> +0.5 V <sup>(1)</sup>
V <sub>CC</sub> Supply Voltage .....	-0.2 V to + V <sub>CC</sub> +0.5 V <sup>(1)</sup>
V <sub>PP</sub> Update Voltage during Block Erase, Flash Write, and Lock-Bit Configuration .....	-0.2 V to +7.0 V <sup>(2)</sup>
Output Short Circuit Current.....	100 mA <sup>(3)</sup>

**NOTICE:** This datasheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

*\*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

**NOTES:**

1. All specified voltages are with respect to GND. Minimum DC voltage is -0.5 V on input/output pins and -0.2 V on V<sub>CC</sub> and V<sub>PP</sub> pins. During transitions, this level may undershoot to -2.0 V for periods <20 ns. Maximum DC voltage on input/output pins and V<sub>CC</sub> is V<sub>CC</sub> +0.5 V which, during transitions, may overshoot to V<sub>CC</sub> +2.0 V for periods <20 ns.
2. Maximum DC voltage on V<sub>PP</sub> may overshoot to +7.0 V for periods <20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.
4. Operating temperature is for extended product defined by this specification.

### 6.2 Operating Conditions

**Table 17. Temperature and V<sub>CC</sub> Operating Conditions (1)**

Symbol	Parameter	Notes	Min	Max	Unit	Test Condition
T <sub>A</sub>	Operating Temperature Commercial Extended		0 -40	+70 +85	°C	Ambient Temperature
V <sub>CC1</sub>	V <sub>CC</sub> Supply Voltage (5 V ± 5%)		4.75	5.25	V	
V <sub>CC2</sub>	V <sub>CC</sub> Supply Voltage (5 V ± 10%)		4.50	5.50	V	

**NOTES:**

1. Device operations in the V<sub>CC</sub> voltage ranges not covered in the table produce spurious results and should not be attempted.

### 6.3 Capacitance (1)

$T_A = +25\text{ }^\circ\text{C}$ ,  $f = 1\text{ MHz}$

Symbol	Parameter	Typ	Max	Unit	Condition
$C_{IN}$	Input Capacitance	6	8	pF	$V_{IN} = 0.0\text{ V}$
$C_{OUT}$	Output Capacitance	8	12	pF	$V_{OUT} = 0.0\text{ V}$

**NOTE:**

1. Sampled, not 100% tested.

### 6.4 DC Characteristics

$T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$  (Extended) and  $T_A = 0\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$  (Commercial)

Sym	Parameter	Notes	Typ	Max	Unit	Conditions
$I_{LI}$	Input Load Current	1		$\pm 1$	$\mu\text{A}$	$V_{CC} = V_{CC\text{ Max}}$ $V_{IN} = V_{CC}$ or GND
$I_{LO}$	Output Leakage Current	1		$\pm 10$	$\mu\text{A}$	$V_{CC} = V_{CC\text{ Max}}$ $V_{out} = V_{CC}$ or GND
$I_{CCS}$	$V_{CC}$ Standby Current	1,3,6	25	100	$\mu\text{A}$	CMOS Inputs $V_{CC} = V_{CC\text{ Max}}$ $CE_{x\#} = RP\# = V_{CC} \pm 0.2\text{ V}$
			2	4	$\text{mA}$	TTL Inputs $V_{CC} = V_{CC\text{ Max}}$ $CE_{x\#} = RP\# = V_{IH}$
$I_{CCD}$	$V_{CC}$ Deep Power-Down Current	16-Mb Commercial Temperature	1	15	$\mu\text{A}$	$RP\# = GND \pm 0.2\text{ V}$ $I_{OUT} (RY/BY\#) = 0\text{ mA}$
		16-Mb Extended Temperature	1	20	$\mu\text{A}$	$RP\# = GND \pm 0.2\text{ V}$ $I_{OUT} (RY/BY\#) = 0\text{ mA}$
		32-Mb Commercial Temperature	1	20	$\mu\text{A}$	$RP\# = GND \pm 0.2\text{ V}$ $I_{OUT} (RY/BY\#) = 0\text{ mA}$
		32-Mb Extended Temperature	1	TBD	$\mu\text{A}$	$RP\# = GND \pm 0.2\text{ V}$ $I_{OUT} (RY/BY\#) = 0\text{ mA}$
$I_{CCR}$	$V_{CC}$ Read Current	1,5,6		50	$\text{mA}$	CMOS Inputs $V_{CC} = V_{CC\text{ Max}}$ $CE_{x\#} = GND$ $f = 8\text{ MHz}$ , $I_{OUT} = 0\text{ mA}$
				65	$\text{mA}$	TTL Inputs $V_{CC} = V_{CC\text{ Max}}$ $CE_{x\#} = V_{IL}$ $f = 8\text{ MHz}$ , $I_{OUT} = 0\text{ mA}$



**6.4 DC Characteristics (Continued)**
 $T_A = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C (Extended) and }T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C (Commercial)}$ 

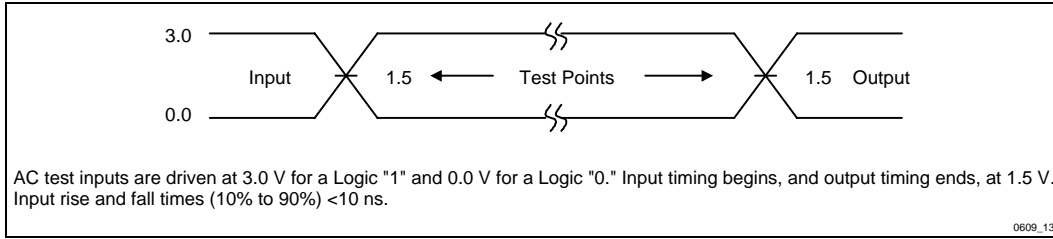
Sym	Parameter	Notes	Typ	Max	Unit	Conditions
I <sub>CCW</sub>	V <sub>CC</sub> Programming and Set Lock-Bit Current	1,7		35	mA	V <sub>PP</sub> = V <sub>PPH</sub>
I <sub>CCE</sub>	V <sub>CC</sub> Block Erase or Clear Block Lock-Bits Current	1,7		30	mA	V <sub>PP</sub> = V <sub>PPH</sub>
I <sub>CCWS</sub> I <sub>CCES</sub>	V <sub>CC</sub> Program Suspend or Block Erase Suspend Current	1,2		10	mA	CEx# = V <sub>IH</sub>
I <sub>PPS</sub> I <sub>PPR</sub>	V <sub>PP</sub> Standby or V <sub>PP</sub> Read Current	1	± 2	± 15	μA	V <sub>PP</sub> ≤ V <sub>CC</sub>
			10	200	μA	V <sub>PP</sub> ≥ V <sub>CC</sub>
I <sub>PPD</sub>	V <sub>PP</sub> Deep Power-Down Current	1	0.1	5	μA	RP# = GND ± 0.2 V
I <sub>PPW</sub>	V <sub>PP</sub> Program or Set Lock-Bit Current	1,7		80	mA	V <sub>PP</sub> = V <sub>PPH</sub>
I <sub>PPE</sub>	V <sub>PP</sub> Block Erase or Clear Block Lock-Bits Current	1,7		40	mA	V <sub>PP</sub> = V <sub>PPH</sub>
I <sub>PPWS</sub> I <sub>PPES</sub>	V <sub>PP</sub> Program Suspend or Block Erase Suspend Current	1	10	200	μA	V <sub>PP</sub> = V <sub>PPH</sub>

**6.4 DC Characteristics (Continued)** $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$  (Extended) and  $T_A = 0\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$  (Commercial)

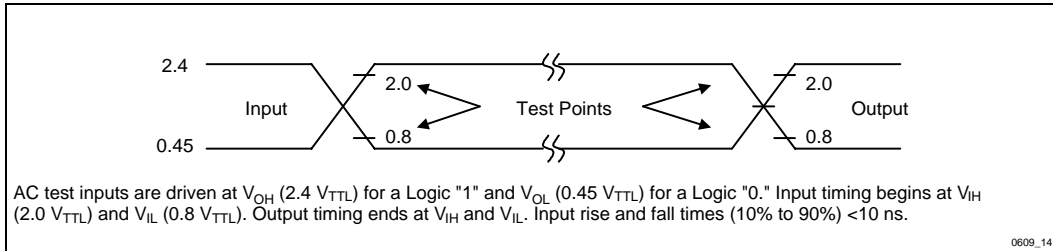
Sym	Parameter	Notes	Min	Max	Unit	Conditions
$V_{IL}$	Input Low Voltage	7	-0.5	0.8	V	
$V_{IH}$	Input High Voltage	7	2.0	$V_{CC} + 0.5$	V	
$V_{OL}$	Output Low Voltage	3,7		0.45	V	$V_{CC} = V_{CC}$ Min $I_{OL} = 5.8\text{ mA}$
$V_{OH1}$	Output High Voltage (TTL)	3,7	2.4		V	$V_{CC} = V_{CC}$ Min $I_{OH} = -2.5\text{ mA}$
$V_{OH2}$	Output High Voltage (CMOS)	3,7	$0.85 \times V_{CC}$		V	$V_{CC} = V_{CC}$ Min $I_{OH} = -2.5\text{ mA}$
			$V_{CC} - 0.4$		V	$V_{CC} = V_{CC}$ Min $I_{OH} = -100\text{ }\mu\text{A}$
$V_{PPLK}$	$V_{PP}$ Lockout Voltage	4,7		1.5	V	
$V_{PPH}$	$V_{PP}$ Voltage	4	4.5	5.5	V	
$V_{LKO}$	$V_{CC}$ Lockout Voltage	8	2.0		V	

**NOTES:**

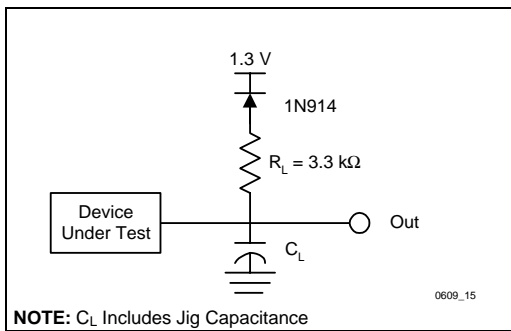
- All currents are in RMS unless otherwise noted. Typical values at nominal  $V_{CC}$  voltage and  $T_A = +25\text{ }^\circ\text{C}$ . These currents are valid for all product versions (packages and speeds).
- $I_{CCWS}$  and  $I_{CCES}$  are specified with the device de-selected. If read or programmed while in erase suspend mode, the device's current is the sum of  $I_{CCWS}$  or  $I_{CCES}$  and  $I_{CCR}$  or  $I_{CCW}$ .
- Includes STS in level RY/BY# mode.
- Block erase, program, and lock-bit configurations are inhibited when  $V_{PP} \leq V_{PPLK}$ . Block erase, program, and lock-bit configurations are not guaranteed between  $V_{PPLK}$  (max) and  $V_{PPH}$  (min) nor above  $V_{PPH}$  (max).
- Automatic Power Savings (APS) reduces typical  $I_{CCR}$  to 1 mA at 5 V  $V_{CC}$  static operation.
- CMOS inputs are either  $V_{CC} \pm 0.2\text{ V}$  or  $\text{GND} \pm 0.2\text{ V}$ . TTL inputs are either  $V_{IL}$  or  $V_{IH}$ .
- Sampled, not 100% tested.
- With  $V_{CC} \leq V_{LKO}$  flash memory writes are inhibited.



**Figure 13. Transient Input/Output Reference Waveform for  $V_{CC} = 5.0\text{ V} \pm 5\%$  (High Speed Testing Configuration)**



**Figure 14. Transient Input/Output Reference Waveform for  $V_{CC} = 5.0\text{ V} \pm 10\%$  (Standard Testing Configuration)**



**Figure 15. Transient Equivalent Testing Load Circuit**

**Test Configuration Capacitance Loading Value**

Test Configuration	$C_L$ (pF)
$V_{CC} = 5.0\text{ V} \pm 5\%$	30
$V_{CC} = 5.0\text{ V} \pm 10\%$	100

## 6.5 AC Characteristics—Read-Only Operations

$T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$  (Extended) and  $T_A = 0\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$  (Commercial)

Versions <sup>(4)</sup>			5 V $\pm$ 5% V <sub>CC</sub>		16 Mb/32 Mb -70/-90			
(All units in ns unless otherwise noted)			5 V $\pm$ 10% V <sub>CC</sub>				16 Mb/ 32Mb -100/-110	
#	Sym	Parameter		Notes	Min	Max	Min	Max
R1	t <sub>AVAV</sub>	Read/Write Cycle Time	16 Mbit	1	70		100	
			32 Mbit	1	90		110	
R2	t <sub>AVQV</sub>	Address to Output Delay	16 Mbit	1		70		100
			32 Mbit	1		90		110
R3	t <sub>ELQV</sub>	CEx# to Output Delay	16 Mbit	2		70		100
			32 Mbit	2		90		110
R4	t <sub>PHQV</sub>	RP# High to Output Delay				400		400
R5	t <sub>GLQV</sub>	OE# to Output Delay		2		30		40
R6	t <sub>ELQX</sub>	CEx# to Output in Low Z		3	0		0	
R7	t <sub>EHQZ</sub>	CEx# High to Output in High Z		3		25		35
R8	t <sub>GLQX</sub>	OE# to Output in Low Z		3	0		0	
R9	t <sub>GHQZ</sub>	OE# High to Output in High Z		3		10		15
R10	t <sub>OH</sub>	Output Hold from Address, CEx#, or OE# Change, Whichever Occurs First		3	0		0	
R11	t <sub>ELFL</sub> t <sub>ELFH</sub>	CEx# Low to BYTE# High or Low		3		5		5
R12	t <sub>FLQV</sub> t <sub>FHQV</sub>	BYTE# to Output Delay	16 Mbit	3		70		100
			32 Mbit	3		90		120
R13	t <sub>FLQZ</sub>	BYTE# to Output in High Z		3		25		30

### NOTES:

1. See AC Input/Output Reference Waveform for maximum allowable input slew rate.
2. OE# may be delayed up to t<sub>ELQV</sub>-t<sub>GLQV</sub> after the falling edge of CEx# without impact on t<sub>ELQV</sub>.
3. Sampled, not 100% tested.
4. See *Ordering Information* for device speeds (valid operational combinations).
5. See Figures 13 through 15 for testing characteristics.

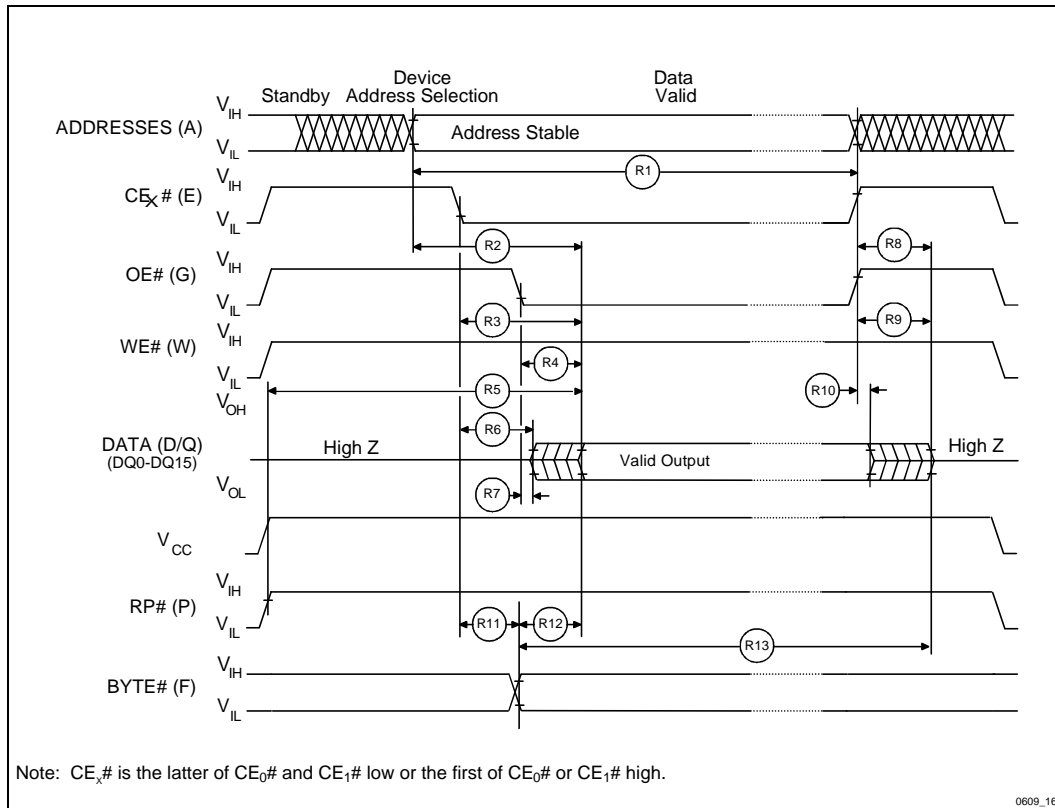


Figure 16. AC Waveform for Read Operations

## 6.6 AC Characteristics—Write Operations<sup>(1, 6)</sup>

T<sub>A</sub> = -40 °C to +85 °C (Extended) and T<sub>A</sub> = 0 °C to +70 °C (Commercial)

Versions <sup>(6)</sup>			5 V ± 5% 5 V ± 10% V <sub>CC</sub>	Valid for All Speeds		Unit
#	Sym	Parameter	Notes	Min	Max	
W1	t <sub>PHWL</sub> (t <sub>PHL</sub> )	RP# High Recovery to WE# (CE <sub>X</sub> # ) Going Low	2	1		µs
W2	t <sub>ELWL</sub>	CE <sub>X</sub> # Setup to WE# Going Low		10		ns
	(t <sub>WLEL</sub> )	(WE# Setup to CE <sub>X</sub> # Going Low)		0		ns
W3	t <sub>WLWH</sub>	WE# Pulse Width		40		ns
	(t <sub>ELEH</sub> )	(CE <sub>X</sub> # Pulse Width)		50		ns
W4	t <sub>DVWH</sub> (t <sub>DVEH</sub> )	Data Setup to WE# (CE <sub>X</sub> # ) Going High	3	40		ns
W5	t <sub>AVWH</sub> (t <sub>AVEH</sub> )	Address Setup to WE# (CE <sub>X</sub> # ) Going High	3	40		ns
W6	t <sub>WHEH</sub>	CE <sub>X</sub> # Hold from WE# High		10		ns
	(t <sub>EHWH</sub> )	(WE# Hold from CE <sub>X</sub> # High)		0		ns
W7	t <sub>WHDX</sub> (t <sub>EHDX</sub> )	Data Hold from WE# (CE <sub>X</sub> # ) High		5		ns
W8	t <sub>WHAX</sub> (t <sub>EHAX</sub> )	Address Hold from WE# (CE <sub>X</sub> # ) High		5		ns
W9	t <sub>WHWL</sub>	WE# Pulse Width High		30		ns
	(t <sub>EHEL</sub> )	(CE <sub>X</sub> # Pulse Width High)		25		ns
W10	t <sub>SHWH</sub> (t <sub>SHEH</sub> )	WP# V <sub>IH</sub> Setup to WE# (CE <sub>X</sub> # ) Going High		100		ns
W11	t <sub>VPWH</sub> (t <sub>VPEH</sub> )	V <sub>PP</sub> Setup to WE# (CE <sub>X</sub> # ) Going High	2	100		ns
W12	t <sub>WHGL</sub> (t <sub>EHGL</sub> )	Write Recovery before Read		0		ns
W13	t <sub>WHRL</sub> (t <sub>EHRL</sub> )	WE# High to STS in RY/BY# Low			90	ns
W14	t <sub>QVSL</sub>	WP# V <sub>IH</sub> Hold from Valid SRD	2,4	0		ns
W15	t <sub>QVVL</sub>	V <sub>PP</sub> Hold from Valid SRD, STS in RY/BY# High	2,4	0		ns

### NOTES:

1. Read timing characteristics during block erase, program, and lock-bit configuration operations are the same as during read-only operations. Refer to *AC Characteristics—Read-Only Operations*.
2. Sampled, not 100% tested.
3. Refer to Table 3 for valid A<sub>N</sub> and D<sub>N</sub> for block erase, program, or lock-bit configuration.
4. V<sub>PP</sub> should be at V<sub>PPH</sub> until determination of block erase, program, or lock-bit configuration success (SR.1/3/4/5 = 0).
5. See *Ordering Information* for device speeds (valid operational combinations).
6. See Figures 13 through 15 for testing characteristics.

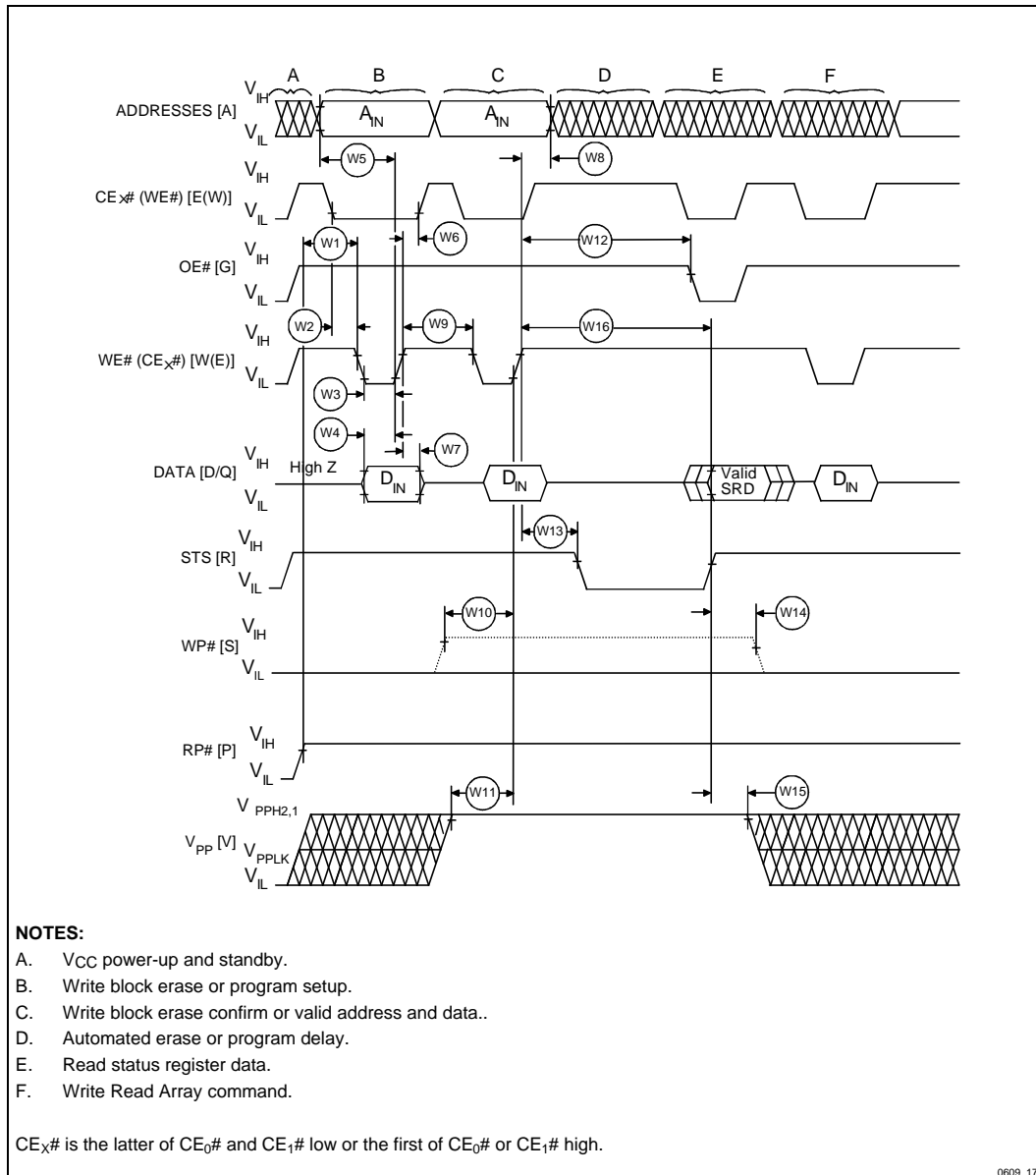


Figure 17. AC Waveform for Write Operations

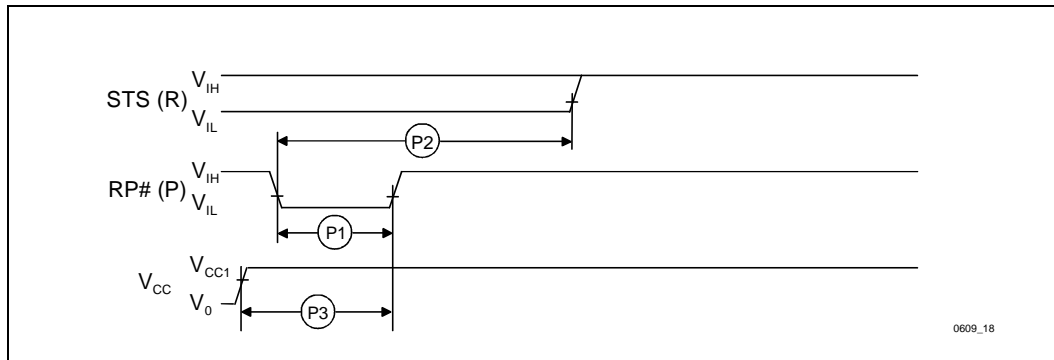


Figure 18. AC Waveform for Reset Operation

Table 18. Reset AC Specifications<sup>(1)</sup>

#	Sym	Parameter	Notes	Min	Max	Unit
P1	$t_{PLPH}$	RP# Pulse Low Time (If RP# is tied to $V_{CC}$ , this specification is not applicable)		100		ns
P2	$t_{PLRH}$	RP# Low to Reset during Block Erase, Program, or Lock-Bit Configuration	2,3		12	$\mu$ s
P3	$t_{5VPH}$	$V_{CC}$ at 4.5 V to RP# High		100		ns

**NOTES:**

1. These specifications are valid for all product versions (packages and speeds).
2. If RP# is asserted while a block erase, program, or lock-bit configuration operation is not executing, the reset will complete within  $t_{PLPH}$ .
3. A reset time,  $t_{PHQV}$ , is required from the latter of STS in RY/BY# mode or RP# going high until outputs are valid.



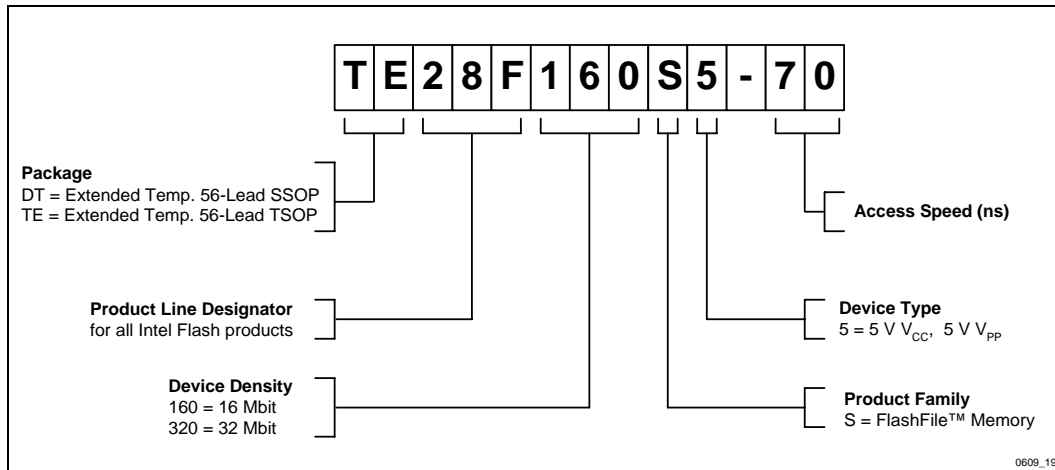
### 6.7 Erase, Write, and Lock-Bit Configuration Performance<sup>(3, 4)</sup> 5 V ± 5%, 5 V ± 10% V<sub>CC</sub>

		Version		Notes	5 V V <sub>PP</sub>		Units
#	Sym	Parameter			Typ <sup>(1)</sup>	Max <sup>(6)</sup>	
W16		Byte/word program time (using write buffer)		5	2	TBD	μs
W16	t <sub>WHQV1</sub> t <sub>EHQV1</sub>	Per byte program time (without write buffer)		2	9.24	90.0	μs
W16	t <sub>WHQV1</sub> t <sub>EHQV1</sub>	Per word program time (without write buffer)		2	9.24	90.0	μs
W16		Block program time (byte mode)		2	0.5	1.0	sec
W16		Block program time (word mode)		2	0.38	0.5	sec
W16		Block program time (using write buffer)		2	0.13	TBD	sec
W16	t <sub>WHQV2</sub> t <sub>EHQV2</sub>	Block erase time		2	0.34	3.5	sec
W16		Full chip erase time	16 Mbit		10.7	112	sec
			32 Mbit		21.4	224	sec
W16	t <sub>WHQV3</sub> t <sub>EHQV3</sub>	Set Lock-Bit time		2	9.24	90.0	μs
W16	t <sub>WHQV4</sub> t <sub>EHQV4</sub>	Clear block lock-bits time		2	0.34	3.5	sec
W16	t <sub>WHRH1</sub> t <sub>EHRH1</sub>	Program suspend latency time to read			5.6	7	μs
W16	t <sub>WHRH2</sub> t <sub>EHRH2</sub>	Erase suspend latency time to read			9.4	13.1	μs

**NOTES:**

1. Typical values measured at T<sub>A</sub> = +25 °C and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Sampled but not 100% tested.
5. Uses whole buffer.
6. Maximum values represent less than 1% of units exposed to greater than 100K cycles

7.0 ORDERING INFORMATION



Order Code by Density		Valid Operational Combinations	
16 Mb	32 Mb	10% V <sub>CC</sub> 100 pF load (16 Mb / 32 Mb)	5% V <sub>CC</sub> 30 pF load (16 Mb / 32 Mb)
TE28F160S5-70		-80	-70
TE28F160S5-100		-100	
DT28F160S5-70	DT28F320S5-90	-80 / -100	-70 / -90
DT28F160S5-100	DT28F320S5-110	-100 / -110	

**8.0 ADDITIONAL INFORMATION (1,2)**

Order Number	Document/Tool
290608	<i>3 Volt FlashFile™ Memory; 28F160S3 and 28F320S3 datasheet</i>
292204	<i>AP-646 Common Flash Interface and Command Sets</i>
292203	<i>AP-645 3 Volt and 5 Volt FlashFile™ Memory Migration Guide</i>
292163	<i>AP-610 Flash Memory In-System Code and Data Update Techniques</i>
297849	<i>Word-Wide FlashFile™ Memory Family 28F160S3, 28F160S5, 28F320S3, 28F320S5 Specification Update</i>
Note 3	<i>28F016SV 16-Mb (1Mbit x 16, 2Mbit x 8) FlashFile™ Memory Datasheet</i>
Note 3	<i>28F016SA 16-Mb (1Mbit x 16, 2Mbit x 8) FlashFile™ Memory Datasheet</i>
Note 3	<i>AP-374 Flash Memory Write Protection Techniques</i>
Note 3	<i>AP-393 28F016SV Compatibility with 28F016SA</i>
Note 3	<i>AP-607 Multi-Site Layout Planning with Intel's FlashFile™ Components, Including ROM Capability</i>
www.mcif.com	<i>Common Flash Interface Specification</i>
Contact Intel/Distribution Sales Office	<i>CFI - Common Flash Interface Reference Code</i>

**NOTES:**

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at <http://www.intel.com> for technical documentation and tools.
3. These documents can be located at the Intel World Wide Web support site, <http://www.intel.com/support/flash/memory>