The HD74LS181 is arithmetic logic unit (ALU)/function generator that have a complexity of 75 equivalent gates. This circuit performs 16 binary arithmetic operations on two 4-bit words as shown in Function Table (Table 1 and 2).

These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer.

When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M).

A full carry look-ahead scheme is made available in this device for fast, simultaneous carry generation by means of two cascade-outputs (pin 15 and 17) for the four bits in the package. When used in conjunction with the HD74182 or HD-74S182, full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown above illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The HD74LS181 will accommodate active-high or active-low data if the pin designations are interpreted as follows.

Pin No.	2	1	23	22	21	20	19	18
Active-high data (Table 1)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3
Active-low data (Table 2)	$\bar{A}_0$	B_0	$\bar{A}_1$	B_1	$\bar{A}_2$	B_2	$\bar{A}_3$	B_3
Pin No.	9	10	11	13	7	16	15	17
Active-high data (Table 1)	F_0	F_1	F_2	F_3	$\bar{C}_n$	$\bar{C}_{n+4}$	X	Y
Active-low data (Table 2)	$\bar{F}_0$	$\bar{F}_1$	$\bar{F}_2$	$\bar{F}_3$	C_n	C_{n+4}	P	G

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-arround or forced carry to provide A-B.

The HD74LS181 can also be utilized as a comparator. The A=B output is internally decoded from the function outputs (F0, F1, F2, 'F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU should be in the subtract mode with Cn=H when performing this comparison. The A=B output is open-collector so that is can be wire-AND connected to give a comparison for more than four bits. The carry output (Cn+4) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

Input Cn	Output C_{n+4}	Active-high data (Table 1)	Active-low data (Table 2)
H	H	$A \leq B$	$A \geq B$
H	L	$A > B$	$A < B$
L	H	$A < B$	$A > B$
L	L	$A \geq B$	$A \leq B$

This circuit have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Table 1 and 2 and include exclusive-OR, NAND, AND NOR, and OR functions.

● Signal Designations

The HD74LS181 together with the HD74182 and HD74-S182 can be used with the signal designations of either Figure 1 or Figure 2. The inversion indicators and the bars over the terminal letter symbols (e.g. $\bar{C}$) each indicate that the associated input or output is active with respect to the selected function of the device when that input or output is low. That is, a low at $\bar{C}$ means "do carry" while a high means "to not carry". The logic functions and arithmetic operations of Figure 2 are given in Table 2.

Figure 1

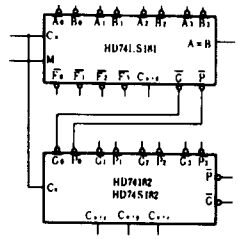
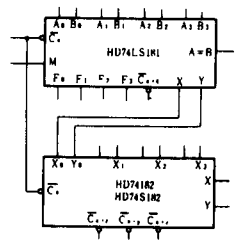


Figure 2



■FUNCTION TABLE

● Table 1

S Inputs				Active-high data		
				M="H"	M="L" : Arithmetic Operations	
S_3	S_2	S_1	S_0	Logic Functions	$\overline{C}_n$="H" (no carry)	$\overline{C}_n$="L" (with carry)
L	L	L	L	$F=\overline{A}$	F=A	F=A plus 1
L	L	L	H	$F=\overline{A+B}$	F=A+B	F=(A+B) plus 1
L	L	H	L	$F=\overline{A}B$	F=A+$\overline{B}$	F=(A+$\overline{B}$) plus 1
L	L	H	H	F=0	F=minus 1 (2's compl)	F=Zero
L	H	L	L	$F=\overline{AB}$	F=A plus A$\overline{B}$	F=A plus A$\overline{B}$ plus 1
L	H	L	H	$F=\overline{B}$	F=(A+B) plus A$\overline{B}$	F=(A+B) plus A$\overline{B}$ plus 1
L	H	H	L	$F=A\oplus B$	F=A minus B minus 1	F=A minus B
L	H	H	H	F=A$\overline{B}$	F=A$\overline{B}$ minus 1	F=A$\overline{B}$
H	L	L	L	$F=\overline{A}+B$	F=A plus AB	F=A plus AB plus 1
H	L	L	H	$F=\overline{A\oplus B}$	F=A plus B	F=A plus B plus 1
H	L	H	L	F=B	F=(A+$\overline{B}$) plus AB	F=(A+$\overline{B}$) plus AB plus 1
H	L	H	H	F=AB	F=AB minus 1	F=AB
H	H	L	L	F=1	F=A plus A*	F=A plus A plus 1
H	H	L	H	F=A+$\overline{B}$	F=(A+B) plus A	F=(A+B) plus A plus 1
H	H	H	L	F=A+B	F=(A+$\overline{B}$) plus A	F=(A+$\overline{B}$) plus A plus 1
H	H	H	H	F=A	F=A minus 1	F=A

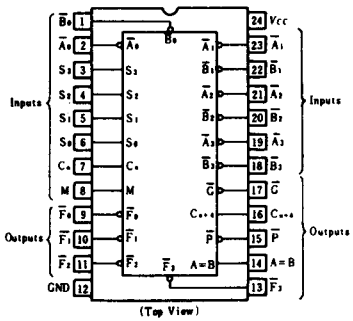
Notes) H; high level, L; low level
* Each bit is shifted to the next more significant position.

●Table 2

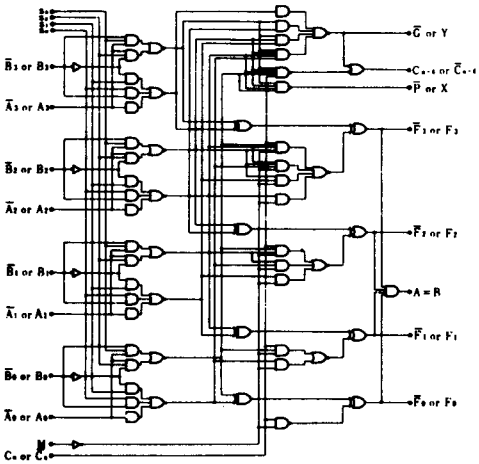
S Inputs				Active-low data		
				M="H"	M="L" : Arithmetic Operations	
S_3	S_2	S_1	S_0	Logic Functions	C_n="L" (no carry)	C_n="H" (with carry)
L	L	L	L	$F=\overline{A}$	F=A minus 1	F=A
L	L	L	H	$F=\overline{AB}$	F=AB minus 1	F=AB
L	L	H	L	$F=\overline{A}+B$	F=A$\overline{B}$ minus 1	F=A$\overline{B}$
L	L	H	H	F=1	F=minus 1 (2's compl)	F=0
L	H	L	L	$F=\overline{A+B}$	F=A plus (A+$\overline{B}$)	F=A plus (A+$\overline{B}$) plus 1
L	H	L	H	F=$\overline{B}$	F=AB plus (A+$\overline{B}$)	F=AB plus (A+$\overline{B}$) plus 1
L	H	H	L	$F=\overline{A\oplus B}$	F=A minus B minus 1	F=A minus B
L	H	H	H	F=A+$\overline{B}$	F=A+$\overline{B}$	F=(A+$\overline{B}$) plus 1
H	L	L	L	F=$\overline{A}$B	F=A plus (A+B)	F=A plus (A+B) plus 1
H	L	L	H	F=A$\oplus$B	F=A plus B	F=A plus B plus 1
H	L	H	L	F=B	F=A$\overline{B}$ plus (A+B)	F=A$\overline{B}$ plus (A+B) plus 1
H	L	H	H	F=A+B	F=A+B	F=(A+B) plus 1
H	H	L	L	F=0	F=A plus A*	F=A plus A plus 1
H	H	L	H	F=A$\overline{B}$	F=AB plus A	F=AB plus A plus 1
H	H	H	L	F=AB	F=A$\overline{B}$ plus A	F=A$\overline{B}$ plus A plus 1
H	H	H	H	F=A	F=A	F=A plus 1

* Each bit is shifted to the next more significant position.

■PIN ARRANGEMENT



■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7.0	V
Input voltage	V_{IN}	5.5	V
Operating temperature range	T_{opr}	−20 ~ +75	℃
Storage temperature range	T_{stg}	−65 ~ +150	℃

■PIN DESIGNATIONS

Item	Functions
$\overline{A}_3, \overline{A}_2, \overline{A}_1, \overline{A}_0$	Word A Inputs
$\overline{B}_3, \overline{B}_2, \overline{B}_1, \overline{B}_0$	Word B Inputs
S_3, S_2, S_1, S_0	Function-Select Inputs
C_n	Ripple-Carry Input
M	Mode Control Input
F_3, F_2, F_1, F_0	Function Outputs
A = B	Comparator Output
$\overline{P}$	Carry Propagate Output
$\overline{C_{n+4}}$	Ripple-Carry Output
$\overline{G}$	Carry Generate Output

■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item		Symbol	Test Conditions		min	typ*	max	Unit
Input voltage		V_{IH}			2.0	–	–	V
		V_{IL}			–	–	0.8	V
Output current △		I_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $V_{OH}=5.5V$		–	–	100	μA
Output voltage △△		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	–	–	V
Output voltage	All outputs	V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$	–	–	0.4	V
				$I_{OL}=8mA$	–	–	0.5	
	output $\overline{G}$			$I_{OL}=16mA$	–	–	0.7	
Input current	Mode	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		–	–	20	μA
	$\overline{A}$, B				–	–	60	
	S				–	–	80	
	Carry				–	–	100	
	Mode	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		–	–	−0.4	mA
	$\overline{A}$, B				–	–	−1.2	
	S				–	–	−1.6	
	Carry				–	–	−2	
	Mode	I_I	$V_{CC}=5.25V$, $V_I=5.5V$		–	–	0.1	mA
	$\overline{A}$, B				–	–	0.3	
	S				–	–	0.4	
	Carry				–	–	0.5	
Short-circuit output current		I_{OS}	$V_{CC}=5.25V$		−20	–	−100	mA
Supply current		I_{CC}**	$V_{CC}=5.25V$	Condition A	–	20	34	mA
				Condition B	–	21	37	
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		–	–	−1.5	V

* $V_{CC}=5V$, $Ta=25°C$

△ A=B output only.

△△ any output except A=B.

** With outputs open, I_{CC} is measured for the following conditions:

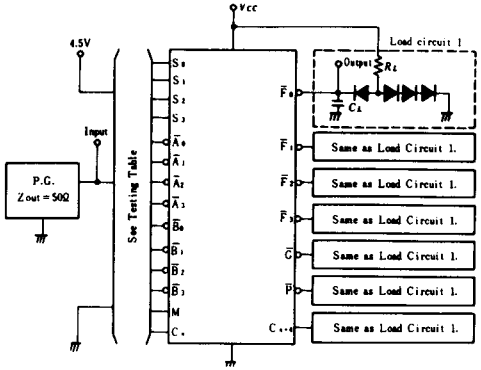
A. S_0 through S_3, M, and $\overline{A}$ inputs are at 4.5V, all other inputs are grounded.

B. S_0 through S_3 and M are at 4.5V, all other inputs are grounded.

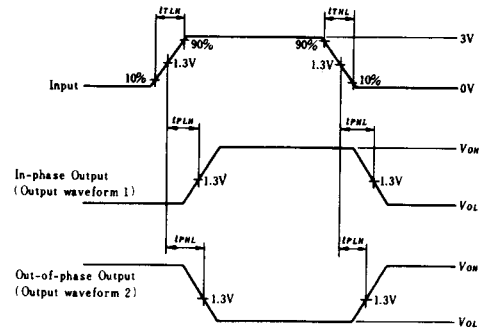
■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$, $C_L=15pF$, $R_L=2k\Omega$)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Propagation delay time	t_{PLH}	C_n	C_{n+4}		–	18	27	ns
	t_{PHL}				–	13	20	
	t_{PLH}	$\overline{A}i$ or $\overline{B}i$	C_{n+4}	M=0V, $S_0=S_3=4.5V$	–	25	38	ns
	t_{PHL}			$S_1=S_2=0V$ (SUM mode)	–	25	38	
	t_{PLH}	$\overline{A}i$ or $\overline{B}i$	C_{n+4}	M=0V, $S_0=S_3=0V$	–	27	41	ns
	t_{PHL}			$S_1=S_2=4.5V$ (DIFF mode)	–	27	41	
	t_{PLH}	C_n	A_n, F	M=0V	–	17	26	ns
	t_{PHL}			(SUM or DIFF mode)	–	13	20	
	t_{PLH}	$\overline{A}i$ or $\overline{B}i$	$\overline{G}$	M=0V, $S_0=S_3=4.5V$	–	19	29	ns
	t_{PHL}			$S_1=S_2=0V$ (SUM mode)	–	15	23	
	t_{PLH}	$\overline{A}i$ or $\overline{B}i$	G	M=0V, $S_0=S_3=0V$	–	21	32	ns
	t_{PHL}			$S_1=S_2=4.5V$ (DIFF mode)	–	21	32	
	t_{PLH}	$\overline{A}i$ or $\overline{B}i$	P	M=0V, $S_0=S_3=4.5V$	–	20	30	ns
	t_{PHL}			$S_1=S_2=0V$ (SUM mode)	–	20	30	
	t_{PLH}	$\overline{A}i$ or $\overline{B}i$	P	M=0V, $S_0=S_3=0V$	–	20	30	ns
	t_{PHL}			$S_1=S_2=4.5V$ (DIFF mode)	–	22	33	
	t_{PLH}	$\overline{A}i$ or $\overline{B}i$	$\overline{F}i$	M=0V, $S_0=S_3=4.5V$	–	21	32	ns
	t_{PHL}			$S_1=S_2=0V$ (SUM mode)	–	13	20	
	t_{PLH}	$\overline{A}i$ or $\overline{B}i$	$\overline{F}i$	M=0V, $S_0=S_3=0V$	–	21	32	ns
	t_{PHL}			$S_1=S_2=4.5V$ (DIFF mode)	–	21	32	
	t_{PLH}	$\overline{A}i$ or $\overline{B}i$	$\overline{F}i$	M=4.5V (logic mode)	–	22	33	ns
	t_{PHL}				–	26	38	
	t_{PLH}	$\overline{A}i$ or $\overline{B}i$	A=B	M=0V, $S_0=S_3=0V$	–	33	50	ns
	t_{PHL}			$S_1=S_2=4.5V$ (DIFF mode)	–	41	62	

■TESTING METHOD



Waveform



Notes) 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

$\overline{\text{SUM}}$ Mode Test Table ($S_0=S_3=4.5V$, $S_1=S_2=M=0V$)

Item	Test inputs	Other inputs		Other data inputs		Test outputs	Output waveform
		4.5V	GND	4.5V	GND		
t_{PLH} / t_{PHL}	$\bar{A}_i$	B_i	–	Remaining $\bar{A}$, B	C_n	F_i	1
t_{PLH} / t_{PHL}	B_i	$\bar{A}_i$	–	Remaining $\bar{A}$, B	C_n	F_i	1
t_{PLH} / t_{PHL}	$\bar{A}_i$	B_i	–	–	Remaining $\bar{A}$, B, C_n	P	1
t_{PLH} / t_{PHL}	B_i	$\bar{A}_i$	–	–	Remaining $\bar{A}$, B, C_n	P	1
t_{PLH} / t_{PHL}	$\bar{A}_i$	–	B_i	Remaining B	Remaining $\bar{A}$, C_n	G	1
t_{PLH} / t_{PHL}	B_i	–	$\bar{A}_i$	Remaining B	Remaining $\bar{A}$, C_n	G	1
t_{PLH} / t_{PHL}	C_n	–	–	All $\bar{A}$	All B	F, C_{n+4}	1
t_{PLH} / t_{PHL}	$\bar{A}_i$	–	B_i	Remaining B	Remaining $\bar{A}$, C_n	C_{n+4}	2
t_{PLH} / t_{PHL}	B_i	–	$\bar{A}_i$	Remaining B	Remaining $\bar{A}$, C_n	C_{n+4}	2

$\overline{\text{DIFF}}$ Mode Test Table ($S_1=S_2=4.5V$, $S_0=S_3=M=0V$)

Item	Test inputs	Other inputs		Other data inputs		Test outputs	Output waveform
		4.5V	GND	4.5V	GND		
t_{PLH} / t_{PHL}	$\bar{A}_i$	–	B_i	Remaining $\bar{A}$	Remaining B, C_n	F_i	1
t_{PLH} / t_{PHL}	B_i	$\bar{A}_i$	–	Remaining $\bar{A}$	Remaining B, C_n	F_i	2
t_{PLH} / t_{PHL}	$\bar{A}_i$	–	B_i	–	Remaining $\bar{A}$, B, C_n	P	1
t_{PLH} / t_{PHL}	B_i	$\bar{A}_i$	–	–	Remaining $\bar{A}$, B, C_n	P	2
t_{PLH} / t_{PHL}	$\bar{A}_i$	B_i	–	–	Remaining $\bar{A}$, B, C_n	G	1
t_{PLH} / t_{PHL}	B_i	–	$\bar{A}_i$	–	Remaining $\bar{A}$, B, C_n	G	2
t_{PLH} / t_{PHL}	$\bar{A}_i$	–	B_i	Remaining $\bar{A}$	Remaining B, C_n	$A=B$	1
t_{PLH} / t_{PHL}	B_i	$\bar{A}_i$	–	Remaining $\bar{A}$	Remaining B, C_n	$A=B$	2
t_{PLH} / t_{PHL}	C_n	–	–	All $\bar{A}$, B	–	C_{n+4}, F	1
t_{PLH} / t_{PHL}	$\bar{A}_i$	B_i	–	–	Remaining $\bar{A}$, B, C_n	C_{n+4}	2
t_{PLH} / t_{PHL}	B_i	–	$\bar{A}_i$	–	Remaining $\bar{A}$, B, C_n	C_{n+4}	1

Logic Mode Test Table ($S_1=S_2=M=4.5V$, $S_0=S_3=0V$)

Item	Test inputs	Other inputs		Other data inputs		Test outputs	Output waveform
		4.5V	GND	4.5V	GND		
t_{PLH} / t_{PHL}	$\bar{A}_i$	B_i	–	–	Remaining $\bar{A}$, B, C_n	F_i	2
t_{PLH} / t_{PHL}	B_i	$\bar{A}_i$	–	–	Remaining $\bar{A}$, B, C_n	F_i	2

PACKAGING INFORMATIONS

T-90-20

Factory orders for circuits described in this databook should include a three-part type number as explained in the following example.

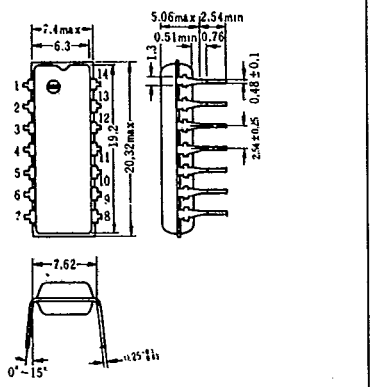
HD 74LS00 P

- Package ; Plastic DIP ; letters P
  Cerdip ; non-letters
- Circuit description
- Prefix : HD ; Hitachi Digital IC

■Plastic DIP

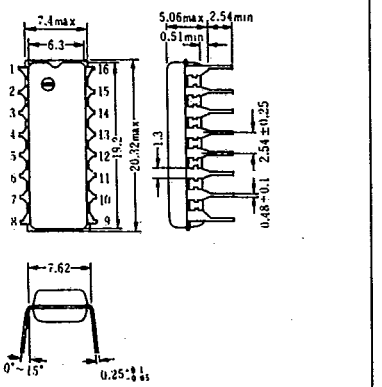
●14 Pin

DP-14



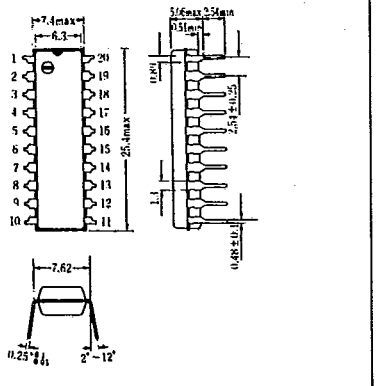
●16 Pin

DP-16



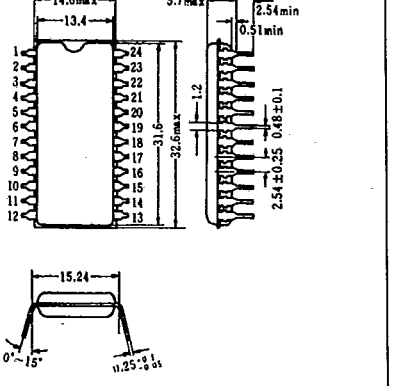
●20 Pin

DP-20



●24 Pin

DP-24

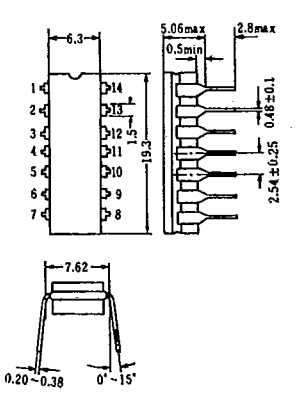


PACKAGING INFORMATIONS

■Cerdip

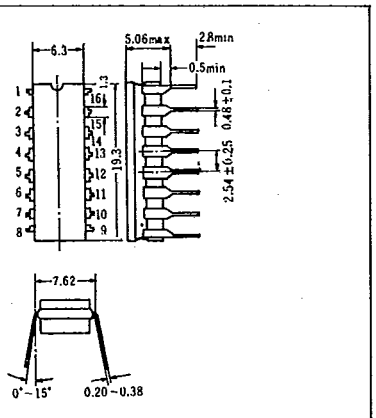
●14 Pin

DG-14



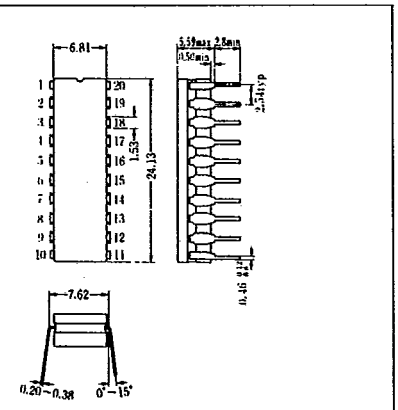
●16 Pin

DG-16



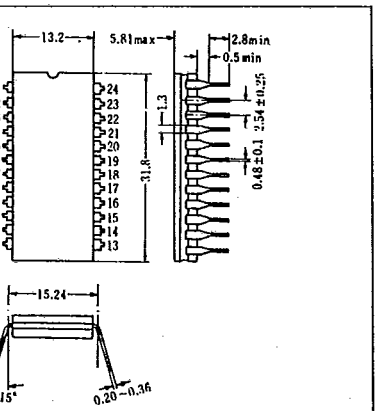
●20 Pin

DG-20



●24 Pin

DG-24



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Hitachi America Ltd. • 2210 O'Toole Ave. • San Jose, CA 95131 • (408) 435-8300