MP8785

CMOS
8-Bit High Speed
Analog-to-Digital Converter

March 1998-3

FEATURES

- 8-Bit Resolution
- 20 MHz Sampling Rate
- DNL = ±1/2 LSB, INL = ±1 LSB (typ)
- Internal S/H Function
- Single Supply: 5 V
- V_{IN} DC Range: 0 V to V_{DD}
- V_{REF} DC Range: 1 V to V_{DD}
- Low Power: 85 mW typ. (excluding reference)
- Latch-Up Free
- ESD Protection: 2000 V Minimum

FEATURES (CONT D)

- Monotonic. No Missing Codes
- 20 Pin Package Available: MP8775
- Power Down Available: MP8786
- 3 V Version: MP87L85

APPLICATIONS

- Digital Color Copiers
- Cellular Telephones
- CCD s and Scanners
- Video Capture Boards

GENERAL DESCRIPTION

The MP8785 is an 8-bit Analog-to-Digital Converter. Designed using an advanced 5 V CMOS process, this part offers excellent performance, low power consumption and latch-up free operation.

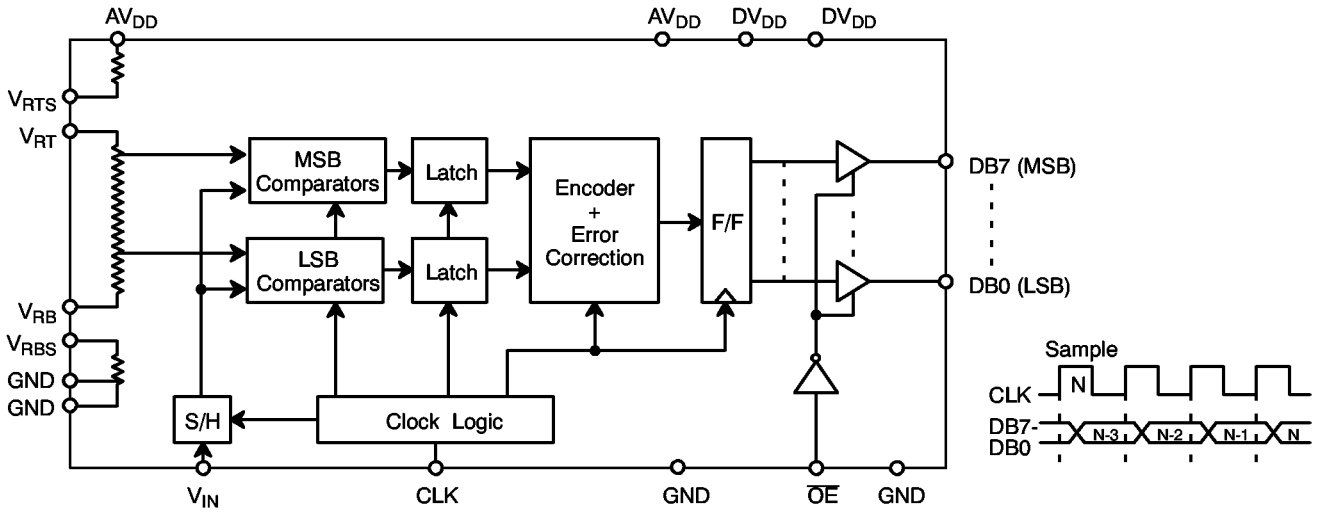
This device uses a two-step flash architecture to maintain low power consumption at high conversion rates. The input circuitry of the MP8785 includes an on-chip S/H function which allows the user to digitize analog input signals between AGND and AV_{DD}. Careful design and chip layout have achieved a low analog input capacitance. This reduces kickback and eases the requirements of the buffer/amplifier used to drive the MP8785.

The designer can choose the internally generated reference voltages by connecting V_{RB} to V_{RBS} and V_{RT} to V_{RTS}, or provide external reference voltages to the V_{RB} and V_{RT} pins. The internal reference generates 0.6 V at V_{RB} and 2.6 V at V_{RT}. Providing external reference voltages allows easy interface to any input signal range between AGND and AV_{DD}. This also allows the system to adjust these voltages to cancel zero scale and full scale errors, or to change the input range as needed.

The device operates from a single +5 V supply. Power consumption is 85 mW at FS = 20 MHz.

Specified for operation over the commercial / industrial (-40 to +85°C) temperature range, the MP8785 is available in Plastic dual-in-line (PDIP) and Surface Mount (SOIC) packages in EIAJ and Jedec.

SIMPLIFIED BLOCK AND TIMING DIAGRAM



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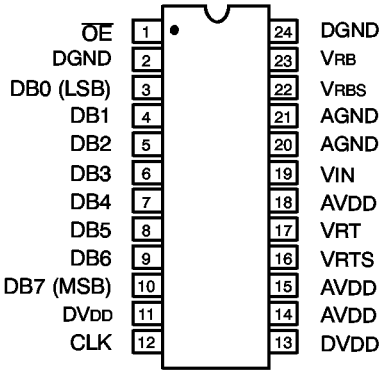
ORDERING INFORMATION

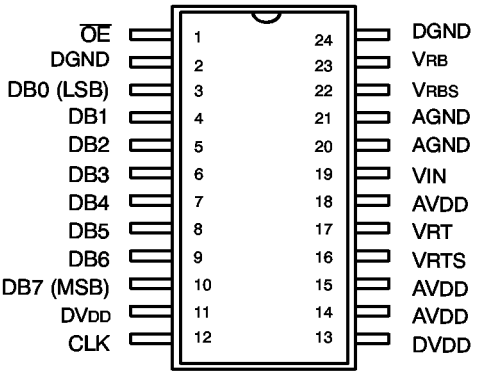
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
SOIC (EIAJ)	-40 to +85°C	MP8785AR	±3/4	1 1/2
SOIC (Jedec)	-40 to +85°C	MP8785AS	±3/4	1 1/2
Plastic Dip (0.300)	-40 to +85°C	MP8785AN	±3/4	1 1/2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



24 Pin PDIP (0.300)



24 Pin SOIC (EIAJ, 0.300)
24 Pin SOIC (Jedec, 0.300)

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	$\overline{OE}$	Output Enable
2	DGND	Digital Ground
3	DB0	Data Output Bit 0 (LSB)
4	DB1	Data Output Bit 1
5	DB2	Data Output Bit 2
6	DB3	Data Output Bit 3
7	DB4	Data Output Bit 4
8	DB5	Data Output Bit 5
9	DB6	Data Output Bit 6
10	DB7	Data Output Bit 7 (MSB)
11	DVDD	Digital Power Supply
12	CLK	Sampling Clock Input

PIN NO.	NAME	DESCRIPTION
13	DVDD	Digital Power Supply
14	AVDD	Analog Power Supply
15	AVDD	Analog Power Supply
16	VRTS	Generates 2.6 V if tied to V_{RT}
17	VRT	Top Reference
18	AVDD	Analog Power Supply
19	VIN	Analog Input
20	AGND	Analog Ground
21	AGND	Analog Ground
22	VRBS	Generates 0.6 V if tied to V_{RB}
23	VRB	Bottom Reference
24	DGND	Digital Ground

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, FS = 15 MHz (50% Duty Cycle), V_{RT} = 2.6 V, V_{RB} = 0.6 V, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		8				Bits
Max. Sampling Rate	FS	15	20		MHz	
ACCURACY (A Grade)[1]						
Differential Non-Linearity	DNL			±3/4	LSB	@ 15 MHz
Differential Non-Linearity	DNL			±1/2	LSB	@ 10 MHz
Integral Non-Linearity	INL			±1 1/2	LSB	Best Fit Line (Max INL - Min INL)/2
Zero Scale Error	EZS		±3		LSB	
Full Scale Error	EFS		±3		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage[3]	V_{RT}		2.6	AV_{DD}	V	
Negative Ref. Voltage[3]	V_{RB}	AGND	0.6		V	
Differential Ref. Voltage[3]	V_{REF}	1.0		AV_{DD}	V	$V_{REF} = V_{RT} - V_{RB}$
Ladder Resistance	R_L	245	350	500	Ω	
Ladder Temp. Coefficient	R_{TCO}		2000		ppm/°C	
Self Bias 1						
Short V_{RB} and V_{RBS}	V_{RB}		0.6		V	
Short V_{RT} and V_{RTS}	V_{RT}-V_{RB}		2		V	
Self Bias 2						
V_{RB} = AGND, Short V_{RT} and V_{RTS}	V_{RT}		2.3		V	
ANALOG INPUT						
Input Bandwidth (-1 dB)[4]	BW		14		MHz	
Input Voltage Range	V_{IN}	V_{RB}		V_{RT}	V	
Input Capacitance[5]	C_{IN}		16		pF	
Aperture Delay	t_{AP}	15	20	25	ns	
DIGITAL INPUTS						
Logical 1 Voltage	V_{IH}	4.0			V	
Logical 0 Voltage	V_{IL}			1.0	V	
DC Leakage Currents[6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK			5		µA	
$\overline{OE}$			5		µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1.*)[7]						
Clock Period[3]	1/FS		50		ns	
High Pulse Width[3]	t_{PWH}		25		ns	
Low Pulse Width[3]	t_{PWL}		25		ns	
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical 1 Voltage	V_{OH}	4.5			V	I_{LOAD} = 4 mA
Logical 0 Voltage	V_{OL}			0.4	V	I_{LOAD} = 4 mA
3-state Leakage	I_{OZ}		10		µA	V_{OUT}=DGND to DV_{DD}
Data Valid Delay[2, 8]	t_{DL}	18	20	25	ns	
Data Enable Delay[2]	t_{DEN}	16	20	25	ns	
Data 3-state Delay[2]	t_{DHZ}	10	12	15	ns	

ELECTRICAL CHARACTERISTICS TABLE (CONT D)

Description	Symbol	25°C Min	25°C Typ	25°C Max	Units	Conditions
AC PARAMETERS						
Differential Gain Error	dg		2		%	FS = 4 x NTSC
Differential Phase Error	d_{ph}		1		Degree	FS = 4 x NTSC
POWER SUPPLIES						
Operating Voltage (AV_{DD}, DV_{DD})[9]	V_{DD}	4.5	5	5.5	V	
Current (AGND + DGND)	I_{DD}		17	25	mA	Does not include ref. current

Notes:

1 *Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/256) is the DNL error (Figure 3.). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (Figure 4.). Accuracy is a function of the sampling rate (FS).*

2 *Guaranteed. Not tested.*

3 *Specified values guarantee functionality. Refer to other parameters for accuracy.*

4 *-1 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.*

5 *See V_{IN} input equivalent circuit (Figure 5.). Switched capacitor analog input requires driver with low output resistance.*

6 *All inputs have diodes to DV_{DD} and DGND. Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.*

7 *t_R, t_F should be limited to >5 ns for best results.*

8 *Depends on the RC load connected to the output pin.*

9 *AGND & DGND pins are connected through the silicon substrate. Connect together at the package and to the analog ground plane.*

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... 7 V
V_{RT} & V_{RB} ..... V_{DD} +0.5 to GND -0.5 V
V_{IN} ..... V_{DD} +0.5 to GND -0.5 V
All Inputs ..... V_{DD} +0.5 to GND -0.5 V
All Outputs ..... V_{DD} +0.5 to GND -0.5 V

Storage Temperature ..... -65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating @ 75°C
PDIP, SOIC 850mW
Derates above 75°C ..... 12mW/°C

Notes

1 *Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.*

2 *Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100μs.*

3 *V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.*

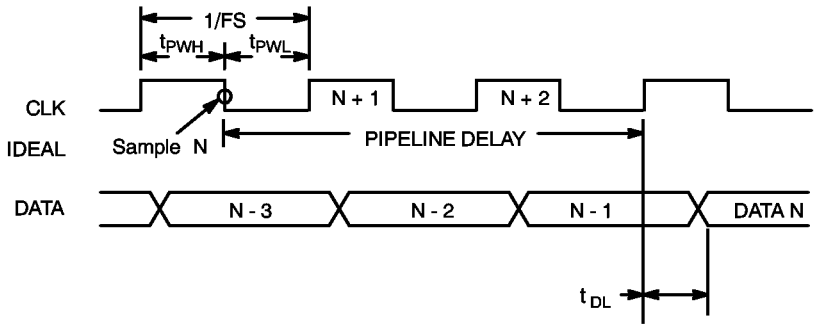


Figure 1. MP8785 Timing Diagram

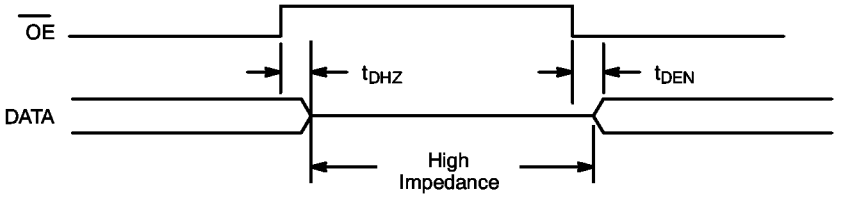
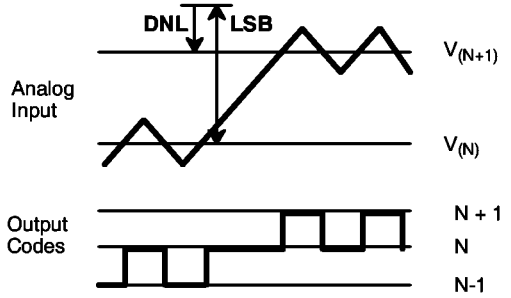


Figure 2. Output Enable/Disable Timing Diagram



Code Width (N) = $V_{(N+1)}$ - $V_{(N)}$
LSB = [V_{RT} - V_{RB}] / 256

$DNL_{(N)}$ = [$V_{(N+1)}$ - $V_{(N)}$] - LSB

Figure 3. DNL Measurement

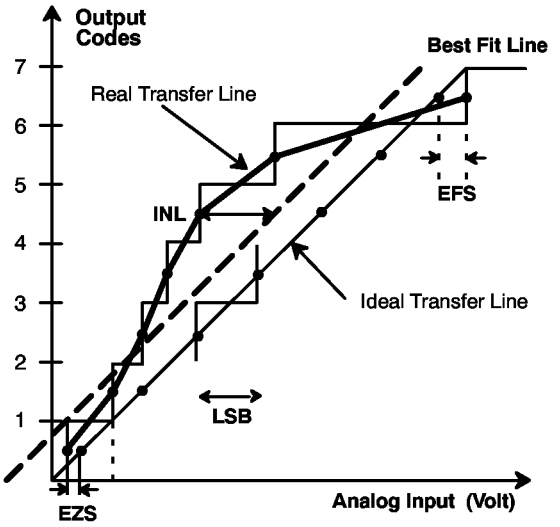


Figure 4. INL Error Calculation

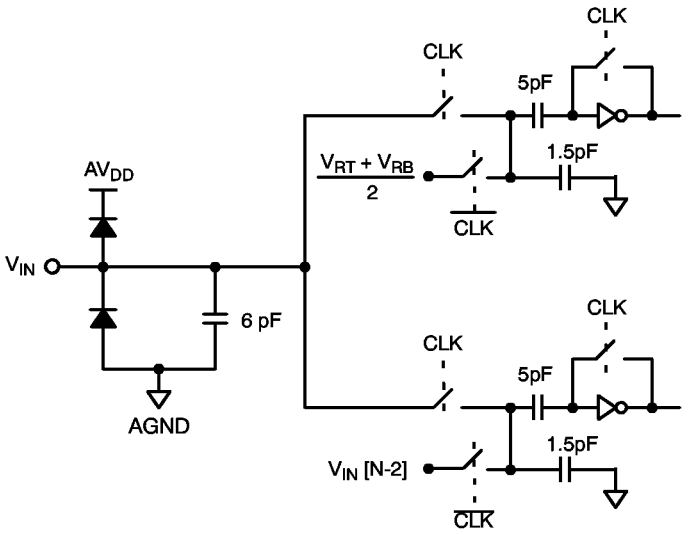


Figure 5. Equivalent Input Circuit

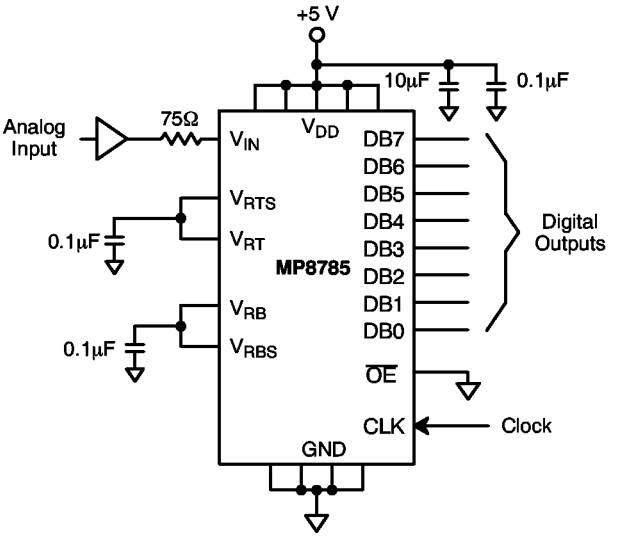


Figure 6. Typical Circuit Connections

APPLICATION NOTES

Signals should not exceed V_{DD} +0.5V or go below GND -0.5V. All pins have internal protection diodes that will protect them from short transients (<100µs) outside the supply range.

AGND and DGND pins are connected internally through the P-substrate. DC voltage differences between GND pins will cause undesirable internal substrate currents.

The power supply (V_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with 0.1µF and 10µF capacitors to AGND, placed as close to the chip as possible.

The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion.

It is possible for the data valid delay (t_{DL}) to be equal to or greater than the high pulse width of the sampling clock (t_{PWH}), See *Figure 1.* This can cause timing related errors. For sample rates above 14 MSPS, use only the rising edge of the sample clock (CLK) to latch data from the MP8785 to other parts of the system.

The reference can be biased internally by shorting V_{RT} to V_{RTS} and V_{RB} to V_{RBS}. This will generate 0.6 V at V_{RB} and 2.6 V at V_{RT} (see *Figure 5.)*.

If the internal reference pins V_{RTS} and/or V_{RBS} are not used, they should be left unconnected.

The output enable pin ($\overline{OE}$) should not be left unconnected. If not controlled by an active signal then it must be tied to DGND.

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