8 Port 10/100 Mbit/s Dual Speed Fast Ethernet Switch

- Supports eight 10/100 Mbit/s Ethernet ports with MII and RMII interface
- Capable of trunking for up to 800 Mbit/s link
- Full- and half-duplex mode operation
- Speed auto-negotiation through MDIO
- Built-in storage of 1K MAC addresses expandable to 16K
- Designed to utilize low-cost SGRAM
- Scalable design for stackable switch implementation
- RoX expansion link supports 4.8 Gbit/s throughput
- Serial EEPROM interface for low-cost system configuration
- Gigabit Ethernet ready
- Automatic source address learning
- Secure mode traffic filtering
- Broadcast storm control
- Port monitoring support
- IEEE 802.3x flow control for full-duplex operation
- Optional backpressure flow control support for half-duplex operation
- Supports store-and-forward mode switching
- VLAN support
- RMON and SNMP support with external management (MIB) device
- 3.3V operation
- Packaged in 456-pin BGA

Product Description

The AL116 is an eight-port 10/100 Mbit/s dual speed Ethernet switch. A low-cost and scalable solution for up to 32 ports is achieved through the use of low-cost buffer memory and Allayer's proprietary RoX™ architecture. In addition, the AL116 supports VLAN and multiple link aggregation trunks.

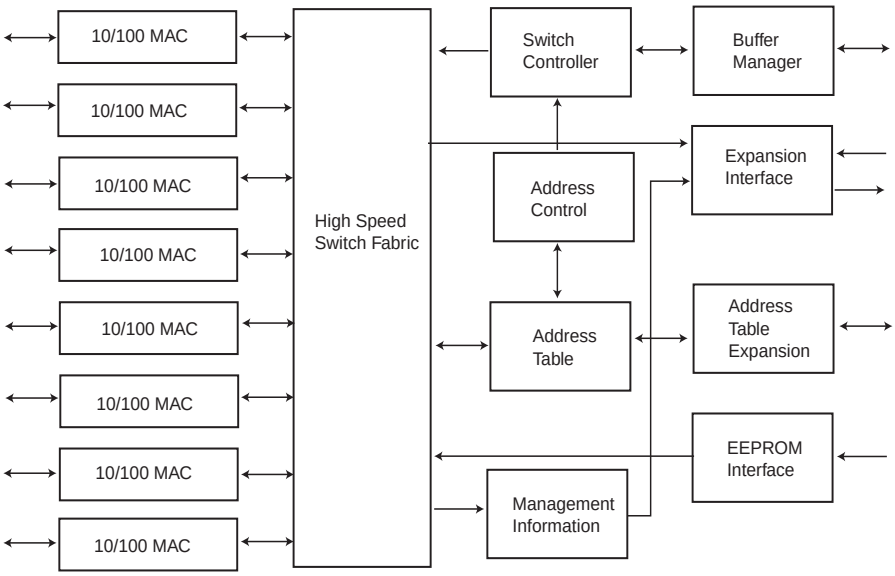

Figure 1 System Block Diagram

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1. AL116 Overview

The RoX interface is a 2.4 Gbit/s interface (4.8 Gbit/s full-duplex). The interface can support up to four switch chips. Various combinations can be used for different configurations. The maximum port configuration will be either 32-100 Mbit/s ports or 24-100 Mbit/s ports plus two Gigabit Ethernet ports.

The RoX interface also supports an external management device, the AL300A. SNMP and RMON are supported through this external management device.

The AL116 provides eight 10/100 Mbit/s Ethernet ports. Each port supports both 10 and 100 Mbit/s data rate. The operation mode is auto-negotiated by the PHY. All ports are full-duplex capable. The device also supports VLAN for workgroup and segment switching applications.

The AL116 also supports trunking applications. The chip provides two optional load balancing schemes, explicit and dynamic. With trunking, it is possible to group up to four full-duplex links together to form a single 800 Mbit/s link.

Data received from the MAC interface is stored in the external memory buffer. The AL116 utilizes cost effective SGRAM to provide 8-Mbit or 16-Mbit of buffer memory.

During transmission, the data is obtained from the buffer memory and routed to the destination port. In the event of a collision during half-duplex operations, the MAC control will back off and retransmit in accordance to the IEEE 802.3 specification.

The AL116 provides two flow control methods. For half-duplex operations, an optional jamming based flow control (also known as backpressure) is available to prevent loss of data. With this method of flow control, the switch will generate a jam signal when the receive-buffer is full. The sending station will not transmit until the line is clear. In the full-duplex mode, the AL116 utilizes IEEE 802.3x as the flow control mechanism.

All ports support multiple MAC addresses. The switch chip supports up to 1K MAC addresses internally. These MAC addresses are shared among all eight ports. Additional SRAM can be added to provide support for 16K MAC addresses.

The initialization and configuration of the switch is programmed by an external EEPROM. For an unmanaged switch design, there is no need for a CPU. Field reconfiguration can be achieved by using a parallel interface to reprogram the EEPROM.

For managed switch applications the AL116 supports network management through the network management option. When the management option is enabled, network statistic for each port are gathered and sent across the RoX bus. The management information base chip on the bus will collect and store the data for network management agent. Access to the statistic counters is provided via the CPU interface of the MIB device.

The AL116 also supports port based VLAN. The VLAN register set is used to configure the destination ports for multicast and broadcast frames.

The device also provides two levels of security for intrusion protection. Security can be implemented on a per port basis.

The AL116 operates only in the store and forward mode. The entire frame is checked for error. Frames with errors are automatically filtered and will not be forwarded to the destination port.

Other features include port monitoring and broadcast storm throttling.

AL116 Pin Diagram

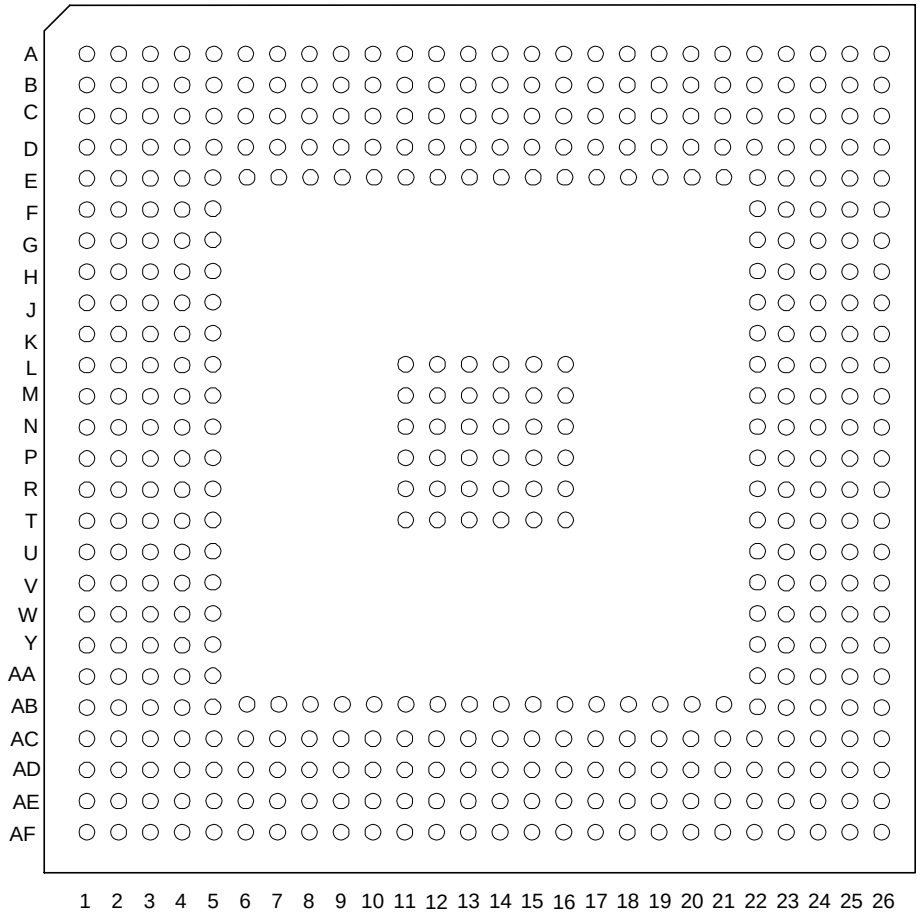

Figure 2 Pin Diagram (Top View)

2. Pin Descriptions

The AL116 also supports RMII interface. When RMII interface is used TXD3, TXD2, TXCLK, RXDV, RXER, and COL should be left unconnected. The RXCLK should be connected to the reference clock. A RXCLK is provided for each individual port to reduce clock skew.

Table 1: RMII/MII Interface (Port 0)

PIN NAME	PIN NO.	I/O	DESCRIPTION
M0TXD3 M0TXD2 M0TXD1 M0TXD0	D3 D2 D1 E3	O	Transmit Data - NRZ data to be transmitted to transceiver. For MII mode, signal TX_EN and TXD0 through TX_D3 are clocked out by the rising edge of TX_CLK. For RMII mode, M0TXD1 and M0TXD0 are clocked out by the RMII reference clock M0RXCLK.
M0TXEN	E2	O	Transmit Enable - Synchronous to the transmit clock in MII mode. For RMII mode, M0TXEN is synchronous to M0RXCLK.
M0TXCLK	E1	I	Transmit Clock Input. 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s. (Not used in RMII mode).
M0RXD3 M0RXD2 M0RXD1 M0RXD0	G1 G3 G4 F1	I	Receive Data - NRZ data from the transceiver. For MII interface, signal RX_DV, RX_ER and RX_D0 through RX_D3 are sampled by the rising edge of M0RXCLK. For RMII mode, M0RXD3 and M0RXD2 are not used. M0RXD1and M0RXD0 are sampled by the rising edge of the RMII reference clock M0RXCLK.
M0RXDV	F2	I	Receive Data Valid. Active high.
M0RXCLK	F3	I	Receive Clock (MII mode). RMII clock for port 0.
M0RXER	F4	I	Receive Data Error. Active high. (Not used in RMII mode).
M0CRS	A1	I	Carrier Sense. Active high.
M0COL	C2	I	Collision Detect. Active high. (Not used in RMII mode).

Table 2: RMII/MII Interface (Port 1)

PIN NAME	PIN NO.	I/O	DESCRIPTION
M1TXD3 M1TXD2 M1TXD1 M1TXD0	N3 N2 N1 P3	O	Transmit Data - NRZ data to be transmitted to transceiver. For MII mode, signal TX_EN and TXD0 through TX_D3 are clocked out by the rising edge of TX_CLK. For RMII mode, M1TXD1 and M1TXD0 are clocked out by the RMII reference clock M3RXCLK.
M1TXEN	P2	O	Transmit Enable - Synchronous to the transmit clock in MII mode. For RMII mode, M1TXEN is synchronous to M3RXCLK.
M1TXCLK	P1	I	Transmit Clock Input. 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s. (Not used in RMII mode).
M1RXD3 M1RXD2 M1RXD1 M1RXD0	T1 T3 T4 R1	I	Receive Data - NRZ data from the transceiver. For MII interface, signal RX_DV, RX_ER and RX_D0 through RX_D3 are sampled by the rising edge of M3RXCLK. For RMII mode, M1RXD3 and M1RXD2 are not used. M1RXD1and M1RXD0 are sampled by the rising edge of the RMII reference clock M3RXCLK.
M1RXDV	R2	I	Receive Data Valid. Active high.
M1RXCLK	R3	I	Receive Clock (MII mode). RMII clock for port 0.
M1RXER	R4	I	Receive Data Error. Active high. (Not used in RMII mode).
M1CRS	M3	I	Carrier Sense. Active high.
M1COL	M1	I	Collision Detect. Active high. (Not used in RMII mode).

Table 3: RMII/MII Interface (Port 2)

PIN NAME	PIN NO.	I/O	DESCRIPTION
M2TXD3 M2TXD2 M2TXD1 M2TXD0	AB3 AB2 AB1 AC3	O	Transmit Data - NRZ data to be transmitted to transceiver. For MII mode, signal TX_EN and TXD0 through TX_D3 are clocked out by the rising edge of TX_CLK. For RMII mode, M2TXD1 and M2TXD0 are clocked out by the RMII reference clock M3RXCLK.
M2TXEN	AC2	O	Transmit Enable - Synchronous to the transmit clock in MII mode. For RMII mode, M2TXEN is synchronous to M3RXCLK.
M2TXCLK	AC1	I	Transmit Clock Input. 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s. (Not used in RMII mode).
M2RXD3 M2RXD2 M2RXD1 M2RXD0	AE3 AF1 AE1 AE2	I	Receive Data - NRZ data from the transceiver. For MII interface, signal RX_DV, RX_ER and RX_D0 through RX_D3 are sampled by the rising edge of M3RXCLK. For RMII mode, M2RXD3 and M2RXD2 are not used. M2RXD1and M2RXD0 are sampled by the rising edge of the RMII reference clock M3RXCLK.
M2RXDV	AD1	I	Receive Data Valid. Active high.
M2RXCLK	AD2	I	Receive Clock (MII mode). RMII clock for port 0.
M2RXER	AD3	I	Receive Data Error. Active high. (Not used in RMII mode).
M2CRS	AA3	I	Carrier Sense. Active high.
M2COL	AA1	I	Collision Detect. Active high. (Not used in RMII mode).

Table 4: RMII/MII Interface (Port 3)

PIN NAME	PIN NO.	I/O	DESCRIPTION
M3TXD3 M3TXD2 M3TXD1 M3TXD0	AD9 AE9 AF9 AD10	O	Transmit Data - NRZ data to be transmitted to transceiver. For MII mode, signal TX_EN and TXD0 through TX_D3 are clocked out by the rising edge of TX_CLK. For RMII mode, M3TXD1 and M3TXD0 are clocked out by the RMII reference clock M3RXCLK.
M3TXEN	AE10	O	Transmit Enable - Synchronous to the transmit clock in MII mode. For RMII mode, M3TXEN is synchronous to M3RXCLK.
M3TXCLK	AF10	I	Transmit Clock Input. 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s. (Not used in RMII mode).
M3RXD3 M3RXD2 M3RXD1 M3RXD0	AF12 AD12 AC12 AF11	I	Receive Data - NRZ data from the transceiver. For MII interface, signal RX_DV, RX_ER and RX_D0 through RX_D3 are sampled by the rising edge of M3RXCLK. For RMII mode, M3RXD3 and M3RXD2 are not used. M3RXD1and M3RXD0 are sampled by the rising edge of the RMII reference clock M3RXCLK.
M3RXDV	AE11	I	Receive Data Valid. Active high.
M3RXCLK	AD11	I	Receive Clock (MII mode). RMII clock for port 0.
M3RXER	AC11	I	Receive Data Error. Active high. (Not used in RMII mode).
M3CRS	AD8	I	Carrier Sense. Active high.
M3COL	AF8	I	Collision Detect. Active high. (Not used in RMII mode).

Table 5: RMII/MII Signal (Port 4)

PIN NAME	PIN NO.	I/O	DESCRIPTION
M4TXD3 M4TXD2 M4TXD1 M4TXD0	AD16 AE16 AF16 AD17	O	Transmit Data - NRZ data to be transmitted to transceiver. For MII mode, signal TX_EN and TXD0 through TX_D3 are clocked out by the rising edge of TX_CLK. For RMII mode, M4TXD1 and M4TXD0 are clocked out by the RMII reference clock M3RXCLK.
M4TXEN	AE17	O	Transmit Enable - Synchronous to the transmit clock in MII mode. For RMII mode, M4TXEN is synchronous to M3RXCLK.
M4TXCLK	AF17	I	Transmit Clock Input. 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s. (Not used in RMII mode).
M4RXD3 M4RXD2 M4RXD1 M4RXD0	AF19 AD19 AC19 AF18	I	Receive Data - NRZ data from the transceiver. For MII interface, signal RX_DV, RX_ER and RX_D0 through RX_D3 are sampled by the rising edge of M3RXCLK. For RMII mode, M4RXD3 and M4RXD2 are not used. M4RXD1and M4RXD0 are sampled by the rising edge of the RMII reference clock M3RXCLK.
M4RXDV	AE18	I	Receive Data Valid. Active high.
M4RXCLK	AD18	I	Receive Clock (MII mode). RMII clock for port 0.
M4RXER	AC18	I	Receive Data Error. Active high. (Not used in RMII mode).
M4CRS	AD15	I	Carrier Sense. Active high.
M4COL	AF15	I	Collision Detect. Active high. (Not used in RMII mode).

Table 6: RMII/MII Signal (Port 5)

PIN NAME	PIN NO.	I/O	DESCRIPTION
M5TXD3 M5TXD2 M5TXD1 M5TXD0	AF26 AE26 AD25 AC24	O	Transmit Data - NRZ data to be transmitted to transceiver. For MII mode, signal TX_EN and TXD0 through TX_D3 are clocked out by the rising edge of TX_CLK. For RMII mode, M5TXD1 and M5TXD0 are clocked out by the RMII reference clock M3RXCLK.
M5TXEN	AC25	O	Transmit Enable - Synchronous to the transmit clock in MII mode. For RMII mode, M5TXEN is synchronous to M3RXCLK.
M5TXCLK	AC26	I	Transmit Clock Input. 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s. (Not used in RMII mode).
M5RXD3 M5RXD2 M5RXD1 M5RXD0	AA26 AA24 AA23 AB26	I	Receive Data - NRZ data from the transceiver. For MII interface, signal RX_DV, RX_ER and RX_D0 through RX_D3 are sampled by the rising edge of M3RXCLK. For RMII mode, M5RXD3 and M5RXD2 are not used. M5RXD1and M5RXD0 are sampled by the rising edge of the RMII reference clock M3RXCLK.
M5RXDV	AB25	I	Receive Data Valid. Active high.
M5RXCLK	AB24	I	Receive Clock (MII mode). RMII clock for port 0.
M5RXER	AB23	I	Receive Data Error. Active high. (Not used in RMII mode).
M5CRS	AE24	I	Carrier Sense. Active high.
M5COL	AE25	I	Collision Detect. Active high. (Not used in RMII mode).

Table 7: RMII/MII Signal (Port 6)

PIN NAME	PIN NO.	I/O	DESCRIPTION
M6TXD3 M6TXD2 M6TXD1 M6TXD0	T24 T25 T26 R24	O	Transmit Data - NRZ data to be transmitted to transceiver. For MII mode, signal TX_EN and TXD0 through TX_D3 are clocked out by the rising edge of TX_CLK. For RMII mode, M6TXD1 and M6TXD0 are clocked out by the RMII reference clock M3RXCLK.
M6TXEN	R25	O	Transmit Enable - Synchronous to the transmit clock in MII mode. For RMII mode, M6TXEN is synchronous to M3RXCLK.
M6TXCLK	R26	I	Transmit Clock Input. 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s. (Not used in RMII mode).
M6RXD3 M6RXD2 M6RXD1 M6RXD0	N26 N24 N23 P26	I	Receive Data - NRZ data from the transceiver. For MII interface, signal RX_DV, RX_ER and RX_D0 through RX_D3 are sampled by the rising edge of M3RXCLK. For RMII mode, M6RXD3 and M6RXD2 are not used. M6RXD1and M6RXD0 are sampled by the rising edge of the RMII reference clock M3RXCLK.
M6RXDV	P25	I	Receive Data Valid. Active high.
M6RXCLK	P24	I	Receive Clock (MII mode). RMII clock for port 0.
M6RXER	P23	I	Receive Data Error. Active high. (Not used in RMII mode).
M6CRS	U24	I	Carrier Sense. Active high.
M6COL	U26	I	Collision Detect. Active high. (Not used in RMII mode).

Table 8: RMII/MII Signal (Port 7)

PIN NAME	PIN NO.	I/O	DESCRIPTION
M7TXD3 M7TXD2 M7TXD1 M7TXD0	H24 H25 H26 G24	O	Transmit Data - NRZ data to be transmitted to transceiver. For MII mode, signal TX_EN and TXD0 through TX_D3 are clocked out by the rising edge of TX_CLK. For RMII mode, M7TXD1 and M7TXD0 are clocked out by the RMII reference clock M3RXCLK.
M7TXEN	G25	O	Transmit Enable - Synchronous to the transmit clock in MII mode. For RMII mode, M7TXEN is synchronous to M3RXCLK.
M7TXCLK	G26	I	Transmit Clock Input. 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s. (Not used in RMII mode).
M7RXD3 M7RXD2 M7RXD1 M7RXD0	E26 E24 E23 F26	I	Receive Data - NRZ data from the transceiver. For MII interface, signal RX_DV, RX_ER and RX_D0 through RX_D3 are sampled by the rising edge of M3RXCLK. For RMII mode, M7RXD3 and M7RXD2 are not used. M7RXD1and M7RXD0 are sampled by the rising edge of the RMII reference clock M3RXCLK.
M7RXDV	F25	I	Receive Data Valid. Active high.
M7RXCLK	F24	I	Receive Clock (MII mode). RMII clock for port 0.
M7RXER	F23	I	Receive Data Error. Active high. (Not used in RMII mode).
M7CRS	J24	I	Carrier Sense. Active high.
M7COL	J26	I	Collision Detect. Active high. (Not used in RMII mode).

Table 9: RoX Input Interface

PIN NAME	PIN NO.	I/O	DESCRIPTION
RID31 RID30 RID29 RID28 RID27 RID26 RID25 RID24 RID23 RID22 RID21 RID20 RID19 RID18 RID17 RID16 RID15 RID14 RID13 RID12 RID11 RID10 RID9 RID8 RID7 RID6 RID5 RID4 RID3 RID2 RID1 RID0	H3 H2 H1 J3 J2 J1 K4 K3 K2 K1 L3 L2 L1 M4 U3 U2 U1 V3 V2 V1 W4 W3 W2 W1 Y4 Y3 Y2 Y1 AA4 AD4 AE4 AF4	I	Ring Input Device.
RIDH	AD5	I	
RICTL7 RICTL6 RICTL5 RICTL4 RICTL3 RICTL2 RICTL1 RICTL0	AE5 AF5 AC6 AD6 AE6 AF6 AD7 AE7	I	Ring Control Signal.
RICTLH	AF7	I	
RICLK	A3	I	Ring In Clock.

Table 10: RoX Output Interface

PIN NAME	PIN NO.	I/O	DESCRIPTION
ROD31 ROD30 ROD29 ROD28 ROD27 ROD26 ROD25 ROD24 ROD23 ROD22 ROD21 ROD20 ROD19 ROD18 ROD17 ROD16 ROD15 ROD14 ROD13 ROD12 ROD11 ROD10 ROD9 ROD8 ROD7 ROD6 ROD5 ROD4 ROD3 ROD2 ROD1 ROD0	B24 A25 B26 B25 C26 C25 D26 D25 D24 K26 K25 K24 L26 L25 L24 M26 M25 M24 V26 V25 V24 V23 W26 W25 W24 Y26 Y25 Y24 AF23 AE23 AD23 AC23	O	Ring Output Device.
RODH	AF22	O	Ring Output Data Header.
ROCTL7 ROCTL6 ROCTL5 ROCTL4 ROCTL3 ROCTL2 ROCTL1 ROCTL0	AE22 AD22 AF21 AE21 AD21 AC21 AF20 AE20	O	Ring Control Data.
ROCTLH	AD20	O	Ring Output Control Header.

Table 11: SGRAM Interface

PIN NAME	PIN NO.	I/O	DESCRIPTION
PBD31 PBD30 PBD29 PBD28 PBD27 PBD26 PBD25 PBD24 PBD23 PBD22 PBD21 PBD20 PBD19 PBD18 PBD17 PBD16 PBD15 PBD14 PBD13 PBD12 PBD11 PBD10 PBD9 PBD8 PBD7 PBD6 PBD5 PBD4 PBD3 PBD2 PBD1 PBD0	C21 B21 A21 D20 C20 B20 C19 B19 A16 D15 A15 D14 C14 B14 A14 D13 C18 B18 C17 B17 A17 D16 C16 B16 A13 D12 A12 D11 C11 B11 A11 B10	I/O	SGRAM Data Sheet.
PBA10_9	B7	O	This pin is connected to address 10 when connected to a 16M SGRAM and address 9 when connected to a 8M SGRAM.
PBA9_8	A10	O	This pin is connected to address 9 when connected to a 16M SGRAM and address 8 when connected to a 8M SGRAM.
PBANC8	A2	O	This pin is connected to address 8 when connected to a 16M SGRAM and no connect to a 8M SGRAM.

Table 11: SGRAM Interface (Continued)

PIN NAME	PIN NO.	I/O	DESCRIPTION
PBA7 PBA6 PBA5 PBA4 PBA3 PBA2 PBA1 PBA0	D9 C9 B9 A9 B8 A8 D7 C7	O	SGRAM address line PBA0-PBA8 are sampled during the ACTIVE command (row address) and READ/WRITE command (column address with PBA8 defining auto precharge).
PBCS#	B5	O	Chip Select. CS# enables and disables the command decoder of the SGRAM.
PBRAS#	A7	O	SGRAM Row Address Strobe.
PBCAS#	C5	O	SGRAM Column Address Strobe.
PBWE#	D5	O	Write Enable.
PBCLK	C23	O	System clock output to drive the SGRAM.

Table 12: External Address Table SRAM Interface

PIN NAME	PIN NO.	I/O	DESCRIPTION
ETD15 ETD14 ETD13 ETD12 ETD11 ETD10 ETD9 ETD8 ETD7 ETD6 ETD5 ETD4 ETD3 ETD2 ETD1 ETD0	G5 H5 K5 M5 R5 T5 W5 Y5 AA5 AB6 AB11 AB12 AB14 AB18 AB19 AB20	I/O	SRAM Data Bus.

Table 12: External Address Table SRAM Interface (Continued)

PIN NAME	PIN NO.	I/O	DESCRIPTION
ETA15 ETA14 ETA13 ETA12 ETA11 ETA10 ETA9 ETA8 ETA7 ETA6 ETA5 ETA4 ETA3 ETA2 ETA1 ETA0	AA22 V22 T22 P22 N22 L22 K22 H22 F22 E22 E21 E20 E16 E15 E14 E13	O	SRAM Address Line.
ETADSC#	E9	O	Synchronous Address Status Controller.
ETADV#	E7	O	Synchronous Address Advance. Used to advance SRAMs internal burst counter.
ETGW#	F5	O	Global Write. Enables a full 32-bit write.
ETOE#	E11	O	Output Enable. Active low. This enables the I/O output driver.
ETCLK	E12	O	System Clock Output.

Table 13: EEPROM Interface

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
EEDIO	A5	I/O	EEPROM Data Input and Output.
EECLK	B4	O	EEPROM Clock.

Table 14: MDIO Interface

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
MDC	AD13	O	PHY Management Clock.
MDIO	AE13	I/O	PHY Management Data Input and Output.

Table 15: Miscellaneous Pins

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
DEVID1 DEVID0	AF13 AC14	I	Device ID Number.
RESET#	AD14	I	Reset
TESTMODE	AE14	I	Test Mode Pin. This pin should be grounded for normal operation.
SRL	AB9	O	Status Serial Output (for testing).
EPBYPASS	AF14	I	This pin bypasses the EEPROM setup. This pin should be tied to ground.
SYSCLK	B6	I	75 MHz system clock.
TRST	D21	O	Reserved for JTAG scan. Testing output. Leave unconnected.
TMS	A22	O	Reserved for JTAG scan. Testing output. Leave unconnected.
TDO	B22	O	Reserved for JTAG scan. Testing output. Leave unconnected.
TDI	C22	O	Reserved for JTAG scan. Testing output. Leave unconnected.
TCLK	D22	O	Reserved for JTAG scan. Testing output. Leave unconnected.

Table 16: Power Interface

PIN NAME	PIN NUMBER	DESCRIPTION
GND	A4, A6, A18, A19, A23, A24, A26, B1, B2, B3, B12, B15, B23, C1, C3, C10, C12, C15, D10, D17, D18, D23, E25, G2, H4, J4, K23, L4, L23, M23, N25, T2, U4, U23, Y23, AA2, AA25, AB4, AC8, AC9, AC10, AC15, AC16, AC20, AD24, AE8, AE15, AE19, AF2, AF3, AB15, AB16, Y22	Ground
Vcc (3.3V)	A20, B13, C4, C6, C8, C13, C24, D4, D6, D8, D19, E4, G23, H23, J23, J25, M2, N4, P4, R23, T23, U25, V4, W23, AC4, AC5, AC7, AC13, AC17, AC22, AE12, AF24, AF25, E17	3.3 V supply voltage.

Table 16: Power Interface (Continued)

PIN NAME	PIN NUMBER	DESCRIPTION
VccM	AD26	Supply voltage for MII. For 5V MII interface, VccM should be 5V. For 3.3V MII interface, VccM should be 3.3V.
NC	E5, E6, E8, E10, E18, E19, G22, J5, J22, L5, N5, P5, R22, U5, U22, V5, AB5, AB7, AB8, AB10, AB13, AB17, AB21, AB22, M22, W22,	No Connect.

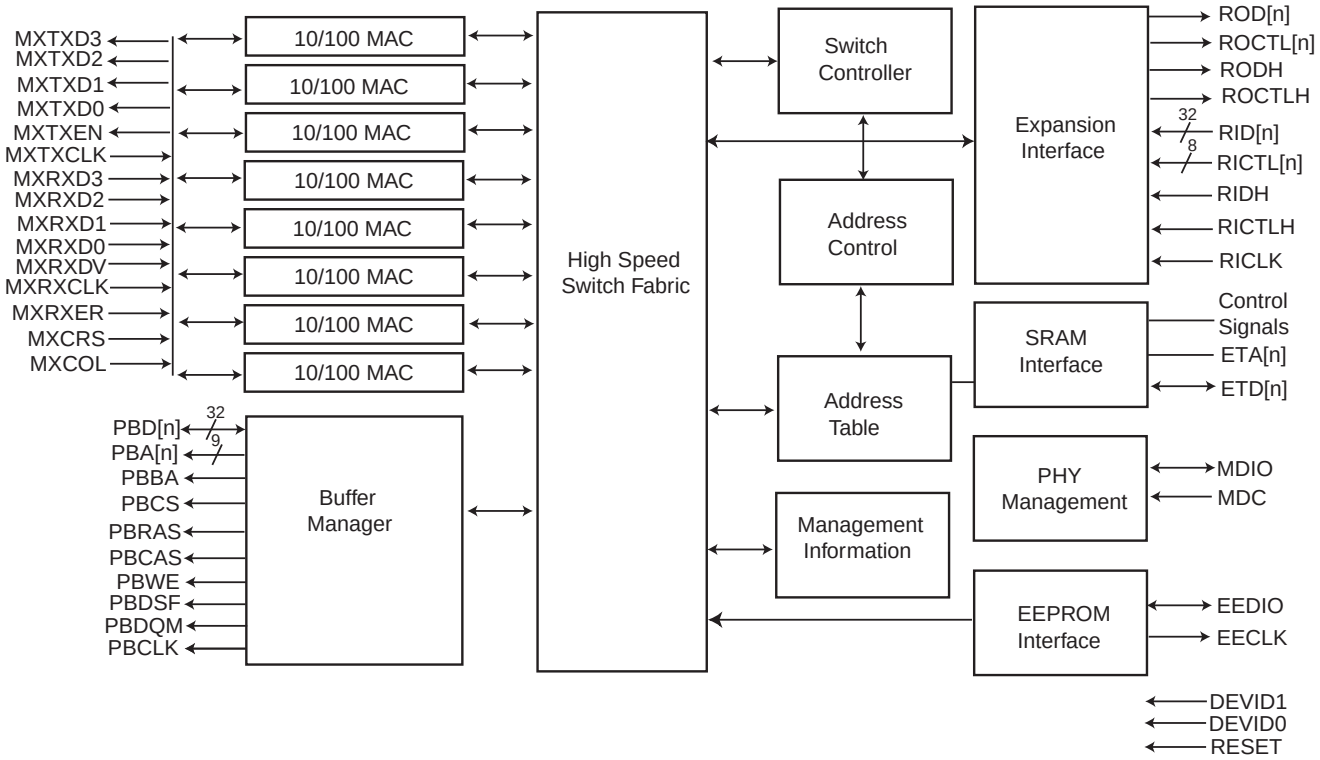

Figure 3 Interface Block Diagram

3. Functional Description

3.1 RoX Interface

The switch system shown in Figure 4 is a 24-port 10/100 Mbit/s switch with two Gigabit Ethernet ports. This system utilizes Allayer's proprietary RoX architecture. The RoX architecture is a ring structure that serves as the system backplane.

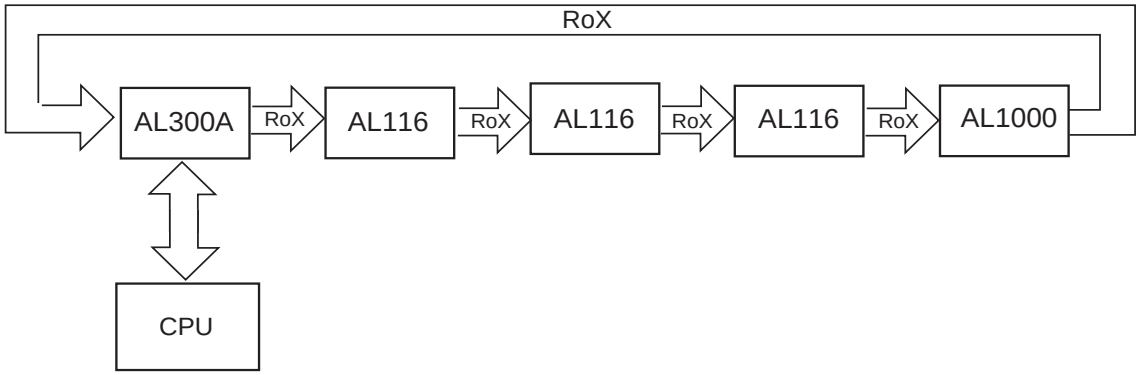

Figure 4 Managed Switch using RoX Bus with 24 Port 100 Mbps + Two Gpbs Ports

The RoX ring is composed of a data ring and a control ring. The data ring is used to transfer frame data, MIB events, as well as system configuration and status report messages. The control ring is used to communicate the RoX ring protocol messages among the devices to set up switch backbone resources for the data transfer on the data ring. Each device on the ring has an input interface for receiving data frames and ring protocol messages from the upstream device, and an output interface for transmitting data frames and ring protocol messages to the downstream device.

The management device (MIB) resides on the RoX ring. It provides the network management function for all the devices in the ring. The MIB device collects the network statistics of the switch system as well as provides system configurations to the devices. The CPU interface is provided by the MIB device. This supporting chip, the AL300A, provides a full set of statistical counters to support both SNMP and RMON network management.

3.2 Data Reception

The port will go into the receive-state when RX_DV in the MII interface is asserted. The MII presents the received data in four-bit nibbles that are synchronous to the receive clock (25 MHz or 2.5 MHz). The AL116 will then attempt to detect the occurrence of the SFD (10101011) pattern. All preamble data prior to SFD are discarded. Once SFD is detected, the frame data is forwarded and stored in the buffer of the switch.

3.2.1 Illegal Frame Length

During the receiving process, the MAC will monitor the length of the received frame. Legal Ethernet frames should have a length of no less than 64 bytes and no more than 1536 bytes. Any frames with illegal frame length are discarded.

3.2.2 Long Frames

The AL116 can handle frames up to 1536 bytes. All frames longer than 1536 bytes will be discarded. If the port continued to receive data after the 1536th byte, the port's data will be filtered. If the port is in half-duplex mode, the port will no longer be able to transmit or receive data during the long frame reception.

3.2.3 False Carrier Events

If the carrier sense (CRS) signal in the MII interface is asserted but the receive data valid (RX_DV) signal is not asserted within 16BT, the port is considered to have a false carrier event. The false carrier event is recorded for the MIB counter.

3.2.4 Frame Filtering

The AL116 will make filtering and forwarding decisions for each frame received based on its frame routing table, VLAN Mapping, port state, and the system configuration.

Under the following conditions, received frames are filtered.

1. The AL116 will check all received frames for errors such as symbol error, FCS error, short event, runt, long event, etc. Frames with any kind of error will not be forwarded to their destination port.
2. Any frame heading to its own source port will be filtered.
3. Frames heading to a disabled receiving port will be filtered.
4. If the input buffer of the port is full, the incoming frame will be discarded. It is recommended that flow control be used to prevent any loss of data. If the flow control option is enabled, this event will not occur. The remote station will transmit frame when the input buffer becomes available.
5. If the frame has any security violation and the security option is enabled at the receiving port.

If the Spanning Tree Protocol is enabled, the AL116 will forward the frame as below.

1. If the port is in the Block-N-Listen state or the Learning state, the frame is forwarded to the CPU when it is a BPDU frame, otherwise the frame is discarded.
2. If the port is in the Forwarding State, forward the frame to the CPU when it is a BPDU frame.

3.3 Frame Forwarding

After a frame is received, its source address (SA) and destination address (DA) are retrieved. The SA is used to update the port's address table as described previously and the DA is used to determine the frame's destination port.

The Address Lookup Engine will attempt to match the destination address with the addresses stored in the address table. If there is a match found, a link between the source port and the destination port is then established.

If the first bit of the destination address is a "0," the frame is regarded as an unicast frame. The destination address is passed to the Address Lookup Engine; which returns a matched destination port number to identify which port should the frame be forwarded to. If the destination port is within the same VLAN of the receiving port, the frame will be forwarded.

If the destination port does not belong to the VLANs specified at the receiving ports, the frame will be discarded. The event will be recorded as a VLAN boundary violation.

There are two ways that the AL116 handles frames with an unknown destination. The forwarding decision is controlled by the Flood Control option (System Configuration register 00). If Flood Control is disabled, the frame will be forwarded to all ports (except the receiving port) within the same VLAN as the receiving port. If the Flood Control option is enabled, the AL116 will forward the frame only to the uplink port specified at the receiving port.

Note: The AL116 defines a port as either a single port or a trunk.

If the port monitoring function is enabled, the frame forwarding decision is also subject to the port monitoring configurations.

If the first bit of the destination address is a "1," the frame will be handled as a multicast or broadcast frame. The AL116 does not differentiate multicast frames from broadcast frames except the reserved bridge management group address, as specified in Table 3.5 of IEEE 802.1d standard. The destination ports of the broadcast frame is all ports within the same VLAN except the source port itself.

If Multicast/Broadcast frame trapping (MCtrap) is enabled, the multicast/broadcast frames will be forwarded to the CPU only.

3.3.1 Broadcast Storm Control

One of the unique features provided by the AL116 is Broadcast Storm control. This option allows the user to limit the number of broadcast frames into the switch. This option can be implemented on a per port basis. A threshold of number of broadcast frames can be programmed in register 01.

When Storm Control is enabled and the number of cumulated non-unicast frames is over the programmed threshold, the broadcast frame is discarded.

If the Storm Control is disabled or the number of non-unicast frames received at the port is not over the programmed threshold, the AL116 will forward the frame to all the ports (except the receiving port) within the VLANs specified at the receiving port. If the CPU port is within the specified VLAN, the frame will also be forwarded to the CPU.

If Broadcast-Storm-drop (BConly_SC) is enabled, the AL116 will only drop broadcast frames but not the multicast frames.

3.3.2 Frame Transmission

AL116 transmits all frames in accordance to IEEE 802.3 standard. The AL116 will send the frames with a guaranteed minimum inter-packet/frame gap (IPG) of 96BT, even the received frames have an IPG less than the minimum requirement. The AL116 also supports transmission of frames with an IPG of 64BT (optional).

3.3.3 Frame Generation

During a transmit process, frame data is read out from the memory buffer and is forwarded to the destination port's PHY device in nibbles. Seven bytes of preamble signal (10101010) will be generated first before the SFD (10101011) and frame data is sent. Four bytes of FCS are sent at last.

Summary of Programmable Control for Transmit and Receive

The control for transmit and receive is on a per port basis. All options are programmable in the Port Configuration Register (registers 0D to 1C).

- Data Rate and Duplex Mode - this option is a per port option. Typically, speed is auto negotiated. For manual override, the appropriate port configuration register has to be programmed.
- Flow Control - the flow control can be implemented independently on a per port basis. The AL116 uses backpressure for half-duplex flow control and IEEE 802.3x for full-duplex flow control.
- Flood Control - the AL116 provides two modes for unmatched address forwarding. If flood-to-all option is elected, the AL116 will forward all unmatched DA frames to all ports.
- Secure Mode - the security option is implemented on a per port basis. When a port is configured to be in secured mode, any security violation will disable the port. A security violation is defined as any frame without a matched SA at the secured port's address table.

3.4 Half Duplex Mode Operation

For half-duplex operation, the MAC logic will abort the transmit-process if collision is detected through the assertion of the collision (COL) signal by the MII. Re-transmission of the frame is scheduled in accordance to IEEE 802.3's truncated binary exponential backoff algorithm. If the transmit process has encountered 16 consecutive collisions, an excessive collision error is reported, and AL116 will not try to re-transmit the frame unless the retry-on-excessive-collision (REC) option is enabled. If retry-on-excessive-collision (REC) is enabled, the number of collisions is reset to zero and transmission is started as soon as 96 bit time of inter-packet gap is passed after the last collision. If a collision is detected after 512BT of the transmission, a late collision error will be reported, but the frame will still be retransmitted after proper backoff time.

The AL116 also provides an option for an aggressive back off in the Port Configuration Register 01.3 (SuperMAC). This option allows the MAC to back off only three slots. This will create a more aggressive channel capture behavior than the standard IEEE backoff algorithm.

3.5 Secure Mode Operation

The AL116 provides security support on a per port basis. Whenever the secure mode is enabled, the port will stop learning new addresses. The address table of each port will remain unchanged. In this mode of operation, the address lookup table will freeze and no additional new address will be learned.

The AL116 provides two levels of security protection. The most severe intrusion protection is disabling a port experiencing intrusion. The security management (SecMgmt bit in register 01) will disable a port if a frame with unlearned SA is received at a secured port (security violation). Once the port is disabled, it can only be enabled by network management. Security management is a global option.

An alternative is to enable security at the local port level without the security management. When the AL116 is configured as such, the device will only discard frames that have security violation.

This is used in an environment where intruders are prevented from accessing the network.

Summary of Programmable Registers

- SecMgmt Register (register 01) - this bit sets the global security management option. The AL116 will partition any port that experience security violations.
- Security Register (register 0D to 1C) - this is a port configuration option. When this option is enabled, the port is secured. When the port receives a security violation frame it will discard the frame if security management is not on and disable the port if security management is on.

3.6 Address Learning

The table lookup engine provides the switching information required routing the data frames. The address look up table is set up through auto address learning (dynamic) or manual entry (static). The static addresses are assigned to the address table by the EEPROM or management device. All static address entries will not be aged or updated by AL116.

After a frame is received by the AL116, the embedded source address (SA) and destination addresses (DA) are retrieved. The source address retrieved from the received frame is automatically stored in a SA buffer. The AL116 will then check for error and security violation, and perform a SA search. If there is no error or security violation, the chip will store the source address in the address lookup table. If the SA has been previously stored in another port's SA table, the AL116 will delete the SA from the previously stored location.

The Individual MAC Address is a 48-bit unique MAC address to be programmed or learned. Bit 0 of a SA will be masked, i.e. no multicast SA.

The AL116 provides an on-chip MACAddress-To-PortID/TrunkID table with up to 1K entries for frame destination look-up operation. Optional external SRAM can be used to increase the number of MAC address lookup to 16K.

The AL116 address table contains both the static addresses input by the CPU or the EEPROM and dynamically learned address. It learns the individual MAC addresses from three different sources.

1. Frames received with no errors from the local ports.
2. Frames forwarded from other devices through the ring to the device.

3. The Table Convergence message received from the ring, which is not issued by the device itself.

If a received frame contains a source address that has already been learned in another port's address table but not aged out, it will perform the following operation based on the switch's configuration.

If the security option is selected for the port, AL116 will consider this as a security violation. If port is a non-protected port, the AL116 will delete the SA from the previous port's address table and update it to the current port's address table. However, if the SA is an static address entry, the address will not be updated.

3.6.1 Address Aging

A port's MAC address register is cleared on power-up, or hardware reset. If the SA aging option is enabled, the dynamically learned SA will be cleared if it is not refreshed in less than programmed time.

Summary of Programmable Options for Address Learning

- Address Aging Time - the address aging and aging time can be programmed in the System Configuration II (register 01). The resolution of the aging time is normally at 1-second increments. If AgeRes (register 02) bit is programmed to 1, the resolution will be in 2-second increments.

- Static Programmed Addresses - up to twenty static addresses can be programmed in the EEPROM address 70 to FF. See the EEPROM section on programming for more detail.

3.7 VLAN Support

Each port of the AL116 can be assigned to one or multiple VLANs. Frames from the source port will only be forwarded to destination ports within the same VLAN domain. A broadcast/multicast frame will be forwarded to all ports within the VLAN(s) of the source port except the source port itself. A unicast frame will be forwarded to the destination port only if the destination port is in the same VLAN as the source port. Otherwise, the frame will be treated as a frame with unknown DA. If the destination port belongs to the another VLAN, the frame will be discarded and the event will be recorded as a VLAN boundary violation.

Each port should be assigned a dedicated uplink port. Unicast frames with unknown destination addresses will be forwarded to the uplink port of the source port. An uplink port can either be a single port or a trunk.

The AL116 provides two VLAN register per ports (register 1D to 2C) for mapping to 32 ports (32 bits). Each register contains a 16-bit bit-map (total of 32 bits) to indicate the VLAN group for the port.

The VLAN registers hold the broadcast destination mask for each source port. A "1" will indicate that the broadcast frames will be routed from the source port to the specified port. Note that the source port bit must be set to "0" within the source port VLAN, because broadcast frames are not routed to the source port.

For setting up VLAN for trunking, please see the section on trunking for detail.

VLAN Set Up Example

A VLAN set up worksheet is provided in Appendix I. Simply by marking the ports you wish to send broadcast frame to, you can complete the VLAN map easily.

Let's assume we want to set up two VLAN groups in a sixteen port switch:

Group 1 consists of: 0, 1, 2, 5, 6, 8, 10, 11, 12, and 15.

Group 2 consists of: 2, 3, 4, 7, 8, 9, 13, 14, and 15.

Note: It might be easier to mark the VLAN ports first and then delete the source ports that you don't want the broadcast frames to be returned.

The completed VLAN bit map is shown in Table 17.

Table 17: VLAN Mapping for Port Based Load Balancing Trunk

	PORT	BIT	PORT 0/REG. 1E	PORT 1/REG. 20	PORT 2/REG. 22	PORT 3/REG. 24	PORT 4/REG. 26	PORT 5/REG. 28	PORT 6/REG. 2A	PORT 7/REG. 2C
DEVICE 1	7	15	1	1	1	1	1	1	1	1
	6	14	0	0	1	1	1	0	0	1
	5	13	0	0	1	1	1	0	0	1
	4	12	1	1	1	0	0	1	1	0
	3	11	1	1	1	0	0	1	1	0
	2	10	1	1	1	0	0	1	1	0
	1	9	0	0	1	1	1	0	0	1
	0	8	1	1	1	1	1	1	1	1

Table 17: VLAN Mapping for Port Based Load Balancing Trunk (Continued)

	PORT	BIT	PORT 0/REG. 1E	PORT 1/REG. 20	PORT 2/REG. 22	PORT 3/REG. 24	PORT 4/REG. 26	PORT 5/REG. 28	PORT 6/REG. 2A	PORT 7/REG. 2C
DEVICE 0	7	7	0	0	1	1	1	0	0	0
	6	6	1	1	1	0	0	1	0	0
	5	5	1	1	1	0	0	0	1	0
	4	4	0	0	1	1	0	0	0	1
	3	3	0	0	1	0	1	0	0	1
	2	2	1	1	0	1	1	1	1	1
	1	1	1	0	1	0	0	1	1	0
	0	0	0	1	1	0	0	1	1	0

3.8 Port Aggregation (Trunking)

The AL116 supports port aggregation/trunking. Port aggregation and trunking is basically a method to treat multiple physical links as a single logical link. The benefit of trunking is to be able to group multiple lower speed links into one higher speed link. For example, four full-duplex 100 Mbit/s links can be used as one single 800-Mbps link. This is very useful for switch to switch, switch to server, and switch to router application.

The AL116 considers a trunk as a single port entity regardless of the trunk composition.

Two to four ports can be grouped together as a single trunk link. The grouping of the ports in the trunk must be from the top four ports or the bottom four ports of the device, i.e. port 0 to 3 or port 4 to 7. A total of eight trunks can be supported by the RoX chip sets.

In a multiple link trunk, the links within the trunk should have equal amount of traffic in order to achieve maximum efficiency. One of the requirements for transmission is that the frames being transmitted must not be out of order. Therefore, some sort of load balancing among the links of the trunk has to be deployed. The AL116 offers two alternative load balancing methods which are selected in the System Configuration Register I (register 00).

3.8.1 Load Balancing

The two load-balancing methods that the AL116 uses to support trunking are port based and MAC address based. The port based load balancing method is an explicit port assignment scheme. It requires each individual port to be assigned to a specific link (trunk port) in the trunk. If the port is not assigned, frames might be routed to the trunk in random and this could cause the frames to go out of order. The port based load balancing trunk can be a two, three or four-port trunk.

During transmit, the frame will be routed from the source port to the assigned trunk port. When a frame is received from any one of the trunk ports, it will be routed to the destination port within the VLAN. In essence, the AL116 treats a trunk as any single port within the same VLAN. If the ports traffic is evenly distributed among all the trunk ports, load balancing is achieved and the aggregate bandwidth of the trunk can be as high as 800 Mbit/s (full-duplex).

The alternative is the MAC address based load balancing. When the AL116 receives a frame with a trunk destination, it will automatically forward the frame to a port in the trunk based on the source MAC address. The MAC address load balancing decision is based on a proprietary algorithm. The algorithm assumes the trunk is a four-port trunk. Therefore, if MAC address based load balancing is used, the trunk must consist of four ports. (Use of MAC based load balancing in a two or three port trunks could result in loss of frame.)

The advantage of port based load balancing is its ability to support two and three port trunks.

3.8.2 Trunk Port Assignment

The maximum number of trunks for Allayer's RoX architecture is eight. The Port Configuration Registers (0D to 1C) provides the ability to designate a port to be a member of a trunk. The trunk can consist of up to four trunk ports. A trunk group must consist of either the top four ports or the bottom four ports. For example, a trunk can consist of either port 0, 1, 2, or 3, or port 4, 5, 6 or 7. Each trunk port's number is in sequence of 00, 01, 10, and 11 corresponding to the order of port of the devices. For example, port 1 and 5 are 01 (See Figure 5).

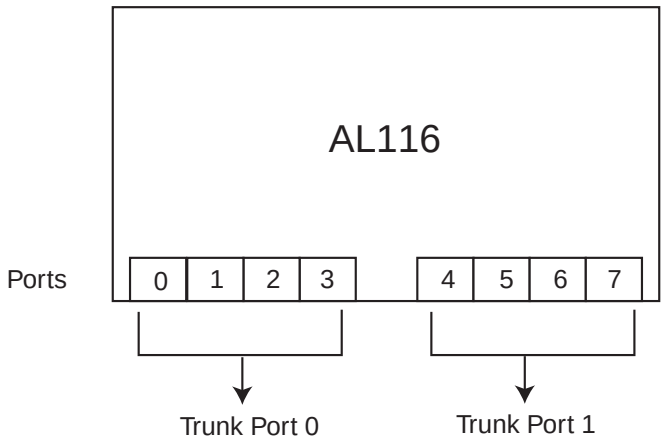

Figure 5 Trunk Port Numbering

3.8.3 Port Based Trunk Loading

For port-based load balancing, a trunk port must be assigned to each port for all defined trunks. The port assignment is done by programming Port to Trunk Port registers (2D to 34). It is recommended that ports be evenly distributed among all trunk ports to prevent overloading any single trunk port. The following is a procedure to set up the trunk.

Port Based Load Balancing Set Up Example

Register bits are reference by X and Y, where “X” is the register number and “Y” is the bit number. At the back of the data sheet a worksheet is provided for port to trunk port and VLAN assignment.

The example is designing an eight-port switch with a three-port trunk.

1. The desired trunk ports are 5, 6, and 7. Therefore, the port configuration register bits 17.9, 19.9, and 1B.9 are set to 1.
2. Assign Port 0 to trunk port 5, Port 1 and 3 to trunk port 6, and port 2 and 4 to trunk port 7. The trunk ports are 5, 6, and 7; therefore the trunk number is 1. The assignment of the port to trunk port register bits should therefore be:

   2D.2=1, 2D.3=0

   2E.2=0, 2E.3=1

   2F.2=1, 2F.3=1

   30.2=0, 30.3=1

   31.2=1, 31.3=1
3. Trunk ports should be assigned with their own the port number in the port to trunk port register. The port to trunk port bits should be:

   32.2=0, 32.3=1

   33.2=1, 33.3=0

   34.2=1, 34.3=1

Table 18: Trunking Port Assignment

	TRUNK PORT	BIT VALUE	PORT 0/REG. 2D	PORT 1/REG. 2E	PORT 2/REG. 2F	PORT 3/REG. 30	PORT 4/REG. 31	PORT 5/REG. 32	PORT 6/REG. 33	PORT 7/REG. 34
Trunk 7 Bits 15, 14	7	11								
	6	10								
	5	01								
	4	00								
Trunk 6 Bits 13, 12	3	11								
	2	10								
	1	01								
	0	00								
Trunk 5 Bits 11, 10	7	11								
	6	10								
	5	01								
	4	00								
Trunk 4 Bits 9, 8	3	11								
	2	10								
	1	01								
	0	00								
Trunk 3 Bits 7, 6	7	11								
	6	10								
	5	01								
	4	00								

Table 18: Trunking Port Assignment (Continued)

	TRUNK PORT	BIT VALUE	PORT 0/REG. 2D	PORT 1/REG. 2E	PORT 2/REG. 2F	PORT 3/REG. 30	PORT 4/REG. 31	PORT 5/REG. 32	PORT 6/REG. 33	PORT 7/REG. 34
Trunk 2 Bits 5, 4	3	11								
	2	10								
	1	01								
	0	00								
Trunk 1 Bits 3, 2	7	11			11		11			11
	6	10		10		10			10	
	5	01	01					01		
	4	00								
Trunk 0 Bits 1, 0	3	11								
	2	10								
	1	01								
	0	00								

3.8.4 MAC Based Load Balancing

For MAC address based load balancing, there is no need to assign a port to a trunk port. The AL116 dynamically assigns MAC address to the trunk port. MAC address based trunks must consist of four trunk ports. The bits are chosen for their randomness. The statistically random bits will ensure good load balancing among all four trunk ports.

The following is a procedure to set up the trunk;

1. Select MAC address loading by setting bit 00.3 to 1.
2. Select the trunk ports using register 0D to 1C bit 9.
3. Assign the ports and the trunk port to the same VLAN using register 1D to 2C.

The port VLAN grouping should include all the trunk ports. Since the AL116 will assign the port by MAC addresses, so frames from any single port may be routed to any trunk ports.

MAC Based Load Balancing Example

For simplicity, the example is an eight port switch with a four-port trunk**.**

1. The desired trunk port is 4, 5, 6, and 7. Therefore, the port configuration register bits 15.9, 17.9, 19.9, and 1B.9 are set to 1.
2. Assigning VLAN. The VLAN map is assigned as shown.

All bits are set to 1 except the ports themselves.

Table 19: VLAN Mapping for MAC Based Load Balancing Trunk

	PORT	BIT	PORT 0/REG. 1E	PORT 1/REG. 20	PORT 2/REG. 22	PORT 3/REG. 24	PORT 4/REG. 26	PORT 5/REG. 28	PORT 6/REG. 2A	PORT 7/REG. 2C
DEVICE 1	15	15	0	0	0	0	0	0	0	0
	14	14	0	0	0	0	0	0	0	0
	13	13	0	0	0	0	0	0	0	0
	12	12	0	0	0	0	0	0	0	0
	11	11	0	0	0	0	0	0	0	0
	10	10	0	0	0	0	0	0	0	0
	9	9	0	0	0	0	0	0	0	0
	8	8	0	0	0	0	0	0	0	0

Table 19: VLAN Mapping for MAC Based Load Balancing Trunk (Continued)

	PORT	BIT	PORT 0/REG. 1E	PORT 1/REG. 20	PORT 2/REG. 22	PORT 3/REG. 24	PORT 4/REG. 26	PORT 5/REG. 28	PORT 6/REG. 2A	PORT 7/REG. 2C
DEVICE 0	7	7	1	1	1	1	0	0	0	0
	6	6	1	1	1	1	0	0	0	0
	5	5	1	1	1	1	0	0	0	0
	4	4	1	1	1	1	0	0	0	0
	3	3	1	1	1	0	1	1	1	1
	2	2	1	1	0	1	1	1	1	1
	1	1	1	0	1	1	1	1	1	1
	0	0	0	1	1	1	1	1	1	1

3.9 Spanning Tree Support

The AL116 has the capability to support implementation of the Spanning Tree Protocol. All ports can be programmed to be in the port state as required by the spanning tree protocol.

If the Spanning Tree Protocol option is enabled, the AL116 will forward the frame as below.

- If the port is in the Block-N-Listen State or the Learning State, the frame is forwarded to the CPU if it is a BPDU frame; otherwise the frame is discarded. All outgoing frames except outgoing BPDUs will be masked from the path to the PHY.
- If the port is in the Forwarding State, the frame is forwarded to the CPU if it is a BPDU frame. All source addresses of the incoming frames from the PHY will be learned and then forwarded based on the switch routing decision. All outgoing frames will be transmitted to the PHY.

If the port is in the learning, all source addresses of the incoming frames from the PHY will be learned. All incoming frames except incoming BPDUs from the PHY will be discarded after being learned; all outgoing frames except outgoing BPDUs will be masked from the path to the PHY.

3.10 Flow Control

The AL116 can operate at two different modes, half- and full-duplex. Each port can operate at either full- or half-duplex and be configured to have flow control enabled or no flow control independently on a per port basis.

3.10.1 Half Duplex Flow Control (Backpressure)

If the half-duplex flow control option is elected, backpressure will be used for flow control. Whenever the occupancy of the receiving frame buffer of a port is full, the MAC of the port will start sending a JAM signal through the port. After sensing the JAM signal, the remote station will defer transmission. Backpressure flow control is applied to ensure that there is no dropped frame.

The AL116 supports two types of backpressure, collision based and carrier based. Carrier based backpressure is generated by the AL116 when the switch port's frame buffer is full. The AL116 will cease to jam the line when the port has buffer space available for frame reception. The IPG of the jamming signal can be programmed be either 64BT or 96BT. Collision Based backpressure is generated by the AL116, only when the switch port receives a frame. The AL116 will cease to jam the line when the line is idle.

The carrier based backpressure has several advantages over collision based backpressure.

1. Collision based backpressure can cause late collisions.
2. After 16 consecutive collisions, the MAC could drop frames. The AL116 has an option not to drop frame after 16 collisions. However, the end terminal may still drop frames.

Therefore, we recommend the use of carrier based back pressure as the preferred method for half-duplex flow control. In this mode of operation, we also recommend that the IPG of the JAM signal should be set at 64BT. This is because if the IPG is at 96BT, the far end terminal might still be able to transmit frame and cause collision. The excessive collision could cause frames to be dropped.

The AL116 also supports collision based backpressure for customers that prefer collision based backpressure.

3.10.2 Full Duplex Flow Control (802.3x)

In the full-duplex mode, the AL116 will transmit and receive frames in accordance to 802.3x. In this mode, the transmission channel and the receiving channel operate independently.

In the incoming direction, whenever the occupancy of the receiving frame buffer of a port is full, the MAC of the port will send out a PAUSE frame with its delay value set to maximum. The PAUSE frame will deter the any incoming frame from flowing into the port. After the occupancy of the receiving frame buffer is reduced below the FlowControlOff threshold, the MAC of the port will then send out a PAUSE frame with the delay value set to zero, to resume receiving the incoming frame flow.

In the outgoing direction, whenever a incoming PAUSE frame with a non-zero delay value is received through a port, the MAC of the port will stop the next frame transmission after the ongoing frame transmission is finished, and start its pause timer. It will resume frame transmission either after the pause timer expired or when a PAUSE frame with a zero delay value is received.

When 802.3x flow control option is elected, the device will program the appropriate bit in the auto-negotiation capability field. When the AL116 is used in the full-duplex mode, it is recommended

that flow control be turned on. This is to prevent the buffer from overflow and loss of frames. If the connected device has no 802.3x capability, then the link is recommended to be set at half-duplex.

3.11 Queue Management

Each port of the AL116 has its own individual transmission and receive queues. All frames come into the AL116 are stored into the shared memory buffer, and are lined up in the transmission queues of corresponding destination port.

Each port of the AL116 has an input frame queue, and a dedicated queue to buffer the locally generated management event messages.

Each output port maintains an output frame queue for, and a dedicated multicast queue for outgoing multicast frame parking. The transmit frame can be from one of two sources, local or from another device on the RoX ring. For an output queue, if the source selected is the multicast queue, the device will set up a channel to copy the frame in the head of the multicast queue to the output queue for transmission.

For an output queue, if the source selected is a local input queue, the device will set up a channel from the local DRAM buffer to the output queue upon the requested DRAM bandwidth that is available.

For an output queue, if the source selected is from another device on the ring, the device will send a message to that device trying to set up a channel through the ring from the source input queue in that device to the local output queue.

For the multicast queue, if the source selected is a local input queue, the device will set up a channel from the local DRAM buffer to the multicast queue upon the requested DRAM bandwidth is available.

For the multicast queue, if the source selected is from another device on the ring, the device will send message to that device trying to set up a channel through the ring from the source input queue in that device to the local multicast queue.

3.12 Uplink Port

The uplink port provides a way to connect the switch to a repeater hub, a workgroup switch, a router, or any type of interconnecting device compliance with IEEE 802.3 standard. The CPU port can also be designated as an uplink port.

If flood control is enabled, the AL116 will send all frames with unmatched DA and multicast/ broadcast frames to the uplink port. It is very important that each port is assigned to an uplink port via the Port Configuration Register (0D to1C), or data frames might be lost. The uplink port should be configured to be within the same VLAN as the source port. If the uplink port is not a member of the VLAN, the broadcast or multicast frames will not be forwarded to its designated uplink port. Multiple VLANs can share the same uplink port.

The AL116 will direct following frames to the uplink port:

1. Frames with unicast destination address that does not match with any MAC address stored in the switch.
2. Frames with broadcast/multicast destination address if the uplink port is in the same VLAN.

Note: When configuring an uplink port, the uplink port should designate itself as the uplink port.

Summary of Programmable Register

- Designate an Uplink Port (register 0D to 1C) - this register provides option to designate the uplink port as either a port, a trunk or a CPU. See detail in register description.

3.13 Port Monitoring

The AL116 supports port monitoring which provides complete network monitoring capability at 100 Mbit/s. A copy of egress (TX) data and ingress (RX) data of the monitored port is sent to their respective snooping ports.

The monitored port is selected by register 06. The AL116 allows the transmit and receive data to be monitored by different snooping ports. The snooping ports are also selected by register 06.

Summary of Programmable Register

- Port Monitoring (register 06) - selects the target monitored port and the snooping port. A 5-bit Port_ID designates the port. The format of the Port_ID is [Dev_ID].[Port_ID]. [Dev_ID] is the device number and [Port_ID] is the port number.

3.14 Media Independent Interface (MII)

The MAC of each port of the AL116 is connected to the PHY through the standard MII interface. For reception, the received data (RXD) are sampled by the rising edge of the receive clock (RX_CLK). Assertion of the receive data valid (RX_DV) signal will cause the MAC to look for start of SFD. For transmission, the transmit data enable (TX_EN) signal is asserted when the first preamble nibble is sent on the transmit data (TXD) lines. The transmit data are clocked out by the rising edge of the transmit clock (TX_CLK).

Prior to any transaction, the AL116 will output thirty-two bits of “1” as preamble signal. After the preamble, a 01 signal is used to indicate the start of the frame.

3.15 Reduced Media Independent Interface (RMII)

The AL116 also supports the RMII interface. The RMII interface can be activated through the use of the System Configuration Register. The RMII has only six signal pins and a clock pin. The signal pins are TXD0, TXD1, RXD0, RXD1, TXEN and CRS. The RXCLK pin is the common reference clock at 50 MHz. The AL116 provides a clock pin for each port to minimize clock skew effect.

Note: When RMII is used, all other pins in the MII interface should be left unconnected.

For reception, the received data (RXD) is sampled by the rising edge of the receive clock (RX_CLK). Assertion of the CRS signal indicates the receive channel is active. The di-bit RXD[1:0] is nominally “00” until the PHY detect a valid SFD and send preamble as “01.” Valid data will follow SFD.

For transmission, the transmit data enable (TX_EN) signal is asserted when the first preamble nibble is sent on the transmit data (TXD) lines. The transmit data are clocked out by the rising edge of the reference clock.

Prior to any data transaction, the AL116 will output di-bits of '01' as preamble signal. After the preamble, a "11" signal is used to indicate the start of the frame.

3.16 PHY Management

The AL116 supports transceiver management through the serial MDIO and MDC signal lines. The device provides two modes of management, master and slave mode. In the master mode of operation, the AL116 controls the operation modes of the link. But in the slave mode the PHY controls the operating mode.

3.16.1 PHY Management MDIO

There is no difference in MDIO operation between MII and RMII. For a write operation, the device will send a "01" to signal a write operation. Following the "01" write signal will be the 5-bit ID address of the PHY device and the 5-bit register address. A "10" turn around signal is then used to avoid contention during a read transaction. After the turn around, the 16 bit of data will be written into the register and afterwards the line will be put in a high impedance state.

For a read operation, the AL116 will output a "10" to indicate read operation after the start of frame indicator. Following the "10" read signal will be the 5-bit ID address of the PHY device and the 5-bit register address. Then, the AL116 will cease driving the MDIO line, and wait for one bit time. During this time, the MDIO should be in a high impedance state. The device will then synchronize with the next bit of "0" driven by the PHY device, and continue on to read 16 bit of data from the register. The detail timing requirement on PHY management signals are described in the section "Timing Requirement."

The MDIO port can be disabled through the use of port configuration register. This allows the engineers to use the 100Base-TX transceiver without auto-negotiation capability or MII to MII interconnect. In this mode of operation, the PHY has no communication with the AL116. Therefore, the AL116 will assert the link status as soon as initialization is completed and assumes the connected PHY is operating at the specified operating duplex mode and speed.

3.16.2 PHY Management Master Mode

In this mode, the AL116 will continuously poll the status of the PHY devices through the serial management interface, without CPU intervention. The device will also configure the PHY capability fields to ensure proper operation of the link. The CPU can access any registers in the PHY devices through the CPU interface provided by the management device, the AL300A.

The configuration of the link is automatic. The link capability is programmed by the AL116 through the port configuration register. The AL116 reads from the standard IEEE PHY registers to determine the auto-negotiated operating speed and mode. If there is a need to manually set the operation mode because of flow control and cabling issues, the AL116 can set the port operation mode manually through the MDIO interface (see EEPROM section for programming the AL116).

If a CPU is used to reprogram the PHY via AL116, the operating mode is changed without reset or powered down. In order to ensure the link is operating in the desired mode, the PHY should renegotiate either through a command or unplugging the RJ45.

3.16.3 PHY Management Slave Mode

In the slave mode, the PHY controls the programming of the operating mode. The AL116 will continuously poll the status of the PHY devices through the serial management interface, without CPU intervention to determine the operation mode of the link. The CPU can access any registers in the PHY devices through the CPU interface provided by the management device AL300A.

This mode of PHY management is very useful for unmanaged switches. The operating mode of the link can be changed by programming the mode pin of the PHY through a jumper without any assistance from the CPU.

The AL116 also supports 100Base-TX transceivers without a MDIO interface or MII to MII interface. When MDIO is disabled, the AL116 will operate in the operation mode specified in the Port Configuration Register (register 0D to 1C).

3.16.4 Non Auto-negotiation Mode

The AL116 can also turn off the auto-negotiation capability of the PHY. When auto-negotiation is turned off, the AL116 is in the slave mode and the transceiver will determine the link's operating mode.

3.16.5 Other PHY Options

Some legacy Fast Ethernet devices and low cost devices have no auto-negotiation capability. In those cases, the transceiver will not be able to perform auto-negotiation. The switch transceiver will typically do a parallel detection and update the information in the transceiver's register. Unfortunately, such register addresses are vendor specific. The AL116 provides a register (register 05) to specify the register address of the PHY to for the AL116 to read. The AL116 will read from that register and configure the port operation accordingly.

Register 05 also provides some additional flexibility's for some of the PHYs in the market. In general, the system designer should set the ID of the PHY devices as 0 for port 0, 1 for port 1, … and 7 for port 7. The Lucent Quad PHY, LU3X54FT, utilizes PHY address 00000 as a broadcast address. Bit 1 of the register 05 allows the AL116 to start with PHY address 01000. This provision allows the engineers to work around PHYs that have problem handling address 00000.

Quad PHYs in the market today have two port-ordering in the chip pinout, clockwise and counter clockwise. Register 05, Bit 2 programs the AL116 port order to go in either direction. This provision enables engineers to easily implement designs with any PHY.

There is also a slow MDIO clock (17 KHz) available for PHY that is not capable of handling high speed MDIO clock. Examples of these PHYs are LXT970 and LXT974.

If for some reason, the transceiver is connected to a device and that device fail to auto-negotiate. The AL116 will default the data rate and duplex mode to the default setting in the port configuration register.

3.17 EEPROM Interface

The AL116 provides three functions with the EEPROM interface; system initialization, obtaining system status, and reconfiguration of the system in real time.

3.17.1 System Initialization

The EEPROM interface is provided so the manufacturer can provide a pre-configured system to their customers. Customers can change or re configure their system and retain their preferences. The EEPROM contains configuration and initialization information, which is accessed at power up and reset. The organization of EEPROM data is shown in Table 20.

The AL116 uses the 24C02 serial EEPROM device (2048 bits organized as 256 bits x 8).

During start up, the AL116 will try to detect the presence of the EEPROM. If no EEPROM is present, the AL116 will be initialized by the CPU attached to the management device on the RoX ring. If no initialization command is received, the device will not operate.

If the reset pin is held low, the AL116's EEPROM interface will go into a high impedance state. This feature is very useful for reprogramming the EEPROM during installation or reconfiguration.

There are two ways that the EEPROM can be reprogrammed, by an external parallel port or the CPU residing on the ring. For reprogramming using a parallel port, a signal is used to hold the RESET pin low; the EEPROM interface will then be in the high impedance state. An external device can then programmed the EEPROM through the EDIO and the ECLK pins. The EEPROM address should be set to be the same as the device ID with A3 (EEPROM) grounded. For example, EEPROM of device 0 has an address of 000 and device 1 has and address of 001.

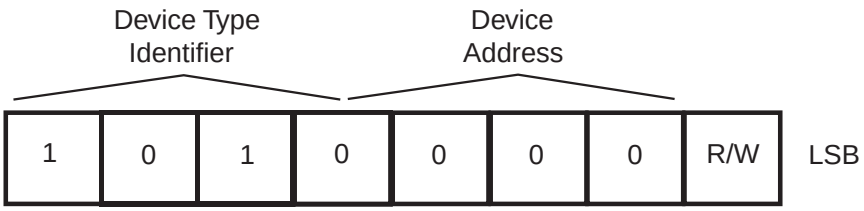

Figure 6 EEPROM Address Format

3.17.2 Start and Stop Bit

The write cycle is started by a start bit and ended by a stop bit. A start bit is a transition from high to low of EEDIO when EEC is high. The operation terminates when EEDIO goes from low to high when EEC is high (Figure 7). Following a start condition, the writing device must output the address of the EEPROM. The most significant four bits of the EEPROM address are the device type identifier. These four bits are 1010. The EEPROM device address should be set to the device ID number.

The EECLK is an output from the AL116. EEDIO is an input if the AL116 is reading the EEPROM or an output if it is writing to it. (See Figure 7 through 10).

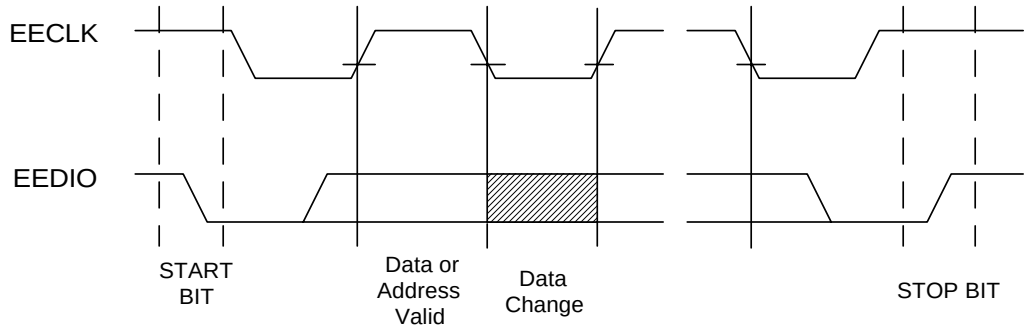

Figure 7 Start and Stop Bit

3.17.3 Write Cycle Timing

When accessing the EEPROM, the reset pin has to be held low before writing operation can begin.

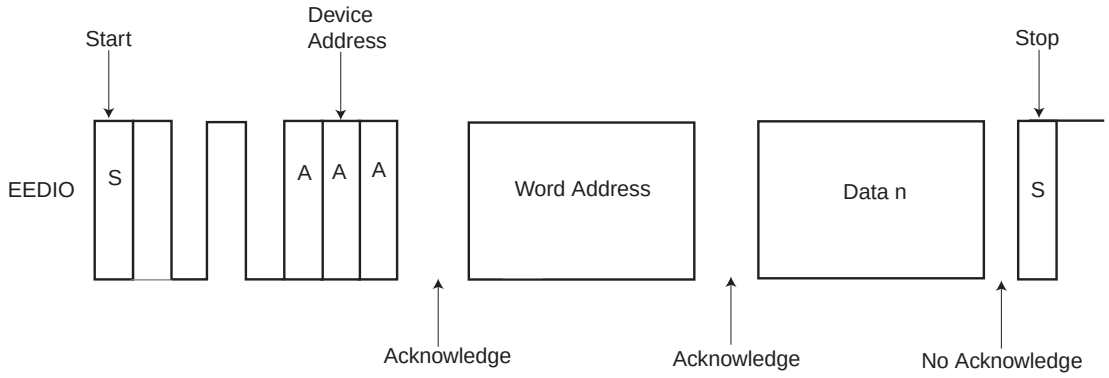

Figure 8 Typical Write Operation

3.17.4 Read Cycle Timing

Read operations are initiated in the same manner as write operations, with the exception that the R/W bit of the EEPROM address is set to a “1.”

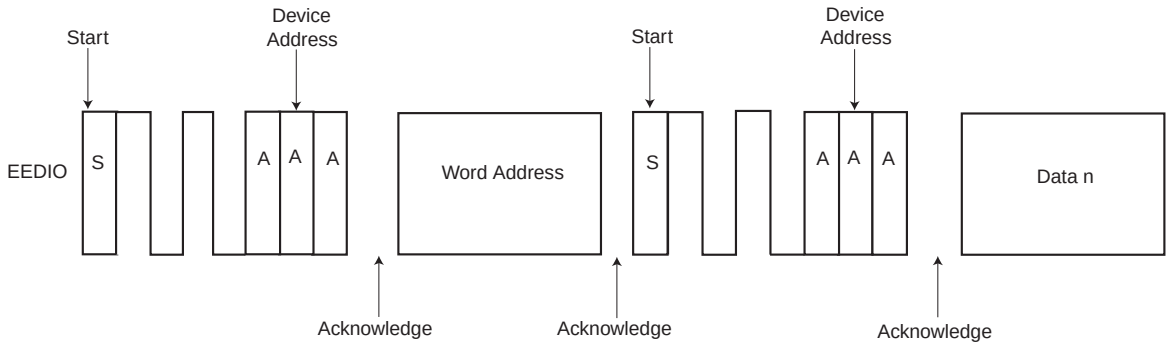

Figure 9 Typical Read Operation

3.17.5 Reprogramming the EEPROM Configuration

There are two ways that the system can be reconfigured. Figure 10 shows an application using the parallel interface to reprogram the EEPROM. In this application, the parallel port holds the reset pins low, and force the EEDIO pins to go in to high impedance. Once the pins are in high impedance, the EEPROM can now be programmed by the parallel port.

Once the parallel port releases the reset pins, the devices will start to download the EEPROM data and reconfigure the devices.

An alternate way of reconfiguring the system is to input the data directly into the AL116. After initialization, the EEPROM interface can act as a virtual EEPROM. In order for this method to work the EEPROM’s address must be 0XX, the AL116’s address will be 1XX. The customer can now program the AL116 as an EEPROM. The read and write timing is the same as an EEPROM.

Because you read as well as write to the AL116, status of the register can be read from the AL116. This will serve as a very useful tool for diagnostic of an unmanaged switch.

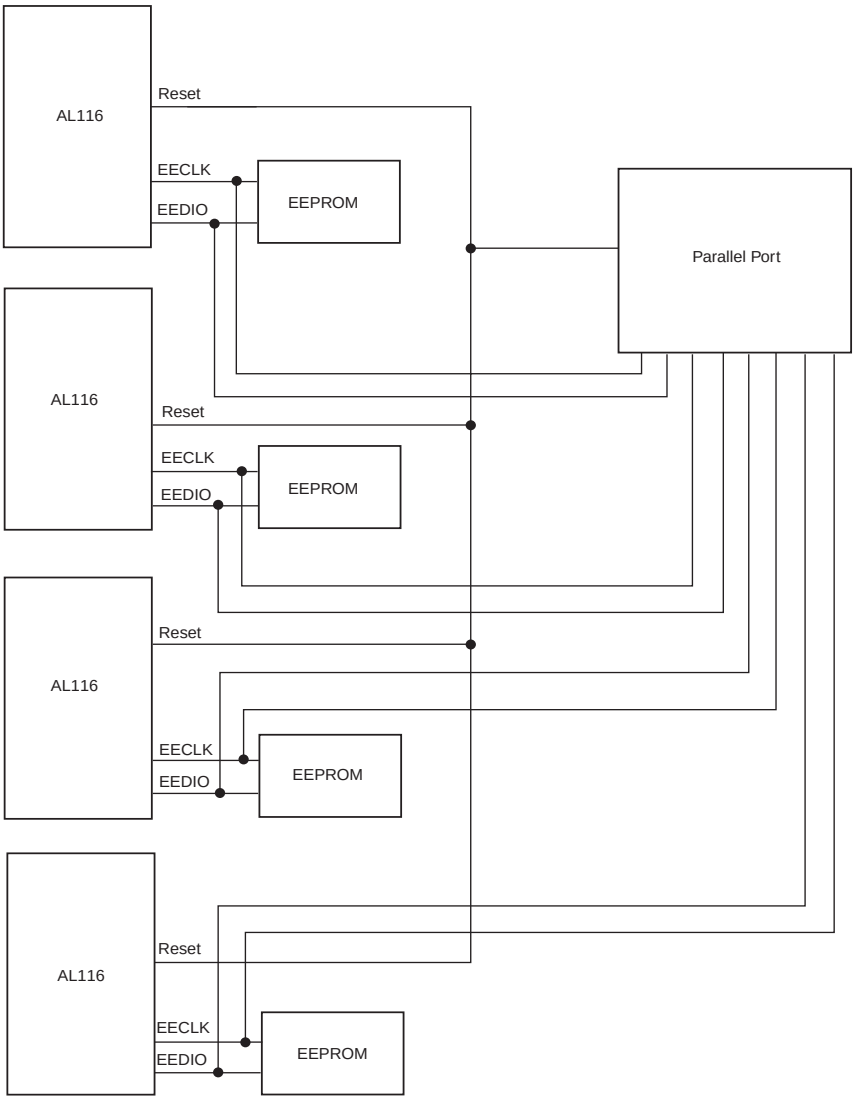

Figure 10 Programming the EEPROM with a Parallel Port

3.17.6 EEPROM MAP

Note: The specific bits in the register are referenced by a "X.Y" notation, where X is the register number and Y is the bit number.

Table 20 shows the EEPROM addresses map cross-referenced to the register/bit set of the AL116. Addresses 00 through 6D are for configuring the device. They are downloaded by the AL116 during reset or power up.

Address 06 and 07 should be programmed as 0000 0001 and 0001 0100.

The address 6F indicates the last address entry. If no static address is used in the switch, the address 6F should be programmed.

Addresses 70 to FF are used for programming the static address entry.

The format of the address is shown as follows when YXXXXX represents:

- If Y=0 then XXXXX is the 5-bit individual port ID number.
- If Y=1, then XXXXX can be either the trunk port represented by 00 followed by the 3 digit [trunk ID] number, or the CPU port represented by 11ZZZ where ZZZ is don't care.

Table 20: EEPROM Addresses

Address 70	Address 71	Address 72-73	Address 74-75	Address 76-77
Reserved	00YXXXXX	MAC Address [42:32]	MAC Address [31:16]	MAC Address [15:0]

Table 21: AL116 EEPROM Mapping

EEPROM PHYSICAL ADDRESS	DESCRIPTION	AL116 REGISTER/BIT
00	System Configuration I [15:8]	00.15 to 00.8
01	System Configuration I [7:0]	00.7 to 00.0
02-03	System Configuration II	01.15 to 01.0
04-05	System Configuration III	02.15 to 02.0
06-07	0000 0001 0001 0100	03.15 to 03.0
08-09	Reserved	04.15 to 04.0
0A-0B	Vendor Specific PHY	05.15 to 05.0
0C-0D	Snooping Port Configuration	06.15 to 06.0
0E-0F	Monitored Src Host I [47:32]	07.15 to 07.0

Table 21: AL116 EEPROM Mapping (Continued)

10-11	Monitored Src Host II [31:16]	08.15 to 08.0
12-13	Monitored Src Host III [15:0]	09.15 to 09.0
14-15	Monitored Dst Host I [47:32]	0A.15 to 0A.0
16-17	Monitored Dst Host II [31:16]	0B.15 to 0B.0
18-19	Monitored Dst Host III [15:0]	0C.15 to 0C.0
1A-1B	Port 0 Configuration I	0D.15 to 0D.0
1C-1D	Port 0 Configuration II	0E.15 to 0E.0
1E-1F	Port 1 Configuration I	0F.15 to 0F.0
20-21	Port 1 Configuration II	10.15 to 10.0
22-23	Port 2 Configuration I	11.15 to 11.0
24-25	Port 2 Configuration II	12.15 to 12.0
26-27	Port 3 Configuration I	13.15 to 13.0
28-29	Port 3 Configuration II	14.15 to 14.0
2A-2B	Port 4 Configuration I	15.15 to 15.0
2C-2D	Port 4 Configuration II	16.15 to 16.0
2E-2F	Port 5 Configuration I	17.15 to 17.0
30-31	Port 5 Configuration II	18.15 to 18.0
32-33	Port 6 Configuration I	19.15 to 19.0
34-35	Port 6 Configuration II	1A.15 to 1A.0
36-37	Port 7 Configuration I	1B.15 to 1B.0
38-39	Port 7 Configuration II	1C.15 to 1C.0
3A-3B	Port 0 VLAN Map I	1D.15 to 1D.0
3C-3D	Port 0 VLAN Map II	1E.15 to 1E.0
3E-3F	Port 1 VLAN Map I	1F.15 to 1F.0
40-41	Port 1 VLAN Map II	20.15 to 20.0
42-43	Port 2 VLAN Map I	21.15 to 21.0
44-45	Port 2 VLAN Map II	22.15 to 22.0
46-47	Port 3 VLAN Map I	23.15 to 23.0
48-49	Port 3 VLAN Map II	24.15 to 24.0
4A-4B	Port 4 VLAN Map I	25.15 to 25.0

Table 21: AL116 EEPROM Mapping (Continued)

4C-4D	Port 4 VLAN Map II	26.15 to 26.0
4E-4F	Port 5 VLAN Map I	27.15 to 27.0
50-51	Port 5 VLAN Map II	28.15 to 28.0
52-53	Port 6 VLAN Map I	29.15 to 29.0
54-55	Port 6 VLAN Map II	2A.15 to 2A.0
56-57	Port 7 VLAN Map I	2B.15 to 2B.0
58-59	Port 7 VLAN Map II	2C.15 to 2C.0
5A-5B	Reserved	
5C-5D	Checksum	47
5E-5F	Port 0 to Trunk Port Assignment	2D.15 to 2D.0
60-61	Port 1 to Trunk Port Assignment	2E.15 to 2E.0
62-63	Port 2 to Trunk Port Assignment	2F.15 to 2F.0
64-65	Port 3 to Trunk Port Assignment	30.15 to 30.0
66-67	Port 4 to Trunk Port Assignment	31.15 to 31.0
68-69	Port 5 to Trunk Port Assignment	32.15 to 32.0
6A-6B	Port 6 to Trunk Port Assignment	33.15 to 33.0
6C-6D	Port 7 to Trunk Port Assignment	34.15 to 34.0
6E	Reserved	
6F	Last Entry Address	
70-71	Static Entry 1 (Port Number)	
72-73	Static Entry 1 (MAC [47:32])	
74-75	Static Entry 1 (MAC [31:16])	
76-77	Static Entry 1 (MAC [15:0])	
78-7F	Static Entry 2	
80-87	Static Entry 3	
88-8F	Static Entry 4	
90-97	Static Entry 5	
98-9F	Static Entry 6	
A0-A7	Static Entry 7	
A8-AF	Static Entry 8	

Table 21: AL116 EEPROM Mapping (Continued)

B0-B7	Static Entry 9	
B8-BF	Static Entry 10	
C0-C7	Static Entry 11	
C8-CF	Static Entry 12	
D0-D7	Static Entry 13	
D8-DF	Static Entry 14	
E0-E7	Static Entry 15	
E8-EF	Static Entry 16	
F0-F7	Static Entry 17	
F8-FF	Static Entry 18	

3.18 SGRAM Interface

All ports of the AL116 work in Store-And-Forward mode so that all ports can support both 10 Mbit/s and 100 Mbit/s data speed. The AL116 utilize a central memory buffer pool, which is shared by all ports within the same device. After a frame is received, it is passed across the SGRAM interface and stored in the buffer. During transmit, the frame is retrieved from the buffer pool and forwarded to the destination port.

The AL116 is designed to use 8 Mbit SGRAM or 16 Mbit SGRAM for cost and performance.

The SGRAM is accessed in page burst access mode for very high speed access. This burst mode is repeatedly accessing the same column. If the burst mode reaches the end of the column address, then it wraps around to the first column address (=0) and continues to count until interrupted by a news read/write, pre-charge, or burst stop command.

The AL116 will initialize the SGRAM automatically. It pre-charges all banks and inserts eight auto–refresh commands. It will also program the mode registers for the AL116 read and write operations.

SGRAM essentially is a SDRAM. Dynamic memories must be refreshed periodically to prevent data loss. The SGRAM has auto-refresh which it also uses to refresh address counters. The SGRAM Auto-refresh command generates a pre-charge command internally in the SGRAM. The AL116 will insert an auto-refresh command once every 15 us.

4. Register Description

Table 22: Register Table Summary

REGISTER ID	REGISTER DESCRIPTION
00	System Configuration I
01	System Configuration II
02	System Configuration III
03	Reserved
04	Testing Register
05	Vendor Specific PHY Status
06	Port Monitoring Configuration
07	Monitored Source Host I [47:32]
08	Monitored Source Host II [31:16]
09	Monitored Source Host III [15:0]
0A	Monitored Destination Host I [47:32]
0B	Monitored Destination Host II [31:16]
0C	Monitored Destination Host III [15:0]
0D	Port 0 Configuration I
0E	Port 0 Configuration II
0F	Port 1 Configuration I
10	Port 1 Configuration II
11	Port 2 Configuration I
12	Port 2 Configuration II
13	Port 3 Configuration I
14	Port 3 Configuration II
15	Port 4 Configuration I
16	Port 4 Configuration II
17	Port 5 Configuration I
18	Port 5 Configuration II
19	Port 6 Configuration I
1A	Port 6 Configuration II

Table 22: Register Table Summary

1B	Port 7 Configuration I
1C	Port 7 Configuration II
1D	Port 0 VLAN Map I
1E	Port 0 VLAN Map II
1F	Port 1 VLAN Map I
20	Port 1 VLAN Map II
21	Port 2 VLAN Map I
22	Port 2 VLAN Map II
23	Port 3 VLAN Map I
24	Port 3 VLAN Map II
25	Port 4 VLAN Map I
26	Port 4 VLAN Map II
27	Port 5 VLAN Map I
28	Port 5 VLAN Map II
29	Port 6 VLAN Map I
2A	Port 6 VLAN Map II
2B	Port 7 VLAN Map I
2C	Port 7 VLAN Map II
2D	Port 0 to Trunk Port Assignment
2E	Port 1 to Trunk Port Assignment
2F	Port 2 to Trunk Port Assignment
30	Port 3 to Trunk Port Assignment
31	Port 4 to Trunk Port Assignment
32	Port 5 to Trunk Port Assignment
33	Port 6 to Trunk Port Assignment
34	Port 7 to Trunk Port Assignment
35	Reserved
36	Reserved
37	Reserved
38	Reserved

Table 22: Register Table Summary

39	System Status Register
3A	Port 0 Operation Status
3B	Port 1 Operation Status
3C	Port 2 Operation Status
3D	Port 3 Operation Status
3E	Port 4 Operation Status
3F	Port 5 Operation Status
40	Port 6 Operation Status
41	Port 7 Operation Status
42	Indirect Resource Access Command
43	Indirect Resource Access Data I
44	Indirect Resource Access Data II
45	Indirect Resource Access Data III
46	Indirect Resource Access Data IV
47	Check Sum

System Configuration Register I (Register 00)

The registers 01 to 03 are global system configuration registers. The option selected in this register affect the overall system operation.

Table 23: System Configuration Register I (Register 00)

BIT	NAME	DESCRIPTION
15	CPUprst	CPU Present. This bit is set by the AL116, when it detects the EEPROM is absent. The device will assume the CPU is present.
14	FloodCtl	Flooding Control. Controls the forwarding of unicast frames with unknown destination received from the non-uplink ports. 0: Disable. Frames received with an unknown unicast destination MAC address will be forwarded to all the ports (excluding the receiving port) within the VLANs specified at the receiving port. 1: Enable. Frames received with an unknown unicast destination MAC address will be forwarded to the uplink port specified for the receiving port.
13	SecMgmt	Security Enforcement. 0: Security Off. The security violation at a secured port will not change its port state. 1: Security On. The security violation at a secured port will cause the port into DISABLE state.
12	AgeEn	Switch Table Entry Aging Control. 0: Disable. The table aging process will be stopped. 1: Enable. The table aging process will be running to age every dynamically learned table entry.
11	TCNVG	Table Convergence Control. 0: Disable. The device will not communicate with other devices about its locally learned MAC table entries. 1: Enable. The device will run a slow background process to periodically transfer locally learned table entries for other devices to learn.
10	STPEN	Spanning Tree Protocol Enable Control. 0: Disable. The BPDU frames received from network ports will be treated as regular broadcast frames. 1: Enable. The BPDU frames received from network ports will be forwarded only to the CPU port.
9	PInMon	Port Incoming Frame Flow Monitoring Enable Cable. 0: Disable 1: Enable
8	POutMon	Port Outgoing Frame Flow Monitoring Enable Cable. 0: Disable 1: Enable

Table 23: System Configuration Register I (Register 00) (Continued)

7	CPUcfgrdy	CPU Configuration Ready. This bit is set by the AL116 when the AL116 is initialized by the CPU. 0: Not initialized. 1: Register file initialization done.
6	NetMgmt	Network Management Enable Control. 0: Disable. The device will not generate MIB events. 1: Enable. The device will generate MIB events and propagate them onto the ring.
5	InitDone	System Initialization Complete. This bit is set by the CPU when initialization is completed under the CPU initialization mode. For unmanaged switch, this bit is not relevant.
4	RMII	0: MII Interface. 1: RMII Interface.
3	L2Trunk	Layer 2 Trunk Loading Method. 0: Port based loading. Trunking decisions will be based on Trunk Port Assignment Registers. 1: MAC address based loading. Trunking decisions will be based on source port MAC addresses.
2	TimeoutEN	Frame Time Out Enable. 0: Device will not timeout frames based on MaxDelay. 1: Device will timeout frames.
1~0	Reserved	Reserved or factory use. Bits should be set to 0.

Table 24: System Configuration Register II (Register 01)

BIT	NAME	DESCRIPTION
15~8	MaxAge	Maximum age for dynamically learned MAC entries. 0000 0000: 1 sec. to 1111 1111: 256 sec.
7~6	MaxDelay	Maximum frame transition delay through the switch. 00: 1 second 01: 2 seconds 10: 3 seconds 11: 4 seconds
5~4	MaxStorm	Maximum number of broadcast frames that can be accumulated in each input frame buffer. 00: 16 frames 01: 32 frames 10: 48 frames 11: 64 frames
3	SuperMAC	0: Disable. Device will perform the IEEE standard exponential back off algorithm when a collision occurs. 1: Enable. When collisions occur, the AL116 will back off up to 3 slots.
2	REC	Retry on Excessive Collision. 0: Normal collision handling. 1: Retry transmission after 16 consecutive collisions.
1~0	L2TbitSel	Select the bits position for MAC address to trunk assignment. 00: Source MAC Address [1:0] 01: Source MAC Address [3:2] 10: Source MAC Address [5:4] 11: Source MAC Address [7:6]

Table 25: System Configuration Register III (Register 02)

BIT	NAME	DESCRIPTION
15	Reserved	Reserved (Must set to 0)
14	DisPHYRst	PHY Reset Option. 0: Reset PHY on link down in MDIO flow. 1: Don’t reset PHY on link down in MDIO flow.
13	StatusReset	Writing a “1” will reset status registers.
12	RegPg	0: First page. 1: Second page.
11	BebSel	Binary Exponential Backoff Select. 0: Normal 1: Binary exponential.

Table 25: System Configuration Register III (Register 02) (Continued)

10	SlowAge	Aging Time Resolution 0: Normal aging. 1: Slow down aging.
9	BpIPG84	Backpressure IPG Select Enable. 0: IPG = 96BT 1: IPG = 64BT
8	IPG64	Standard IPG Control. 0: IPG = 96BT 1: IPG = 64BT
7~6	PRate	Backpressure Port Rate. (Collision based)
5	SG16M	SGRAM Select. 0: 8Mbit/s SGRAM 1: 16Mbit/s SGRAM
4	BPCOL	Backpressure Control. 0: Carrier based. 1: Collision based.
3	ETEnb	External Table Enable. 0: Disable 1: Enable
2	ET16K	Table Size Selection. 0: 8K 1: 16K
1	MCTrap	1: Multicast/Broadcast Frame forward to CPU only.
0	FlowCtrlBC	0: Flow control multicast. 1: Flow control broadcast.

Reserved Register (Register 03)

This register is reserved for Allayer's use. The bits should be set as 0000 0001 0001 0100.

Testing Register (Register 04)

This register is reserved for Allayer's use. The bits should be set as 0000 0000 0000 1000.

Vendor Specific PHY Register (Register 05)

This register is used to program vendor specific PHY options. It is also used for programming the Vendor Specific PHY register location and bit location of the operation status.

Table 26: Vendor Specific PHY Register (Register 05)

BIT	NAME	DESCRIPTION
15	PHYAD	Setting this bit to 1 will program the MDIO PHY address to addresses 16 to 23.
14	MCIkSpd	Setting this bit to 1 will reduce the MDIO clock speed to 17HKz.
13	PortOrder	Setting this bit to 1 will reverse the PHY ID/port number of the switch.
12~8	PHYOpReg	PHY's Operation Status Register Number.
7~4	PHYSpBit	PHY's Data Rate Status Register Bit Number.
3~0	PHYDxModeBit	PHY's Operating Duplex Mode Status Register Bit Number.

Port Monitoring Configuration Register (Register 06)

This register configures port monitoring. It sets the monitored port and the TX and RX snooping ports.

Table 27: Port Monitoring Configuration Register (Register 06)

BIT	NAME	DESCRIPTION
15	Reserved	Bit should be set at 0.
14~10	MdPID	Monitored Port ID.
9~5	MgIPID	Snooping Port ID for incoming frame flow.
4~0	MgOPID	Snooping Port ID for outgoing frame flow.

RMON Source and Destination Registers (Registers 07 to 0C)

These registers are used by the RMON manager for frame counting. The RMON manager counts the frames to (destination) and from (source) these MAC addresses stored in the register.

The 48 bit MAC address is programmed in three separate registers. Source MAC address is stored in registers 07 to 09 and destination MAC address in register 0A to 0C.

Table 28: RMON Source and Destination Registers (Registers 07 to 09)

REGISTER	BIT	NAME	DESCRIPTION
07	15~0	SRCMAC[47:32]	Monitored Source Host MAC Address
08	15~0	SRCMAC[31:16]	Monitored Source Host MAC Address
09	15~0	SRCMAC[15:0]	Monitored Source Host MAC Address

Table 29: RMON Source and Destination Registers (Registers 0A to 0C)

REGISTER	BIT	NAME	DESCRIPTION
0A	15~0	DSTMAC[47:32]	Monitored Destination Host MAC Address
0B	15~0	DSTMAC[31:16]	Monitored Destination Host MAC Address
0C	15~0	DSTMAC[15:0]	Monitored Destination Host MAC Address

Port Configuration Registers (Registers 0D to 1C)

Registers 0D to 1C are for local port configuration. There are two port configurations per port. Port 0 port configuration uses register 0D and 0E, Port 1 register 0F and 10, etc.

Port Configuration Register I

- Uplink ID - this is a six-bit link ID to assign an uplink port to the local port. The uplink port can be one of three types; a single port, a trunk or a CPU port.

  If the uplink is a single port, the format of the port is [0][Dev_ID][Port_ID]

  If the uplink is a trunk, then the bits should read [100][trunk number]. The trunk number is numbered [Dev_ID][Trunk_ID].

  If the local port is an uplink port, the uplink ID should be its own port ID. Any frame with unlearned SA will then be filtered.

Table 30: Port Configuration Register I

BIT	NAME	DESCRIPTION
15~10	UpLinkID	Uplink ID associated with the port. 0XXYYY: Port ID with XX as the device ID and YYY as the port ID. 100XXN: Trunk ID with XX as the device ID and N as the trunk ID. 111XXX: The CPU Port. Others: Reserved.
9	Tmember	Trunk Member Port. 0: Individual port. 1: Member of trunk port.
8	Reserved	Bit should be set to zero.
7	StormCTL	Broadcast Storm Control Enable. 0: Storm control disable. The broadcast frame will not be throttled. 1: Storm control enable. If the accumulated number of broadcast frames in the input buffer of the port is over the threshold specified in the system configuration register, new incoming broadcast frames will be discarded until the number has been reduced below the threshold.
6	Security	Intrusion Protection. Security control for the frames received from non-uplink ports. 0: Security off. The forwarding decision made about frames received from the port will not involve the source MAC address checking. 1: Security on. The frames received from the port with an unknown source MAC address or with source MAC address learned previously from another port will be discarded.
5	CPUOn	The CPU Port VLAN Membership. 0: Non-member. Broadcast frames received from the port will not be forwarded to the CPU port. 1: Member. Broadcast frames received from the port will be forwarded to the CPU port in addition to other member ports specified in the VLAN Map register of the port (excluding the source port).
4	LrnDis	Learning Disable. 0: Source address from this port will be learned. 1: Source address from this port will not be learned.

Table 30: Port Configuration Register I (Continued)

3~2	PortST	Port State Control. 00: Disable. All incoming frames from the PHY will be discarded; all outgoing frames will be masked from the path to the PHY. 01: Blocking-N-Listening. All incoming frames except incoming BPDUs from the PHY will be discarded; all outgoing frames except outgoing BPDUs will be masked from the path to the PHY. 10: Learning. The source information of all incoming frames from the PHY will be learned; all incoming frames except incoming BPDUs from the PHY will be discarded after being learned; all outgoing frames except outgoing BPDUs will be masked from the path to the PHY. 11: Forwarding. The source information of all incoming frames from the PHY will be learned; all incoming frames will be forwarded based on the switch routing decision; all outgoing frames will be transmitted to the PHY.
1~0	Reserved	Reserved (Must set to 0)

Table 31: Port Configuration Register II

BIT	NAME	DESCRIPTION
15~12	Reserved	Reserved
11	FlowCtrlFdEn	Flow Control Full Duplex Enable.
10	FlowCtrlHdEn	Flow Control Half Duplex Enable.
9~6	MDIOCfg[3:0]	MDIO Configuration. 0001: Master mode PHY management. 0010: Slave mode PHY management. 0111: Force mode.
5	MDIODis	MDIO Disable. 0: MDIO is enabled. 1: MIDO is disabled.
4	LinkUp	This bit is not relevant when MDIO is enabled. When MDIO is disabled, this bit forces the port into link up or link down state. 0: Link Down. 1: Link Up.
3	PrtMode100F	100 Full Duplex Mode.
2	PrtMode100H	100 Half Duplex Mode.
1	PrtMode 10F	10 Full Duplex Mode.
0	PrtMode 10H	10 Half Duplex Mode.

Port VLAN Map Registers (Registers 1D to 2C)

These registers provide the VLAN map for each port.

A VLAN worksheet is provided in Appendix I.

Table 32: Port VLAN Map Registers (Registers 1D to 2C)

REGISTER	BIT	NAME	DESCRIPTION
1D Port0 1F Port1 21 Port2 23 Port3 25 Port4 27 Port5 29 Port6 2B Port7	15~8	Dev3Map	Port VLAN Map corresponding to the port7~port0 of the device with Dev_ID of 11. 0: Non-member port. 1: Member port.
1D Port0 1F Port1 21 Port2 23 Port3 25 Port4 27 Port5 29 Port6 2B Port7	7~0	Dev2Map	Port VLAN Map corresponding to the port7~port0 of the device with Dev_ID of 10. 0: Non-member port. 1: Member port.
1E Port0 20 Port1 22 Port2 24 Port3 26 Port4 28 Port5 2A Port6 2C Port7	15~8	Dev1Map	Port VLAN Map corresponding to the port7~port0 of the device with Dev_ID of 01. 0: Non-member port. 1: Member port.
1E Port0 20 Port1 22 Port2 24 Port3 26 Port4 28 Port5 2A Port6 2C Port7	7~0	Dev0Map	Port VLAN Map corresponding to the port7~port0 of the device with Dev_ID of 00. 0: Non-member port. 1: Member port.

Port Trunk Port Assignment Registers (Registers 2D to 34)

The Port to Trunk Port assignment register assigns a port to a trunk for port-based load balancing trunking. Please see example in the trunking section.

A port to trunk port work sheet is provided in Appendix II.

PORT NUMBER	REGISTER
0	2D
1	2E
2	2F
3	30
4	31
5	32
6	33
7	34

Table 33: Port Trunk Port Assignment Registers (Registers 2D to 34)

BIT	NAME	DESCRIPTION
15~14	Trunk 7	Trunk Port of Trunk 7 00: Port 4, 01: Port 5 10: Port 6, 11: Port 7
13~12	Trunk 6	Trunk Port of Trunk 6 00: Port 0, 01: Port 1 10: Port 2, 11: Port 3
11~10	Trunk 5	Trunk Port of Trunk 5 00: Port 4, 01: Port 5 10: Port 6, 11: Port 7
9~8	Trunk 4	Trunk Port of Trunk 4 00: Port 0, 01: Port 1 10: Port 2, 11: Port 3
7~6	Trunk 3	Trunk Port of Trunk 3 00: Port 4, 01: Port 5 10: Port 6, 11: Port 7
5~4	Trunk 2	Trunk Port of Trunk 2 00: Port 0, 01: Port 1 10: Port 2, 11: Port 3

Table 33: Port Trunk Port Assignment Registers (Registers 2D to 34)

BIT	NAME	DESCRIPTION
3~2	Trunk 1	Trunk Port of Trunk 1 00: Port 4, 01: Port 5 10: Port 6, 11: Port 7
1~0	Trunk 0	Trunk Port of Trunk 0 00: Port 0, 01: Port 1 10: Port 2, 11: Port 3

Table 34: System Status Register (Register 39)

BIT	NAME	DESCRIPTION
15	EPTimeOut	EEPROM Time Out. 0: EEPROM initialized the device. 1: Device is ready to be programmed by the CPU.
14	CheckSumEr	EEPROM Checksum Error.
13	SGRAMinit	SGRAM Initialization Done.
12	SRAMinit	SRAM Initialization Done.
11	REGinit	Register Initialization Done.
10~7	Traffic Counter	Traffic Counter.
6~4	Reserved	
3~0	Chip ID	0000: AL116

Port Operation Status Registers (Register 3A to 41)

Registers 3A to 41 are status indication on a per port basis. These are read only register. Port 0 port status is in register 3A; Port 1 register 3B…and port 7 register 41.

Table 35: Port Operation Status Registers (Register 3A to 41)

BIT	NAME	DESCRIPTION
15	LinkFail	Port Link Status. 0: Normal 1: Fail
14	PHYError	Port PHY Status. 0: Normal 1: Error
13	Sviolation	Port Security Violation. 0: Normal 1: Violation
12	FlowCtrl	Flow Control. If port mode ([1:0]) is 2'b01 or 2'b11: 0: Pause disable. 1: Pause enable. If port mode ([1:0]) is 2'b00 or 2'b10: 0: Back pressure based on CRS. 1: Back pressure based on collision.
11	Stormed	Port Broadcast Storm Status. 0: Normal 1: Stormed
10	InBFull	Port Input Buffer Full Status. 0: Normal 1: Input buffer full experienced.
9	TblUNAVL	Table Entry Unavailability for MAC Learning. 0: Normal 1: Unavailability experienced.
8	Jabbered	Port Jabber Status. 0: Normal 1: Jabber experienced.
7	LateCOL	Port Late Collision Status. 0: Normal 1: Late collision experienced.
6	TxPaused	Port Transmit Pause Status. 0: No transmit pause experienced. 1: Transmit pause experienced.
5	CRSLoss	Port Carrier Sense Loss During Transmission Status. 0: No carrier sense loss experienced. 1: Carrier sense loss experienced.

Table 35: Port Operation Status Registers (Register 3A to 41) (Continued)

4	FalseCRS	False Carrier Status. 0: Normal 1: False carrier experienced.
3	Underflow	Transmit Queue Underflow Status. 0: Normal 1: Underflow experienced.
2	TimeOut	Frame Time Out. 0: Normal 1: Frame time out experienced.
1~0	PortMode	Port Operating Mode. 00: 10Mb half-duplex. 01: 10Mb full-duplex. 10: 100Mb half-duplex. 11: 100Mb full-duplex.

Indirect Resource Access Command Register (Register 42)

This register is used for managing the resource of the switch.

Table 36: Indirect Resource Access Command Register (Register 42)

BIT	NAME	DESCRIPTION
15	CmdDone	Command Done. 0: Execute new command. 1: Command done.
14	Operation	Read/Write Operation Command. 0: Read operation. 1: Write operation.
13~11	ResType	Type of Accessed Resource. 000: PHY registers. 001: EEPROM 010: SGRAM 011: MAC address table 1; Read: MAC table address read. Write: MAC address learn. 100: MAC address table 2; Read: MAC address search. Write: MAC address delete. 101-111: Reserved
10	ExtRD	External MAC Address Table Read. If ResType = 011 and Operation = 0 0: On-chip address table read. 1: Off-chip address table read.
9~0	ResAddr	The Address of the Entry within the Accessed Resource.

Table 37: Indirect Resource Access Data I Register (Register 43)

BIT	NAME	DESCRIPTION
15~0	IRAData	Indirect Resource Access Data 1.

Table 38: Indirect Resource Access Data II Register (Register 44)

BIT	NAME	DESCRIPTION
15~0	IRAData	Indirect Resource Access Data 2.

Table 39: Indirect Resource Access Data III Register (Register 45)

BIT	NAME	DESCRIPTION
15~0	IRAData	Indirect Resource Access Data 3.

Table 40: Indirect Resource Access Data IV Register (Register 46)

BIT	NAME	DESCRIPTION
15~0	IRAData	Indirect Resource Access Data 4.

Table 41: Check Sum (Register 47)

BIT	NAME	DESCRIPTION
15~8	CheckSum	Check Sum value of AL116 register contents.
7~0	Reserved	

5. Timing Requirements

Table 42: MII Transmit Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{tdv}	TXCLK to TXD valid time.	4	-	12	ns
t_{txev}	TXCLK to TXEN valid time.	4	-	12	ns

Table 43: RMII Transmit Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{tdv}	TXCLK to TXD valid time.	3	-	9	ns
t_{txev}	TXCLK to TXEN valid time.	3	-	14	ns

Note: Delays are assuming 10pf loading on the output pins.

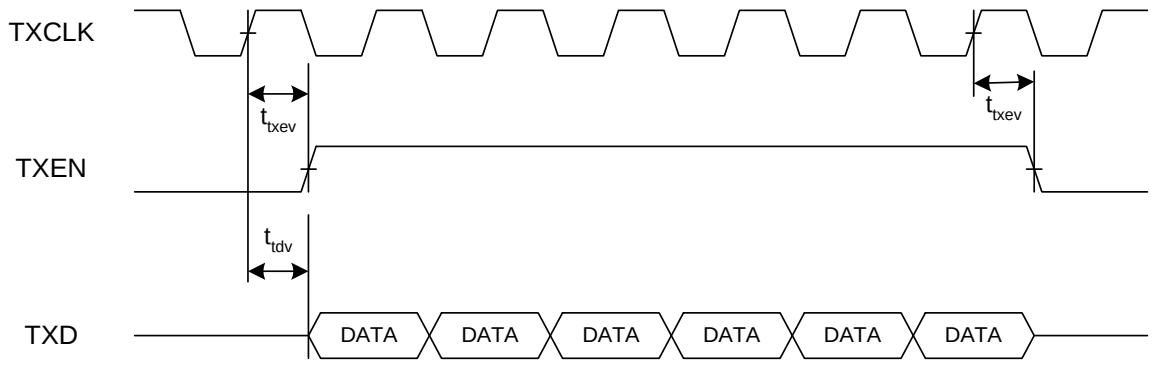

Figure 11 RMII/MII Transmit Timing Diagram

Table 44: MII Receive Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{rxds}	RX_DV, RXD, RX_ER, setup time.	10	-	-	ns
t_{rxdh}	RX_DV, RXD, RX_ER hold time.	5	-	-	ns

Table 45: RMII Receive Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{rxds}	RX_DV, RXD, RX_ER, setup time.	3	-	-	ns
t_{rxdh}	RX_DV, RXD, RX_ER hold time.	3	-	-	ns

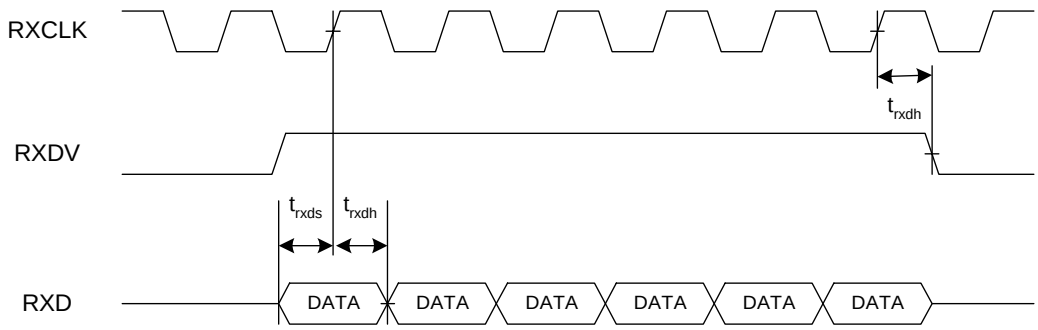

Figure 12 RMII/MII Receive Timing Diagram

Table 46: RoX Bus Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{roxs}	Setup time.	2	-	-	ns
t_{roxh}	Hold time.	2	-	-	ns

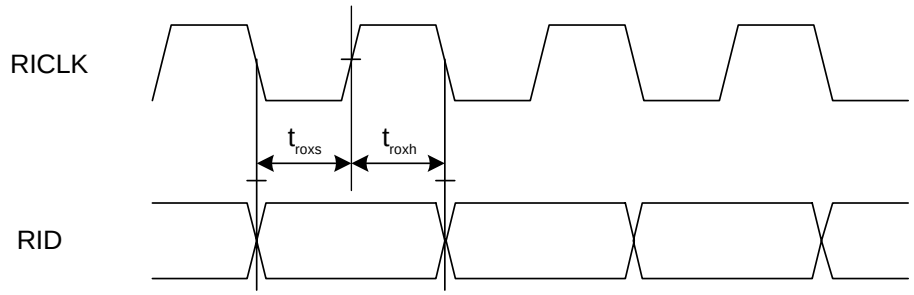

Figure 13 RoX II Bus Timing

Table 47: PHY Management (MDIO) Read Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{ch}	MDC high time	420	425	430	ns
t_{cl}	MDC low time	420	425	430	ns
t_{mc}	MDC period	840	850	860	ns
t_{ms}	MDIO setup time	10	-	15	ns
t_{mh}	MDIO hold time	10	-	-	ns

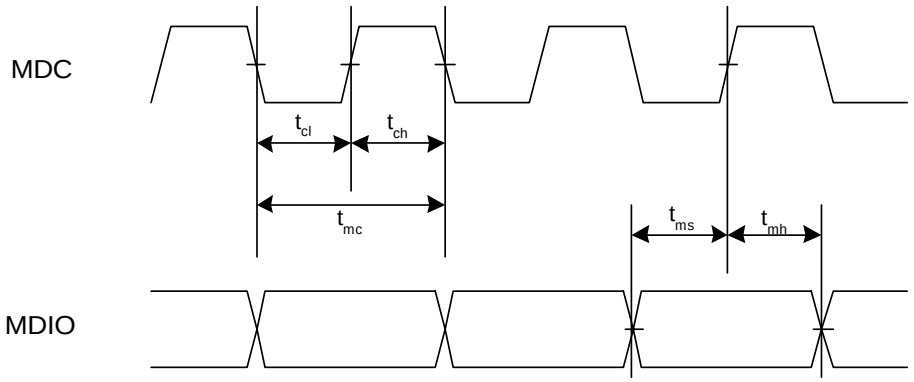

Figure 14 PHY Management Read Timing

Table 48: PHY Management Write Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{ch}	MDC high time	420	425	430	ns
t_{cl}	MDC low time	420	425	430	ns
t_{mc}	MDC period	840	850	860	ns
t_{d}	MDIO output delay	40	-	52	ns

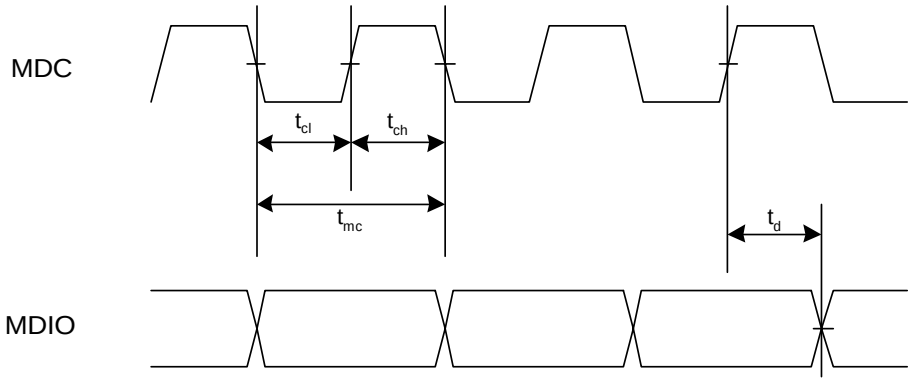

Figure 15 PHY Management Write Timing

Table 49: SGRAM Refresh Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{AH}	Access hold time	1	-	-	ns
t_{AS}	Access setup time	3	-	-	ns
t_{CH}	PBCS#, PBRAS#, PBWE# hold time	1	-	-	ns
t_{CHI}	Clock high level width	3.5	-	-	ns
t_{CK}	System clock cycle time	13	-	-	ns
t_{CKH}	CKE hold time	1	-	-	ns
t_{CKS}	CKE setup time	3	-	-	ns
t_{CL}	Clock low level width	3.5	-	-	ns
t_{CS}	PBCS#, PBRAS#, PBWE# setup time	3	-	-	ns
t_{RP}	Precharge command period	30	-	-	ns
t_{RC}	Auto-refresh to auto-refresh period	90	-	-	ns

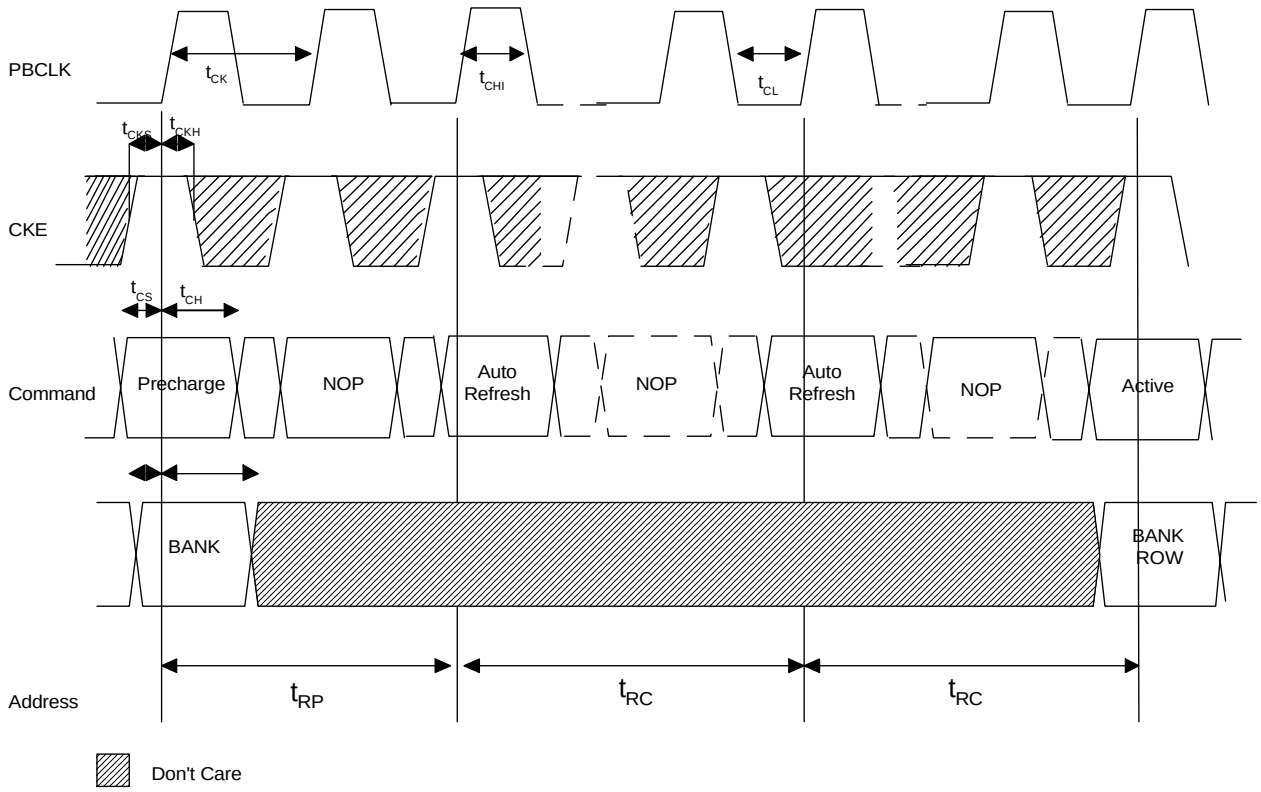

Figure 16 SGRAM Refresh Timing

Table 50: SGRAM Read Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{AC}	Access time	-	-	10	ns
t_{AH}	Access hold time	2	-	-	ns
t_{AS}	Access setup time	2.5	-	-	ns
t_{CH}	PBCS#, PBRAS#, PBWE# hold time	1	-	-	ns
t_{CHI}	Clock high level width	3	-	-	ns
t_{CK}	System clock cycle time	13	-	-	ns
t_{CKH}	CKE hold time	2	-	-	ns
t_{CKS}	CKE setup time	3	-	-	ns
t_{CL}	Clock low level width	3	-	-	ns
t_{CS}	PBCS#, PBRAS#, PBWE# setup time	2.5	-	-	ns
t_{HZ}	Data out high impedance time	-	-	8	ns
t_{LZ}	Data out low impedance time	2	-	-	ns
t_{OH}	Data out hold time	2	-	-	ns
t_{RAS}	Active to precharge command period	48	-	-	ns
t_{RCD}	Active to read delay	24	-	-	ns

Note: This timing requirement is for a SGRAM running at CAS Latency 2. Typically a -8 speed grade SGRAM needs to be used.

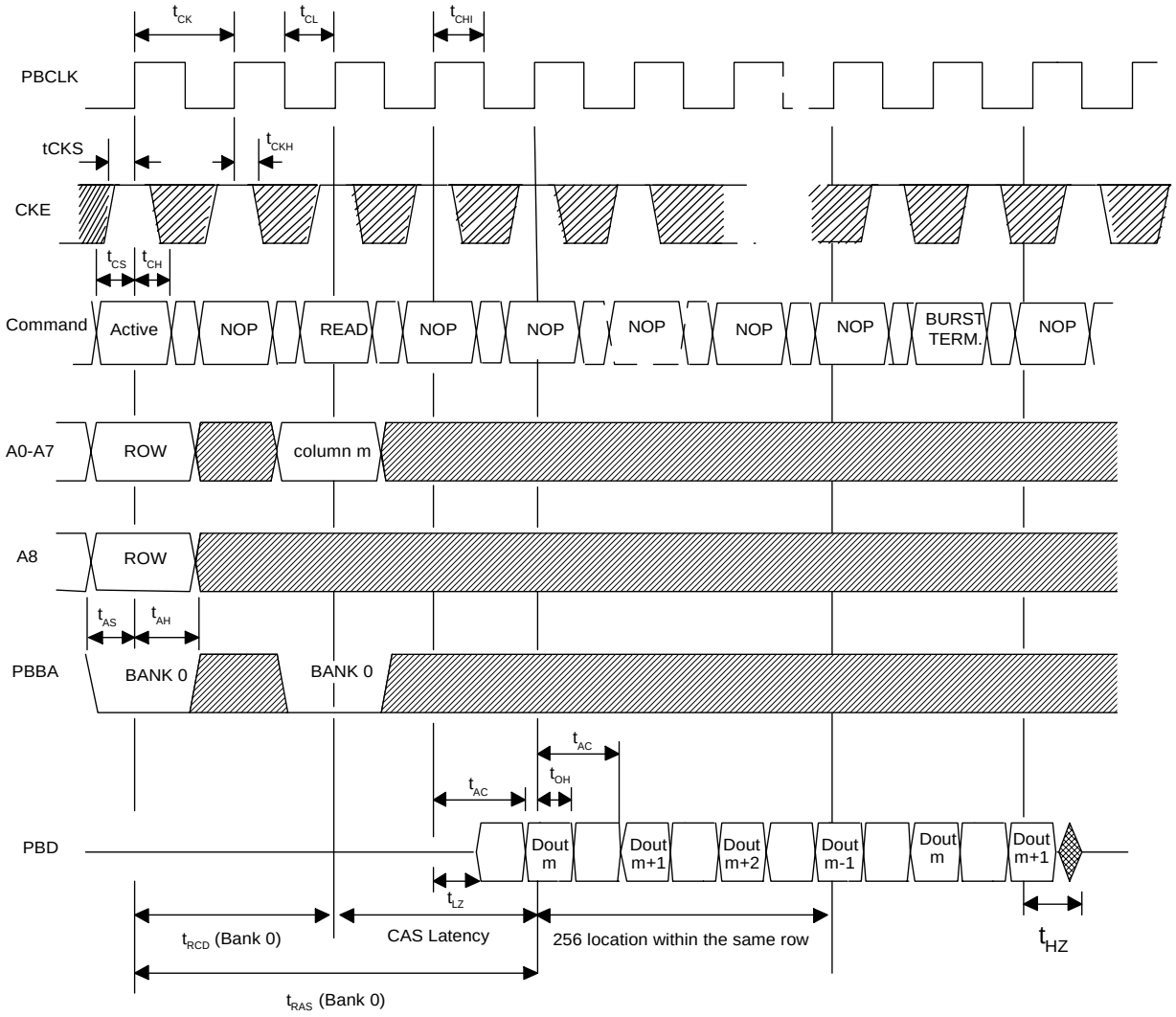

Figure 17 SGRAM Read Timing

Table 51: SGRAM Write Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{AH}	Access hold time	2	-	-	ns
t_{AS}	Access setup time	2.5	-	-	ns
t_{CH}	PBCS#, PBRAS#, PBWE# hold time	1	-	-	ns
t_{CHI}	Clock high level width	3	-	-	ns
t_{CK}	System clock cycle time	13	-	-	ns
t_{CKH}	CKE hold time	2	-	-	ns
t_{CKS}	CKE setup time	3	-	-	ns
t_{CL}	Clock low level width	3	-	-	ns
t_{CS}	PBCS#, PBRAS#, PBWE# setup time	2.5	-	-	ns
t_{DH}	Data in hold time	1	-	-	ns
t_{DS}	Data in setup time	2.5	-	-	ns
t_{RAS}	Active to precharge command period	48	-	100,000	ns
t_{RCD}	Active to read delay	24	-	-	ns

Note: This timing requirement is for a SGRAM running at CAS Latency 2. Typically a -8 speed grade SGRAM needs to be used.

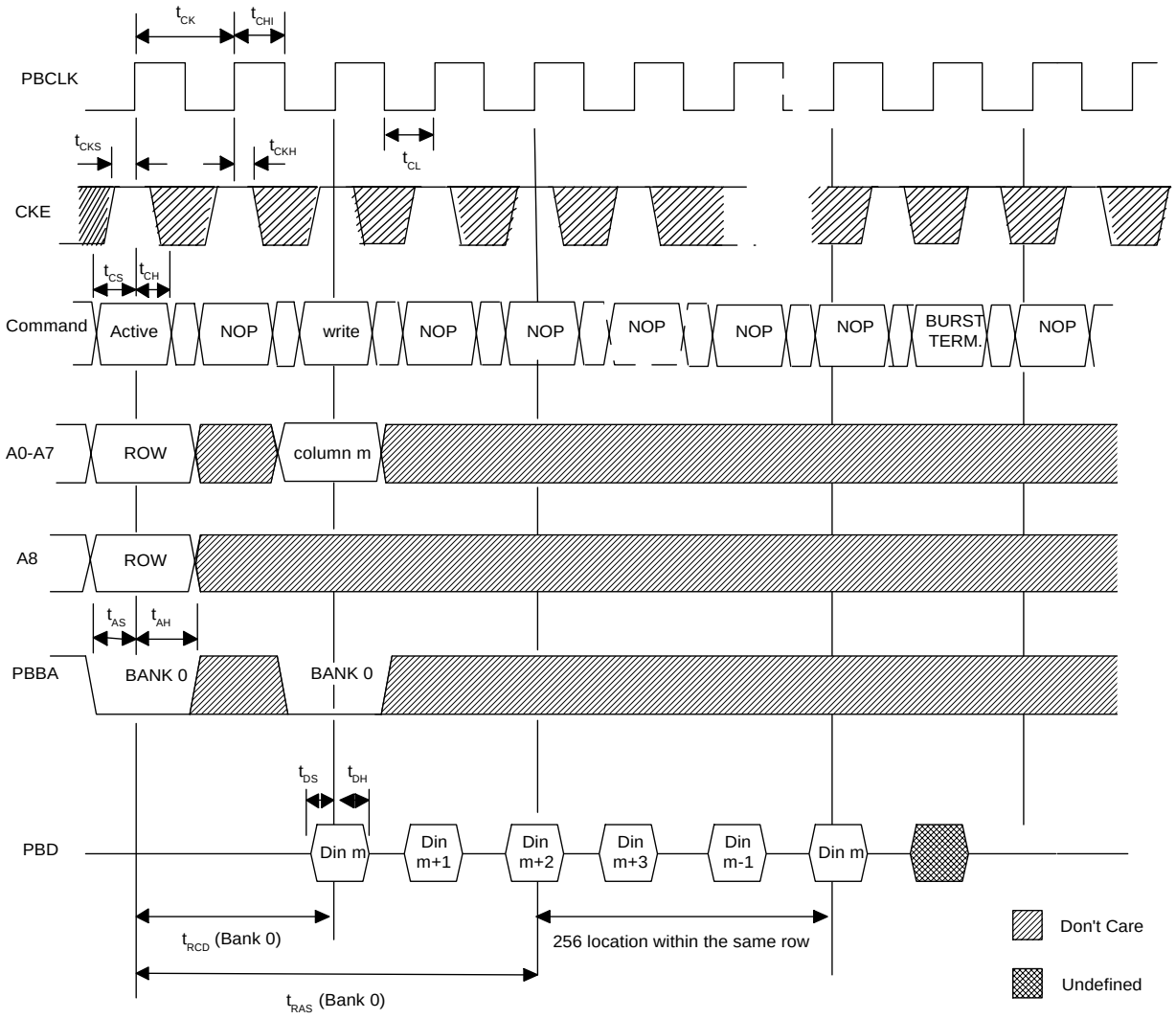

Figure 18 SGRAM Write Timing

6. Electrical Specifications

Note: Operation at absolute maximum ratings could cause permanent damage to the device.

Table 52: Maximum Ratings

DC Supply Voltage (Vcc)	-0.3V ~ + 3.6V
DC Input Voltage	-0.3 ~ Vcc + 0.3V
DC Output Voltage	-0.3 ~ Vcc + 0.3V
DC Supply Voltage to MII	-0.6V to 6.0V
DC Input Voltage to MII	-0.6 to Vcc5 + 0.3V
DC Output Voltage to MII	-0.6 to Vcc5 + 0.3V
Storage Temperature	-55 ^{o}C to +150 ^{o}C

Table 53: Recommended Operation Conditions

Supply Voltage	3.3V ± 0.3V
Operating Temperature	0 ^{o}C to 70 ^{o}C
Power Dissipation	1.7 W (typical)

Table 54: DC Electrical Characteristics

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Voh	Output Voltage-High, Ioh=4mA	2.4	-	-	V
Vol	Output Voltage-Low, Ioh=4mA	-	-	0.4	V
Ioz	High Impedance State Output Current	-10	-	10	uA
Iih	Input Current-high (With No Pull-up or Pull-down)	-10	-	10	uA
Iil	Input Current-low (With No Pull-up or Pull-down)	-10	-	10	uA
Vih	Input High Voltage	0.7*Vcc	-	-	V
Vil	Input Low Voltage	-	-	0.3*Vcc	V
Icc	Supply Current	-	-	-	mA

7. AL116 Mechanical Data

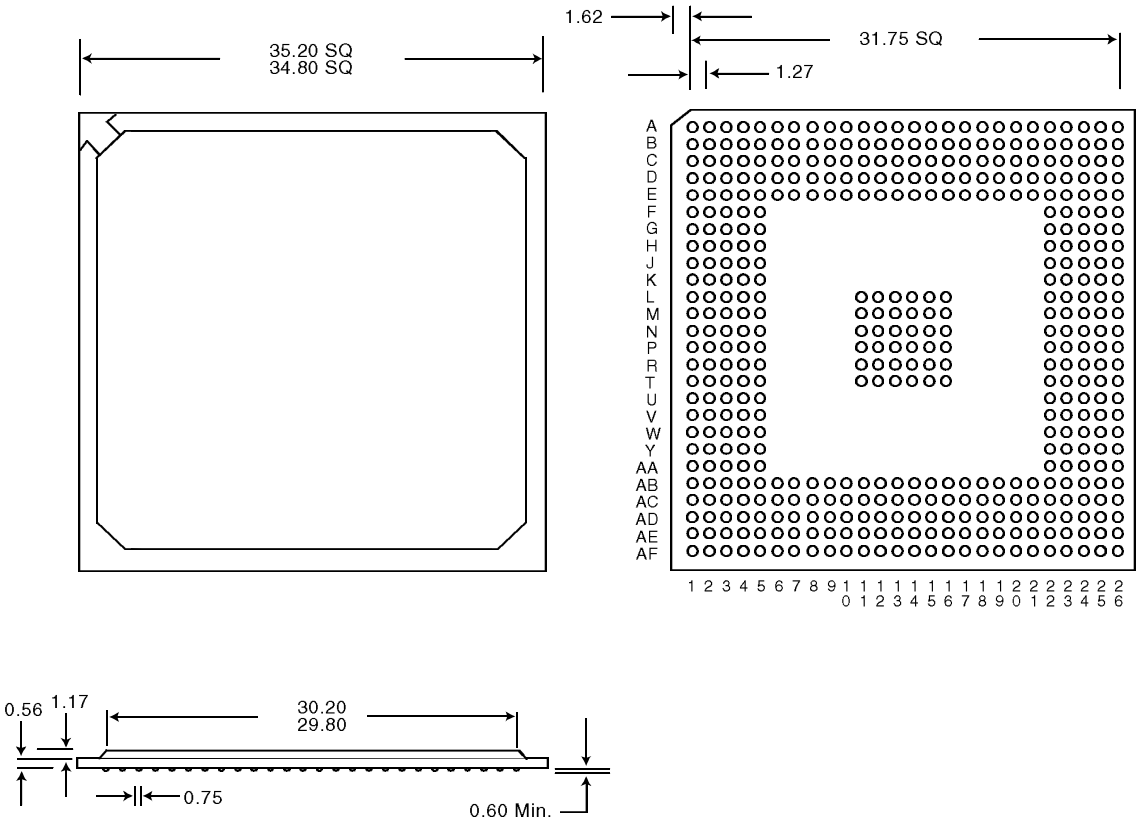

Figure 19 AL116 Mechanical Dimensions

8. Appendix I (VLAN Mapping Work Sheet)

PORT	BIT	PORT 0/REG. 1E	PORT 1/REG. 20	PORT 2/REG. 22	PORT 3/REG. 24	PORT 4/REG. 26	PORT 5/REG. 28	PORT 6/REG. 2A	PORT 7/REG. 2C
7	7								
6	6								
5	5								
4	4								
3	3								
2	2								
1	1								
0	0								

9. Appendix II (Port to Trunk Port Assignment Work Sheet)

	TRUNK / PORT	BIT/ VALUE	PORT 0/REG. 2D	PORT 1/REG. 2E	PORT 2/REG. 2F	PORT 3/REG. 30	PORT 4/REG. 31	PORT 5/REG. 32	PORT 6/REG. 33	PORT 7/REG. 34
TRUNK 1 BITS 3, 2	7	11								
	6	10								
	5	01								
	4	00								
TRUNK 0 BITS 1, 0	3	11								
	2	10								
	1	01								
	0	00								

10. Appendix III (Suggested Memory Components)

Note: This is only a partial list of memory components that can be used in Allayer devices.

The AL116 uses Frame Buffer SGRAM chips that require 32-bit wide SGRAM or SDRAM, that is 75 MHz or faster with CAS Latency 2.

The AL116 uses MAC Table Memory SSRAM chips that require Sync Burst pipelined SSRAM, 75 MHz or faster.

DEVICE	FREQ.	8 Mbit SGRAM	16 Mbit SGRAM	SSRAM
AL116	75 MHz	MoSys - MG802C256Q-10 Etron - EM635327Q-8	MoSys - MG802C512L-8 Etron - EM636227Q-8 Hitachi - HM5216326FP-8 Winbond - W971632AF-8	Micron - MT58LC64K32D8LG-11 IDT - 71V632S6PF

Revision History

Rev. 1.4 (7/13/99)

1. Added memory information in appendix III.

Rev. 1.4a (7/28/99)

1. Reformatted document.

2. Added new PHY management timing diagrams.

3. Added new RMII and MII timing diagrams.

Rev. 1.5 (9/22/99)

1. Switched pin numbers AF20 and AC21 in RoX output interface table.

2. Changed pin number B5 to B4 in EEPROM interface table.

3. Added pin names TRST, TMS, TDO, TDI, and TCLK to miscellaneous pins table.

4. Added AC15, D6, M22, and B17 to power interface table.

Prelim. 1.6 (11/8/99)

1. Updated table 25, pins 15-11 (system config. reg. III).

2. Updated MII transmit timing diagram.

3. Corrected tables 1-8 to reflect transmit signals are clocked out by the rising edge of the TX_CLK.

Prelim. 1.6 to Rev. 1.0 (5/00)

1. Fully released document.

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