SIEMENS

ICs for Communications

Synchronous Digital Hierarchy Transceiver SDHT

PXB 4240

Version 1.2

Preliminary Data Sheet 10.96

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Edition 10.96

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PXB 4240 **Revision History:** **Current Version: 10.96**		
Previous Version: Preliminary Data Sheet Version 1.1		
Page (in Version 1.1)	Page (in Version 1.2)	Subjects (changes since last revision)
page 59	page 68	Change of SDHT version value from 01 to 02 in the SDHT register.
-	page 58	Change of boundary scan ID from 1002C083 to 2002C083.
page 16	page 17	Change of XATMLOOP from active low to active high.
page 12	page 14	Change of INT from active high to active low.
page 17	page 18	Change of SLPINT from active low to active high.
page 60	page 82	Change of the address from both Test Mode bits Z21GEN and Z21EVAL.
page 17	page 18	Correction of the activation level of XSONET.
-	page 49	Introduction of a new control bit ATC for the activation of the performance counters.
page 58, page 59	page 68	Clarification of the Register Address Mapping.
page 78, page 79	page 97 page 97	Change of the read cycle of the microprocessor interface without usage of the ALE in such a way that the read deactivation during two successive read cycles is only determined by either the CS or the RD signal.
page 78, page 79	page 97 page 97	Clarification of the Microprocessor Timing Characteristics.
-	page 95	Clarification of the JTAG Timing Characteristics.
page 74 - page 79	page 87 - page 97	Update of the Electrical Characteristics.
-	page 58	Introduction of the Boundary Scan Table.
page 32	page 35	Correction of the State Diagrams for the Pointer Evaluation.
-	page 65	Summary of Loopback Applications.
page 64	page 78	Correction of the default values of the Mode registers after the Hardware reset.
page 12	page 13	Addition of pull-up/down resistors into the list of pin description.

1 Overview

The Synchronous Digital Hierarchy Transceiver (SDHT) is a member of the Siemens ATM chip set. SDHT is a complete Synchronous Optical Network/Synchronous Digital Hierarchy (SONET/SDH) framer for 155–MBit/s ATM implementations including Transmission Convergence (TC) Sublayer processing for ATM payloads. TC Sublayer processing includes cell delineation, Header Error Control (HEC) processing and payload scrambling according to ITU–T and The ATM Forum specifications.

The SDHT chip can be programmed to work in either ATM or VC-4 mode. In the ATM mode, SDHT provides the ATM layer with ATM cells via its Utopia level 1 interface. This mode is needed by equipment which really terminate the SDH network, for instance an ATM-Switch or an ATM-NIC with a STM-1 interface. The other VC-4 mode is needed by a broadband network termination equipment B-NT1 which is used at the public UNI. At this point, the network operator tests the availability of the broadband UNI only with the functionalities given by the SDH network. This means that the B-NT1 has to extract or insert the VC-4 into the STM-1 signal without any ATM processing. This functionality is provided by the SDHT in the VC-4 mode.

The TC Sublayer of the Physical Layer is handled according to ITU-T recommendation [I.432]. Cell header insertion/correction and discarding of idle/unassigned cells can be disabled. The insertion of idle/unassigned cells cannot be switched off, but is automatically suppressed if sufficient data is provided to SDHT for filling the STM–1/ STS–3c payload.

Mapping/demapping of ATM cells into/out of the STM–1 or STS–3c frames, overhead handling, and Operations and Maintenance (OAM) functions are performed according to ITU–T, Bellcore, ANSI, and The ATM Forum recommendations and specifications. Parameters which differ between STM–1 and STS–3c are separately programmable. The SDHT then performs all the OAM functions required for Loss of Signal (LOS), and adds the release condition for LOS.

In keeping with the modularity of the Siemens ATM chip set, the industry-standard UTOPIA interface [UTOP_1, UTOP_2] is used by SDHT and other components of the ATM chip set.

SDHT has a serial data interface operating at LVDS levels (Low–Voltage Differential Signal for SCI, defined by IEEE standard 1596.3 [LVDS]), which can be connected directly to optical driver circuits, and a generic 16–bit Microprocessor Interface for control of the chip. SDHT can be controlled by, and the overhead and status data is provided to, a 16– or 8–bit microprocessor. For example, an i80C186/8 may be connected directly to the SDHT. This µP interface is used identically in all members of the Siemens ATM chip set except the Segmentation and Reassembly Element (SARE), which uses the PCI interface. Additionally, SDHT has extra functions to control peripherals at the board level, e.g. clock switching, laser shutdown or closing loops.

The SDHT is offered in a Metric Quad Flat Pack package with 160 pins. It operates at a voltage of 3.3V. The power dissipation is less than 0.7 W. The chip includes a power down mode.

SIEMENS

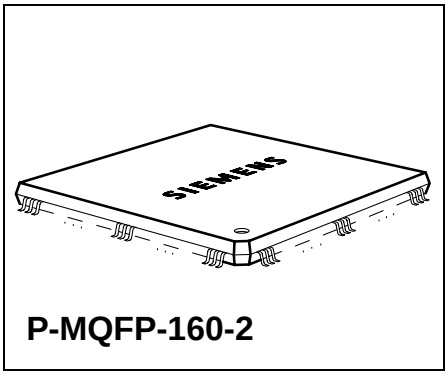
Synchronous Digital Hierarchy Transceiver SDHT

PXB 4240

Version 1.1

CMOS

1.1 Features



P-MQFP-160-2

- 155 Mbit/s transmission rate
- 2 operating modes: ATM and VC–4
- Single–port UTOPIA Interface
- 16–bit generic Microprocessor Interface
- Serial interface to optical transceiver
- Transmit Functions
  - User data rate of149.76 Mbit/s Cell–level handshake input buffer of 4 ATM cells depth
  - Clock monitoring of the UTOPIA clock
  - Generation of the HEC byte
  - Mapping of ATM cells into STS–3c/STM–1 payload capacity
  - Generation of POH:
    Generation of J1, B3, C2, G12, H4 bytes
    F2, Z1, Z3, Z5 bytes are programmable via registers
  - Building of TOH /SOH (SONET/ITU–T) and addition of payload pointer:
    Generation of A1, A2, B1, K2, Z2#1, Z2#3 bytes
    F1, K1, Z1, Z2#2 bytes are programmable via registers
    D1, D2, D3 bytes, programmable
    D4 through D12 bytes programmable
  - Generation of AU–4 pointer with positive or negative justification
  - Frame Scrambling (except start pattern)
  - Output of serial, differential data stream with 155.52 Mbit/s and Low–Voltage Differential Signal (LVDS) levels according to IEEE Standard 1596.3 [LVDS]
- Receive Functions
  - Serial, differential data input with 155.52 Mbit/s and LVDS levels
  - Synchronization to frame start pattern according to ITU–T Recommendation [G.738]
  - Descrambling of Frames
  - AU–4 pointer evaluation
  - ATM payload extraction
  - HEC synchronization

Type	Ordering Code	Package
PXB 4240	Q67101-H6593	P-MQFP-160-2

- ATM cell payload descrambling
- HEC evaluation: correction or detection and mode switchover according to ITU–T Recommendation [I.432].
- Counting of cell header corrections, discarded cells due to errors, discarded unassigned/idle cells and cells output to the UTOPIA interface
- Removal of unassigned/idle cells
- Output buffer size of 4 ATM cells

• Control Functions
- 16–bit Microprocessor Interface for chip control and line management
- Selectable 16–bit or 8–bit bus width
- Line status and alarm monitoring with built–in one–second timer
- Latched error status bits for alarm and error monitoring with low software load
- Automatic laser shutdown support

• General
- Data path loops built–in
- JTAG boundary scan [JTAG]
- 0.5 micron low power CMOS process
- Single 3.3 V supply
- Low power consumption, less than 0.7 W
- 160–pin P–MQFP–160–2 package

1.2 Logic Symbol

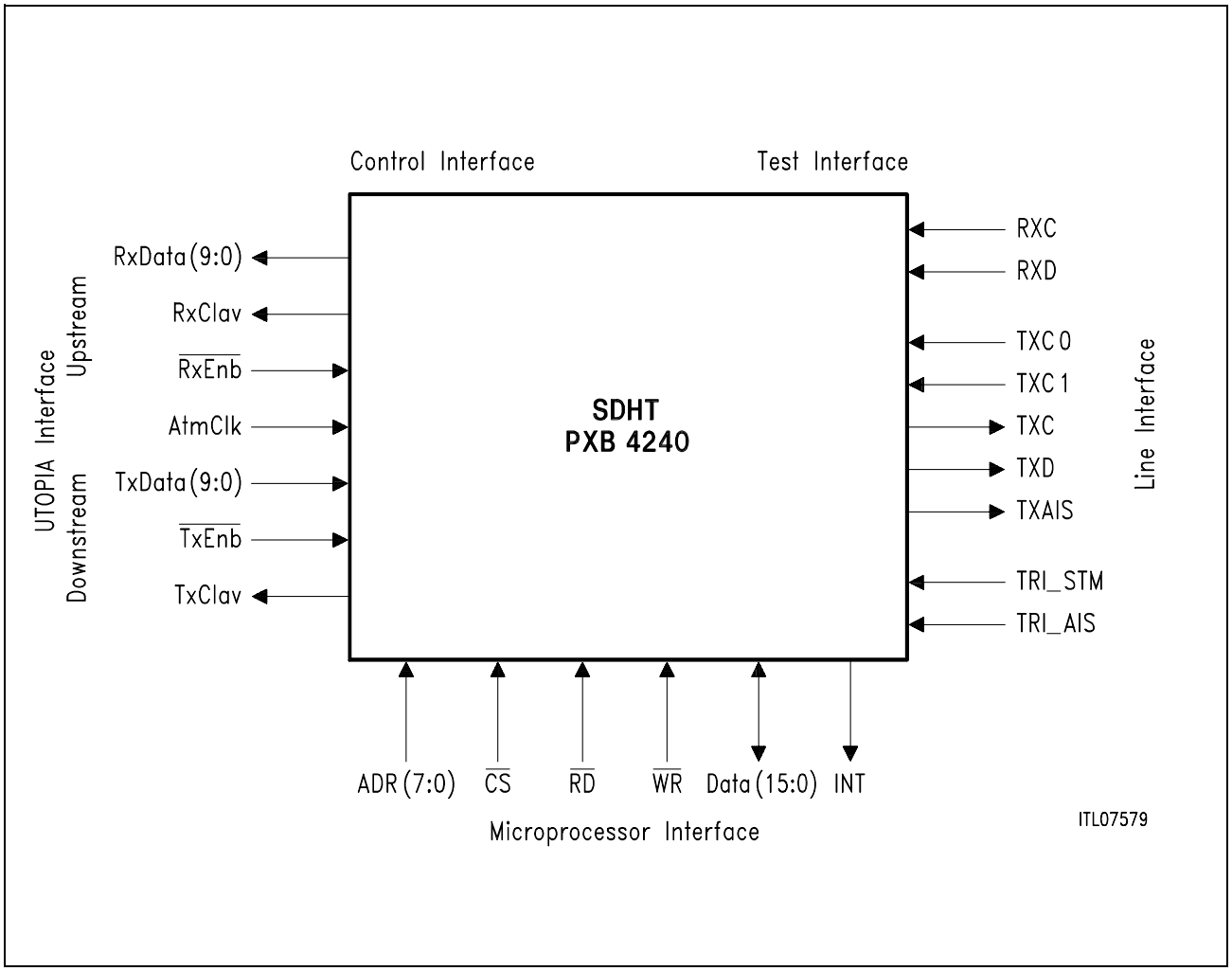


Figure 1
SDHT Logic Symbol

1.3 Pin Configuration

(top view)

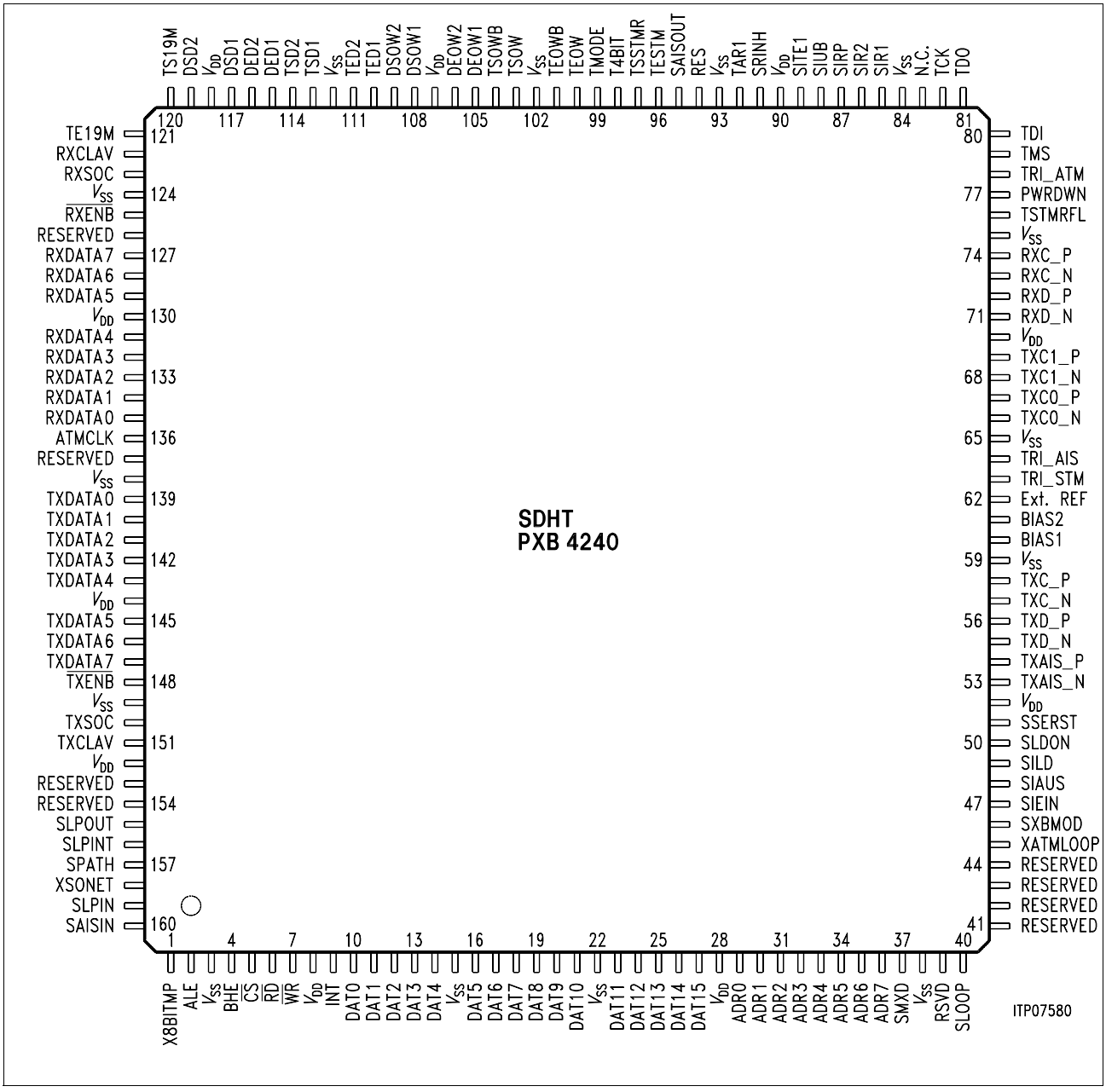


Figure 2
SDHT Pin Configuration

1.4 Pin Definitions and Functions

- Symbols with an * attached indicate active low signals
- Pins with a 1) attached are connected with an internal pull up resistor
- Pins with a 2) attached are connected with an internal pull down resistor

Table 1
Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
Microprocessor Bus Interface			
1 1)	X8BITMP*	I	**Bus Width Select** When low; an 8–bit data bus configuration is selected (default). When high, a 16–bit data bus configuration is selected.
2 2)	ALE	I	**Address Latch Enable** Falling edge indicates a valid address on the Address bus.
4 2)	BHE*	I	**Bus High Enable** in 16-bit mode indicates together with ADR(0) which bus portion to write to a register. See section 3.2.1.
5 1)	CS*	I	**Chip Select** A low signal selects the SDHT for read/write operations
6 1)	RD*	I	**Read** A low signal indicates a read operation. When the SDHT is selected via CS, the RD low signal enables the bus drivers to output data from an internal register addressed via ADR<7–0>.
7 1)	WR*	I	**Write** A low signal indicates a write operation. When the SDHT is selected via CS, the WR low signal loads an internal register selected via ADR<7–0> with the data available on the DAT<15–0> bus.

Table 1
Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
9	INT*	O	**Interrupt Request** INT serves as general interrupt request for the Interrupt Status Register. INT is active low. This is a wired AND output. An external pull–up resistor is required.
27–23 , 21–16 , 14–10	DAT(15)–(11), DAT(10)–(5), DAT(4)–(0)	I/O	**Microprocessor Data Bus** When X8BITMP* is high, a 16–bit wide data bus is used. When X8BITMP* is low, an 8–bit wide data bus (DAT 7-0) is used. When SMXD is high, DAT 7-0 will also carry the address
36–29 [2]	ADR(7)–(0)	I	**Microprocessor Address Bus** When SMXD is low, this is a separate address bus. When SMXD is high, these pins are not used.
37 [1]	SMXD	I	**Bus Mode Select** When low, a demultiplexed configuration is selected. When high, a multiplexed address and data bus configuration is selected.
39	Rsvd		**Reserved**
UTOPIA Interface			
41–44	Rsvd		**Reserved**
122	RxClav	O	**UTOPIA Receive Cell Available** When high, indicates availability of a complete cell in the FIFO.
123	RxSOC	O	**UTOPIA Receive Start–of–Cell** This line is set high by the SDHT during output of the first byte of an ATM cell.
125 [2]	RxEnb*	I	**UTOPIA Receive Enable** This line is driven by the ATM Layer device to enable and select the SDHT for cell transfer via the receive interface. When low, valid data and the SOC will be sampled.

Table 1
Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
126	Rsvd		**Reserved**
127–129, 131–135	RxData 7–5, RxData 4–0	O	**UTOPIA Receive Data** Receive Data Bit 7–0; e.g. data demapped from an STM–1 frame.
136 [2)]	AtmClk	I	**UTOPIA Clock** Delivered from the ATM layer, drives both Receive and Transmit portions of the UTOPIA Interface in the SDHT.
137	Rsvd		**Reserved**
147–145[2)], 143–139[2)]	TxData 7–5, TxData 4–0	I	**UTOPIA Transmit Data Bus** Transmit Data Bit 7–0; e.g., data to be mapped into an STM–1 frame.
148 [2)]	TxEnb*	I	**UTOPIA Transmit Enable** This line is driven by the ATM Layer device to enable and select the SDHT for cell transfer via the transmit interface
150 [2)]	TxSOC	I	**UTOPIA Transmit Start–of–Cell** This line is set high by the ATM Layer device during the transmission of the first byte of an ATM cell.
151	TxClav	O	**Transmit Cell Available** Indicates ability to accept one more ATM cell into the SDHT. This signal goes low 4 clock cycles before the FIFO is full if the OCTLVL bit is 1. It goes low 1 clock cycle before the FIFO is full if the OCTLVL bit is 0.
120	TS19M	O	**Transmit reference clock** only for VC-4 mode
121	TE19M	O	**Receive clock** only for VC-4 mode

Line Interface

Table 1
Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
53	TxAIS_N	O	**Serial P–AIS Output–Negative**
54	TxAIS_P	O	**Serial P–AIS Output–Positive**
55	TxD_N	O	**Serial Data–Negative** Output of Tx part
56	TxD_P	O	**Serial Data–Positive** Output of Tx part
57	TXC_N	O	**Reference Clock–Negative** Output of Tx part
58	TXC_P	O	**Reference Clock–Positive** Output of Tx part, TxD valid at rising edge
63 [2)]	TRI_STM	I	**Tristate Line Interface**
64 [2)]	TRI_AIS	I	**Tristate AIS signals**
66	TxC0_N	I	**Trigger Clock–Negative** Input to Tx part
67	TxC0_P	I	**Trigger Clock–Negative** Input to Tx part
68	TXC1_N	I	**Local Clock–Negative** Input to Tx part
69	TXC1_P	I	**Local Clock–Positive** Input to Tx part
71	RxD_N	I	**Serial Data Input–Negative** Input to Rx part
72	RxD_P	I	**Serial Data Input–Positive** Input to Rx part
73	RxC_N	I	**Master Clock–Negative** Input to Rx part
74	RxC_P	I	**Master Clock–Positive** Input to Rx part. RxD sampled at rising edge
SDHT Chip Control			
40	SLOOP*	O	**Switched to External Loop**

Table 1
Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
45 [2]	XATMLOOP	I	**Switch to ATM Loop** When high closes a loop at the Payload Interface; selection of section or path termination mode is determined by pin SPATH (rather than mode bit SVCEN).
46 [2]	SXBMOD	I	**Switch Payload Interface to VC-4 Mode** When low at reset, configures the payload interface to UTOPIA protocol. When high at reset, configures payload interface to special protocol required for VC-4 mode
47 [2]	SIEIN	I	**LOS Interrupt Input** Indicates loss of signal.
48 [2]	SIAUS	I	**Transmission Failure Interrupt** Indicates laser power is too low or modulation current is too high.
49 [2]	SILD	I	**Laser Shut Down Interrupt Input** Indicates automatic laser shutdown was requested.
50	SLDON	O	**Switch Laser On** When high, indicates to opt. transmitter to switch on the laser.
51	SSERST*	O	**Switch to Local Clock Oscillator** When low, indicates to external device to switch to Local Clock Oscillator.
76 [2]	TSTMRFL	I	**Test Pin** Do not connect
77	PWRDWN	I	**Power Down Status Input** If high, puts SDHT chip core into lower power mode. This mode is not active at the moment. Therefore do not connect this pin.
78 [1]	TRI_ATM	I	**Tristate Payload Interface**
85 [1]	SIR1*	I	**Non–dedicated Interrupt input 1** Available for external interrupt assignment.

Table 1
Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
86 [2]	SIR2	I	**Non–dedicated Interrupt input 2** Available for external interrupt assignment.
87 [1]	SIRP*	I	**Redundant Power Interrupt Input** Indicates switch to battery power.
88 [1]	SIUB*	I	**Supply Voltage Interrupt input** Indicates supply voltage warning.
89 [1]	SITE1*	I	**Temperature Interrupt Input** Indicates temperature warning.
91 [1]	SRINH*	I	**Force R–INH transmission**
92 [2]	TAR1*	I	**Local Clock Switching Condition** Include SISTD (Rx clock failure), LOF (Loss of Frame), and SXCB2 in generation of local clock switching condition
94 [2]	RES	I	**Reset** Global chip reset, active high
95	SAISOUT*	O	**STM–1 Signal Failure**
155	SLPOUT	O	**Loopback Command Indication** Reflects the state of bit 7 of the received Z2#1 overhead byte.
156 [2]	SLPINT*	I	**Set LPINT** Determines reset state of bit LPINT. SLPINT is active low with internal pull-down resistor.
157 [1]	SPATH	I	**Set as Path Termination** On reset, configure SDHT as path termination: ATM mode when high at reset, VC-4 mode when low at reset (see mode bits SVCEN and SATSCR)
158 [1]	XSONET*	I	**Switch to SONET Mode** On reset, set up SDHT in STS–3c mode: STS-3c when low at reset, STM-1 when high at reset
159 [2]	SLPIN	I	**Force Section Loopback** When high, SDHT turns on the internal section loop at its Line Interface

Table 1
Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
160 [1)]	SAISIN*	I	**Force P–AIS Transmission**
Low-Rate Serial Interface			
100	TEOW	O	**64 kHz Receiver Clock** E1 & E2 receiver bit clock 64 kHz; data are valid at the falling edge
101	TEOWB	O	**8 kHZ Receiver Clock** E1 & E2 receiver byte clock 8 kHz; bytes start at the rising edge
103	TSOW	O	**64kHz Transmitter Clock** E1 & E2 transmitter bit clock 64 kHz; data are latched at the falling edge
104	TSOWB	O	**8 kHz Transmitter Clock** E1 & E2 transmitter byte clock 8 kHz; bytes start at the rising edge
105	DEOW1	O	**Serial E1 data output** Received E1 overhead byte
106	DEOW2	O	**Serial E2 data output** Received E2 overhead byte
108 [2)]	DSOW1	I	**Serial E1 data input** Transmitter E1 overhead byte
109 [2)]	DSOW2	I	**Serial E2 data input** Transmitter E2 overhead byte
110	TED1	O	**192 kHz Receiver Clock** D1–D3 receiver bit clock; data are valid at falling edge
111	TED2	O	**576 kHz Receiver Clock** D4–D12 receiver bit clock; data are valid at falling edge
113	TSD1	O	**192 kHz Transmitter Clock** D1–D3 transmitter bit clock; data are latched at falling edge

Table 1
Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
114	TSD2	O	**576 kHz Transmitter Clock** D4–D12 transmitter bit clock; data are latched at falling edge
115	DED1	O	**Serial D data output** Receiver D1–D3 overhead bytes
116	DED2	O	**Serial D data output** Receiver D4–D12 overhead bytes
117 [2)]	DSD1	I	**Serial D data input** Transmitter D1–D3 overhead bytes.
119 [2)]	DSD2	I	**Serial D data input** Transmitter D4–D12 overhead bytes
JTAG Boundary Scan			
79 [1)]	TMS	I	**Test Mode Select** JTAG Boundary Scan command input
80 [1)]	TDI	I	**Test Data Input** Data sampled with rising clock edge
81	TDO	O	**Test Data Output** Data change with falling clock edge
82 [1)]	TCK	I	**Test Clock** JTAG Boundary Scan test clock input
Miscellaneous			
96 [2)]	TESTM	I	**Reserved (test pin)** do not connect
97 [2)]	TSSTMR	I	**Reserved (test pin)** do not connect
98 [2)]	T4BIT	I	**Reserved (test pin)** do not connect
99 [2)]	TMODE	I	**Reserved (test pin)** do not connect
153 [2)]	Rsvd		**Reserved**

Table 1
Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
154	Rsvd		**Reserved**
Power			
3, 15, 22, 38, 59, 65,75, 84, 93, 102,112, 124,138, 149	VSS	I	**Power Ground**
8, 28, 52, 70, 90, 107,118, 130,144, 152	VDD	I	**Positive Power Supply**
60	OBIAS		**Input Bias** To be connected via 10 kΩ resistor to ground.
61	IBIAS		**Output Bias** To be connected via 10 kΩ resistor to ground.
62	ext. Ref		**External Reference** Connect to 1.2 V to adjust LVDS common mode voltage
83	NC		**No Connect**

1.5 System Integration

The Siemens ATM chip set includes five chips which can be used in a variety of Adapter and Switch applications.

Table 2 ATM Devices Available from Siemens

ASM	ATM Switching Matrix, PXB 4310
ASP-up	ATM Switch Preprocessor (Upstream), PXB 43201
ASP-down	ATM Switch Preprocessor (Downstream), PXB43202
SARE	Segmentation and Reassembly Element, PXB 4110
SDHT	Synchronous Digital Hierarchy Transceiver, PXB 4240
IWE8	Interwoking Element for 8 T1/E1 lines, PXB 4220

For a passive ATM NIC Adapter Card for use in workstations or Personal Computers, a minimal number of chips is required. Without an on–board controller, control of the Adapter Card is done by the host processor of the PCI system. The SDHT delivers and receives ATM cells via the UTOPIA interface to/from the SARE chip (PXB 4110) which performs the ATM Layer functions as well as segmentation and reassembly. If more than 32 virtual connections are to be supported by the SARE chip, RAM is required as shown. The SDHT is controlled by the host microprocessor via the SARE using the Peripheral Control feature. A typical configuration is shown in Figure 3:

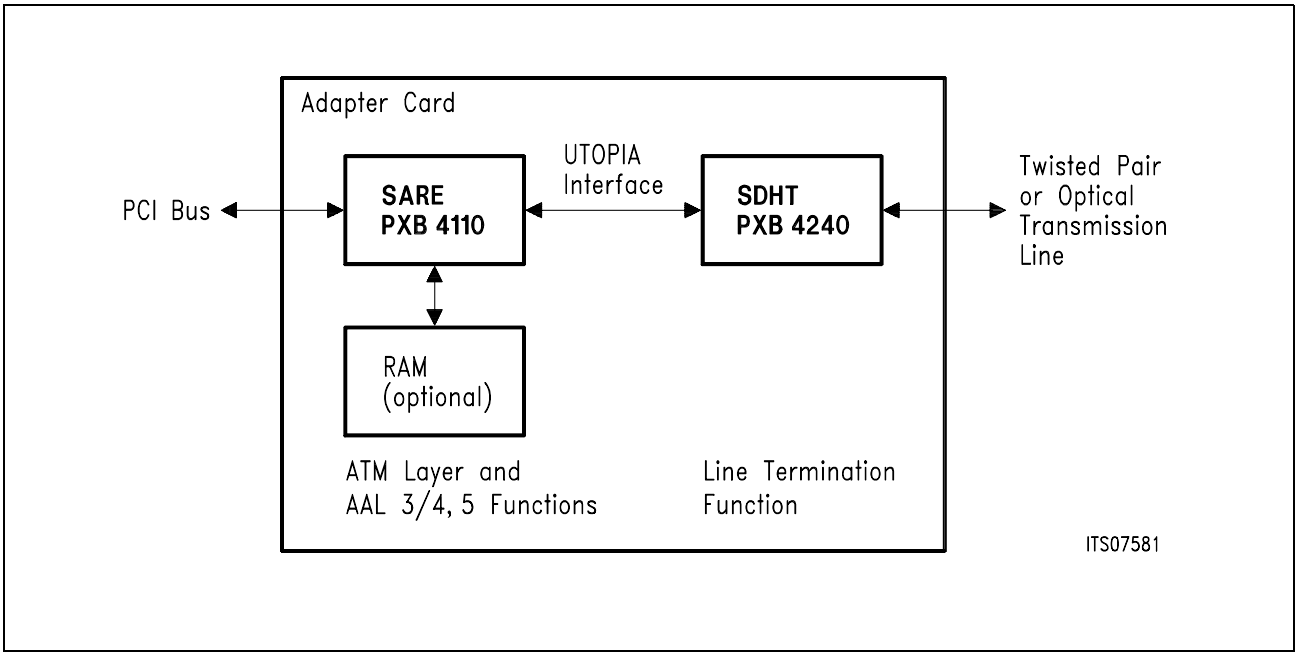


Figure 3
ATM Adapter Card Example

SDHT can also be used in a Line Card for an ATM Switch as shown in Figure 4. In this application, the SDHT is connected via the UTOPIA interface to the ASP chips (PXB43201/2).

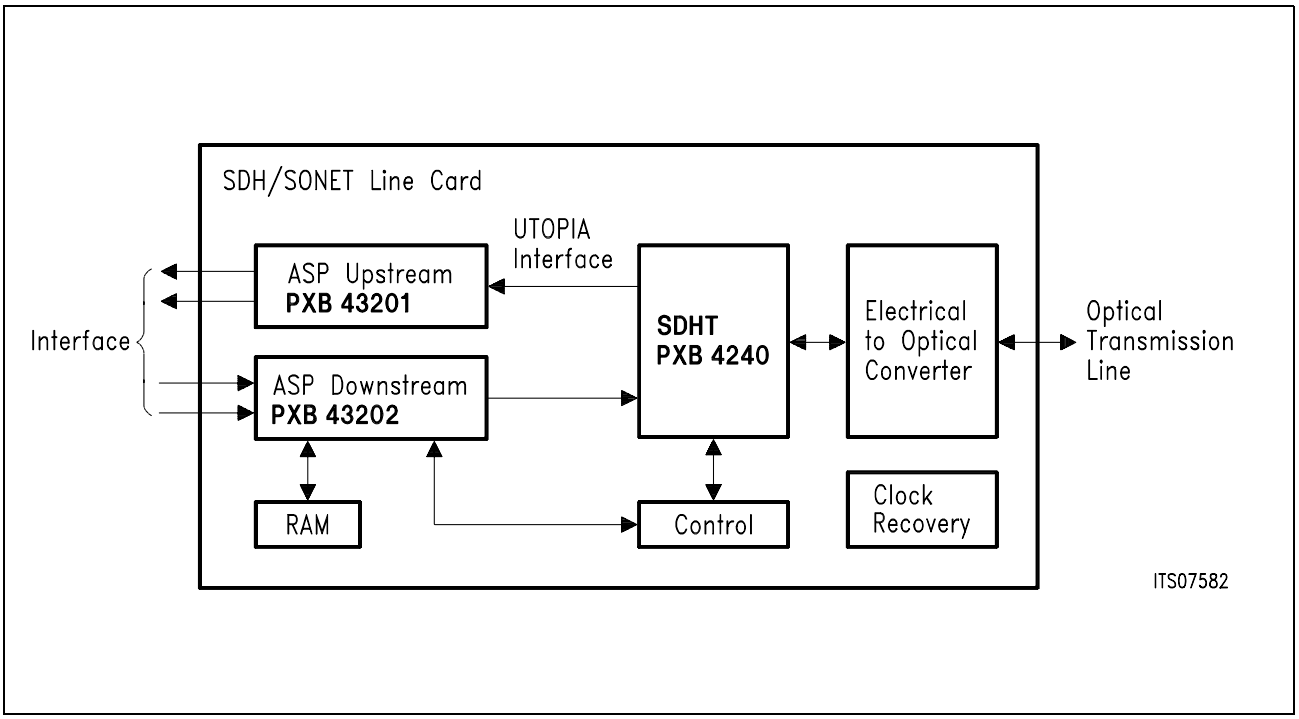


Figure 4
SDH/SONET Line Card Example

2 Functional Description

The SDHT performs five major functions: Cell–Rate Decoupling, HEC Header Generation and Verification, Cell Delineation, Transmission Frame Generation and Adaptation, and Receive Frame Recovery. See Figure 5. The combination of these functions achieves the task of framing data for transmission and receipt from an SDH or SONET–based Physical Layer medium. Specifically, the SDHT chip:

– assembles a stream of cells into a stream of transmission frames by mapping ATM cells into STM–1 or STS–3c frames, and
– de-assembles a stream of transmission frames into a stream of cells for proper reception by extracting ATM cells out of STM–1 or STS–3c frames.

These capabilities are defined in the Transmission Convergence (TC) Sublayer of the ATM Physical Layer specification [UNI-1].

The SDHT chip interfaces with the ATM Layer via a standard UTOPIA interface and interfaces with the Physical Medium Sublayer via its LVDS-level Line Interface. These interfaces, as well as microprocessor, Low Rate Serial and Control Interfaces, and JTAG boundary scan, are detailed in Chapter 3.

2.1 Functional Block Diagram

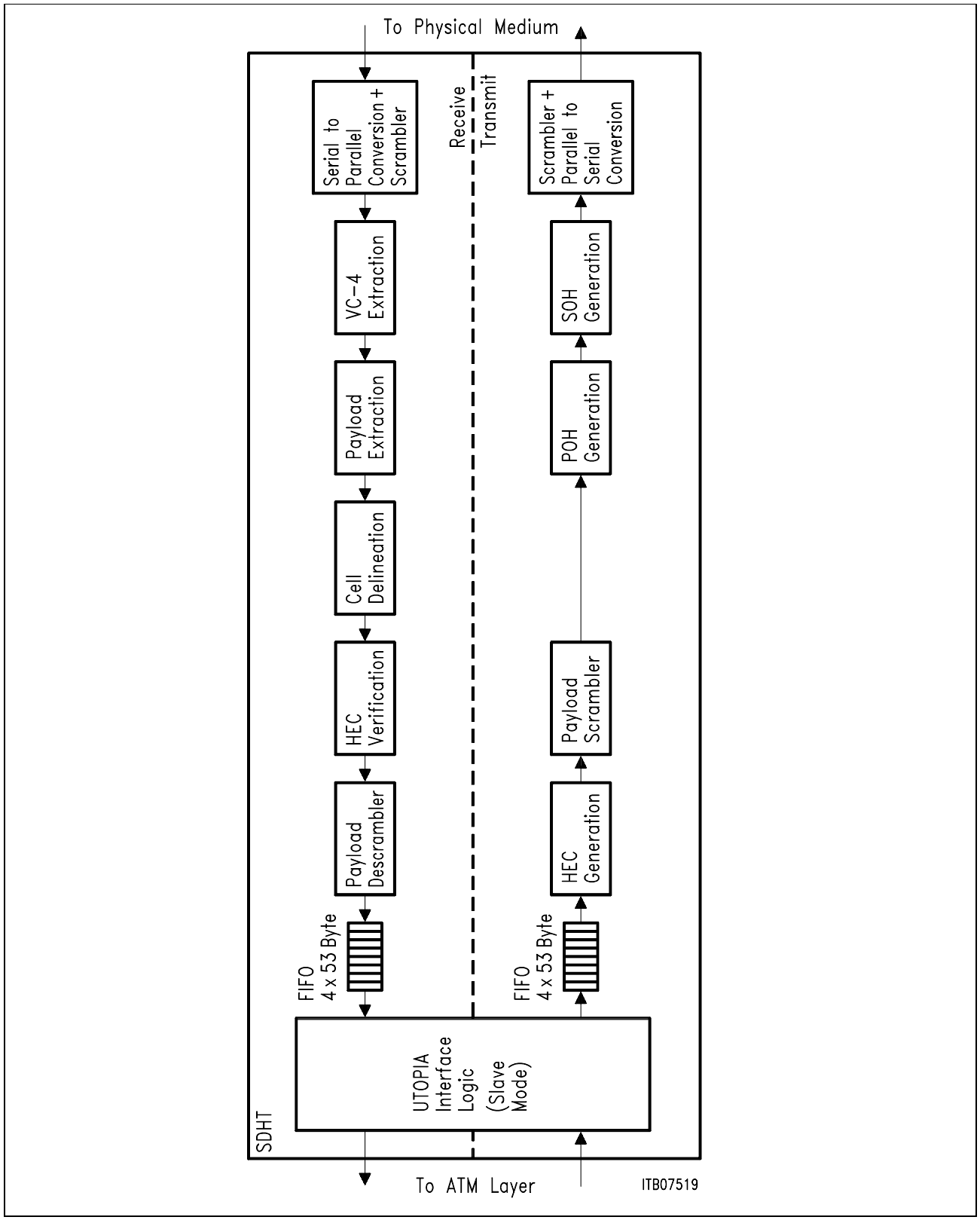


Figure 5
SDHT Block Diagram

2.2 Transmit Frame Generation and Adaptation

The SDHT chip generates and adapts frames for transmission on the physical medium in several steps. See Figure 5. In simple terms, the SDHT receives ATM cells from the ATM Layer via the UTOPIA or payload interface. Up to four ATM cells are temporarily stored in FIFOs before the SDHT performs cell-rate decoupling on them—adding Idle cells to fill a complete STM–1 (SDH) or STS–3c (SONET) Frame. The SDHT chip first generates the ATM cell header's Header Error Control (HEC) byte. The HEC byte is used by the receiving node to detect and correct single–bit errors in the ATM Cell Header. The SDHT scrambles everything except the cell headers, and generates and attaches the Path OverHead (POH) and Section OverHead (SOH) bytes to the complete frame. This completes the generation of a transmit frame. The frame is now passed through a Parallel to Serial converter to the physical transmission medium. The following section describes in more detail the special features and tasks associated with each step.

Note: For simplicity, only SDH names are used in this document. Specific differences between SDH and SONET names are indicated in Appendix 7.1. Unless mentioned specifically, all properties explained with SDH can be applied to, or programmed by a microprocessor for use with, SONET.

2.2.1 STM-1 Frame Structure

For construction of STM-1 signals, the user data (ATM cells) are mapped into a C–4 container. The ATM cells have a length of 53 bytes each, comprised of a 48–byte payload and 5–byte header. The ATM cell header includes a HEC byte which is calculated by the SDHT chip. This calculation may be disabled by clearing the bit ENHEC in register CONFIG 1H, which also disables the Rx header correction. A C–4 container is comprised of a block of 9 lines by 260 bytes. Since this is not an integer multiple of 53, the ATM cells "slide" within the C–4.

The C–4, containing the ATM cells, is combined with the Path OverHead (POH) byte to form a Virtual Container, VC–4. (See Figure 6.) Then the Section OverHead (SOH) and the Administrative Unit (AU–4) pointer are added to build an STM–1 frame. The STM–1 data rate is 155.52–Mbit/s, with a user data rate of 149.76–Mbit/s. An STM–1 frame consists of 2430 octets that are arranged as 9 lines with 270 bytes each. Figure 7 shows a complete STM–1 frame. Note also that Figure 6 depicts the mapping of ATM cells into STM–1 frames.

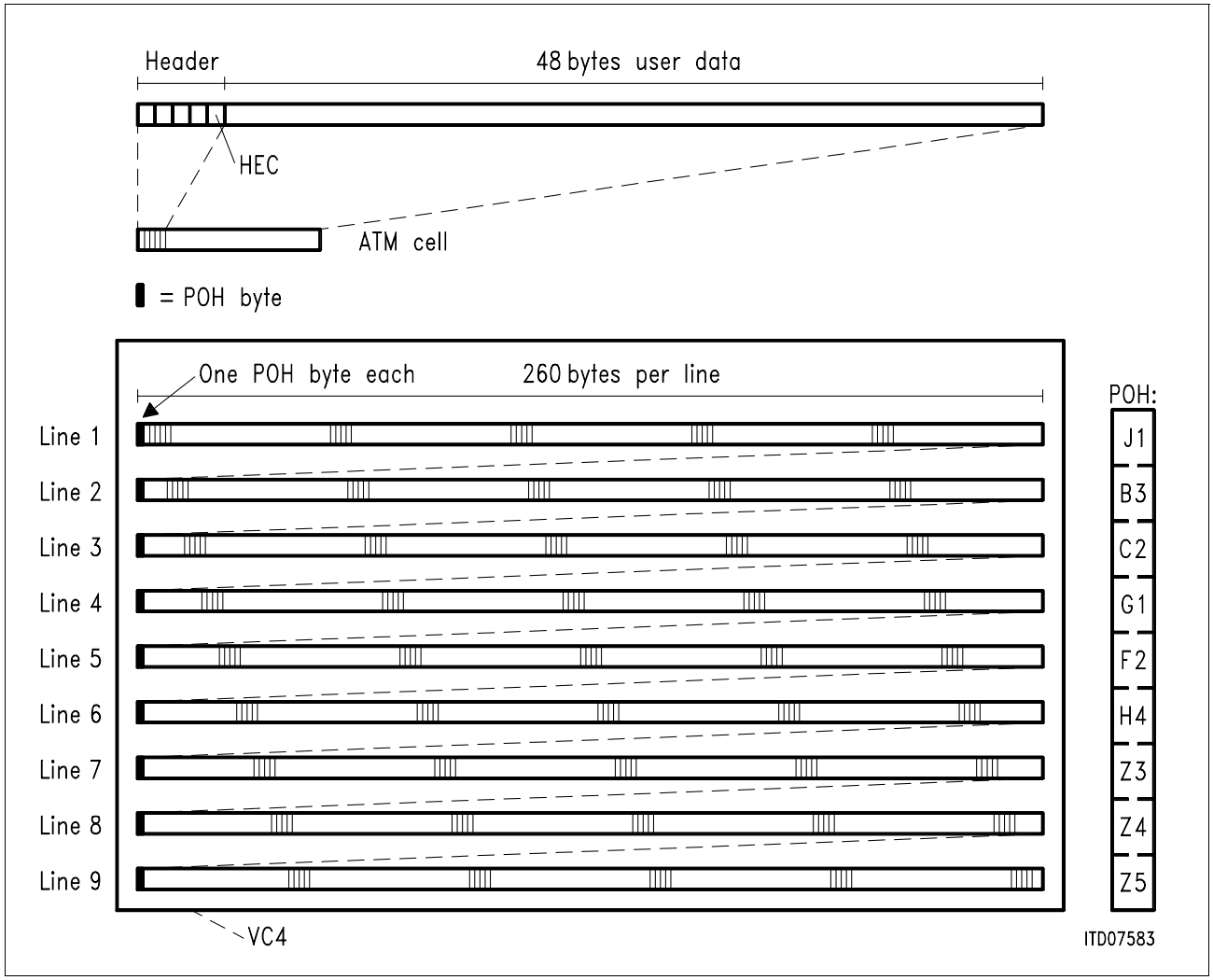


Figure 6
Virtual Container–4

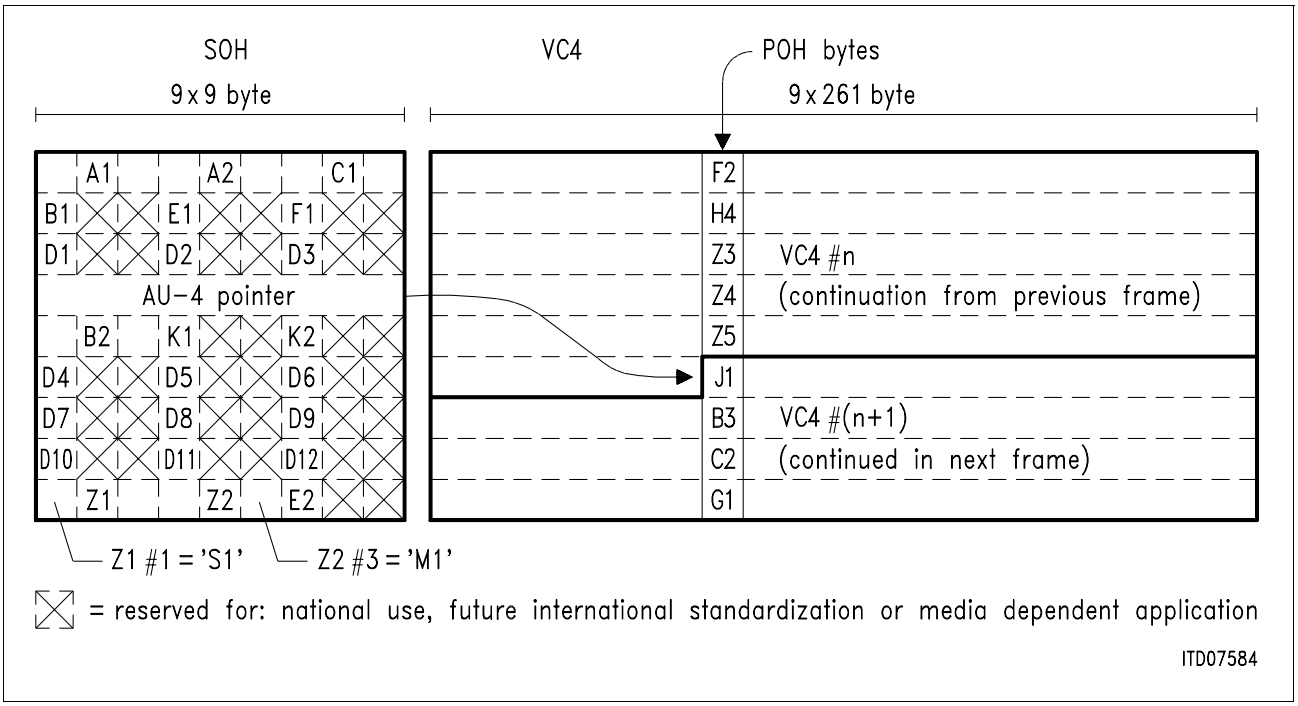


Figure 7
STM-1 Frame Structure

Note: The parameters which are different between STM–1 and STS–3c are all separately programmable by microprocessor or at start up. Two items concerning STS–3c are worth noting: The STS–3c "Path RDI" (former "Path Yellow") and the STM–1 "Path FERF" are coded similarly and both are supported, while the former STS–3c "Path FERF" (G1 bits 1–4: 1001) is not implemented. The STS–3c detection of LOS (sequence of zero bits) is not implemented in SDHT, but needs to be detected externally and fed into the SDHT by the pin SIEIN. The SDHT then performs all the OAM required for LOS, and also adds the release condition for LOS "2 valid frame patterns received".

2.2.2 Overhead Handling

SDH/SONET utilize two overheads: The SOH, which is reserved for signalling between section terminating equipment, and the POH, which is used for signalling between the transmission path terminations of the STM–1 line. The SOH consists of two parts. See Figure 8. The R–SOH for regenerator sections, which comprises the first three rows of the SOH; and the M–SOH for multiplexer sections, comprising lines 5 to 9. For SDH, the AU–4 pointer is placed at row four between R–SOH and M–SOH, but it does not belong to the SOH (together with the VC–4, it forms the AU–4). For SONET, the payload pointer belongs to the LOH (=M–SOH). For practical use, this theoretical difference is without consequence. The SDHT does not handle R–SOH and M–SOH differently, except for the generation of the parity bytes B1 and B2: The parity byte B1 (in the R–SOH) is built over the whole STM–1 frame after scrambling, whereas the triple parity byte B2 (in the

M–SOH) is built before scrambling, but does not include the R-SOH (but the pointer is included). Another parity byte (B3, in the POH) is used for path related bit error monitoring and thus is calculated over one VC–4.

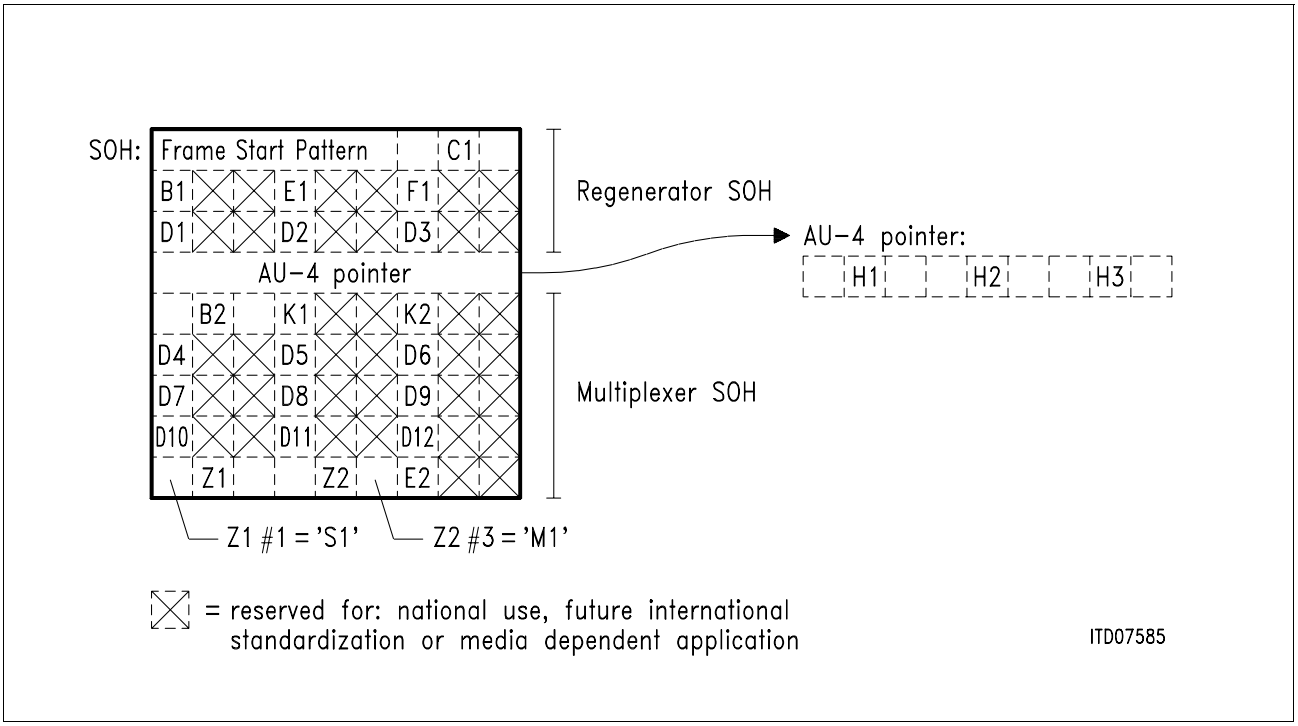


Figure 8
SOH and AU-4 Pointer

The handling of overhead bytes is described in Table 3 (SOH) and Table 4 (POH).

Table 3 Handling of SOH for SDH and TOH for SONET Bytes

SOH/ TOH Byte(s)	Transmitter Setting	Receiver Evaluation	Remark
A1, A2	F6, 28	Frame synchronization	
C1#1–#3	SDH:01, AA, AA SONET: 01, 02, 03	Selecting SDH/ SONET:config bit C1US	
B1	BIP–8 (over complete STM–1 frame after scrambling)	BER eval. for regenerator section	Affects status SXCB1
E1	serial input orderwire#1	serial output orderwire#1	Interface: see Chapter 3
F1	µP programmable	µP readable	

Table 3 Handling of SOH for SDH and TOH for SONET Bytes (cont'd)

SOH/ TOH Byte(s)	Transmitter Setting	Receiver Evaluation	Remark
D1–D3	µP programmable or serial input DCC1	µP readable or serial output DCC1	Select by mode bit SDC1; interface: see Chapter 3
H1,H2 #1	AU–4 pointer, P–AIS;ss bits µP programmable	AU–4 pointer, P–AIS ss bits µP programmable	
H1,H2 #2	CI (9B,FF); dd bits µP programmable	CI; dd bits µP programmable	
H1,H2 #3	CI (9B,FF); dd bits µP programmable	CI; dd bits µP programmable	Register Config 2L
B2	BIP–24 (over STM-1 frame without R SOH, before scrambling)	BER eval. for multiplexer section	Affects status SXCB2 and SSDB2
K1, K2	K1: µP programmable; K2: signalling MS–FERF: 'uuuu u110'not signalling MS–FERF: 'uuuu uuuu'with 'u': µP programmable	µP readable K1K2 is accepted only if been received 3 consecutive times equally. new K1K2 accepted => status SAPSCMD.K2 only: if one of the following patterns has been received for 3 (SONET: 5) times, the related state is set: xxxx x110: MS–FERF; xxxx x111: MS–AIS others: release MS–FERF and MS–AIS	The accepted K1K2 can be read only during 125 µs after the activation of SAPSCMD. Rx MS–FERF =>stat. SEFERFRx MS–AIS => stat. SESAIS selecting 3/ 5 times: Config bits LAISUS, LFERFUS
D4–D12	µP programmable or serial input DCC2	µP readable or serial output DCC2	Select by mode bit SDC2; interface: see Chapter 3

Table 3 Handling of SOH for SDH and TOH for SONET Bytes (cont'd)

SOH/ TOH Byte(s)	Transmitter Setting	Receiver Evaluation	Remark
Z1#1(S1)	µP programmable	µP readable; special algorithm for acceptance: 'abcd eeee':'a', 'b', group 'eeee': only accepted, after being unchanged for three consecutive times.'c', 'd': accepted at once.new 'eeee' accepted => status SSYSTCH	
Z1#2–#3	µP programmable	µP readable	
Z2#1	Mode 'LPINT must equal 1	µP readable; If mode 'LPINT'=0: all bits accepted at once.If mode 'LPINT'=1: 'i i i i i a l r', with:'i': bit is accepted immediately 'a', 'l': accepted after six times been unchanged, only while SDHT receives valid frames.'r': Like 'a', 'l'; but a zero is accepted already after 3 times.Meanings: As mentioned left.	The accepted bit 'l' is provided to the pin SLPOUT and to the status bit HWLOOPON; an accepted 'r' sets the status bit 'SERINH'.
Z2#2	µP programmable	µP readable	
Z2#3(M1)	'1bbb bbbb''bbbbbbb': number of detected B2 errors (S FEBE) for feed back	'1bbb bbbb''bbbbbbb': number of fed back B2 errors (S FEBE)	
E2	Serial input orderwire #2	Serial output orderwire #2	Interface: see Chapter 3

Table 4 Handling of POH Bytes

POH Byte	Transmitter Setting	Receiver Evaluation	Remark
J1	00		Only for path termination
B3	BIP–8 (over VC–4)	BER eval. for path	Only for path termination; affects status SXCB3.
C2	13(hex), except mode 'UEQ': 0	UEQ detection: three times C2=0;UEQ release: three times C2>0	Only for path termination; sending UEQ => no stuffing
G1	'bbbb f111''bbbb': number of detected B3 errors (P–FEBE) for feed back'f': P–FERF signalling	'bbbb f111''bbbb': number of fed back B3 errors (P–FEBE)'f': signals P–FERF; accepted after being received 3 (SONET: 10!) times.	Only for path termination; Rx P–FERF => status SERAI.selecting 3/ 10 times:Config bit PRAIUS
H4	µP programmable or ATM cell pointer: The latter indicates distance in bytes to the next ATM header (0...52)	µP readable	Only for path termination; selection by Config 1H bit ATMPTR
F2, Z3–5	µP programmable	µP readable	Only for path termination

2.2.3 AU-4 Pointer Functions

For SDH, the pointer actions are performed according to ITU–T G.709 and G.783 [G.70x, G.78x], annex B, whereas for SONET, BELLCORE TR–NWT–000253 [TR_253] is applicable. The items which differ between them are programmable via the Config2L register.

The AU–4 Pointer is 9-bytes in length; made up of H1, H2, and H3. See Figure 8. The AU–4 Pointer contains a pointer value, NDF codes, ss bits, and a Concatenation Indication (CI) which includes dd bits. See Figure 9.

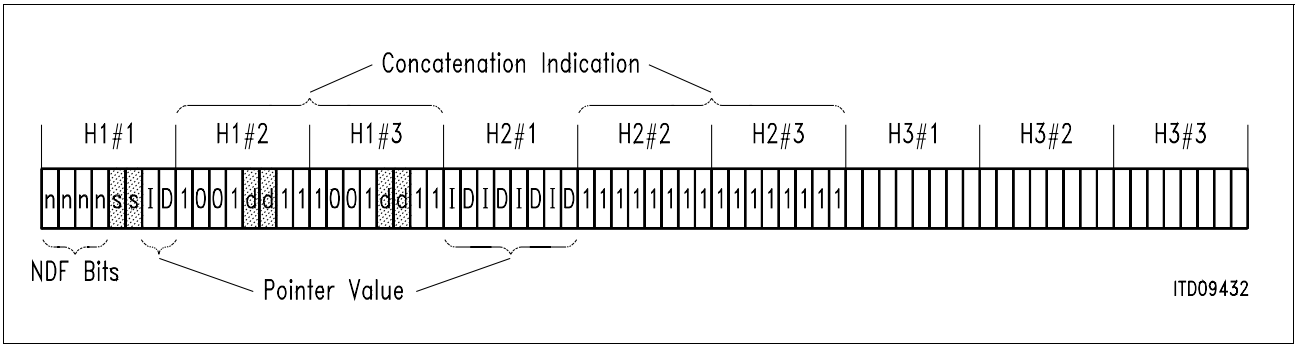


Figure 9 Structure of the AU-4 (or payload) Pointer

The Pointer value is contained in H1#1, bits 7 and 8, and H2#1. The pointer value contains the relative starting position of the user data within the virtual container from the last H3 byte (SOH bytes are not included in the account). The actual byte offset is three times the pointer value, where the pointer value can be from 0 to 782. Thus, the virtual container can start at an arbitrary three byte group and slide slowly within the frame.

The ss bits are contained in H1#1, bits 5 and 6. For SDH, the ss bits should be set to 10 (binary) and evaluated as a Loss of Pointer (LOP) error. The threshold for the various LOP conditions is programmable via the Config1L register. For SONET, the ss bits must be set to 00 (binary), but not evaluated.

The Concatenation Indication is contained in H1#2 and 3, and H2#2 and 3.The dd bits contained inside the CI can be programmed for both generation and evaluation via the Config1L register bit CIEN. Evaluation of the dd bits can be disabled even if the CI evaluation is enabled.

The NDF bits are contained in H1#1, bits 1-4. The NDF codes '0000', '0011', '1100', '1111', '1010', '0101' are interpreted as invalid NDF codes. This is enabled by the configuration bit ENINVNDF (default zero). If this bit is set, an invalid NDF code is treated as an invalid pointer (e.g. a pointer value above 782 or invalid ss bits).

For details of the pointer evaluation, with and without CI evaluation, see the state diagrams in Figures 10 and 11.

Note: General note: Norm_point counters, Inv_point counters, Inv_point_conc counters and NDF_enable counters are reset to 0 with all state transitions.

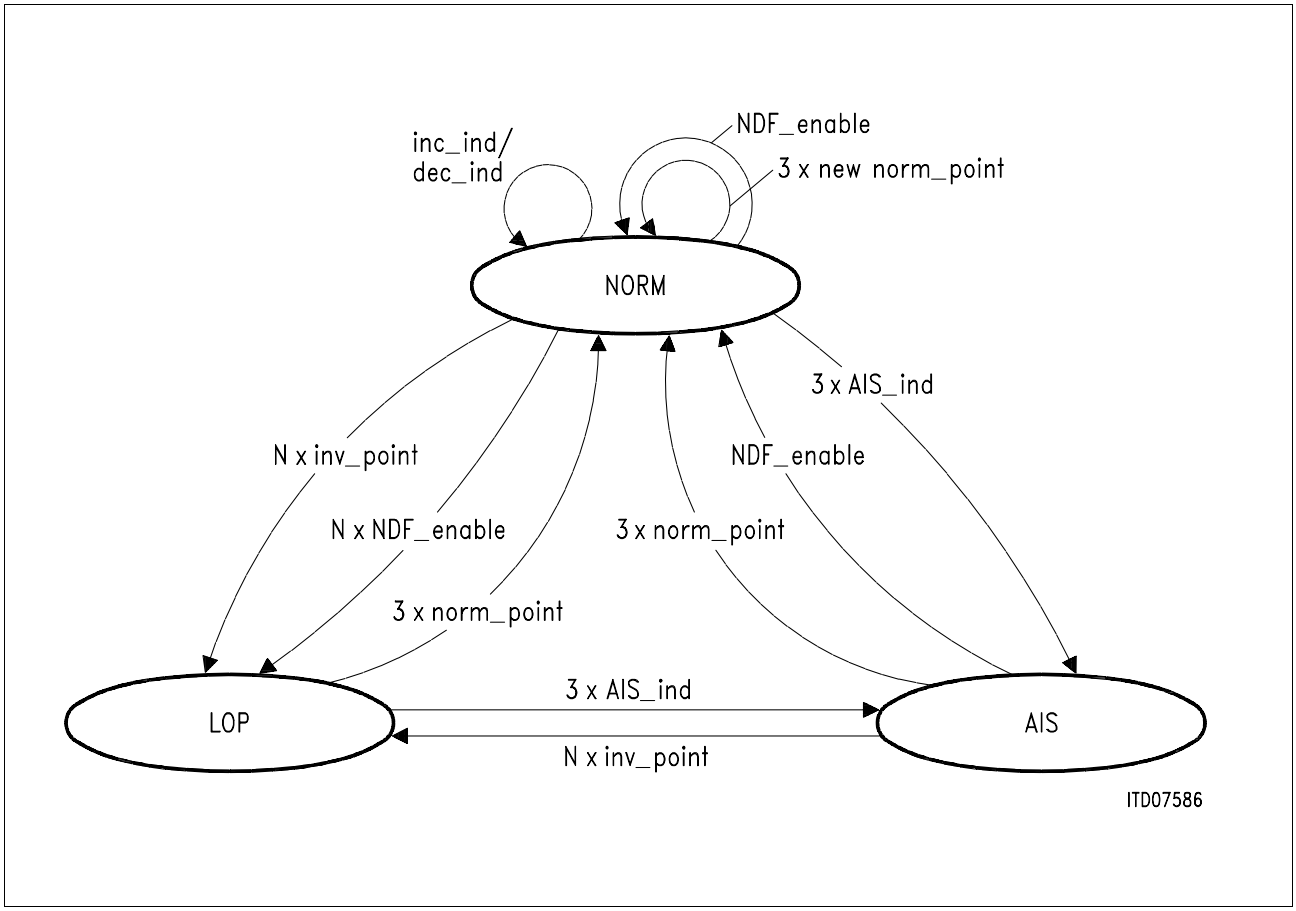


Figure 10
State Diagram of Pointer Evaluation, Normal

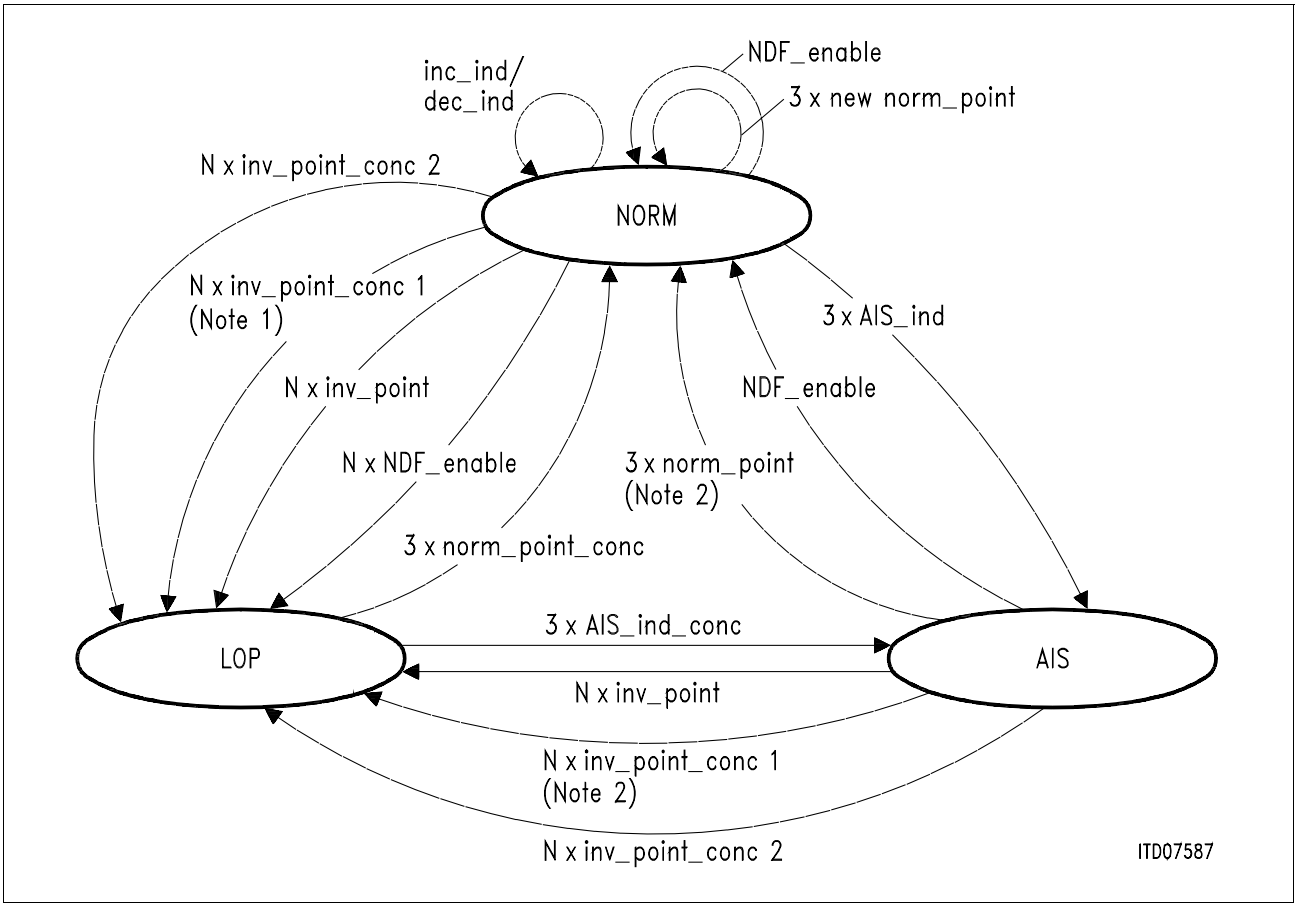


Figure 11
State Diagram of Pointer Evaluation, with Concatenation Indication

Note 1: This transition NORM -> LOP can occur along with other NORM -> NORM transitions in H1, H2 (Incr_ind, Decr_ind etc.). Priority is given to the transition to LOP state.

Note 2: This transition AIS -> NORM can occur along with AIS -> LOP transition (Reception of N inv_point_conc; along with norm_point in the last 3 of the N frames or NDF_enable in the Nth frame). Priority is given to the transition to Norm state.

Explanation of Names and Notes in Figures 10 and 11:

Evaluation Only for H1#1 and H2#1:

Norm_point	normal NDF + ´ss´ + offset value in range
NDF_enable	NDF enabled +´ss´ + offset value in range
AIS_ind	= (1111 1111; 1111 1111)
Incr_ind	Normal NDF + ´ss´ + majority of I bits inverted + no majority of D bits inverted + previous NDF_enable, incr_ind or decr_ind more than 3 times ago.

Decr_ind	Normal NDF + ´ss´ + majority of D bits inverted + no majority of I bits inverted + previous NDF_enable, incr_ind or decr_ind more than 3 times ago.
Inv_point	Any other than above + norm_point with offset value not equal to active offset.

Evaluation Only for H1#2 and H1#3, H2#2 and H2#3:

Conc_ind = (1001 dd11; 1001 dd11; 1111 1111; 1111 1111)

The dd bits are different for SONET/ SDH: see text above.

Inv_point_conc 1 (H1#2; H2#2) ≠ (1001 dd11; 1111 1111)

Inv_point_conc 2 (H1#3; H2#3) ≠ (1001 dd11; 1111 1111)

Evaluation for H1#1–3 or H2#1–3:

AIS_ind_conc	All ones in H1#1, H2#1, H1#2, H2#2, H1#3, H2#3
norm_point_conc	Norm_point + Conc_ind

If SDHT receives a pointer with all bits set to one for three consecutive times, it recognizes the Pointer Alarm Indicator Signal (P–AIS). When SDHT transmits P– AIS (activated by pin SAISIN=low or mode bit SAISMP=1), it sets all bits of H1, H2, H3 (each #1–#3), and the VC–4 to '1'. After returning to normal transmission, it sets NDF to force the receiving counterpart to accept the new pointer value immediately. P–AIS is transmitted as long as it is activated, even if the activation lasts for less than three frames.

2.2.4 Cell-Rate Decoupling

The SDHT chip has the capability to perform cell–rate decoupling while generating a transmit frame. It inserts, or pads, the frame payload with idle/unassigned cells in order to fill an STM–1 frame.

2.2.5 Stuffing

Before the data received from the UTOPIA or payload interface is mapped into the STM–1 frame, it is buffered in a 24-byte FIFO. The Stuffing decision is based upon the fullness of the FIFO. If there is an overflow or underflow in the FIFO, the Interrupt Status register SIST bit is set. This resets the FIFO, and any stuffing decisions not yet processed are cleared. If the SDHT is set to transmit UEQ (Unequipped), stuffing actions are suppressed. The positive and negative stuffing events during the recent second period can be read by µP.

2.2.6 Scrambling of ATM Cell Payloads

ATM cell payloads are scrambled before being transmitted, and descrambled after being received, by a $X^{43}+1$ self–synchronizing scrambler. During HUNT or PreSYNC state, the

ATM payloads are not descrambled. The ATM cell headers are neither scrambled nor do they change the internal scrambler state.

If no ATM data is present to be transmitted, this may be signalled by UEQ (unequipped). This has to be indicated to the SDHT by the µP by setting the mode bit SUEQEN to '1'. Then, the SDHT sets the C -byte (POH) to zero (the entire C–4 is set to zero, too). If the SDHT receives a zero C2 byte, it assumes UEQ, and thus suppresses the ATM sync alarm ('SSYATM').

2.3 Receive Frame Recovery

The SDHT chip receives frames and recovers ATM cells from the physical medium in several steps. The received frame first passes through a serial to parallel converter and any Idle cells are removed in the cell-rate decoupling process. The SDHT then extracts the payload information (SDH/SONET or VC–4) and proceeds to identify the individual cell boundaries (cell delineation). Any lost cells are also counted. Once the cell boundaries are known, the SDHT can then verify the HEC byte of the cell header. The SDHT chip first detects the existence of the HEC byte and then corrects any single–bit errors it encounters. HEC errors are counted. ATM cells, after unscrambling the payload, are presented to the FIFO of 4 cells depth and ultimately to the ATM Layer for flow control, muxing, etc. The following sections describe in more detail the special features and tasks associated with each step.

2.3.1 STM-1 Synchronization

The first 6 bytes (A1 and A2 SOH bytes) of each STM–1 frame are the frame start pattern. They contain hexadecimal values F6, F6, F6, 28, 28, and 28, which are used by the receiver to synchronize to the beginning of the frame. The receiver part of the SDHT only evaluates the bytes 2 to 5 of the frame start pattern (frame alignment pattern (FAP): F6, F6, 28, 28, hexadecimal values).

In order to keep the frame start pattern unique, the whole frame except the first 9 bytes is scrambled by a 2^7–1 Pseudo Noise (PN) pattern. The PN generator is reset at every frame start, and delivers a scrambling polynomial. Both the PN pattern and the scrambling polynomial are implemented according to ITU–T recommendation G.709.

The STM-1 synchronization procedure matches ITU–T Recommendation G.783. If a synchronization has not yet taken place (Out of Frame state = OOF), the data stream is compared bit by bit with the FAP. Once a match has been found, the SDHT is in the Pre SYNC state. If another FAP is detected exactly one frame period later, the SDHT is fully synchronized (SYNC state), otherwise it falls back into OOF. While in SYNC state, the SDHT compares the bytes 2 to 5 of each incoming frame with the FAP. If this comparison fails in five consecutive frames, the SDHT goes back to OOF and a new synchronization procedure starts.

For SDH, an OOF state immediately sets the Loss of Frame (LOF) state. For SONET, there is a delay of 3-ms from OOF to LOF (=24 frames). To accommodate the protocol

differences, the SDHT chip can be programmed using the Config1L Register bit LOFUS to be compatible with the desired protocol. For the realization of the 3-ms delay, no integration timer is used, i.e. whenever OOF goes inactive, the timer is reset, and a new OOF starts the timer from zero. Furthermore, OOF going inactive resets LOF immediately.
After frame synchronization has been established, SDH/SONET descrambling is performed and VC-4 containers are retrieved via the AU-4 pointer mechanism.

2.3.2 ATM Cell Synchronization

ATM cell synchronization is performed on the received C–4 payload according to ITU–T I.432 specifications.

If the configuration bit ATMPTR (see Table 3.9) is set to '1', the H4 byte of the POH is set to the distance from the H4 to the next cell start (in bytes, range 0–52; Table 3.1a), but it is not evaluated by the receiver. Otherwise, it may be accessed by the µP.

On the received C–4 payload, ATM cell synchronization according to ITU-T I.432 is performed. The algorithm is based on the structure of the cell header, which comprises four bytes ATM information and one CRC protection byte (the 'HEC', generator polynomial X^8+X^2+X+1, EXOR 55hex). If not synchronized at all (HUNT state), the SDHT watches the data stream byte by byte, until five continuous bytes result in a valid HEC. At this point, the SDHT assumes it has found a cell header and switches to PreSYNC state. Then, the cell stream is investigated every 53 bytes for a valid header. If the investigation finds an invalid header once during the next 6 assumed headers, the SDHT jumps back to the HUNT state. But if the SDHT finds an additional six consecutive valid headers at the proper distance (53 bytes), it goes into synchronization. It stays synchronized unless 7 consecutive invalid headers are found; then it switches back to the HUNT state. The ATM synchronization is also reset to HUNT state due to the same condition as for generation of the signal SAISOUT (except LOC, since LOC is the result of an ATM synchronization reset).

During HUNT and PreSYNC state, the ATM sync alarm SSYATM is set, and the ATM data stream at the UTOPIA interface is disabled. While the ATM cell stream is disabled, the number of cells is counted that could have been transmitted during that time. The counter value (maximum 2^{16}-1) for the recent second interval can be read by the microprocessor.

An additional counter is implemented for OCD events (OCD: Out of Cell Delineation defect). This counter is incremented every time, the OCD state is entered, i.e. ATM synchronization is lost. Counting is inhibited while the bit ATC in the mode register is set.

2.3.3 HEC Header Verification

On the received synchronized cell stream, single–bit error correction is performed on the cell header using the HEC algorithm. This may be disabled by clearing the bit ENHEC in register CONFIG 1H, which also disables the Tx HEC insertion. Cells with single–bit

errored headers are corrected only if the preceding cell did not experience a header error, otherwise they are discarded. Cells with multiple errored headers are discarded.

2.3.4 Cell-Rate Decoupling

Cell Rate Decoupling is performed implicitely by elimination of any idle/unassigned cells, as no idle or unassigned cells are transferred via UTOPIA.

2.4 Additional Functions

2.4.1 STM-1 Loop

An STM-1 loop can be closed in two ways: An external loop is indicated by the pin SLOOP: When this pin is low, it is an indication to a device outside the SDHT to loop back the STM -1 signal coming out of the SDHT to the SDHT' STM-1 input.

The internal loop may be programmed to be transparent (data sent out is identical to data looped back) or not transparent. For the non transparent loop, an extra P AIS signal is generated to be sent out of the STM-1 interface. This extra P AIS signal is a fixed bit pattern (even for the overheads), not programmable by the µP. The only alarm that can be transmitted by this extra P–AIS signal is S FERF in case of LOS.

Which loop should be closed is determined by the bit LOOPINT in the test mode register: If LOOPINT is set, the internal loop is chosen. What the SDHT outputs at the STM 1 side during an internal loop, is programmed via the bit LOOPAIS in the same register: If LOOPAIS is cleared, the loop will be transparent, otherwise P AIS is provided to the STM 1 side. Both bits LOOPINT and LOOPAIS only take effect, if the mode bit LPINT is high. Notice, that the mode bit LPINT affects also the generation and evaluation of the Z2#1 byte.

Whether a loop should be switched, is controlled by the input pin SLPIN and the mode bit SLOOP: If either of these two is activated, the loop is closed.

2.4.2 Path Trace Handling

Cyclic 16–byte sequence via the J1 byte with the most significant bit as synchronization bit ('1' in the first byte, '0' elsewhere). Two 16–byte memories hold the path traces received and to be transmitted, respectively.

The Tx RAM (registers J1s(0-15)) is programmed by the µP, and the contents are inserted into the J1 byte cyclically. Synchronization information is not inserted automatically. Zeroes are inserted into J1 until J1s(15) has been written the first time.

The Rx RAM (registers J1r(0-15)) is filled on demand: The µP sets the bit ACQPT in register test mode L to '1' (default is 0). Then the SDHT starts acquiring the path trace, beginning with a byte with the MSB = 1, followed by 15 bytes with the MSB = 0. During acquisition, every J1 byte with a MSB = 1 leads to a restart of the acquiring algorithm.

After a successful end of this acquiring algorithm, the bit PTACK in the interrupt status register 2L becomes set. Now, the acquired path trace can be read from the Rx RAM.

If ACQPT is reset to '0' before the acquiring algorithm is finished, the automatic restart is disabled. Thus, a random 16 byte J1 sequence will be acquired.

Before a next acquisition is started, both ACQPT and PTACK must be reset.

The internal RAM is for each Rx and Tx 16 bytes. The Tx RAM can be read and written by the µP, the Rx RAM is read-only for the µP.

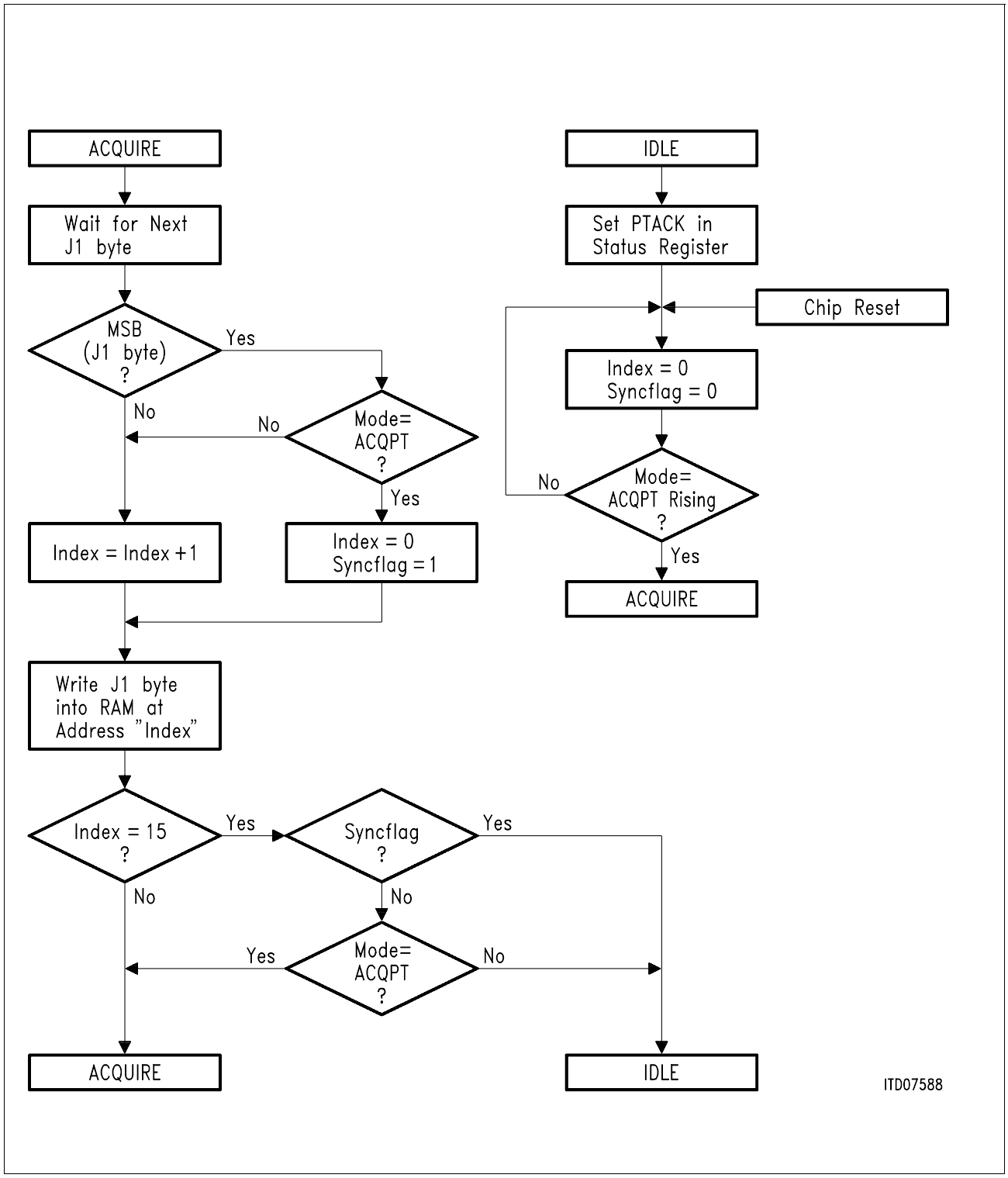


Figure 12
Flow of Path Trace Acquiring Algorithm

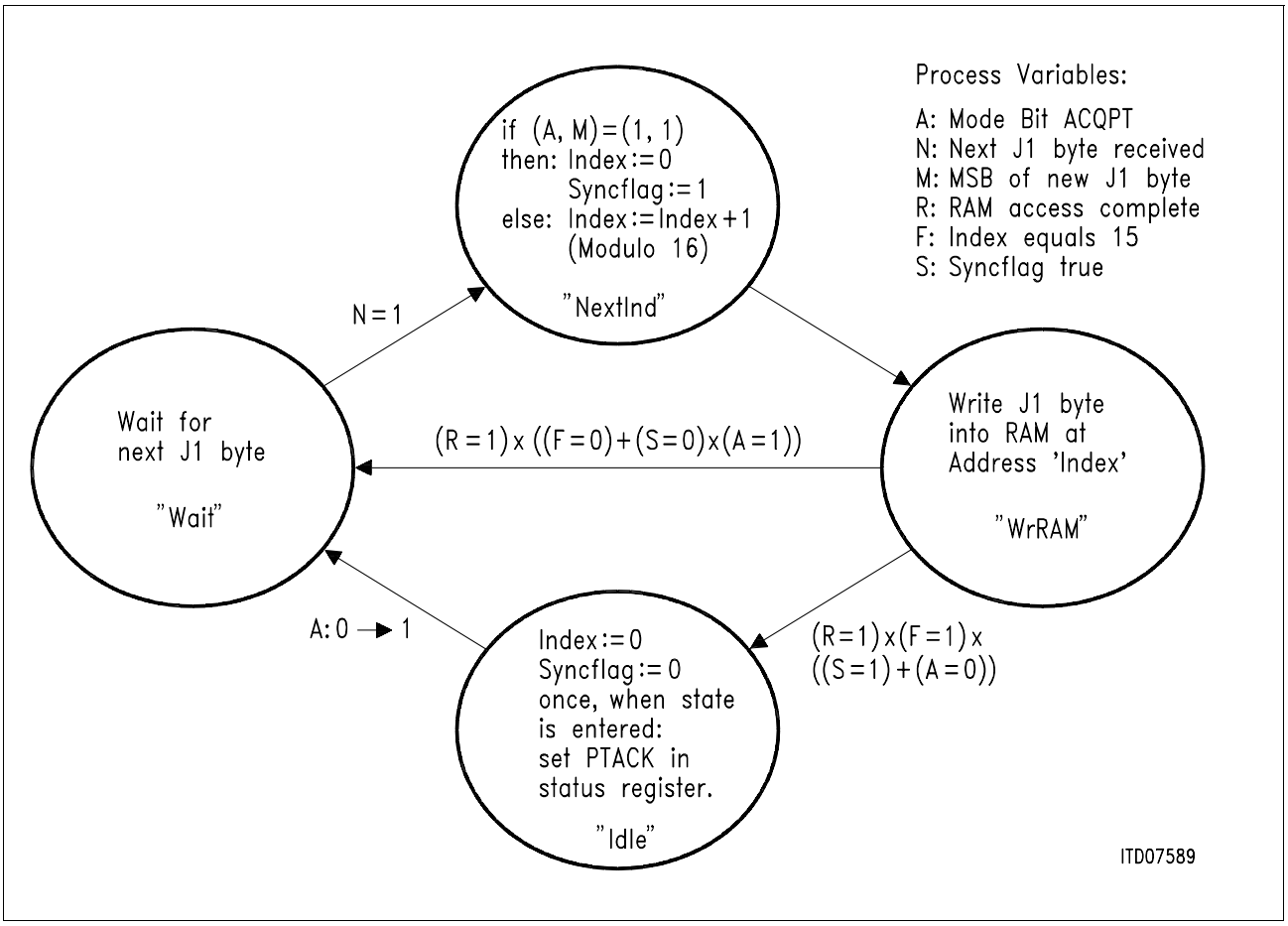


Figure 13
State Diagram of Path Trace Acquiring Algorithm

2.4.3 Detection of a Signal Label Mismatch

If the received C–2 byte (path termination only) is different from 13 hex (indication for ATM payload) or from 01 hex (indication for non specific payload), the bit SLM1 (Status Register 3L) is set. If this happens 5 times in a 50 ms window, the bit SLM5 (Status Register 3L) is set. SLM5 is reset again if the received C2 byte was correct at least 5 times in a 50 ms window. The state diagram is shown in Figure 14.

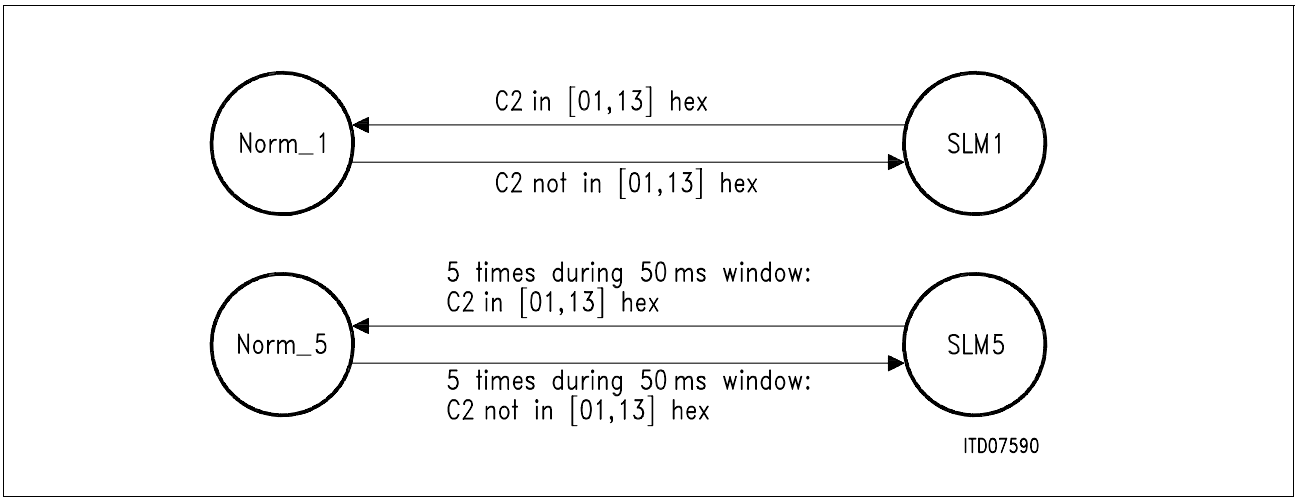


Figure 14 Signal Label Mismatch Detection

2.4.4 Section Termination Mode

Standard operation of the SDHT is in path termination mode. To use the SDHT in multiplexer section termination mode instead, the µP or SPATH pin must map VC–4 cells into STM–1 frames directly (rather than ATM cells into STM-1 frames). SPATH is evaluated only on an SDHT hardware reset, and the resulting default values of the Mode and Config registers may be modified by the µP afterwards.

If the SDHT is switched to section termination mode, all functions concerning ATM mapping/demapping and POH calculation/evaluation are stopped. The POH evaluation is not automatically reset when the SDHT is switched from path mode to section mode during operation. Thus, if the SDHT is switched to section mode during operation, already detected path related alarms like SSYATM or SERAI remain set. For the adaptation of the payload interface to the section termination mode, see Chapter 2.7.

2.4.5 Internal Timers

For statistical evaluations, there are two timers implemented: 1 second and 5 milliseconds. Both are provided with clock by the transmit part and are provided to the SDHT' receive part, too. After a reset, the first interval is 1.28 s and 8–ms, respectively.

The statistical evaluations gated by these timers for counters are as follows (see also Figure 18):

- 1 second:

  Counters of bit errors for B1, B2, B3

  Counters of lost ATM cells

  Counters of far end bit errors reported by P FEBE, S FEBE

  Counters for stuffing events

  UTOPIA cell counters

Latched status and latched release status register

- 5 ms:

Counters and detection circuit of excessive bit error rates based on B1, B2, B3

Rx UTOPIA frequency counter

Each time a one second interval is finished, and the µP readable registers are updated with the values acquired internally, the TIMER bit in the Status Register is set.

2.5 Initialization

The SDHT is reset by either activating the pin SERES (active high) or writing a '1' and subsequently a '0' to the bit SMRES in the Mode register. After the reset is deactivated, the SDHT awakes as follows:

If there was a HW reset (i.e. per pin), the mode and config registers are set to their default values as described in Chapter 4.

After start up, the laser is turned off. It has to be turned on by µP.

After a SW reset (i.e setting the mode bit SMRES and again resetting it), the mode and config registers contain their values written into during the reset phase. Bits to which nothing is written during the reset phase, keep their values from before the reset. The test mode registers in contrary are reset also during a SW reset.

Table 5 Reset Values for Programmable SDHT Registers

Register Name	Value after HW Reset	Value after SW Reset
Mode Registers	see Chapter 4.4 Tables 16 and 18	Value from before, may be changed by µP
Config Registers	see Chapter 4.5, Tables 21 and 22	Value from before, may be changed by µP
Test Mode Registers	AF 00 (hex)	
Mask registers	0	
SD threshold / SD control	see Chapter 4.6	
Excessive BER thresholds	FF hex.	
all other programmable registers	0	

2.6 Error Detection

Errors on chip are detected mostly during the data stream evaluation. Additionally, a few detectors have been added:

SIVCA, SISTA, SISTD: These status bits indicate a fault in the time frame counters; or just a missing clock. SITAKT indicates a missing clock at any clock input. SITAKT has a

gate time of 2,45 µs, SIVCA, SISTA and SISTD are gated with 607,5 µs. The SISTD may appear sporadically, when the SDHT has lost its STM–1 synchronization.

The test mode bits SSYATMT, SLOPT, SIXBT, SXCB2T, SXCB3T may be set to test their related error detectors. If a test is activated, the related bit in the test status register should be set afterwards. For the usage of the Test Mode Register, see the description in Chapter 4.4.

2.7 VC–4 Mode

The SDHT is switched to VC–4 mode (only multiplexer section termination) via the mode register (chapter 4.4) or optionally while the payload loop is closed. Then, the RxSoC (TxSoC) signal indicates the beginning of the VC–4, the J1 byte; the RxClav(TxClav, TxEnb) signal enables both, C-4 and POH, thus the complete VC-4 which is transported via RxData(TxData). The timing in VC-4 mode is the same as in ATM mode; however, a special interface protocol will be used instead of UTOPIA, requiring additional clocking TE19M(ATMClk, TS19M). In VC–4 mode, the payload interface will not be shut down due to any error conditions. More details on the VC-4 mode will be given in a seperate document in the future.

3 Interface Descriptions

The SDHT chip contains five interfaces: Payload/UTOPIA, Microprocessor, Line, Control, and JTAG Boundary Scan. A detailed description of each interface follows.

3.1 Payload/UTOPIA Interface

Payload data is expected at the payload interface, which can be configured for ATM cell exchange or for VC–4 exchange. For ATM cell exchange, the SDHT utilizes a standard UTOPIA Interface. SDHT maps the payload data into STM–1 or STS–3c frames.

The UTOPIA Interface (Universal Test and Operations Physical Interface for ATM) is an industry standard interface defined by The ATM Forum for the exchange of ATM cells between a Physical Layer device (PHY) and the ATM Layer (ATM).

The ATM Forum defined the basic UTOPIA Interface in the Level 1 document in March 1994 [UTOP_1]. The more complete Level 2 document [UTOP_2], which was published after the April 1995 meeting, contains not only functional enhancements but also clarifications of the Level 1 document. Both documents are required for a complete understanding of the interface.

The Level 1 UTOPIA standard has the following features:

– Up to 33–MHz operation (maximum data rate of 264 Mbit/s)
– Transmit and receive path operation (see Figure 15).
– Multi–PHY configuration capability
– 53–byte cell format
– 8–bit data bus option
– Serial or parallel microprocessor style management interface option

The SDHT contains a universal Level 1 and Level 2 compatible UTOPIA Interface module, providing an 8–bit data bus and up to 33 MHz operation. In addition, the SDHT UTOPIA Interface contains built–in FIFOs, multiple statistical counters, and can be programmed to handle various cell formats. The SDHT’s Microprocessor Interface is available for management functions. Single–port, cell level handshaking is supported.

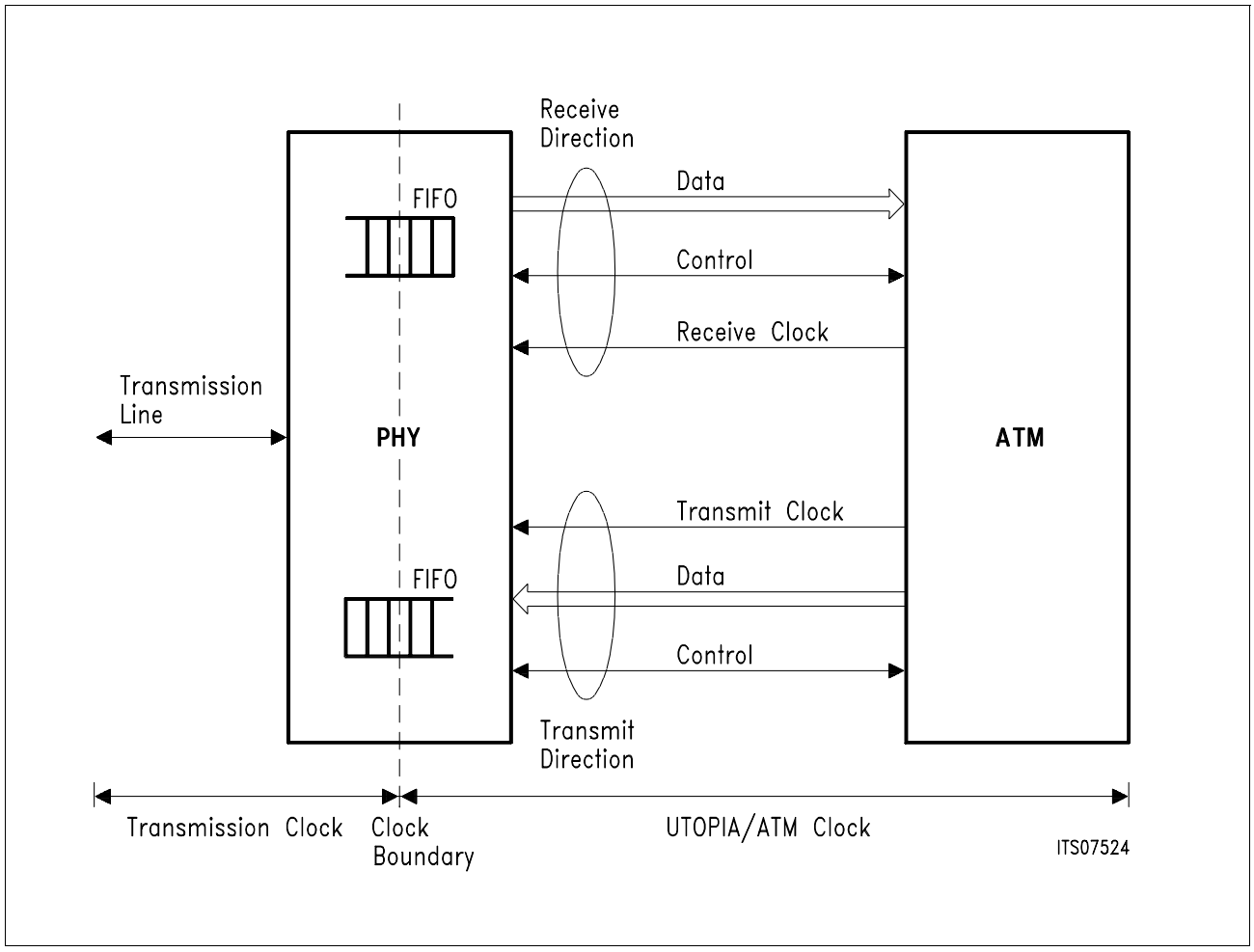


Figure 15
UTOPIA Reference Configuration

3.1.1 UTOPIA Hardware Functions

3.1.1.1 Clocking

As PHY chips are defined for various transmission speeds, The ATM Forum specified the use of an ATM Layer Master Clock, making it responsible for clocking both transmit and receive operations. Therefore, any PHY chip containing a UTOPIA Interface must manage clock adaptation between the transmission clock and the UTOPIA (=ATM) clock. This can be handled using elastic FIFO-buffers, for example.

Additionally, two reference timing signals, RxRef* and TxRef*, are defined in the UTOPIA documents. These signals are intended to provide 8 kHz receive and transmit reference clocks. The SDHT does not support the RxRef* and TxRef* signals specifically; however, it provides alternate 8 kHz receive and transmit clocks (TEOWB / TSOWB) for any required reference timing.

The UTOPIA Interface of the SDHT is operated with a clock of up to 33 MHz, which is used by both receive and transmit interfaces. This clock is delivered from the ATM Layer and input at the ATMCLK pin. It can be completely asynchronous to the system clock of the SDHT. Lower values for the UTOPIA clock can be chosen as long as the resulting data rate is high enough to transport the maximum data rate of the SDHT across the 8–bit interface.

The SDHT chip enables monitoring of the Clock at the UTOPIA Interface. Since the ATM clock at the UTOPIA interface is specified to be within the certain range, a go/nogo–supervision is not applicable. Thus, at the UTOPIA interface, a 16–bit counter is counting the UTOPIA clock cycles divided by 5 during a 5–ms period. Thus, the result is the clock frequency in kHz. This monitoring is implemented for the UTOPIA clock received at the ATMCLK pin. The result can be read from the register ATMRXCLK.

As with all UTOPIA implementations from Siemens, the maximum clock is increased from 25 MHz to at least 26 (in this case 33) MHz. Because of the universal clock distribution system for the Siemens ATM chip set, all clocks are delivered as multiples of 25.92 MHz. The universal clock system can be used only if all chips of a system are from the Siemens ATM chip set. In mixed environments with components from other manufacturers, only the standard frequencies can be used.

In order to reduce the clock speed a parallel data bus is used. The direction from PHY to ATM is defined as receive direction, the direction from ATM to PHY is defined as transmit direction. Handshake signals control the transfer of cells. These handshake signals are asymmetric, designating the ATM layer as master who controls the cell transfer.

3.1.1.2 FIFOs

Because the data transfer is cell oriented, FIFOs which can hold more than one cell are necessary to avoid lost data. For simple and robust FIFO control, a capacity of 4 ATM cells for both Rx and Tx FIFOs was chosen. An overflow of the Rx FIFO or Tx FIFO is signalled to the status bits OFUTORX and OFUTOTX, respectively. These FIFOs are used to manage cell level handshaking and clock adaptation between the system clock and UTOPIA clock.

For inserting and discarding of Physical Layer cells, two formats with different headers are supported: The ITU–T idle cell header (00 00 00 01 52) and the US unassigned cell (00 00 00 00 53). For both Rx and Tx, the bit IDLEUS (register config 1H) selects which is used. The discarding of Physical Layer cells is controlled by the bit ENIDLE in the register Config1H. The insertion of Physical Layer cells cannot be disabled by a mode bit, but is automatically suppressed as long as the Tx FIFO is not empty.

The master for data transfer is the ATM Layer side: Data is transferred only after the ATM side has set an enable signal.

The HEC Insertion for the Tx direction and the HEC correction are performed in the SDHT. This can be disabled by the mode bit ENHEC in the register Config1H (1: enabled; default).

3.1.1.3 Cell Counters

Five on–chip, one–second interval counters are available for gathering statistics related to received ATM cells. They include:

– RXHECCOR: cell header corrections
– RXHECDIS: discarding cells due to header errors
– RXIDLE: discarding of idle/unassigned cells
– RXINFO: cells output to the interface
– RXOCD: out of cell delineation

The counters for RXHECCOR, RXHECDIS, RXIDLE, and RXINFO are 20 bits and for RXOCD 16 bits wide. Counting operation is inhibited when the bit ATC in the Mode Register is set. The value of ATC-bit is 0 after reset.

3.1.1.4 Signal Descriptions

In addition to the signal descriptions outlined below, refer to the standards documents [UTOP_1] and [UTOP_2] for additional details.

AtmClk is the common operating clock of both receive and transmit part of the UTOPIA interface of the UTPT, delivered from ATM to PHY. Its maximum frequency is 33 MHz. All other signals of the interface are output and sampled with the rising edge of this clock.

The signals of the UTOPIA receive interface (from PHY to ATM) are:

RxData(7–0) is an 8–bit data bus. RxData(7) is the Most Significant Bit (MSB). As a special feature of the SDHT, RxData[7:0] is set to all zeros if the ATM requests a cell transfer by asserting RxEnb* even if there is no further cell available (RxClav has been deasserted).

RxSOC, Start–of–Cell, is a signal indicating the first octet of a cell. It is set to one when the first octet of a cell is put on the bus by the SDHT and is zero in all other cases, except when it is in high impedance state. It is set to low by the PHY if the ATM requests a cell by asserting RxEnb*, but there is no further cell available.

RxClav is the 'Cell available' signal from PHY to ATM. Its value is dependent on the transmission state of the SDHT: if the SDHT is just transmitting a cell via the UTOPIA receive interface, RxClav indicates the availability of the actually transmitted cell, i.e. it is asserted. If the SDHT is not transmitting it indicates the availability of a complete cell in the receive FIFO, ready to be transmitted. This behavior is independent of the state of the RxEnb* signal. The SDHT will never pause during an ATM cell transmission by deasserting RxClav.

RxEnb* controls the data flow from PHY to ATM. If it goes into unassigned state the PHY stops the transmission of data octets in the next clock cycle.

The signals of the UTOPIA transmit interface are:

TxData (7–0), is an 8–bit data bus. TxData(7) is the MSB.

TxSOC, Transmit Start–of–Cell**,** is a signal indicating the first octet of a cell. It is set to one when the first octet of a cell is transmitted and is zero in all other cases.

TxClav indicates the storage availability for the actually received cell via the transmit interface until the 44th payload octet. After the 44th payload octet and during the time the PHY is not receiving a cell TxClav indicates the availability of the storage space for a complete new cell.

TxEnb* is asserted by the ATM if valid data is transmitted to the PHY. If it is deasserted the SDHT ignores the value of TxData (7–0) and TxSOC.

3.1.1.5 Timing

As the timing of the UTOPIA signals is critical, the interconnection lines should be as short as possible. See Chapter 5 for timing diagrams.

3.1.2 Handshake Examples

The Level 2 UTOPIA specification includes even examples describing the handshake mechanisms used between the UTOPIA Interface and an ATM Layer device. See figures 16 to 22 and the UTOPIA specification, Level 2, Figures 3.3–3.6 and 3.8–3.10.

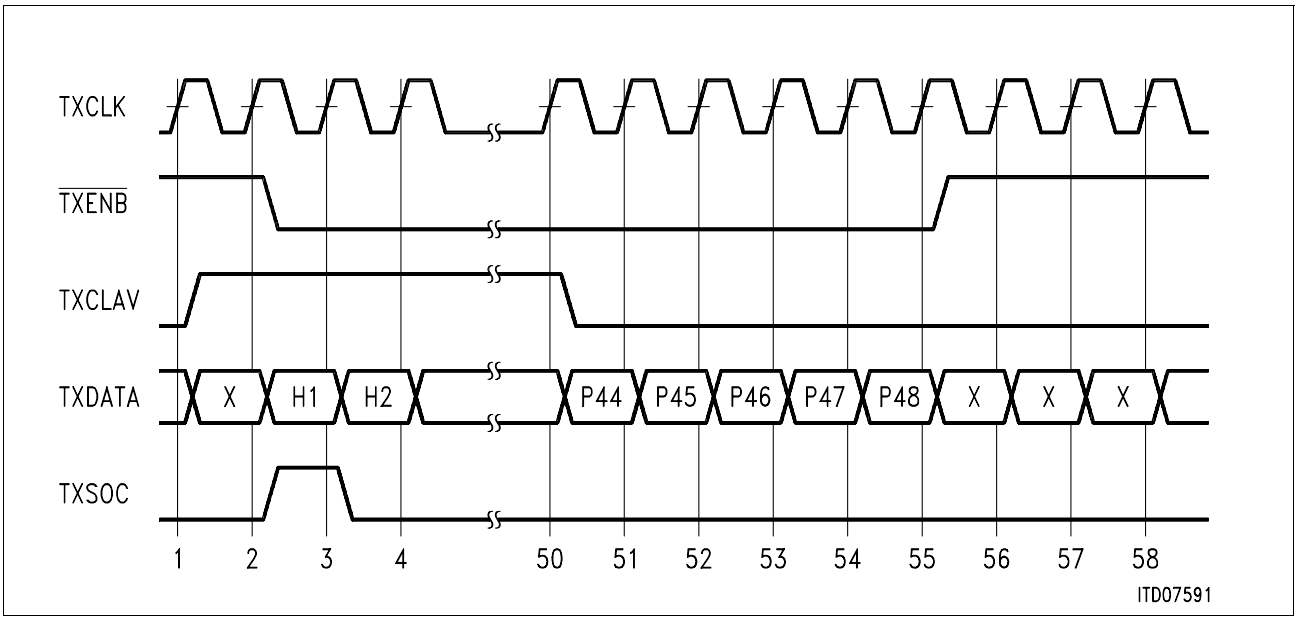


Figure 16
TxClav Example #1

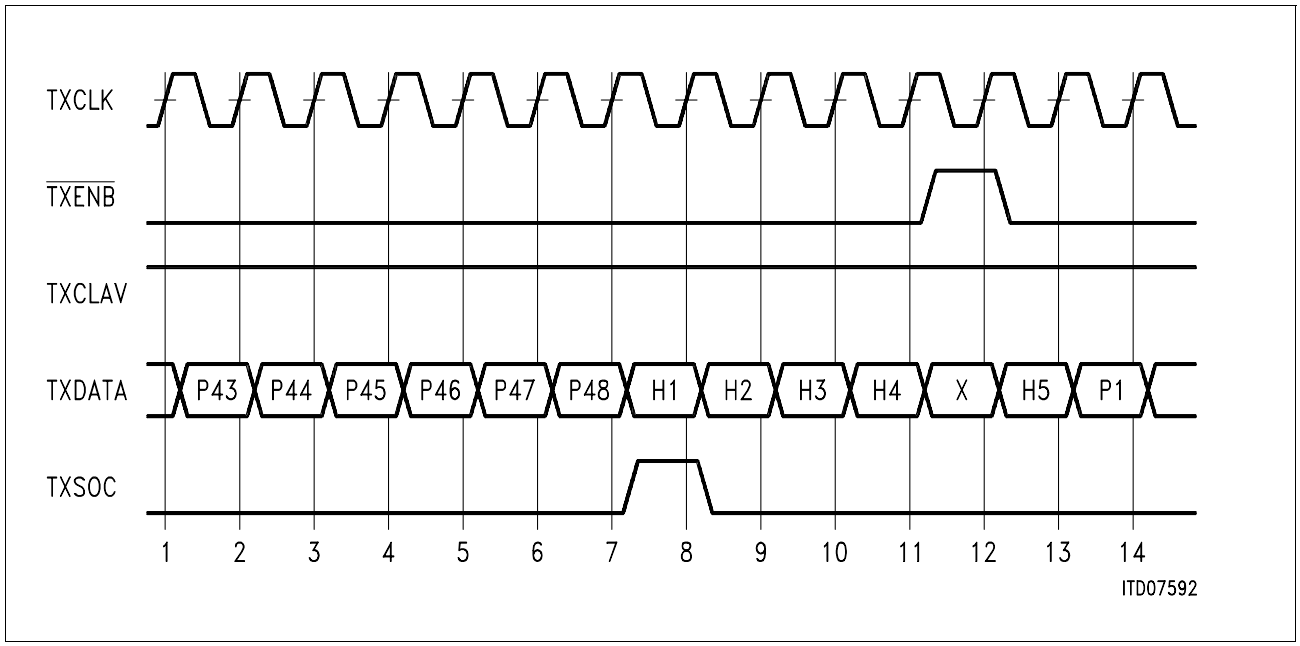


Figure 17
TxClav Example #2

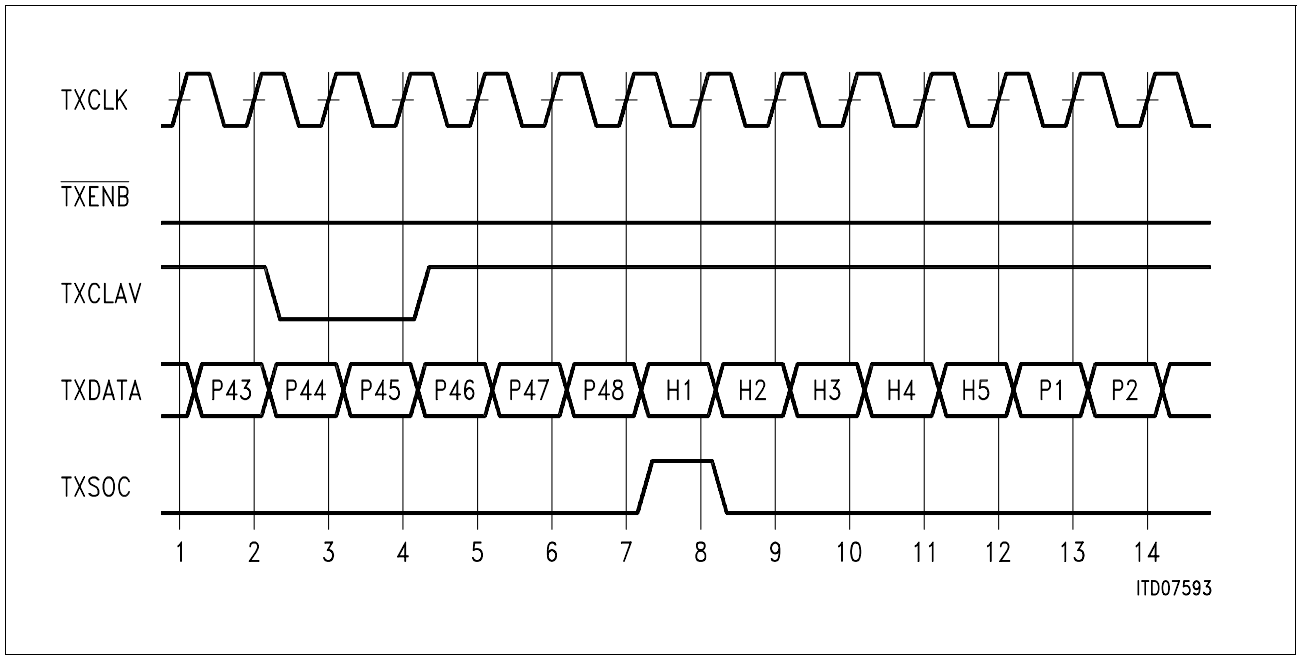


Figure 18
TxClav Example #3

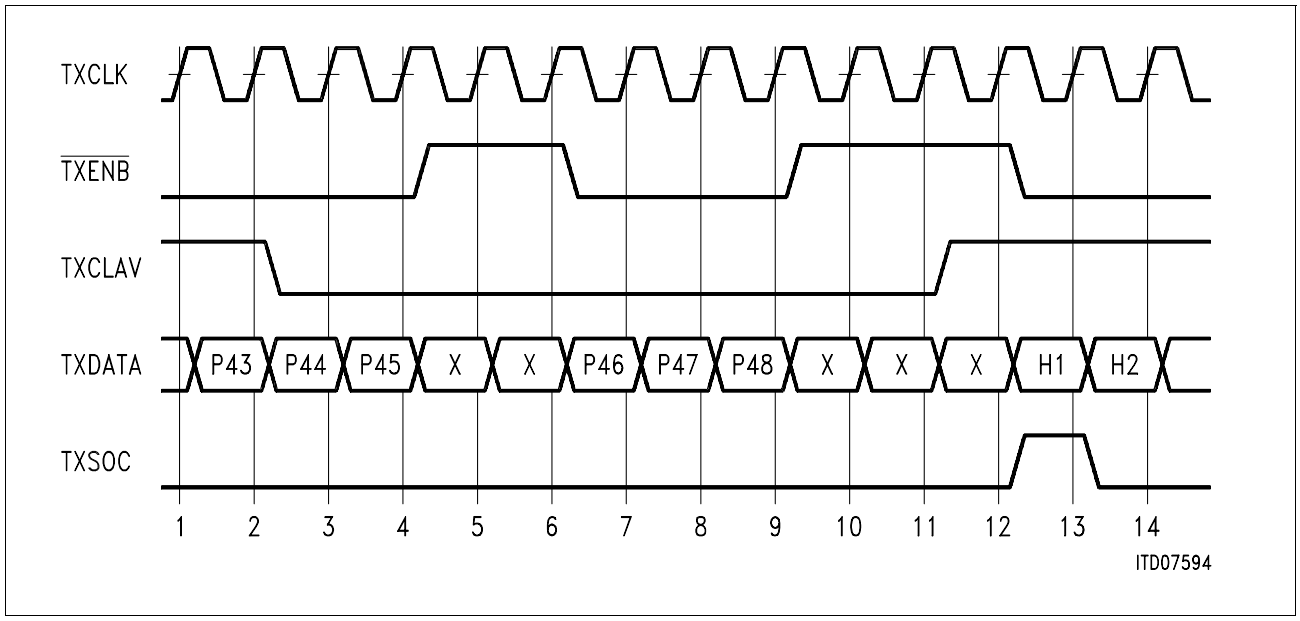


Figure 19
TxClav Example #4

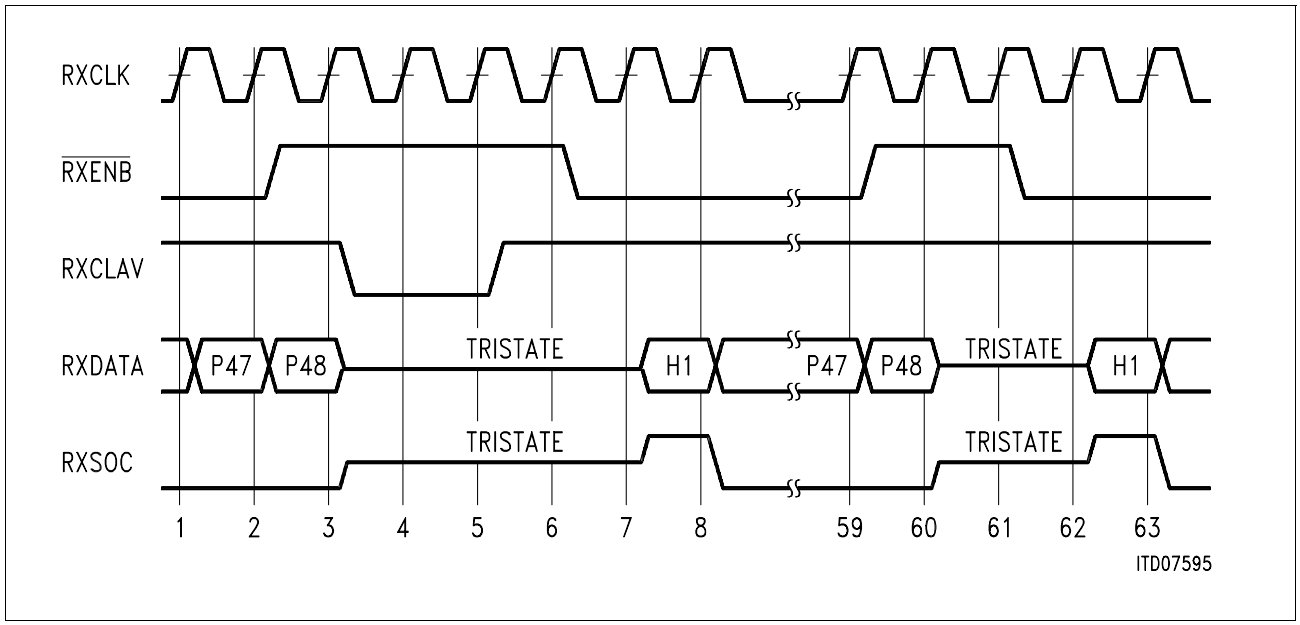


Figure 20
RxClav Example #1

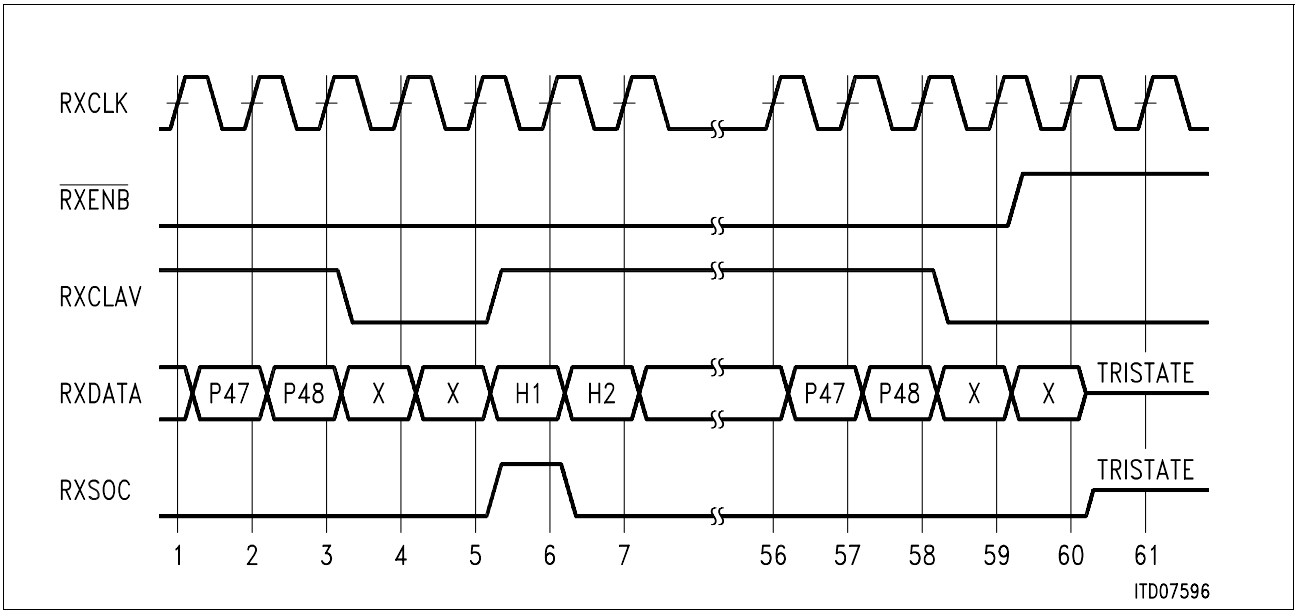


Figure 21
RxClav Example #2

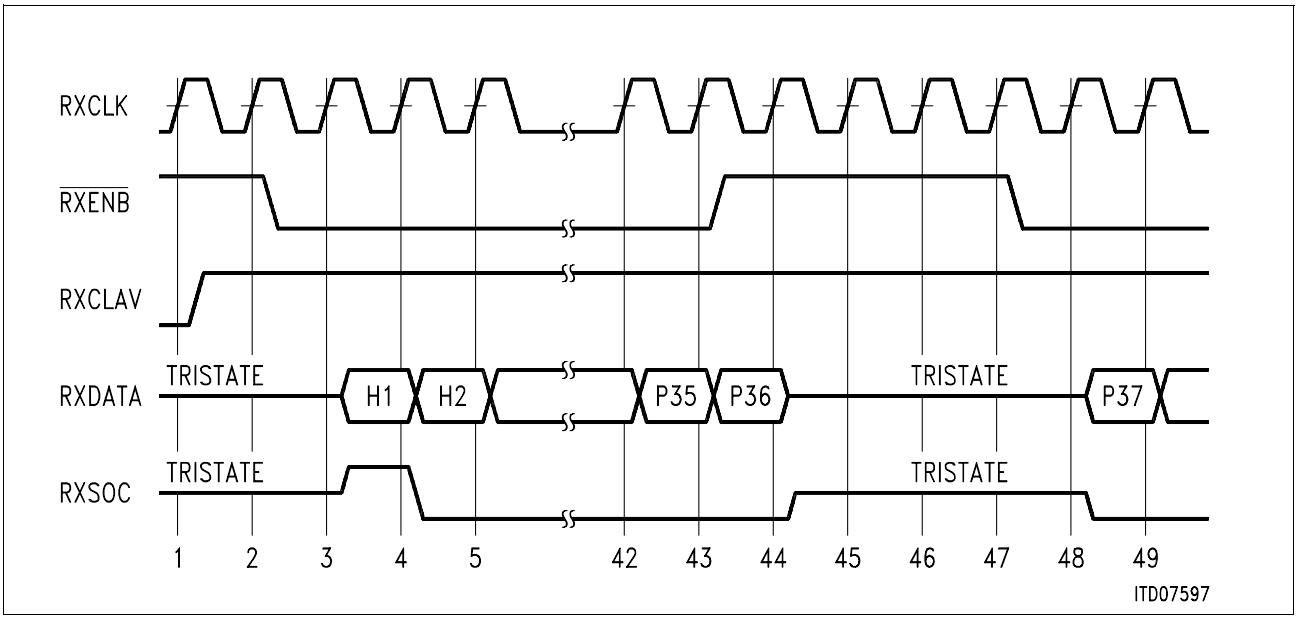


Figure 22
RxClav Example #3

3.1.3 UTOPIA (Rx) During Receiving Error Conditions

When the received STM–1 signals error conditions leading to a P–AIS error condition, the internal cell delineation is reset to the HUNT state. Thus, no more cells are provided

to the UTOPIA block internally. Cells already contained in the Rx FIFO remain accessible.

3.1.4 Switching Between UTOPIA and VC-4

The Payload Interface is switched to UTOPIA mode by the bit ENUTOPIA in the Config1H Register (1: UTOPIA enabled; default is inverted level of pin SXBMOD during HW reset). SDHT is switched to VC–4 mode for multiplexer section termination applications. Switching to VC–4 mode can be accomplished either via the Mode Register or optionally, when the Payload Loop is closed. Then, the RxSoc (TxSoC) signal indicates the beginning of the VC–4 container at the J1 byte. The RxClav (TxEnb) signal enables both C–4 and POH, to complete the VC–4.

3.1.5 PHY Cell Insertion

For inserting and discarding of physical layer cells, two formats with different headers are supported: The ITU–T idle cell (header: 00 00 00 01 52), and the US unassigned cell (00 00 00 00 55). The bit IDLEUS (register config 1H) selects for both Rx and Tx, which one is used (1: US unassigned cell; default: inverted level at pin XSONET during HW reset). The discarding of physical layer cells is controlled by the bit ENIDLE in the register config 1H (1: discarding enabled; default: 1). The insertion of physical layer cells cannot be disabled by a mode bit, but is automatically suppressed, as long as the Tx FIFO is not empty.]

3.1.6 Bit Ordering

There are different ways for ordering the bits in a byte. For overhead and STM–1 data, the SDHT chip uses the ITU–T description (MSB = bit 1, LSB = bit 8). For the µP interface and ATM interface, the SDHT orders bits as is customary in general computing (MSB = bit 7, LSB = bit 0). See Table 6.

Table 6 Bit Ordering in the SDHT

	MSB							**LSB**
Overhead Blocks, STM–1 data	1	2	3	4	5	6	7	8
µP Interface, payload Interface	7	6	5	4	3	2	1	0

Overhead blocks consisting of more than one byte (e.g. A1 which has 3 bytes), the individual bytes are numbered in the order they are transmitted (e.g. A1#2 = the second

A1 byte). For registers comprising more than one byte, the most significant byte is associated with the highest address.

3.2 Microprocessor Interface

This is the universal, generic, 16–bit microprocessor interface which is used for all Siemens ATM chips except the SARE chip. Using 8 address lines, this microprocessor interface provides direct access to up to 256 internal 8–bit registers. Additionally, a mode with only an 8–bit data bus is available for use with an 8–bit microprocessor (e.g. 80188).

The SDHT may be used with an 8– or 16–bit microprocessor with separated or multiplexed address and data buses. The way it is used is determined by the level at the input pins SMXD (high: multiplexed) and X8BITMP* (high: 16–bit interface). Table 1, in Chapter 1, summarizes the microprocessor interface signals

3.2.1 8–bit/16–bit Bus Width Selection

If X8BITMP* is high, the complete 16–bit wide data bus DAT(15–0) is used, and data may be written into the SDHT wordwise or bytewise. Writing to the bus is controlled by the signal at BHE and the address bit 0, ADR(0). For writing words, both BHE and ADR(0) have to be low. For writing single bytes, BHE must be the inverted ADR(0).

Table 7 Access Types in 16-bit mode

A0	BHE	data source	access type
0	0	DAT<0-15>	word access at even address
0	1	DAT<0-7>	byte access at even address
1	0	DAT<8-15>	byte access at odd address
1	1		not allowed

During a read access, the SDHT delivers the data wordwise.

If X8BITMP* is low, only the lower half of the data bus is used, DAT(7–0). The data transfer must be performed bytewise. I this case, the pin BHE has no function. The value of X8BITMP* must not change during operation.

3.2.2 Multiplexed/ Non-multiplexed Bus Mode

If SMXD is high, the multiplexed bus mode is selected. In this mode, the SDHT’s Microprocessor Interface connects directly to Intel '186 series (for 16–bit wide data transfer) or '188 series (for 8–bit wide data transfer) processors. In particular, DAT<15–0> (DAT<7–0>) is the 16–bit (8–bit) wide multiplexed address/data bus and may be connected directly to the processor bus. To the address, only the bits 7–0 are relevant. For these, the SDHT contains internal latches gated by ALE: While ALE = low, the

address is held. Internal reading is triggered by the falling edge of ALE regardless of the state of RD* or CS*. For the timing of ALE vs. address lines, see Chapter 5.

If the SMXD control pin is low or not connected, the address latch feature is disabled, and the SDHT must be connected to demultiplexed address and data buses. In this mode, SDHT pins ADR<7–0> are the address inputs, and the pins DAT<15–0> (or DAT<7–0> for 8 –bit bus width) are the pure data bus. In this mode, the ALE pin may be not connected. This makes the timing of the falling edge of CS* vs. address bus important (see Chapter 5 for details). But if the ALE pin is used in this mode, the CS is not validated until ALE is low, and the timing of ALE has to be according instructions in Chapter 5. The use of ALE is autodetected with the first occurrence of a rising edge; once ALE has been used, it must be used until the next chip reset occurs.

3.3 Line Interfaces

3.3.1 High–Speed Serial Interface (155.52–Mbit/s STM–1)

The SDHT Line Interface for 155.52 Mbit/s is compliant with the IEEE Standard 1596.3 (Low–Voltage Differential Signals, LVDS). The single 3.3 V supply voltage provided on the SDHT does not permit the use of shifted or pseudo ECL logic levels.

LVDS defines a differential signal with 250 mV swing that is compatible with low–voltage circuitry including CMOS technology. Only 2.5 mA is required for the generation of this differential voltage across a 100 Ohm termination resistance. This provides low power dissipation of the transceivers.

The SDHT uses LVDS levels for all the differential high-speed I/O.

Standard general purpose LVDS output voltage levels are defined by IEEE as a differential output voltage of 250 to 400 mV anywhere in the range of 0.925 to 1.475 V, with an offset voltage of 1.125 to 1.275 V.
In case of the SDHT the output levels are adjustable by an external reference voltage and a bias resistor connected at pins OBIAS and ext. REF, respectively. The default resistance and voltage values given in table 8 result in an output voltage swing slightly bigger than in IEEE 1596.3 in order to facilitate interfacing to ECL devices: The DC characteristics of the SDHT LVDS I/O’s are shown in Chapter 5.3.

3.3.1.1 Timing

For timing adjustment at the serial 155 Mbit/s interface, both Rx and Tx data lines are clocked at the rising edge of their respective clock.

3.3.1.2 Switching to Local Clock (for Tx side)

For the Tx part, normally the Trigger Clock TXC0 is used. In case of switching to local clock, TXC1 is selected if the mode bit ENTXC1 in register test mode H (default: 0) is set. If this mode bit is cleared, the SDHT uses TXC0 in either case.

Clock switching is performed on 155 MHz level. The selected clock is also provided to the output TXC. See also chapter 3.5.3.

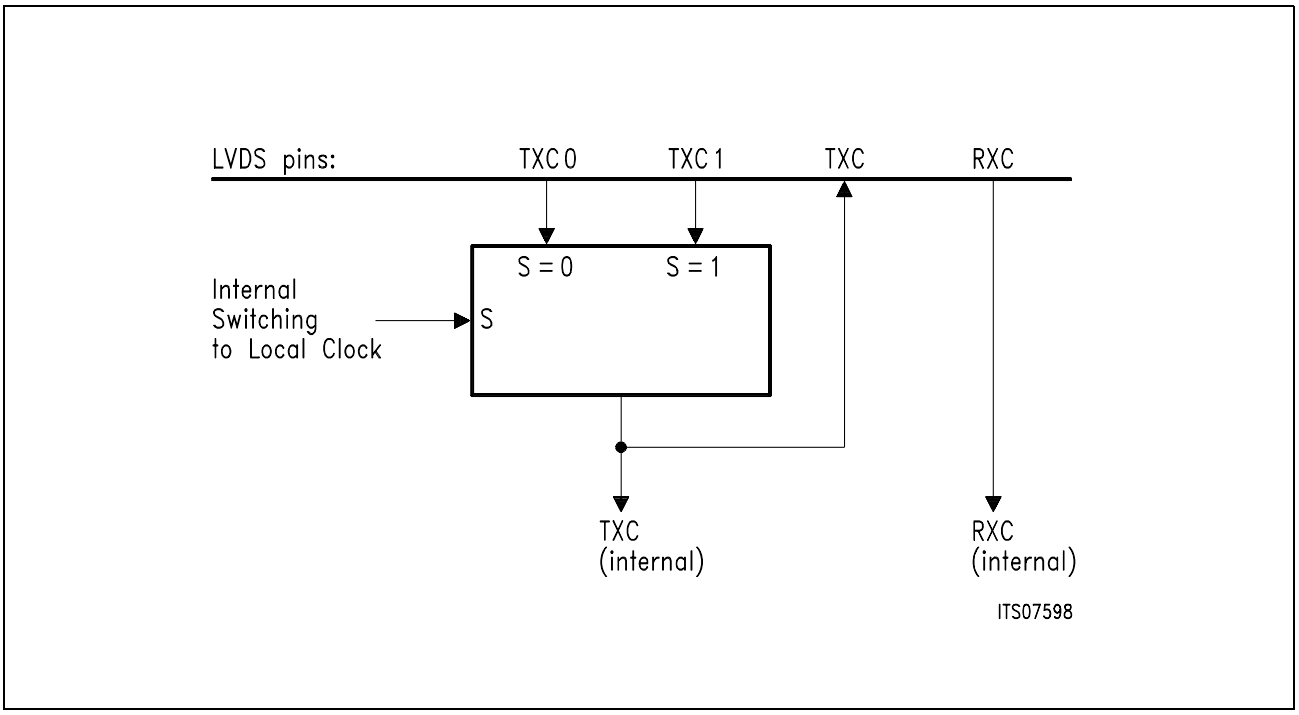


Figure 23
SDH Clock Switching

3.3.1.3 No Boundary Scan

Boundary scan is not implemented at the serial 155.52 Mbit/s interface.

3.3.1.4 Switching Off the High Speed Serial Output

Controlled by the configuration bit 'ENSEROFF' (ENable of switching the SERial output OFF), the high speed serial data output TXD is switched to all zeroes when SLDON is low. This does not affect the internal loop.

The bit ENSEROFF is placed in the test mode H register (1: switching off enabled; default: 0)

3.3.1.5 ATM Loop

The XATMLOOP pin is active high with internal pull-down resistor. Therefore the XATMLOOP pin can be both open or connected to ground for the normal operation mode (no active loopback at the utopia interface). An high XATMLOOP pin will close a loop at the payload interface from the receiver outputs to the transmitter inputs. When the payload interface loop is closed, the mode of operation (selection of either section or

path termination) will be determined by the SPATH pin, rather than by the mode bit SVCEN.

3.3.2 Low–Rate Serial Interfaces

For special applications, the SDHT chip provides access to the STM–1 section overhead bytes shown in Table 8 via serial interfaces with low data rate.

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Table 8 SOH Bytes Accessible by Low Data Rate Serial Interfaces

Overhead Bytes	Application	Data Rate	SDHT Pins
E1	Regenerator section orderwire	64 kbit/s	DSOW1, DEOW1, TSOW, TSOWB, TEOW, TEOWB
E2	Multiplexer section orderwire	64 kbit/s	DSOW2, DEOW2, TSOW, TSOWB, TEOW, TEOWB
D1–D3	Regenerator section communication DCC1	192 kbit/s	DSD1, DED1, TSD1, TED1
D4–D12	Multiplexer section communication DCC2	576 kbit/s	DSD2, DED2, TSD2, TED2

3.4 Boundary Scan Interface

JTAG boundary scan is available on all signal pins except the High–Speed Line Interface pins (LVDS data and clock inputs and outputs) and Power Supply pins.

The SDHT chip supports the JTAG boundary scan subset for board tests. Internal chip test is not supported. For the boundary scan description in detail, refer to the JTAG specifications [JTAG]. The Boundary Scan ID number is 2002C083H.

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Table 9 SDHT Boundary Scan Table

Boundary Scan Number	PIN-Nr.	Signal-Name	Type	Number of Scan Cells
1	85	SIR1	I	1
2	86	SIR2	I	1
3	87	SIRP	I	1
4	88	SIUB	I	1
5	89	SITE1	I	1
6	91	SRINH	I	1
7	92	TAR1	I	1

Table 9 SDHT Boundary Scan Table (cont'd)

Boundary Scan Number	PIN-Nr.	Signal-Name	Type	Number of Scan Cells
8	94	RES	I	1
9	95	SAISOUT	O	2
10	96	TESTM	I	1
11	97	TSSTMR	I	1
12	98	T4BIT	I	1
13	99	TMODE	I	1
14	100	TEOW	O	2
15	101	TEOWB	O	2
16	103	TSOW	O	2
17	104	TSOWB	O	2
18	105	DEOW1	O	2
19	106	DEOW2	O	2
20	108	DSOW1	I	1
21	109	DSOW2	I	1
22	110	TED1	O	2
23	111	TED2	O	2
24	113	TSD1	O	2
25	114	TSD2	O	2
26	115	DED1	O	2
27	116	DED2	O	2
28	117	DSD1	I	1
29	119	DSD2	I	1
30	120	TS19M	O	2
31	121	TE19M	O	2
32	122	RxClav	O	2
33	123	RxSOC	O	2
34	125	RxEnb*	I	1
35	126	reserved	O	2

Table 9 SDHT Boundary Scan Table (cont'd)

Boundary Scan Number	PIN-Nr.	Signal-Name	Type	Number of Scan Cells
36	127	RxData 7	O	2
37	128	RxData 6	O	2
38	129	RxData 5	O	2
39	131	RxData 4	O	2
40	132	RxData 3	O	2
41	133	RxData 2	O	2
42	134	RxData 1	O	2
43	135	RxData 0	O	2
44	136	AtmClk	I	1
45	139	TxData 0	I	1
46	140	TxData 1	I	1
47	141	TxData 2	I	1
48	142	TxData 3	I	1
49	143	TxData 4	I	1
50	145	TxData 5	I	1
51	146	TxData 6	I	1
52	1	X8BITMP	I	1
53	2	ALE	I	1
54	4	BHE	I	1
55	5	CS	I	1
56	6	RD	I	1
57	7	WR	I	1
58	9	INT	O	2
59	10	DAT(0)	I/O	3
60	11	DAT(1)	I/O	3
61	12	DAT(2)	I/O	3
62	13	DAT(3)	I/O	3
63	14	DAT(4)	I/O	3

Table 9 SDHT Boundary Scan Table (cont'd)

Boundary Scan Number	PIN-Nr.	Signal-Name	Type	Number of Scan Cells
64	16	DAT(5)	I/O	3
65	17	DAT(6)	I/O	3
66	18	DAT(7)	I/O	3
67	19	DAT(8)	I/O	3
68	20	DAT(9)	I/O	3
69	21	DAT(10)	I/O	3
70	23	DAT(11)	I/O	3
71	24	DAT(12)	I/O	3
72	25	DAT(13)	I/O	3
73	26	DAT(14)	I/O	3
74	27	DAT(15)	I/O	3
75	29	ADR(0)	I	1
76	30	ADR(1)	I	1
77	31	ADR(2)	I	1
78	32	ADR(3)	I	1
79	33	ADR(4)	I	1
80	34	ADR(5)	I	1
81	35	ADR(6)	I	1
82	36	ADR(7)	I	1
83	37	SMXD	I	1
84	40	SLOOP	O	2
85	41	reserved	O	2
86	42	reserved	O	2
87	43	reserved	O	2
88	44	reserved	O	2
89	45	XATMLOOP	I	1
90	46	SXBMOD	I	1
91	47	SIEIN	I	1

Table 9 SDHT Boundary Scan Table (cont'd)

Boundary Scan Number	PIN-Nr.	Signal-Name	Type	Number of Scan Cells
92	48	SIAUS	I	1
93	49	SILD	I	1
94	50	SLDON	O	2
95	51	SSERST	O	2
96	63	TRI_STM	I	1
97	64	TRI_AIS	I	1
98	76	TSTMRFL	I	1
99	78	TRI_ATM	I	1

3.5 Control Signal Interface

This interface includes control pins for mode select, alarms, etc. This set of pins is used for special control functions like raising an interrupt, loop switching etc.

The pins SIAUS, SIEIN, SILD, SITE1*, SIUB*, SIRP*, SIR1*, and SIR2 set the corresponding bit in the SDHT status register. So, each can generate an interrupt if its respective mask register bit is set, too. Except for SIEIN and SILD which trigger special functions, the SIxxx pins may be freely used as they are not dedicated by implementation. In order to avoid confusion, however, the signals should be used as described Chapter 1, which gives a summary of the SDHT control pins.

3.5.1 LOS Detection

The SIEIN pin should be connected to an active high loss of signal (LOS) detector on board. If SIEIN is high, the SDHT will transmit MS-FERF backwards (and, if set up as path termination, P-FERF) and activate the output pins SAISOUT* and SSERST*. For inhibiting of the SIEIN pin by setting the test mode bit LOSOFF, see Chapter 4.

When the signal at SIEIN has changed to low, LOS is released immediately or, if the bit LOSUS (register config 1L) is set (US mode), after receipt of 2 valid framing patterns.

Note: Using the SDHT in US mode, does not permit detection of LOS without a receive clock. This happens if the clock recovery shuts down before LOS is signalled to the SDHT.

3.5.2 Laser Shutdown

For automatic laser shutdown in case of a broken fibre or too much laser power, the SILD pin should be connected to an active high signal indicating these faults. If SILD is high, the SDHT starts the laser shutdown timer and, after 0.5 s, deactivates the laser control output pin SLDON and resets the mode bit SLDEN (see Table 18). If SILD goes low before 0.5 s have expired, the shutdown timer is reset. After automatic shut down, the laser can be turned on again by setting SLDEN. If SILD is still low, a new 0.5 s interval will start.

The 0.5 s count down is only working well if a suitable Tx clock is provided to the SDHT.

The automatic laser shutdown is disabled when the test mode bit DISASD (default: 0) is set.

3.5.3 Switching to Local Clock

For use on equipment like NT1 or TA (which use the recovered receive clock for transmission), the SDHT supports switching to local clock in case of a disturbed receive signal. Conditions for switching to local clock are: LOS is detected (via pin SIEIN set high); the mode bit SERSMP is set by the microprocessor. If the pin TAR1* is tied to ground, any of the following conditions switch to the local clock, too: Clock monitoring shows defect in the receive clock (status SISTD); LOF; excessive BER is detected by evaluation of the B2 bytes (status SXCB2).

The output pin SSERST* pin (active low) serves as an indication for an external device to switch the transmit clock of the system from the regenerated receive clock to a local clock. SSERST* is activated, if one of the conditions above is met, and the mode bit ENERST in register test mode H (0: disabled; default: 1) is set.

If the bit ENERSTXB in the test mode register is set to 1 (is default), switching to local clock also affects the payload interface in VC-4 mode.

Switching to local clock may also be done by the SDHT directly, by selecting TXC1 instead of TXC0 internally. This is enabled by the bit ENTXC1 in register test mode H (0: disabled; default: 0).

3.5.4 P-AIS Generation and Pins

If not set up as path termination, a low level at the SAISIN* pin forces the SDHT to transmit P-AIS (else, the SAISIN* pin is ignored). The signal input at SIASIN* is not latched frame by frame, but sampled exactly in the moment, when P–AIS may be

inserted in the STM–1 frame. Thus, short pulses at SAISIN* may or may not result in transmission of P–AIS.

The output pin SAISOUT* (active low) is activated when at least one of the following conditions is detected: LOS (via SIEIN high), LOF, MS AIS, LOP, LOC (only at path termination; suppressed if UEQ is received), or received P–AIS. So, for transferring a P–AIS condition in a section terminating equipment (e.g. an NT1) between two SDHT connected at the payload interface, their pins SAISOUT* and SAISIN* should be connected crosswise.

3.5.5 Loop Remote Control, Remote Inhibit

The SLPOUT pin reflects the state of bit 7 of the received Z2#1 overhead byte which may be used to make another, connected, SDHT switch on its section loop back via its SLPIN pin. The state of SLPIN is reflected in the status bit HWLOOPON. If the SLPIN pin is active or the bit SLOOP in the mode register is set, the SDHT turns on the internal section loop at its Line Interface (both mode bit LPINT and test mode bit LOOPINT set) or activates the SLOOP output pin (either LPINT or LOOPINT not set).

If the SRINH* input pin becomes active, the SDHT sets bit 8 of the Z2#1 overhead byte in the transmitted signal. SRINH* may be used as a far end power fail (FEPF) signal, helping the FW to ignore alarms during a far end power down. Receiving SRINH* sets the status bit SERINH.

The following flow chart illustrates the loopback scenario:

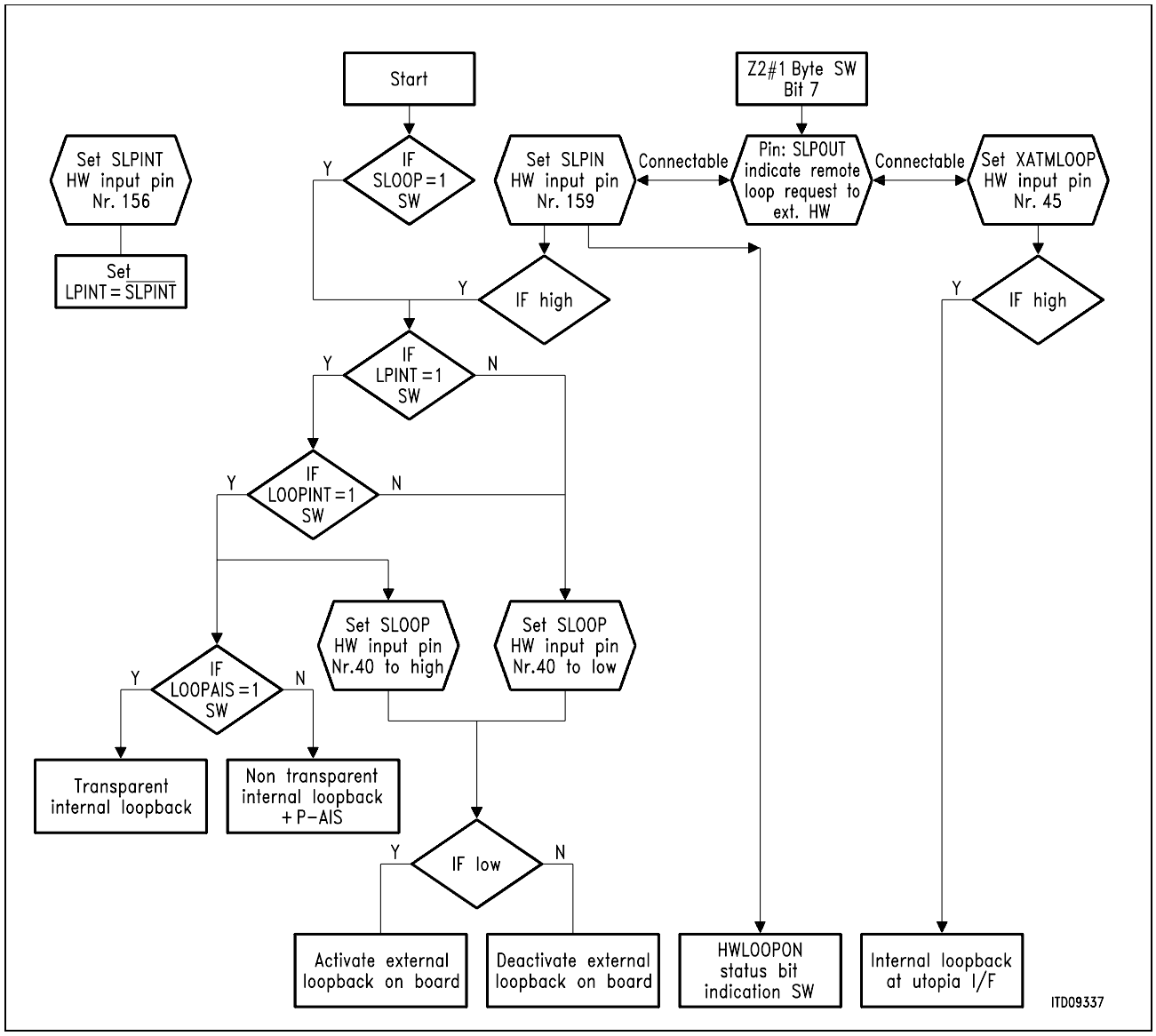

Figure 24
SDH Flow Chart for Loopback Applications

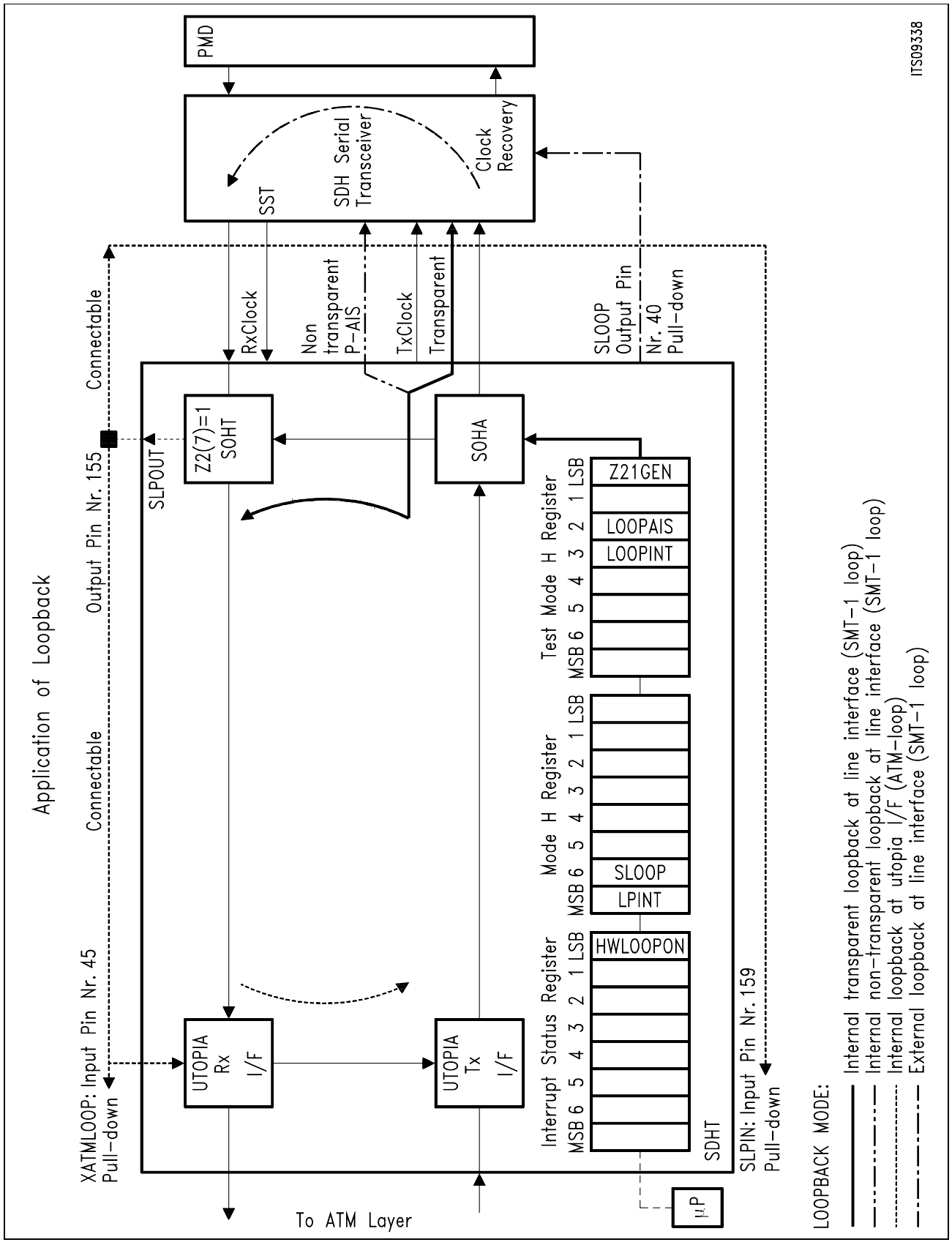
PMD
SDH Serial Transceiver
Clock Recovery
SST
RxClock
Non transparent P-AIS
TxClock
Transparent
SLOOP Output Pin Nr. 40 Pull-down
Connectable
Output Pin Nr. 155
SLPOUT
Z2(7)=1 SOHT
SOHA
Application of Loopback
Connectable
XATMLOOP: Input Pin Nr. 45 Pull-down
UTOPIA Rx I/F
UTOPIA Tx I/F
Test Mode H Register
MSB 6 5 4 3 2 1 LSB
Z21GEN
LOOPAIS
LOOPINT
Mode H Register
SLOOP
LPINT
Interrupt Status Register
HWLOOPON
SDHT
SLPIN: Input Pin Nr. 159 Pull-down
µP
To ATM Layer
LOOPBACK MODE:
Internal transparent loopback at line interface (SMT-1 loop)
Internal non-transparent loopback at line interface (SMT-1 loop)
Internal loopback at utopia I/F (ATM-loop)
External loopback at line interface (SMT-1 loop)
ITS09338

Figure 25

SDH Loopback Applications

3.5.6 Chip Reset

By driving the SERES pin to high level for at least one microsecond, the complete SDHT chip is reset. The pins SPATH, SLPINT and XSONET determine the default values of the mode and configuration registers after a HW chip reset.

4 Register Description

4.1 SDHT Register Summary

The internal SDHT registers can be accessed bytewise or wordwise, where 1 word = 16 bits. Table 10 presents all the registers in summary form. Following sections provide detailed descriptions by type of register.

Table 10 SDHT Register Summary

Register(s)	Address Range	Access Type	Description
SOH bytes "...s"		Read/Write	SOH bytes ('s' for 'send')
C1	51H		STM Identifier
B1	-		BIP-8 Reg. Section
E1	-		Orderwire
F1	50H		User channel
D1 - D12	40H - 4EH		Data Comm. Channel
B2	-		BIP-24 Mult. Section
K1, K2	70H, 71H		APS & MS-AIS/RDI
Z1#1 (S1)	54H		Syn. Status
Z1#2, Z1#3	55H, 56H		
Z2#1, Z2#2	57H, 5BH		
Z2#3 (M1)	-		MS-REI
E2			Orderwire
SOH bytes "...r"		Read Only	Received SOH bytes
C1	53H		STM Identifier
B1	-		BIP-8 Reg. Section
E1	-		Orderwire
F1	52H		User channel
D1 - D12	60H–6EH		Data Comm. Channel
B2	-		BIP-N*24 Mult. Section
K1, K2	72H, 73H		APS & MS-AIS/RDI
Z1#1 (S1)	58H		Syn. Status
Z1#2, Z1#3	59H, 5AH		
Z2#1, Z2#2	5CH, 5DH		
Z2#3 (M1)	5EH		MS-REI
E2	-		Orderwire

Table 10 SDHT Register Summary (cont'd)

Register(s)	Address Range	Access Type	Description
POH bytes "...s"		Read/Write	POH bytes ('s' for 'send')
J1	00H–0FH		Path Trace
B3	-		Path BIP-8
C2	-		Signal Label
G1	-		Path Status
F2	80H		Path User Channel
H4	81H		Position Indicator
Z3 (F3)	86H		Aut. Prot. Switching (APS)
Z4 (K3)	87H		Spare
Z5 (N1)	88H		Network Operator Byte
POH bytes "...r"		Read Only	Received POH bytes
J1	10H–1FH		Path Trace
B3	-		Path BIP-8
C2	85H		Signal Label
G1	84H		Path Status
F2	82H		Path User Channel
H4	83H		Position Indicator
Z3	8AH		Aut. Prot. Switching (APS)
Z4	8BH		Spare
Z5	8CH		Network Operator Byte
Mode	94H–95H	Read/Write	Mode bits (refer to Tables 12 and 14)
Config	9EH–9FH, C6H–C7H	Read/Write	Configuration bits for enhanced functions (e.g. for SONET functionality and pointer evaluation)
Interrupt Status	90H–93H, C0H	Read/Write (Note)	Interrupt status bits (refer to Tables 12 and 13)
Interrupt Mask	98H–9BH, C2H	Read/Write	Interrupt mask bits
Latched Status	A0H–A1H, AEH–AFH, C4H	Read Only	Latched interrupt status bits
Release Interrupt Status	D0H–D4H	Read/Write (Note)	Interrupt status for inverted states
Release Interrupt Mask	D8H–DCH		Mask bits for release interrupt status register
Latched Release	C8H–CCH	Read Only	Latched inverted interrupt status bits

Table 10 SDHT Register Summary (cont'd)

Register(s)	Address Range	Access Type	Description
Test Mode	96H–97H	Read/Write	Test mode bits (refer to Tables 12 and 19)
Test Status	9CH–9DH	Read Only	Test status bits(refer to Tables 12 and 23)
UTOPIA (1 Sec.) Monitoring RXHECCOR RXHECDIS RXIDLE RXINFO. ATMRXCLK RXOCD	E0H–F3H E0 - E2H E4 - E6H E8 - EAH EC - EEH F0 - F1H F3 - F3H	Read Only	**20 Bit Counters** for Rx cell statistics cell header correction discarded cells discarded idle cells user cells to Utopia IF **16 Bit counters** for clock cycle out of cell delineation
Latched (1Sec.) Error Counters' B1 B2 B3 S-FEBE (REI) P-FEBE (REI) Tx point. stuffing lost ATM cells	 A2 - A3H A4 - A5H A6 - A7H AA - ABH A8 - A9H BC - BFH AC - ADH	Read Only	**16 Bit Counters** for BIP-8 errors, Reg. Section BIP-24 errors, Mul. Section BIP-8 errors, Path Remote Error Indication Remote Error Indication pos./neg. stuffing events
Bit Error Thresholds for B1 B2 B3 B2 SD B2 SD control	 B2 - B3H B4 - B5H B6 - B7H B8 - BAH BBH	Read/write	**12 Bit Thresholds** for excessive B1-BER B2-BER B3-BER and signal degrade see chapter 4.6.1
Chip Version	FFH	Read Only	SDHT Version (02 fixed value)

Note: Bits to which "1" is written will be cleared if the state is no longer active; write "0" to bit: no change

4.2 SDHT Register Address Mapping Summary

The next table shows the comprehensive address mapping of the SDHT registers.

Table 11
Register Address Mapping Summary

low order	high order 4 address bits (Hex)													
addr. bits	0.	1.	4.	5.	6.	7.	8.	9.	A.	B.	C.	D.	E.	F.
.0	J1s (0)	J1r (0)	D1s	F1s	D1r	K1s	F2s	interrupt status 1 L	latched status 1 L		interrupt status 3 L	release int. status 1 L		ATM RxClk
.1	J1s (1)	J1r (1)	D2s	C1s	D2r	K2s	H4s	interrupt status 1 H	latched status 1 H			release int. status 1 H	Rx Hec-Cor	
.2	J1s (2)	J1r (2)	D3s	F1r	D3r	K1r	F2r	interrupt status 2 L	B1 error	Excessive BER	Interrupt mask 3 L	release int. status 2 L		Rx OCD
.3	J1s (3)	J1r (3)		C1r		K2r	H4r	interrupt status 2 H	count	threshold B1		release int. status 2 H		
.4	J1s (4)	J1r (4)	D4s	Z1# 1s	D4r		G1r	mode L	B2 error	Excessive BER	latched status 3 L	release int. status 3 L		
.5	J1s (5)	J1r (5)	D5s	Z1# 2s	D5r		C2r	mode H	count	threshold B2			Rx HecDis	
.6	J1s (6)	J1r (6)	D6s	Z1# 3s	D6r		Z3s	test mode L	B3 error	Excessive BER	config 2 L			
.7	J1s (7)	J1r (7)		Z2# 1s			Z4s	test mode H	count	threshold B3	config 2 H			
.8	J1s (8)	J1r (8)	D7s	Z1# 1r	D7r		Z5s	interrupt mask 1 L	P-FEBE		lached release 1 L	release int. mask 1 L		
.9	J1s (9)	J1r (9)	D8s	Z1# 2r	D8r			interrupt mask 1 H	error count	B2 SD threshold	latched release 1 H	release int. mask 1 H	Rx Idle	reserved

Table 11
Register Address Mapping Summary (cont'd)

low order addr. bits	high order 4 address bits 0.	1.	4.	5.	6.	7.	8.	9.	A.	B.	C.	D.	E.	F.
.A	J1s (10)	J1r (10)	D9s	Z1# 3r	D9r		Z3r	interrupt mask 2 L	S-FEBE		latched release 2 L	release int. mask 2 L		for test
.B	J1s (11)	J1r (11)		Z2# 2s			Z4r	interrupt mask 2 H	error count	B2 SD control	latched release 2 H	release int. mask 2 H		
.C	J1s (12)	J1r (12)	D10 s	Z2# 1r	D10r		Z5r	test sta-tus L	lost ATM cells	positive stuffing	latched release 3 L	release int. mask 3 L		
.D	J1s (13)	J1r (13)	D11s	Z2# 2r	D11r			test sta-tus H	count	count (Tx)			Rx Info	
.E	J1s (14)	J1r (14)	D12 s	Z2# 3r	D12r			config 1L	latched status 2 L	nega-tive stuffing				
.F	J1s (15)	J1r (15)						config 1H	latched status 2 H	count (Tx)				Version

4.3 Control Registers

There are four types of Control Registers: Status, Mode, Configuration, and Test.

Table 12 SDHT Status and Mode Bits

Register	MSB	bit6	bit5	bit4	bit3	bit2	bit1	LSB
Interrupt Status 1L	SIVCA	SISTA	SISTD	SITAKT	SIAUS	SIEIN	SILD	SSDB2
Interrupt Status 1H	SLOP	SSYATM	SXCB1	SXCB2	SXCB3	SYN155	SEPAIS	SESAIS
Interrupt Status 2L	**PTACK**	SEUEQ	**SAPSCMD**	**SAPSTAT**	SIXB	SEFERF	SERAI	**SIST**
Interrupt Status 2H	SITE1	SERINH	SIUB	SIRP	**TIMER**	SIR1	SIR2	OOF
Interrupt Status 3L			SLM5	SLM1	OFUTOTX	OFUTORX	**SSYSTCH**	HWLOOPON
Mode L	SSTEN	SVCEN	SATSCR	SSTSCR	SDC1	SDC2	SERSMP	SMRES
Mode H	LPINT	SLOOP	SUEQEN	SAISMP	SLDEN	SRAIMP	SDFERF	XCBAIS
Config 1L	C1US	LOFUS	LOSUS	LAISUS	K1K2US	PRAIUS	NUS	UNDEFUS
Config 1H	ENIDLE	ATMPTR	RAIINH	LOCRAIINH	ENHEC	OCTLVL	ENUTOPIA	IDLEUS
Config 2L	ENINVNDF	CIEN	ED	D1	D0	ES	S1	S0
Config 2H								ATC
Test Mode L	SSYATMT	ACQPT	DISASD	SLOPT	SIXBT	LOSOFF	SXCB2T	SXCB3T
Test Mode H	ENERSTXB	ENSEROFF	ENERST	ENTXC1	LOOPINT	LOOPAIS	Z21EVAL	Z21GEN
Test Status L	SSYATME			SLOPE	SIXBE		SXCB2E	SXCB3E

Note: Bits marked in bold and empty bits are always zero in the Latched Release Status Registers.

4.3.1 Status Registers and Interrupt Generation

Table 12 gives an overview of the SDHT Status and Mode Register bits. Table 13 provides a descriptive summary of the individual bits.

The names of some status bits correspond to the control inputs specified in Chapter 2. There are three sets of status bits: The Interrupt Status Registers, the Latched Status Registers, and the Latched Release Status Registers.

In the Interrupt Status Register, the status bits are sticky, meaning once set, they remain set until the processor explicitly clears the bits by writing a "1" to the corresponding bit position in the Interrupt Status Register. But the status bit cannot be cleared as long as the related internal status (or, if external, the related pin) is active. The bits TIMER, SSYSTCH, SAPSTAT and SAPSCMD do not correspond to a quasi–static internal status, and thus can always be reset.

Whether an interrupt is generated or not is determined by the Interrupt Mask Registers. The mapping of the bits in the Mask Registers is exactly the same as in the Interrupt Status Registers. E.g., the bit 5 of the register 'mask 1H' corresponds to the bit 5 of the register 'status 1H'. If both the interrupt status bit and the corresponding bit in the Interrupt Mask Register are set for a given bit, an interrupt is created. Otherwise, no interrupt is provided by the SDHT.

Another set of status bits is located in the Latched Status Registers. The bit mapping of the latched status registers 3, 4 and 6 is identical to that of the interrupt status registers 1, 2 and 5, respectively. These registers are latched simultaneously with the error counter registers once a second. During the sample time of one second, the status bits are stored in latches (that means they are sticky), and bit errors, lost ATM cells, and stuffing events are counted. The source of the stuffing events is the transmitter FIFO. At the end of the sample interval, the stored status bits and the error count values are latched into the readout registers which can be read by the processor for 1 second, and the RS-registers and then the counters are cleared.

The release interrupt status registers are completely identical to the interrupt status registers, except that the inverted status is latched. Thus, they show that the status related to a set bit has been inactive at least once since the bit has been cleared the last time. Like with the interrupt status register, each bit of the release interrupt status registers will be cleared when a '1' is written to, except the status is still inactive.

The generation of an interrupt is controlled by the release mask registers the same way it is with the interrupt status registers.

Finally, there are the latched release status registers. They show the same behavior as the latched status registers, except that they are latching the inverted status. I.e. a set bit means that the related status has not been active at least once in the previous one second interval.

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Table 13 SDHT Status Bit Descriptions (Grouped Bytewise)

Name	Description	Triggered By ...
SIVCA	HW failure in VC-4 assembler circuit	On-chip HW supervision
SISTA	HW failure in STM-1 assembler circuit	On-chip HW supervision
SISTD	HW failure in STM-1/VC-4 disassembler circuit	On-chip HW supervision
SITAKT	Clock failure; may cause SIVCA, SISTA, SISTD!	On-chip clock supervision
SIAUS	Laser power too low or modulation current too high (transmission failure 'TF')	Pin SIAUS = high
SIEIN	Loss of signal	Pin SIEIN = high
SILD	Automatic laser shutdown requested	(Pin SILD=high)and(testmd. DISASD=0)
SSDB2	Signal degrade for multiplexer section (B2)	Evaluation of B2
SLOP	Loss of AU pointer	LOP
SSYATM	Loss of ATM cell synchronization(only if SVCEN is set and no UEQ is received)	(not UEQ received) and (SVCEN=1) and LOC
SXCB1–3	Excessive bit error ratio	Eval. B1–3: bit errors exceed threshold.
SYN155	Loss of frame	LOF
SEPAIS	Receipt of Path AIS	H1#1, H2#1: all ones
SESAIS	Receipt of Section AIS	K2-byte = xxxxx111
PTACK	16 consec. bytes sampled in Rx path trace register	End of sampling algorithm
SEUEQ	Receive of UEQ (only for path termination point)	C2-byte = 00000000
SAPSCMD	Receive of a new APS command	K1 or K2 have changed
SAPSTAT	Change of APS relevant line state	Change of: [(Pin SIAUS) or LOS or LOF or SD(B2) or SIVCA or SISTA or SISTD]

Table 13 SDHT Status Bit Descriptions (Grouped Bytewise) (cont'd)

Name	Description	Triggered By ...
SIXB	UTOPIA Interface fault	Wrong behavior of PSATM or PSCELL
SEFERF	Receipt of S FERF [Generation: Figure 28]	K2-byte = xxxxx110
SERAI	Receipt of P FERF (don´t care unless path termination point) [Generation: Figure 28]	G1 byte = xxxx1xxx
SIST	Stuffing error during assembly of STM-1 frame	FIFO over/underflow in transmit part
SITE1	Temperature warning	Pin SITE1 = low
SERINH	Reception of R-INH	Z2#1 byte = xxxxxxx1
SIUB	Supply voltage warning	Pin SIUB = low
SIRP	Battery switch-over	Pin SIRP = low
TIMER	Status bits and error counters have been latched	8000 frames clock (= 1 second)
SIR1	For optional external interrupt (active low)	Pin SIR1 = low
SIR2	For optional external interrupt (active high)	Pin SIR2 = high
OOF	Out of frame	OOF and (LOFUS=1)
SLM1/5	Signal label mismatch	Once wrong/ 5 times in 50 ms wrong
OFUTOTX/ RX	OverFlow of UTOPIA ATM FIFO	FIFO full and attempt to write in FIFO
SSYSTCH	SDH sychronization status	Change in Z1#1 bits 5...8
HWLOOPON	STM 1 loop closed due to HW signal	Pin SLPIN = high

4.4 Mode Registers (Including setup at HW/ SW Reset)

Table 14 gives a brief overview of the Mode bits.

On a hardware reset, the state of the SVCEN and SATSCR mode bits are determined by the control input SPATH. The LPINT is determined by $\overline{\text{SLPINT}}$ (SLPINT is active low

Table 14 SDHT Mode Bit Descriptions (Grouped Bytewise)

Name	Default after HW Reset	Description (meaning if bit = 1, unless otherwise noted)
SSTEN	1	Enable STM-1 assembler/disassembler and all clocks
SVCEN	Pin SPATH	Enable VC-4 assembler/disassembler
SATSCR	Pin SPATH	Enable ATM scrambler
SSTSCR	1	Enable STM-1 scrambler
SDC1	1	Enable serial interface for DCC1 (192 kbit/s)
SDC2	1	Enable serial interface for DCC2 (576 kbit/s)
SERSMP	0	Switch to local clock oscillator by making the SSERST control pin active
SMRES	0	Chip reset
LPINT	Must be programmed to 1	LPINT is 1 after a hardware reset and must not be changed.
SLOOP	0	Activate loopback (see also test mode bits LOOPINT, LOOPAIS)
SUEQEN	0	Force transmission of UEQ
SAISMP	0	Force transmission of P-AIS
SLDEN	0	Switch-on of laser by making the SLDON control pin active. After automatic laser shutdown, this bit is reset to zero; to turn on the laser again, let the µP write a 1 into this bit.
SRAIMP	0	Force transmission of P-FERF
SDFERF	0	Enable transmission of S-FERF on detection of signal degrade (SD)
XCBAIS	0	Enable transmission of S-FERF (at path termination P-FERF) and activation of SAISOUT control pin on detection of excessive BER of B2 (related status bit SXCB2)

with internal pull down. Therefore SLPINT can be both open or connected to ground for the normal operation mode) . However, the mode bits SVCEN, SATSCR and LPINT may be changed arbitrarily by the microprocessor.

The values of the mode registers after a hardware reset are shown in Table 15.

Table 15 Mode Register After a Hardware Reset

SPATH	Mode H	Mode L
L	1000 0000	1001 1100
H	1000 0000	1111 1100

A software reset works in a manner similar to a hardware reset, except that the bits of Mode and Config Registers are not affected by a software reset. The SDHT is held in the reset state as long as the mode bit SMRES is set. Therefore, to reset the SDHT chip by software, the processor must both set and clear the SMRES bit. The SMRES bit is cleared by writing a "0" to the corresponding bit position of the Mode Register. Since writing to the Mode Register also affects the other bits, the processor has to supply their correct setting when clearing the SMRES bit.

Examples for different values of the mode register and their meanings are given in Table 16.

Table 16 Example Mode Register Set Up Values (Normal Operation)

Mode Register Value	Description
CA90H	STM–1 signal processing enabled, no path termination, internal STM–1 loop closed, laser on, S-FERF on SD, DCC2 not on serial interface
CA94H	STM–1 signal processing enabled, no path termination, internal STM–1 loop closed, laser on, S-FERF on SD, DCC2 on serial interface
4AF4H	STM–1 signal processing enabled, path termination, external STM–1 loop closed, laser on, S-FERF on SD, DCC2 on serial interface
4AF0H	STM–1 signal processing enabled, path termination, external STM–1 loop closed, S-FERF on SD, DCC2 not on serial interface

4.5 Configuration Registers

The Configuration Registers control the settings for the SONET/SDH differences (Config 1L) including pointer calculation and evaluation (Config 2L), and the selection and usage of the H4 byte and RAI (Config 1H). In Table 17, the bits are explained.

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Note: If the XSONET setup pin is not connected or if it is tied to high, the SDHT comes up in SDH mode. If XSONET is tied to low, the SONET mode is selected. The mode of operation may be arbitrarily changed by the µP afterwards however. The Configuration Registers are not affected by a software reset.

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Table 17
SDHT Configuration Bit Descriptions (Grouped Bytewise)

Default after HW Reset for:			Description of Bit Function
Name of Config bit	**XSONET low**	**XSONET high/NC**	**Meaning for bit = 1 [Meaning for bit = 0 in square brackets]**
C1US	1	0	C1#2, C1#3 set to 02, 03 [AA, AA]
LOFUS	1	0	LOF becomes active, if OOF persists for at least 3 ms [immediately]
LOSUS	1	0	Release from LOS, if two valid framing patterns have been received after pin SIEIN becomes inactive [immediately, after pin SIEIN becomes inactive]
LAISUS	1	0	Detection / release of MS AIS and MS FERF in 5 frames [3 frames]
K1K2US	1	0	Acceptance of K1K2 in 5 frames [3 frames]
PRAIUS	1	0	Detection / release of P FERF in 10 frames [3 frames]
NUS	1	0	Detection of LOP in 8 frames [9 frames]
UNDEFUS	1	0	Undefined bytes in SOH are set to 0000 0000 [1111 1111]
ENIDLE	1		Enable discarding of physical cells
ATMPTR	0		H4 byte transmitted is pointer to next ATM cell [written by µP]
RAIINH	0		Tx of P FERF due to received R INH (status SERINH) is enabled [disabled]
LOCRAIINH	0		Tx of P FERF due to LOC is disabled [enabled]
ENHEC	1		Enable HEC insertion (Tx) and Header corredtion (Rx)
OCTLVL	0		After TxClav going low, TxFIFO can hold additional 4 bytes [1 byte]
ENUTOPIA	inverted pin SXBMOD		Switch payload interface to UTOPIA
IDLEUS	1	0	As physical cells, use unassignad cells [use idle cells]
ENINVNDF	0		Enable detection of invalid NDF codes
CIEN	0		Evaluation of Concatenation Indication (H1,2#2,3) is enabled [disabled]

Table 17
SDHT Configuration Bit Descriptions (Grouped Bytewise) (cont'd)

Default after HW Reset for:			Description of Bit Function
Name of Config bit	**XSONET low**	**XSONET high/NC**	**Meaning for bit = 1 [Meaning for bit = 0 in square brackets]**
ED	0		Evaluation of dd bits of pointer (bits 5&6 of H1#2,3) is enabled [disabled]
D1	0	1	Value of most significant d bit (for both, generation and evaluation)
D0	0		Value of least significant d bit (for both, generation and evaluation)
ES	0	1	Evaluation of ss bits of pointer (bits 5&6 of H1#1) is enabled [disabled]
S1	0	1	Value of most significant s bit (for both, generation and evaluation)
S0	0		Value of least significant s bit (for both, generation and evaluation)
ATC	0		activates counters of gathering statistics

Table 18
Configuration Registers After a Hardware Reset

SXBMOD	XSONET	CONF2L	CONF1H	CONF1L
L	L	0000 0000	1000 1011	1111 1111
L	H	0001 0110	1000 1010	0000 0000
H	L	0000 0000	1000 1001	1111 1111
H	H	0001 0110	1000 1000	0000 0000

4.5.1 Test Registers, LOS Inhibit

The Test Status Register comprises a subset of the interrupt status bits. In the test mode controlled by the Test Mode Register, the selected on-chip error detectors are forced to trigger, and the resulting status bits are redirected from the Interrupt Status Register to the Test Status Register. For example, the detector of ATM synchronization SSYATM shall be tested. Therefore, SSYATMT in the test mode register has to be set. As a result, in the test status register SSYATME must appear. During the time of test, the respective bit SSYATM in the interrupt status register is disabled, and a loss of ATM synchronization in the real data cannot be detected. As a result of disabling the bit for the status register, the latched status bit is also inhibited, but the respective latched release bit will be set.

The test of SXCB2 has the side effect of generating bit errors which will be counted in the B2 errors second counter and activate signal degrade (status bit SSDB2, depending on the SD threshold).

The test of SXCB3 has the side effect of generating bit errors which will be counted in the B3 errors second counter.

Since the detection of excessive BER is gated with 5 ms (see Figure 26), both detection and release are delayed up to 5 ms after setting or clearing of their related test bit SXCB2T or SCXB3T. Due to the delay of the release, the internal excessive BER state will be still active after the interrupt line is switched back to the interrupt status register, and so, the related interrupt status bit will become set, too.

For the tests of SSYATM, SLOP, and SIXB, there are no side effects on the Status Register: If the test mode bit 2, LOSOFF, is set, the generation of SAISOUT due to SIEIN (signalling LOS) is turned off. This helps to avoid a distortion of the data stream, in ATM mode, by the generation of P–AIS, when an STM–1 loop is closed and the external interface detects a LOS condition. In VC–4 mode, the data stream is not disturbed in any way. If the Test Mode Register bit DISASD is set, automatic laser shutdown occurs after receiving an active SILD signal for 0.5 s.

Note: Unlike the mode and config registers, the test mode registers are reset during a software reset.

Table 19
SDHT Test Mode Bit Descriptions

Name of config-bit	Default after any reset	In case of ...	Description of bit function; Meaning for bit = 1 [Meaning for bit = 0 in square brackets]
SSYATMT	0	-	Test status bit SSYATM (result in test status register bit SSYATME)
ACQPT	0	-	Start acquiring path trace
DISASD	0	-	Disable automatic laser shutdown
SLOPT	0	-	Test status bit SLOP (result in test status register bit SLOPE)
SIXBT	0	-	Test status bit SIXB (result in test status register bit SIXBE)
LOSOFF	0	-	Suppress consequences of LOS (input pin SIEIN) to data flow
SXCB2T	0	-	Test status bit SXCB2 (result in test status register bit SXCB2E)

Table 19
SDHT Test Mode Bit Descriptions (cont'd)

Name of config-bit	Default after any reset	In case of ...	Description of bit function; Meaning for bit = 1 [Meaning for bit = 0 in square brackets]
SXCB3T	0	-	Test status bit SXCB3 (result in test status register bit SXCB3E)
ENERSTXB	1	Local clock	Switch TEATM to Tx octet clock (suppressed during STM 1 loop).
ENSEROFF	0	Laser shut down	Switch serial STM 1 output to all zeroes.
ENERST	1	Local clock	Indicate at pin SSERST* (e.g. for external switching).
ENTXC1	0	Local clock	Switch Tx clock input from TXC0 to TXC1.
LOOPINT	1	Loop	Switch internally [Indicate at output pin SLOOP]
LOOPAIS	1	Loop	Switch nontransparently and output P AIS [Switch transparently]
Z21GEN	1	-	set Z2#1 bit 6 (LSB: bit 8) automatically as remote loop acknowledge [by µP]
Z21EVAL	1	-	enabling the acceptance algorithms for Z2#1

4.6 Performance Monitoring and Alarm Handling

4.6.1 Performance Monitoring

The statistical evaluations are shown in Figure 26.

A very special function is the signal degradation detection:

The detected bit errors (via B2) are accumulated during Ns frames. If the result reaches or exceeds the value L, for M consecutive times, the internal status 'signal degradation' is set. Then, if the result did not reach L, this again for M consecutive times, the internal status 'signal degradation' is reset. The status bit SSDB2 is an indicator for this internal status.

The values Ns, M, L can be programmed by the µP. The bit mapping is from MSB to LSB:

MMMM LLLL | XXXX NNNN | NNNN NNNN | NNNN NNNN; after reset: 35 00 01 04. Thus, the default values are: M=3, L=5, Ns=260. This means a BER threshold of 10-6.

To change one of the values Ns, M or L, use the following procedure:

– Reset the register (M, L) to zero to clear the internal counters and a potentially active signal degrade state;
– Set Ns to its requested value;
– Program the register (M, L) to the required values for M and L.

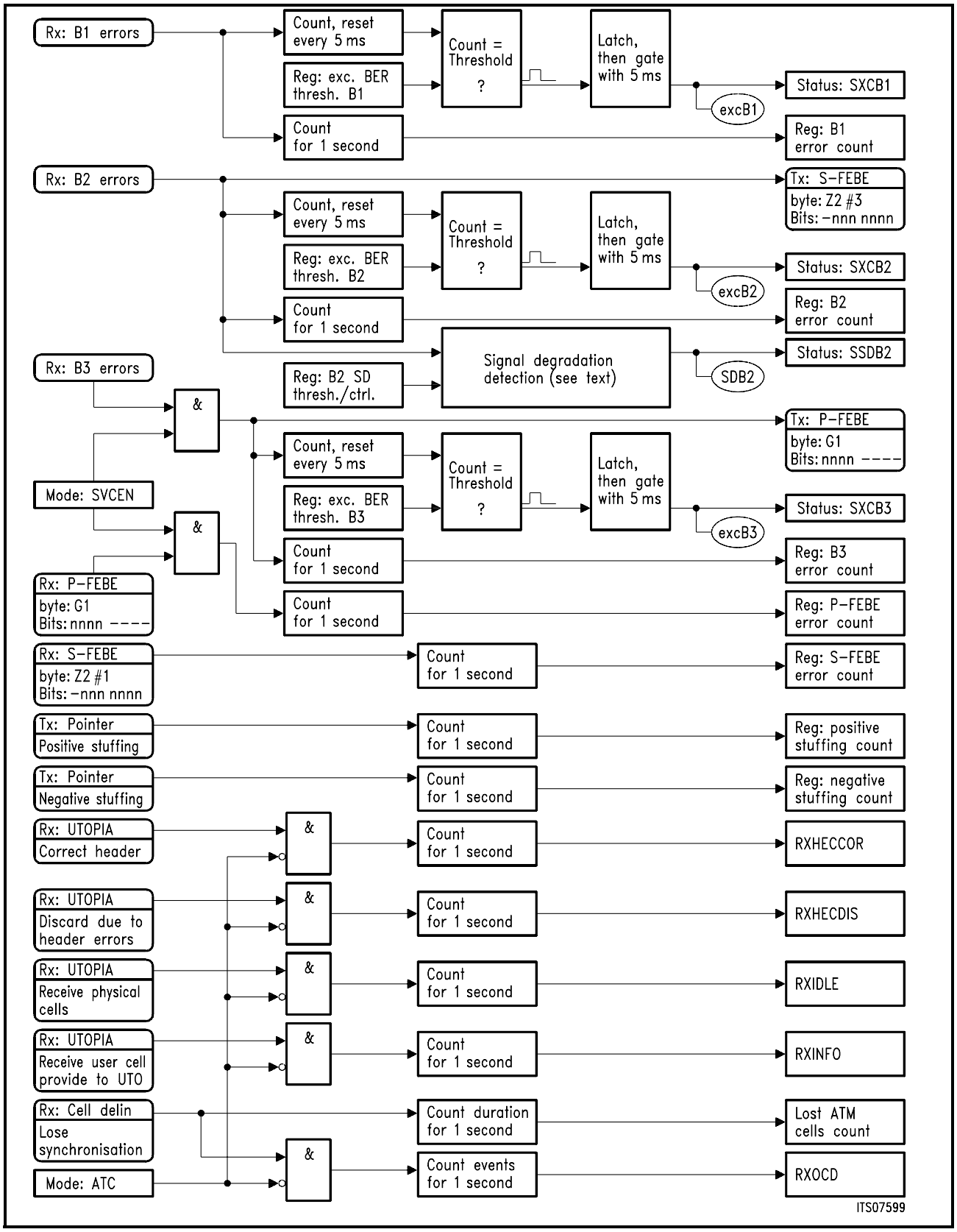

Figure 26
Performance Monitoring

4.6.2 Alarm Handling

The alarm handling is shown in Figure 28. For special functions (e.g. loop) refer to Figure 27.

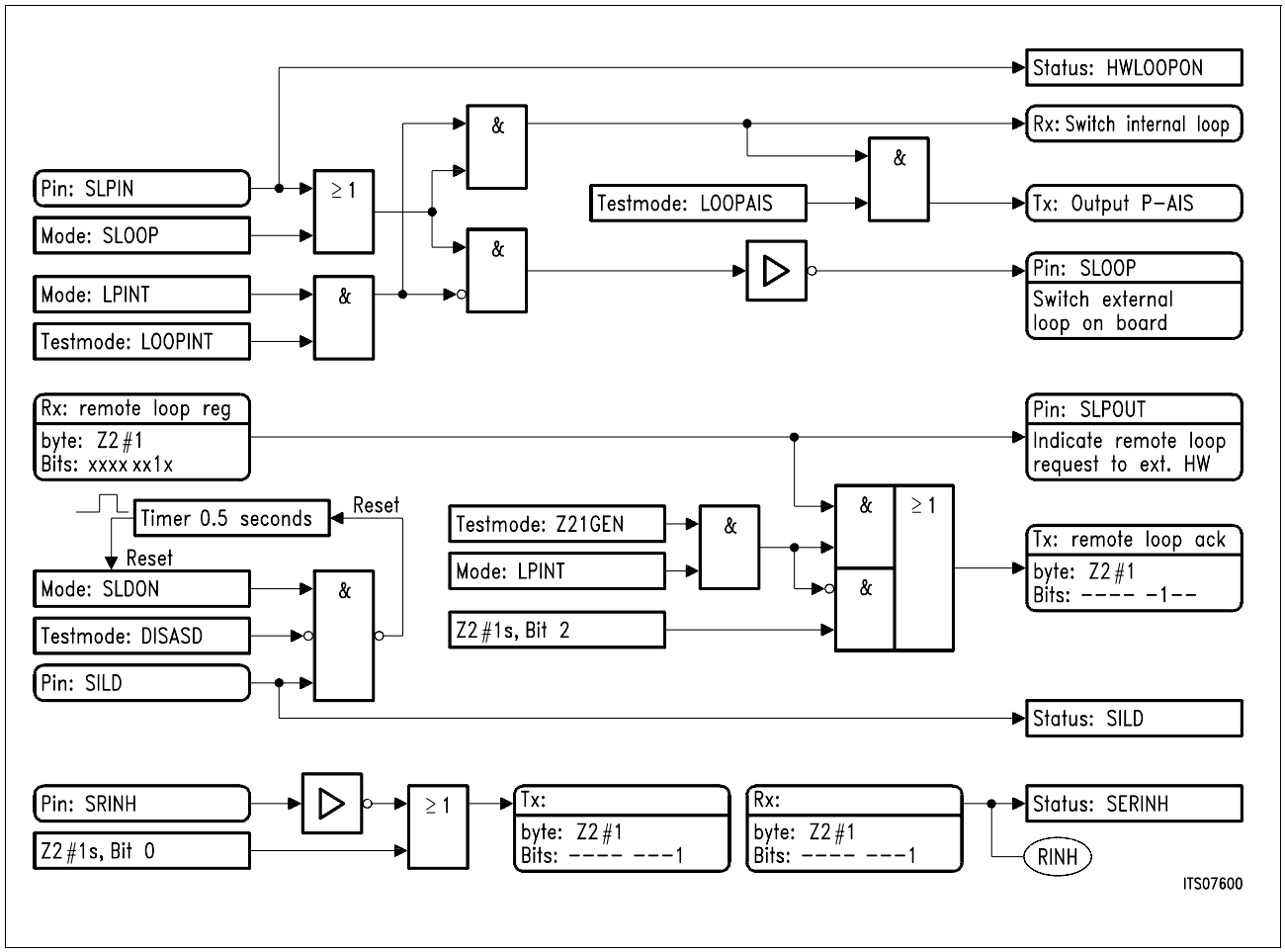

Figure 27
Special OAM Functions

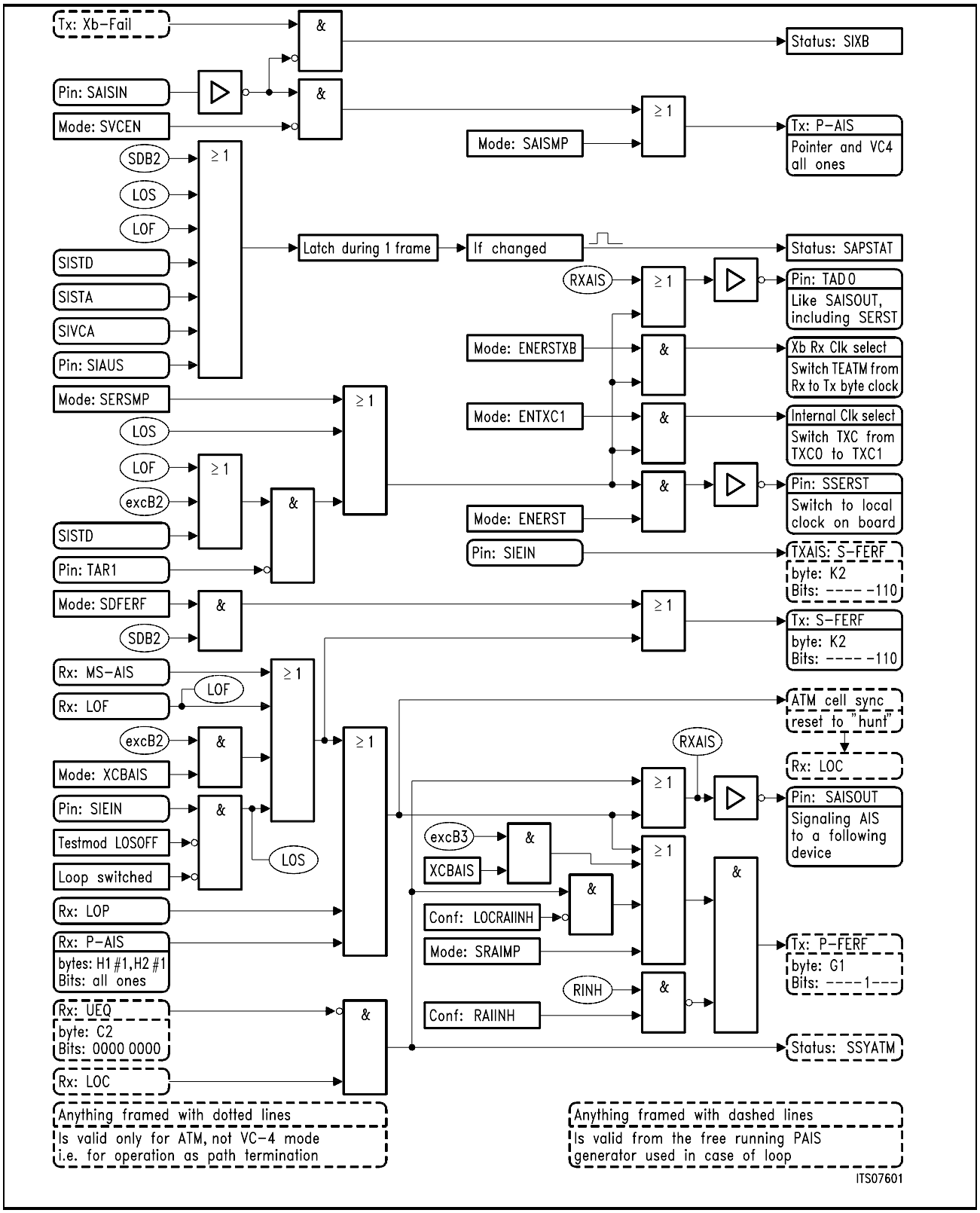

Figure 28
Alarm Handling

Note: Only Status Registers with preprocessing are shown

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 20
Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply Voltage	V_S	3.3V±5%	V
Input Voltage	V_I	-0,5 to 5,5V	V
Output Voltage	V_O	-0.5 to 3.465V	V
Input/Output (bidirectional) Voltage	$V_{I/O}$	-0.5 to 3.465V	V
Ambient temperature under bias: (without forced cooling)	T_A	0 to 70	°C
Maximum Power consumption	P	0.7	W
Storage temperature	T_{stg}	125	°C

The SDHT shows the following electrical characteristics: V_S is 3.3V and Icc is 150mA. The load condition is 0mA at the digital pins (IOH = IOL) and 6mA at the LVDS pads (IOH_LVDS = IOL_LVDS).

Note: Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

5.2 DC Characteristics for for all interfaces except the line interface

The line interface includes OBIAS, IBIAS, ext. Ref and signal pins listed in table 3 without the TRI_AIS and TRI_SDH signal pins

Table 21
DC Characteristics

Symbol	Parameter	Min.	Max.	Conditions
VIL	Input LOW voltage	- 0.3 V	0.8 V	for I and I/O pins
VIH	Input HIGH voltage	2.0 V	5.5 V	for I pins
VIH	Input HIGH voltage	2.0 V	3.465 V	for I/O pins

Table 21
DC Characteristics (cont'd)

Symbol	Parameter	Min.	Max.	Conditions
VOH	Output HIGH voltage	2.4 V		IOH = 8mA @ 2.4 V
VOL	Output LOW voltage		0.5 V	IOL = 8mA @ 0.5 V
IOH	Output current at HIGH voltage	8mA		
IOL	Output current at LOW voltage	8mA		
IIH	Input current at HIGH voltage	66µA	100µA	for I and I/O Pins with internal pull down resistor
			1µA	for I and I/O Pins with internal pull up resistor
IIL	Input current at LOW voltage		1µA	for I and I/O Pins with internal pull down resistor
		66µA	200µA	for I and I/O Pins with internal pull up resistor
ILI	Input leakage current	-1µA	1µA	
ILO	Output leakage current (TRI-STATE output, VO=0 to VDD	-1µA	1µA	

5.3 Line Interface DC characteristics

Table 22
Line Interface DC characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input high voltage	V_{IH}	-	1.9	V
Input low voltage	V_{IL}	0.5	-	V
Input differential voltage	$V_{ID}=V_{IH}-V_{IL}$	0.1	-	V
Output high voltage *)	V_{OH}	1.41	1.535	V
Output low voltage *)	V_{OL}	0.935	1.06	V
Output differential voltage *)	$V_{OD}=V_{OH}-V_{OL}$	0.4	0.55	V

*) Values are adjustable by bias resistor OBIAS. The values given in the table refer to default bias settings of table 18 and result in a higher output voltage swing (V_{OD}) than given in IEEE 1596.3. This is useful for interfacing to a PECL input.

5.4 Capacitances

Table 23
Capacitances

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance	C_{IN}		3	pF
I/O capacitance	$C_{I/O}$		3	pF
Load capacitance (not for LVDS Output)	C_{Load}		120	pF

5.5 AC Characteristics

T_A = 0 to 70 °C , V_{CC} = 3.3 V ± 5 % , V_{SS} = 0 V

All inputs are driven to V_{IH} = 2.4 V for a logical “1”
and to V_{IL} = 0.4 V for a logical “0”

All outputs are measured at V_H = 2.0 V for a logical “1”
and at V_L = 0.8 V for a logical “0”

The AC testing input/output waveforms are shown below.

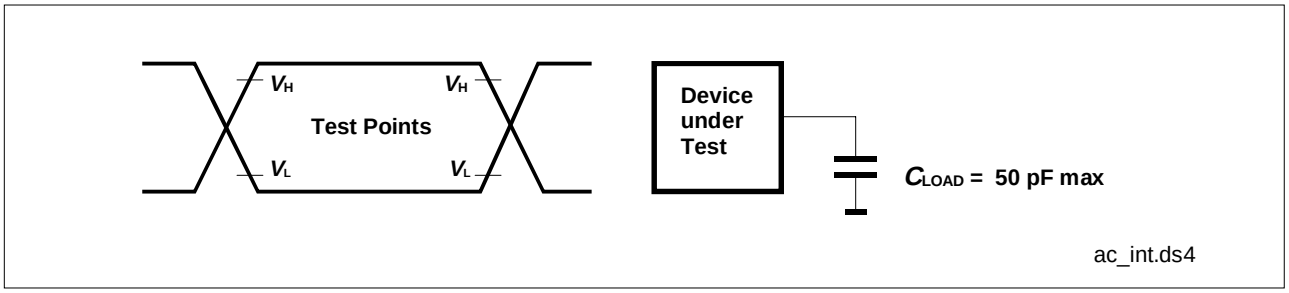

Figure 29
Input/Output waveform for AC measurements

5.6 AC Characteristics of the Line Interface

The timing of the serial STM-1 line interface is described in the following figure and table:

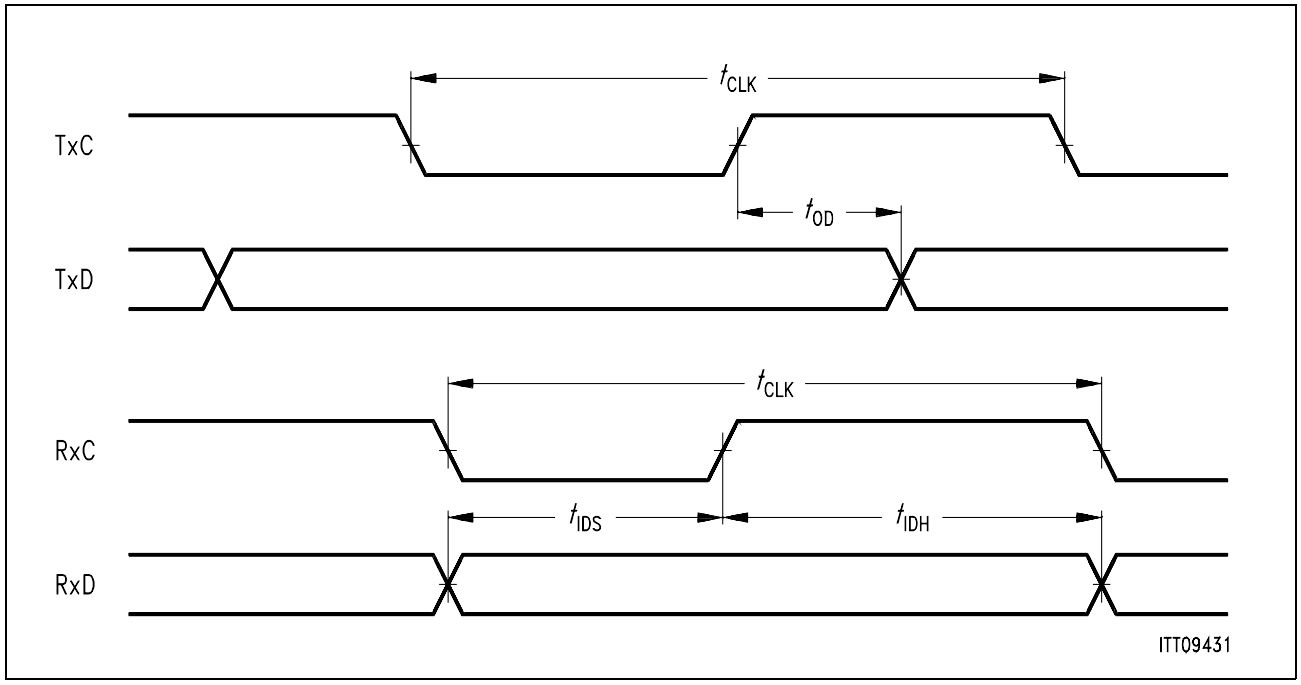

Figure 30
Line interface timing diagram

Table 24
Line interface timing characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
RxD input data setup	t_{IDS}	1.5	-	ns
RxD input data hold	t_{IDH}	0.5	-	ns
TxD output delay to TXC	t_{OD}		1.5	ns

5.7 UTOPIA AC Values

The timing requirements for UTOPIA receive and transmit directions for 33 MHz, 8-bit bus are given in the Tables 26 and 29.

Table 25 displays the general conditions for UTOPIA timing.

Table 25
General Conditions on UTOPIA Interface Timing

Parameter	Typ.	Min.	Max.
Input capacitance of input or input/output signal	10 pF		
Input and output timing reference level	1.4 V		
Input and output timing reference level	1.4 V		

Table 26
AC Characteristics of UTOPIA Interface

Signal name	Direction	Description	Min.	Max.
AtmClk	A=>P	AtmClk frequency (nominal)	0	33 MHz
		AtmClk duty cycle	40 %	60%
		AtmClk peak-to-peak jitter (Note 1)	-	5 %
		AtmClk rise/fall time (Note 2)	-	3 ns
TxData[7–0]	A=>P			
TxSOC				
TxEnb*	A=>P	Input setup to AtmClk	8 ns	-
TxClav	A<=P	Input setup to AtmClk	8 ns	-
		Input hold from AtmClk	1 ns	-
		Signal going low impedance to AtmClk	10 ns	-
		Signal going high impedance to AtmClk	10 ns	-
		Signal going low impedance from AtmClk	1 ns	-
		Signal going high impedance from AtmClk	1 ns	-

Table 26
AC Characteristics of UTOPIA Interface (cont'd)

Signal name	Direction	Description	Min.	Max.
RxData[7–0]	A<=P	Input setup to AtmClk	8 ns	-
RxSOC		Signal going low impedance to AtmClk	10 ns	-
		Signal going high impedance to AtmClk	10 ns	-
		Signal going low impedance from AtmClk	1 ns	-
		Signal going high impedance from AtmClk	1 ns	-
RxEnb*	A=>P	Input setup to AtmClk	8 ns	-
RxClav	A<=P	Input setup to AtmClk	8 ns	-
		Input hold from AtmClk	1 ns	-
		Signal going low impedance to AtmClk	10 ns	-
		Signal going high impedance to AtmClk	10 ns	-
		Signal going low impedance from AtmClk	1 ns	-
		Signal going high impedance from AtmClk	1 ns	-

The most criticial parameter in Table 26 is the hold time of 1 ns. This is outlined in Figure 31. The worst case propagation delay for the signals on the interconnection lines could be zero. Therefore the chips must guarantee a minumum propagation delay (min-delay in Figure 31) from the clock input to the resulting data change at the outputs.

Note 1: measured from one rising edge to the next rising edge

Note 2: measured at transmit side (driver), unloaded, between 10% and 90% / 90% and 10% levels of VOH

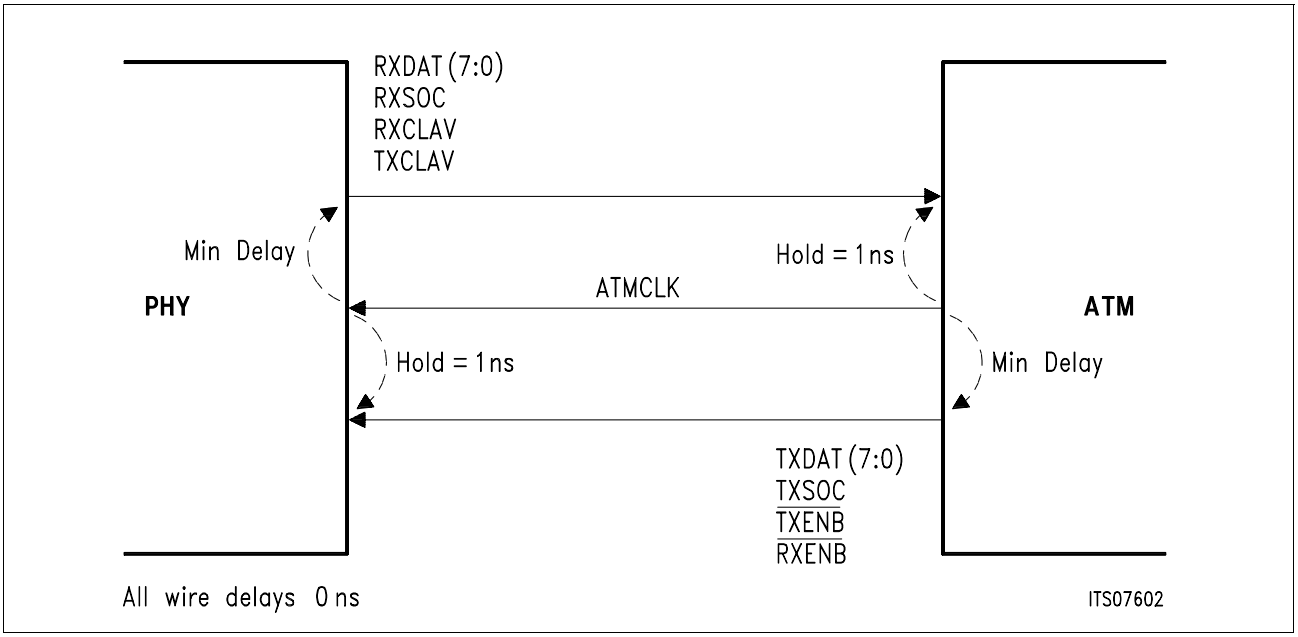

Figure 31
Timing Relationship for UTOPIA Signals

5.8 AC Characteristics of JTAG Interface

The timing of the JTAG interface is described in the following figure and table:

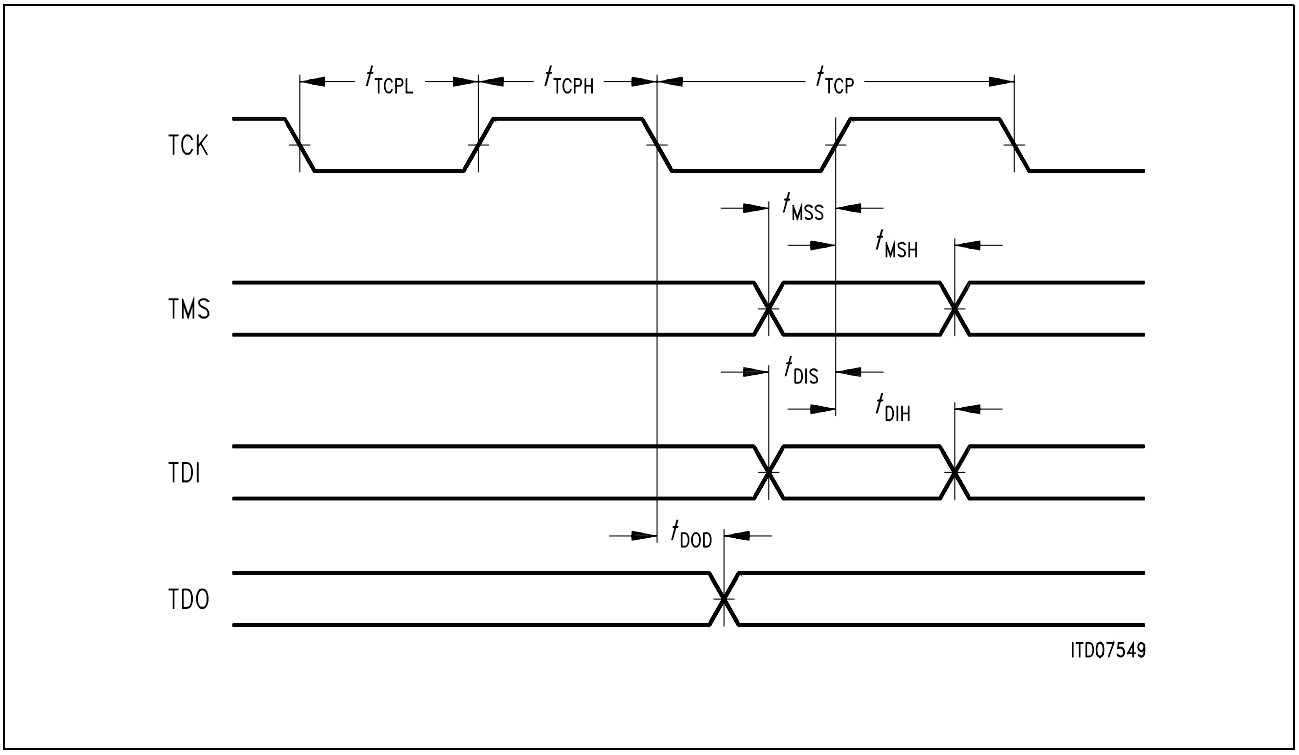

Figure 32
JTAG interface timing diagram

Table 27
JTAG interface timing characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Test clock period	t_{TCP}	250		ns
Test clock period low	t_{TCPL}	120		ns
Test clock period high	t_{TCPH}	120		ns
TMS setup time to TCK	t_{MSS}	120		ns
TMS hold time to TCK	t_{MSH}	120		ns
TDI setup time to TCK	t_{DIS}	120		ns
TDI hold time from TCK	t_{DIH}	120		ns
TDO valid delay from TCK	t_{DOD}		15	ns

5.8.1 Microprocessor Timings

The address timing is shown in Figure 33, and the data timings in Figures 34 and 30. The capacitive load should not exceed 100 pF at any output of the microprocessor interface. If the load is moderately higher than 100 pF, add 1 ns for each 10 pF to the data output delay. The input load comprises a capacity below 16 pF and pull-down resistor of typical 50 kOhms (20–140 kOhm).

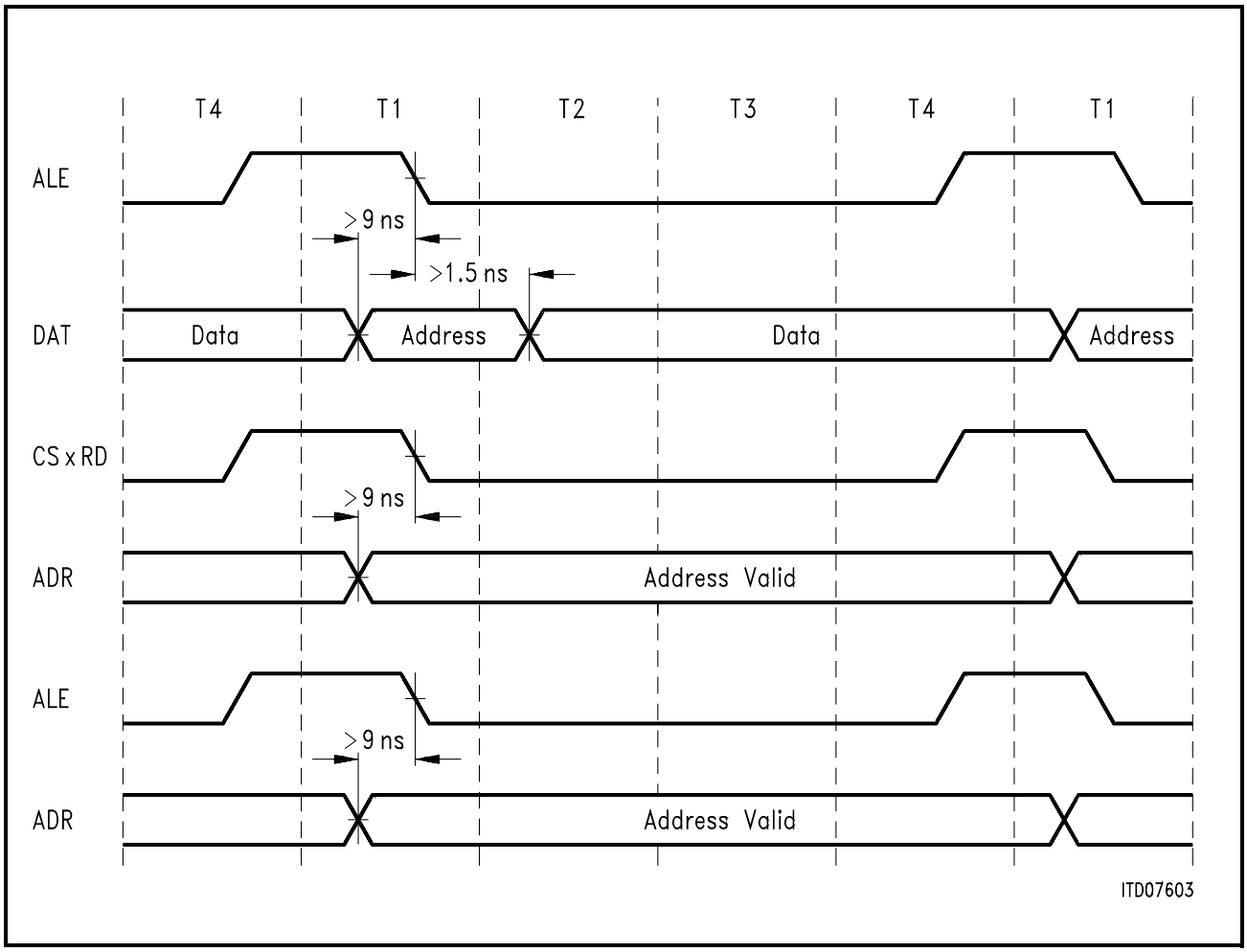

Figure 33
SDHT Address Setup and Hold Times

top: multiplexed AD bus or separated buses with ALE used;

middle: separated buses with ALE not used

bottom: separated buses with ALE used

The minimum write cycle time (CS + WR is active low) should be at least 100ns.

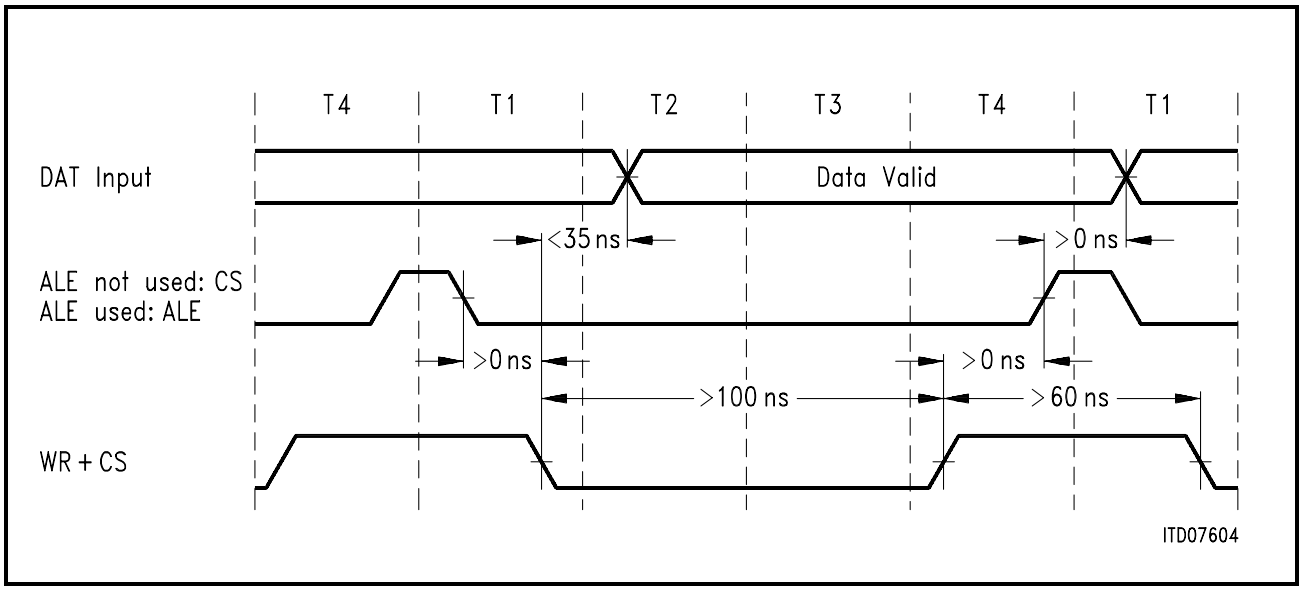

Figure 34
SDHT Write CycleTiming (setup, hold, pulse width)

The minimum inactive read cycle time (CS + RD is inactive high) between two successive read operation should be greater than 60ns.

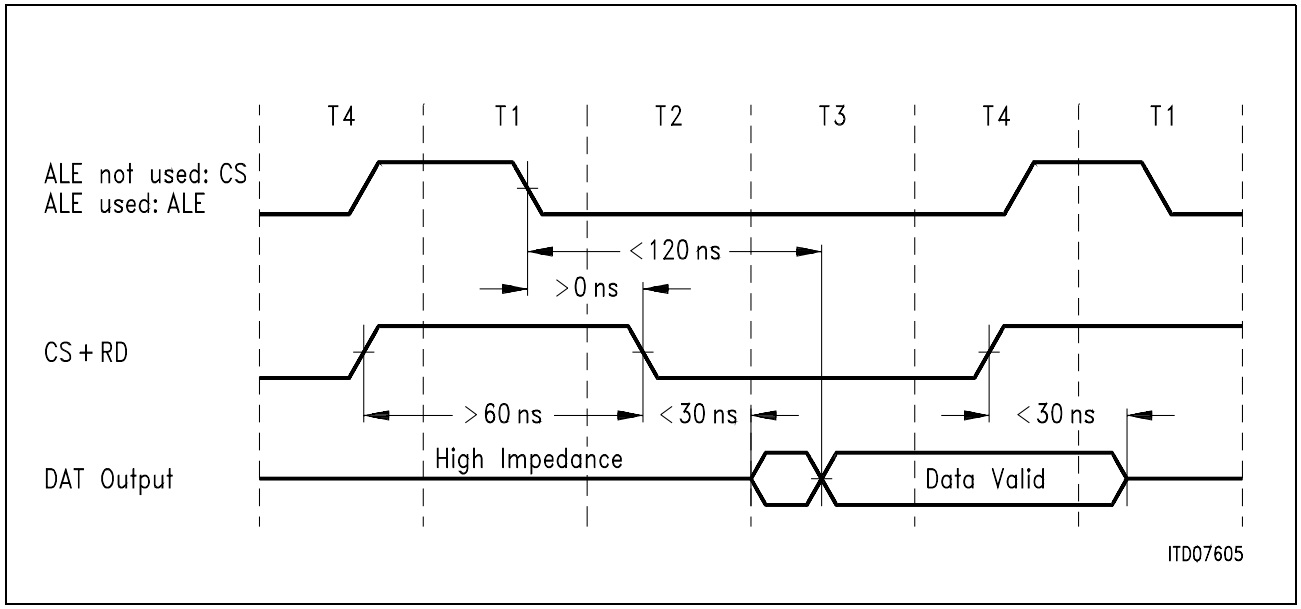

Figure 35
SDHT Read Cycle Timing (CS ->RD setup; others delay)

6 Packaging Outline

The SDHT is packaged in a 160–pin plastic quad flat package.

P-MQFP-160-1
(Plastic Metric Quad Flat Package)

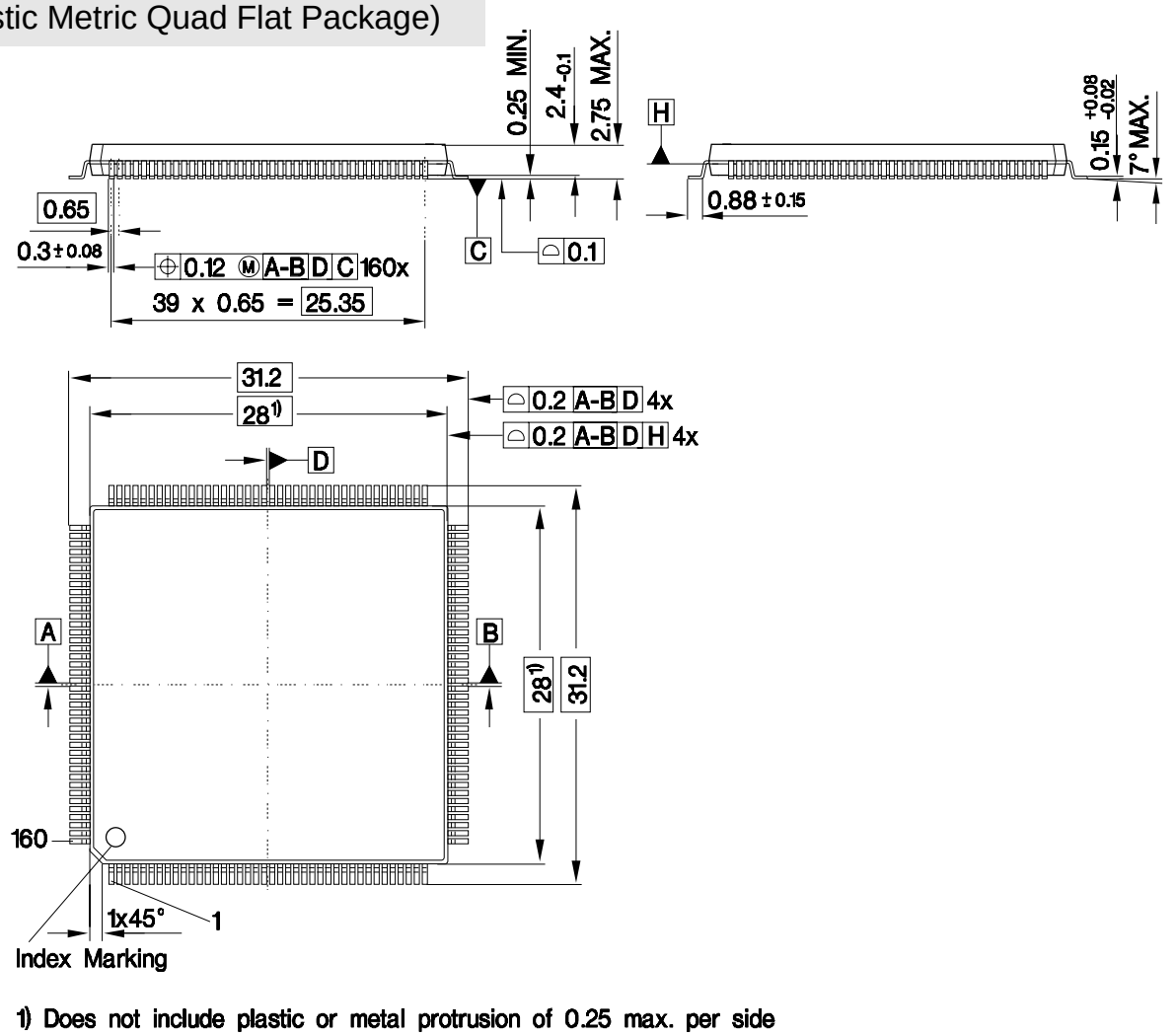

Figure 36
SDHT package (shown from side and from top).

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm

7 Appendices

7.1 SDH Versus SONET Terminology

Table 28 Terminology Comparison for SDH and SONET

SDH (ITU)	SONET (Bellcore/ANSI)
STM-1	STS–3c
SOH = R-SOH + M-SOH	TOH = SOH + LOH
MS-AIS, MS-FERF, MS-FEBE, P-FERF, P-FEBE	L-AIS, L-RDI, L-FEBE, P-RDI, P-FEBE
AU-4 pointer	Payload Pointer
VC-4, POH	SPE, POH
C-4 (= VC-4 without POH)	Payload Capacity
The AU-4 pointer does not logically belong to the SOH.	The payload pointer logically belongs to the LOH
AU-4 (= VC-4 + AU pointer)	no equivalent

7.2 References

Table 29 References

[UNI 3.1]	The ATM Forum, "ATM User-Network Interface Specification," Version 3.1, July 21, 1994
[I.432]	ITU-T Recommendation I.432, "B-ISDN User-Network Interface—Physical Interface Specification," June 1992
[I.610]	ITU-T Recommendation I.610, “B-ISDN Operation and Functions,” June 1992
[G.78X]	ITU-T Recommendation G.781-784,
[ANSI-T1]	ANSI T1E1.2/93-020, “Broadband ISDN—Customer Installation Interfaces Physical Media Dependent Specification, Draft, June 1993
[G.738]	ITU-T Recommendation G.738,
[G.70x]	ITU-T Recommendation G.70x, "Network Node Interface for the Synchronous Digital Hierarchy," (merged version, in COM 15, R22E), June 21, 1994

Table 29 References (cont'd)

[ANSI-SDH]	ANSI T1.105a-1991, "Digital Hierarchy —Supplement to Optical Interface Rates and Formats Specifications (SONET)"—Draft, May 7, 1991
[ANSI-ATM]	ANSI T1E1.2/94-002R1, "Broadband ISDN and DS1/ATM User-Network Interfaces: Physical Layer Specification,"
[TR_253]	Bellcore TR-NWT-000253, "Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria", December 1991
[TA_1112]	Bellcore TA-NWT-001112, "Broadband ISDN–User to Network Interface and Network Node Interface: Physical Layer Generic Criteria", July 1993
[UTOP_1]	"UTOPIA, An ATM–PHY Interface Specification," Level 1, Version 2.01, March 21, 1994
[UTOP_2]	"UTOPIA, An ATM–PHY Interface Specification," Level 2, Version 0.8, April 10, 1995
[JTAG]	Joint Test Action Group JTAG Boundary Scan Standard, IEEE 1149.1
[LVDS]	IEEE Std 1596.3-1994, "IEEE Standard for Low–Voltage Differential Signals for SCI (LVDS)", Draft 1.00, December 30, 1993

7.3 Acronyms

Table 30 Acronyms

AAL	ATM Adaptation Layer
AIS	Alarm Indication Signal
ANSI	American National Standards Institute
ASP	ATM Switch Preprocessor, Siemens chip, PXB 43201/2
ATM	Asynchronous Transfer Mode
AU–4	Administrative Unit Type 4
BER	Bit Error Rate
BIP-n	Bit Interleaved Parity, n bits
C-4	SDH Container 4
CCITT	Consultative Committee on International Telephone and Telegraph, part of ITU
CI	Concatenation Indication
CRC	Cyclic Redundancy Check

Table 30 Acronyms (cont'd)

FAP	Frame Alignment Pattern
FEBE	Far End Block Error
FERF	Far End Receive Failure
HDLC	High level Data Link Control
HEC	Header Error Check/Control
IEEE	Institute for Electrical and Electronic Engineers
ITU-T	International Telecommunications Union– Telecommunication Section
J1	First byte of the VC-4; first octet in SPE
JTAG	Joint Test Action Group (creators of the Boundary Scan)
L-	concerning the Line (ANSI equivalent of ITU's multiplexer section)
LOH	Line OverHead
LOS	Loss Of Signal
LVDS	Low Voltage Differential Signal IEEE Draft specification 1596.3
M-SOH	Multiplexer Section OverHead
MS-	concerning the Multiplexer Section (CCITT equivalent to ANSI's line)
NT-1	Network Termination Type 1
OAM	Operation and Maintenance function
P-	concerning the Path
PHY	Physical Layer, Layer 1 of the OSI Model
PN	Pseudo Noise (=pseudo random)
POH	Path OverHead
R-INH	Remote INHibit (=power fail at far end)
RAI	Remote Alarm Indication
RDI	Remote Defect Indication
RIB2	Redundant Interface Board 2
R SOH	Regenerator Section OverHead
SARE	Segmentation and Reassembly Element, Siemens chip, PXB 4110
SD	Signal Degradation
SDHT	Synchronous Digital Hierarchy Transceiver, Siemens chip, PXB 4240
SLMB	Subscriber Line Module Broadband
SLT	Subscriber Line Termination

Table 30 Acronyms (cont'd)

SOC	Start Of Cell
SOH	Section OverHead
SONET	Synchronous Optical NETwork
SPE	Synchronous Payload Envelope
STM-1	Synchronous Transport Mode 1, 155–Mbit/s
STS-3c	Synchronous Transport System, Level 3, concatenated payload
TA	Terminal Adapter
TF	Transmission Failure
TOH	Transmission OverHead
UEQ	UnEQuipped (=no ATM source connected)
UTOPIA	Universal Test and Operations Physical Interface for ATM
UTPT	Unshielded Twisted Pair Transceiver, Siemens chip, PXB 4230
VC-4	Virtual Container 4
VCC	Virtual Channel Connection
VDD	Connection to positive power supply
VSS	Connection to ground