SONET/SDH/ATM OC-12 QUAD TRANSCEIVER S3038

FEATURES

- Complies with Bellcore and ITU-T specifications
- Supports 622.08 Mbps (OC-12)
- Quad transmitter incorporating phase-locked loop (PLL) clock synthesis from a low speed reference clock
- Quad receiver PLL provides clock and data recovery
- Selectable reference frequencies of 38.88 MHz, or 77.76 MHz
- Interface to both LVPECL and TTL logic
- 8-bit TTL datapath
- Compact 23mm x 23mm 208 TBGA package
- Diagnostic loopback mode
- Low jitter LVPECL interface
- Single 3.3V supply
- Local Loopback

APPLICATIONS

- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

GENERAL DESCRIPTION

The S3038 SONET/SDH Quad transceiver chip is a fully integrated serialization/deserialization SONET OC-12 (622.08 Mbit/s) interface device. The chip performs all necessary serial-to-parallel and parallel-to-serial functions in conformance with SONET/SDH transmission standards. The device is suitable for SONET-based ATM applications. Figure 1 shows a typical network application.

On-chip clock synthesis is performed by the high-frequency phase-locked loop on the S3038 Quad transceiver chip allowing the use of a slower external transmit clock reference. Clock recovery is performed on the device by synchronizing its on-chip VCO directly to the incoming data stream. The S3038 also performs SONET/SDH frame detection. The chip can be used with a 38.88 MHz, or 77.76 MHz reference clock, in support of existing system clocking schemes.

The low jitter LVPECL interface guarantees compliance with the bit-error rate requirements of the Bellcore and ITU-T standards. The S3038 is packaged in a 23mm x 23mm 208 TBGA.

Figure 1. System Block Diagram

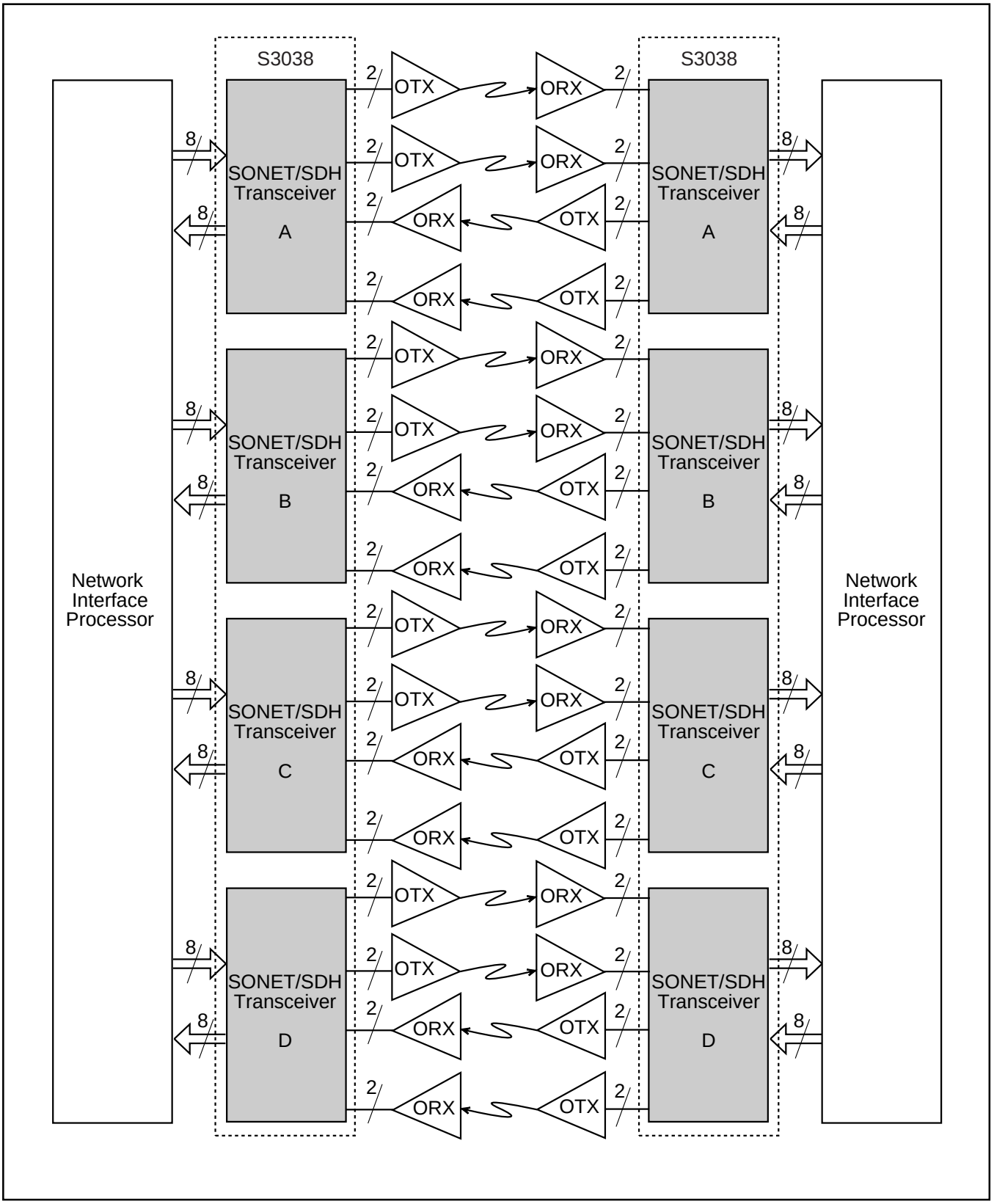


Figure 2. S3038 Input/Output Diagram

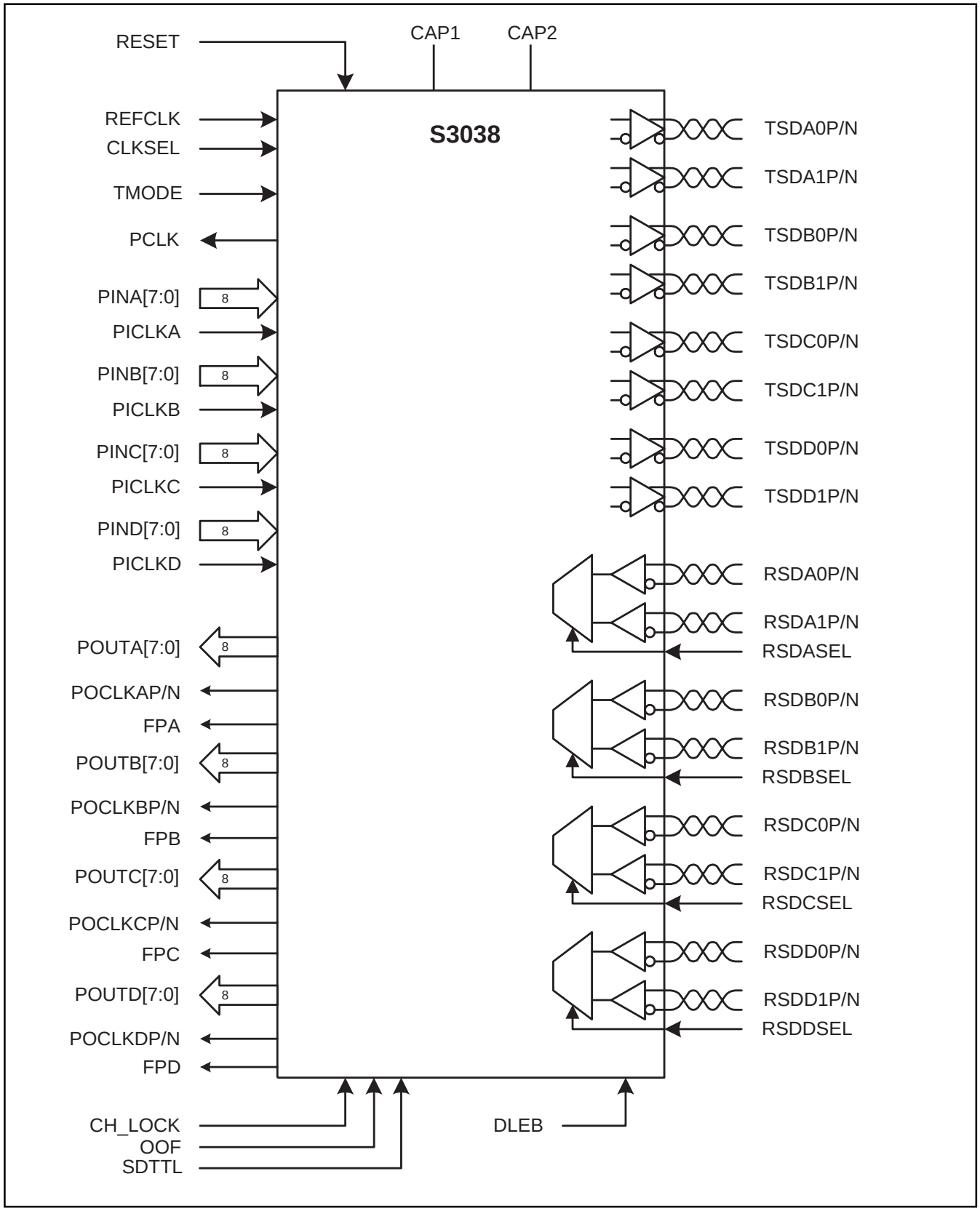


Figure 3. Transmitter Block Diagram

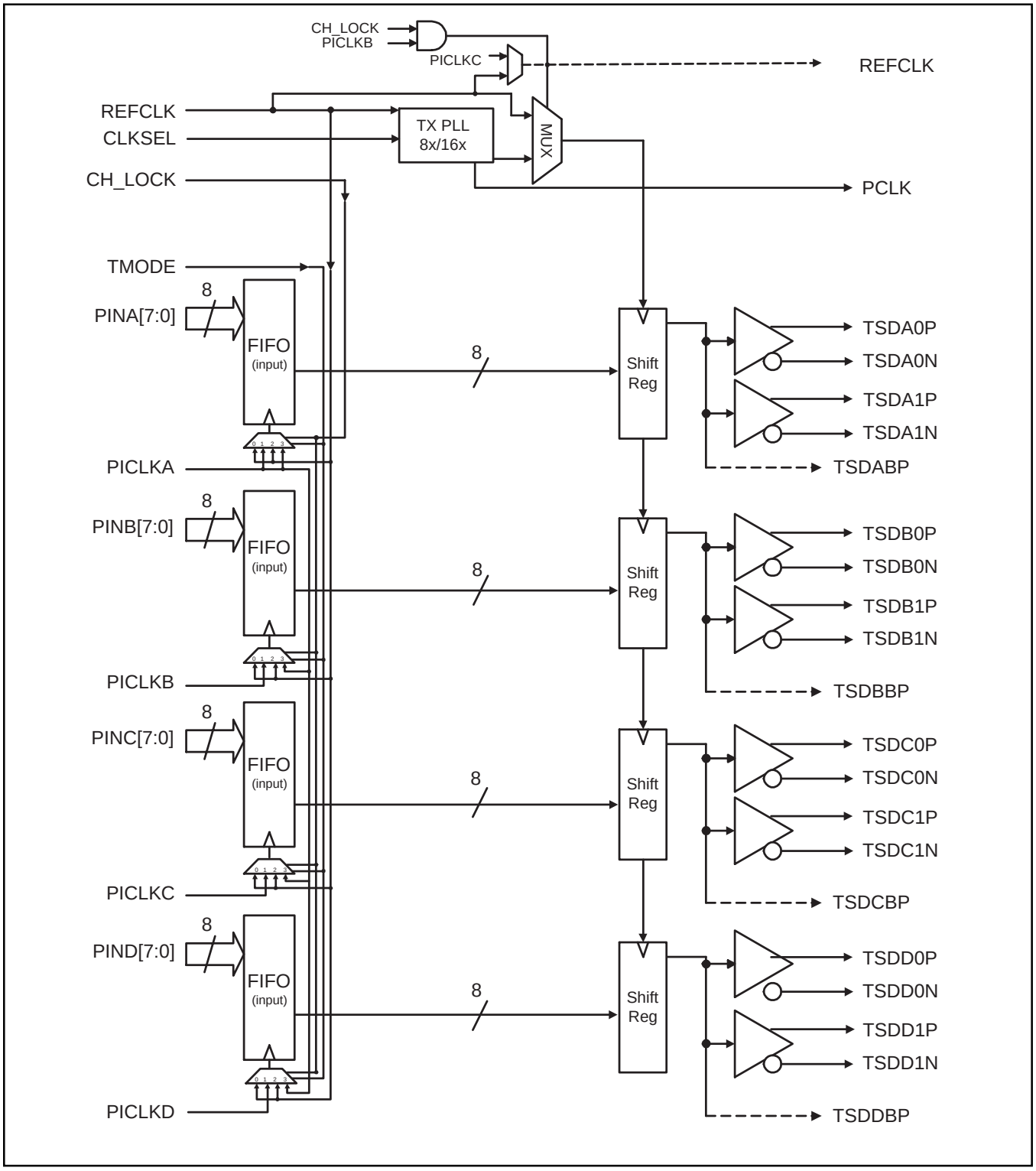
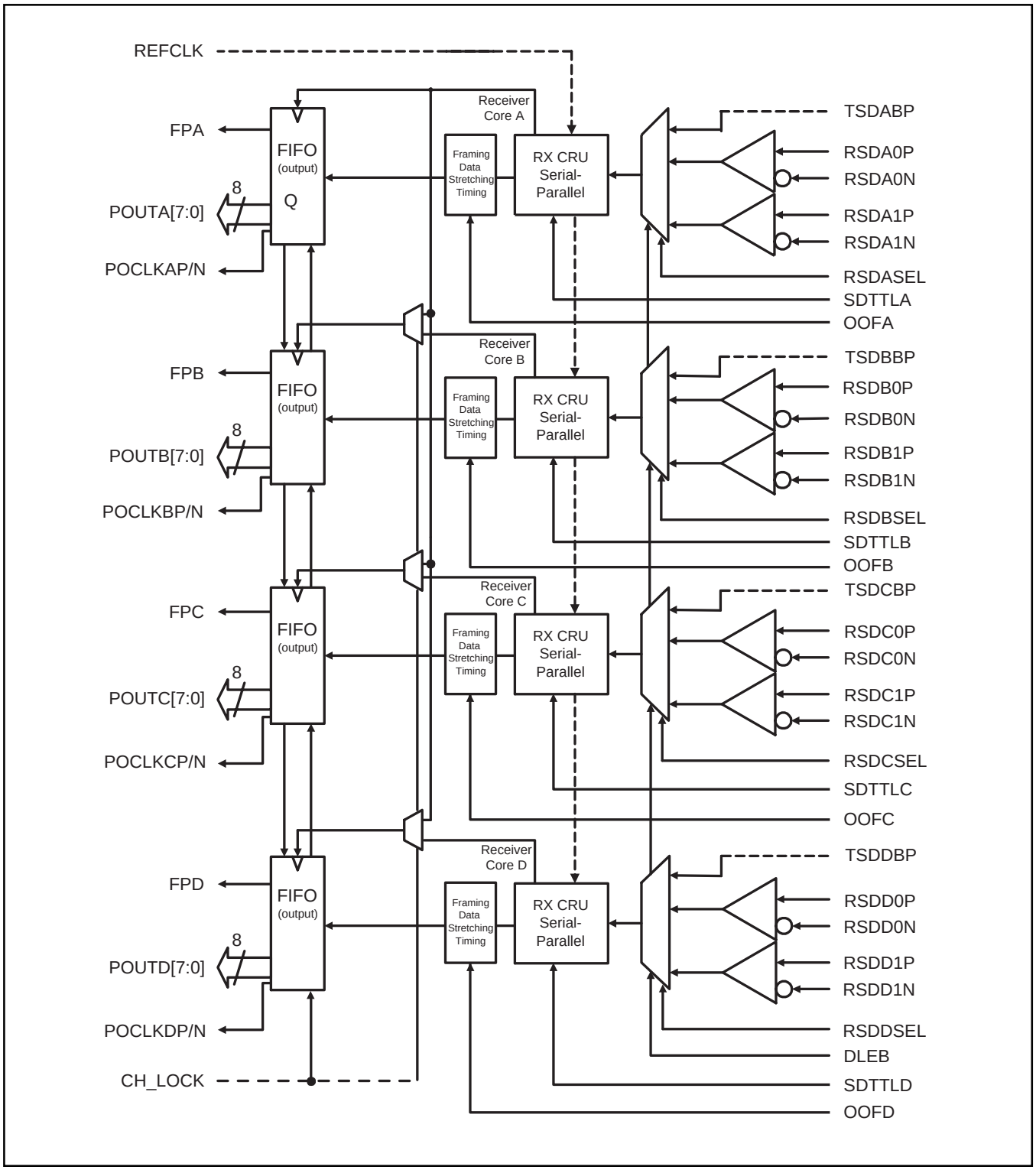


Figure 4. Receiver Block Diagram



SONET OVERVIEW

Synchronous Optical Network (SONET) is a standard for connecting one fiber system to another at the optical level. SONET, together with the Synchronous Digital Hierarchy (SDH) administered by the ITU-T, forms a single international standard for fiber interconnect between telephone networks of different countries. SONET is capable of accommodating a variety of transmission rates and applications.

The SONET standard is a layered protocol with four separate layers defined. These are:

- Photonic
- Section
- Line
- Path

Figure 5 shows the layers and their functions. Each of the layers has overhead bandwidth dedicated to administration and maintenance. The photonic layer simply handles the conversion from electrical to optical and back with no overhead. It is responsible for transmitting the electrical signals in optical form over the physical media. The section layer handles the transport of the framed electrical signals across the optical cable from one end to the next. Key functions of this layer are framing, scrambling, and error monitoring. The line layer is responsible for the reliable transmission of the path layer information stream carrying voice, data, and video signals. Its main functions are synchronization, multiplexing, and reliable transport. The path layer is responsible for the actual transport of services at the appropriate signaling rates.

Data Rates and Signal Hierarchy

Table 1 contains the data rates and signal designations of the SONET hierarchy. The lowest level is the basic SONET signal referred to as the synchronous transport signal level-1 (STS-1). An STS-*N* signal is made up of *N* byte-interleaved STS-1 signals. The optical counterpart of each STS-*N* signal is an optical carrier level-*N* signal (OC-*N*). The S3038 chip supports OC-12 rates (622.08 Mbps).

Frame and Byte Boundary Detection

The SONET/SDH fundamental frame format for STS-12 consists of 36 transport overhead bytes followed by Synchronous Payload Envelope (SPE) bytes. This pattern of 36 overhead and 1044 SPE bytes is repeated nine times in each frame. Frame and byte boundaries are detected using the A1 and A2 bytes found in the transport overhead. (See Figure 6.)

For more details on SONET operations, refer to the Bellcore SONET standard document.

Figure 5. SONET Structure

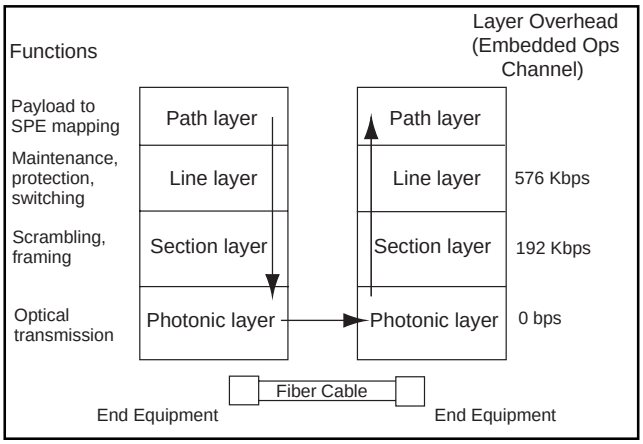
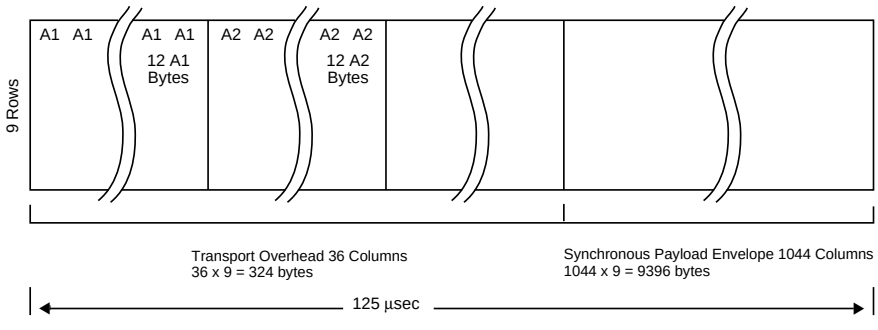


Table 1. SONET Signal Hierarchy

Elec.	CCITT	Optical	Data Rate (Mbps)
STS-1		OC-1	51.84
STS-3	STM-1	OC-3	155.52
STS-12	STM-4	OC-12	622.08
STS-24	STM-8	OC-24	1244.16
STS-48	STM-16	OC-48	2488.32

Figure 6. STS–12/OC–12 Frame Format



S3038 OVERVIEW

The S3038 quad transceiver implements SONET/SDH serialization/deserialization, transmission, and frame detection/recovery functions. This chip can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation and recovery, and system timing. The system timing circuitry consists of management of the datastream, framing, and clock distribution throughout the front end.

The S3038 is divided into a transmitter section and a receiver section. The sequence of operations is as follows:

Transmitter Operations:

1. 8-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver Operations:

1. Clock and data recovery from serial input
2. Frame detection
3. Serial-to-parallel conversion
4. 8-bit parallel output

Internal clocking and control functions are transparent to the user.

FUNCTIONAL DESCRIPTION

QUAD TRANSMITTER OPERATION

The S3038 quad transceiver chip performs the serializing stage in the processing of a transmit SONET STS-12 bit serial data stream. It converts the 8-bit parallel 77.76 Mbyte/sec data stream into a bit serial format at 622.08 Mbps.

A high-frequency bit clock can be generated from a 77.76 MHz frequency reference by using an integral frequency synthesizer consisting of a phase-locked loop circuit with a divider in the loop.

Diagnostic loopback is provided (transmitter to receiver). See Other Operating Modes.

Clock Synthesizer

The clock synthesizer is a monolithic PLL that generates the serial output clock phase synchronized with the input reference clock (REFCLK).

The REFCLK input must be generated from a crystal oscillator which has a frequency accuracy that meets the value stated in Table 11 in order for the TSCLK frequency to have the same accuracy required for operation in a SONET system. Lower accuracy crystal oscillators may be used in applications less demanding than SONET/SDH.

The on-chip PLL consists of a phase detector, which compares the phase relationship between the VCO output and the REFCLK input, a loop filter which converts the phase detector output into a smooth DC voltage, and a VCO, whose frequency is varied by this voltage.

The loop filter generates a VCO control voltage based on the average DC level of the phase discriminator output pulses. A single external clean-up capacitor is utilized as part of the loop filter. The loop filter's corner frequency is optimized to minimize output phase jitter.

Table 2. Reference Frequency Options

CLKSEL	REFERENCE CLOCK FREQUENCY	OPERATING MODE
1	38.88 MHz	STS-12
0	77.76 MHz	STS-12

Timing Generator

The timing generation function provides an 8-bit parallel rate version of the transmit serial clock. This circuitry also provides an internally generated load signal, which transfers the PIN[7:0] data from the parallel input register to the serial shift register.

The PCLK output is an 8-bit parallel rate version of the transmit serial clock at 77.76 MHz. PCLK is intended for use as an 8-bit parallel clock for upstream multiplexing and overhead processing circuits. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the data coming into and leaving the S3038 device.

Parallel-to-Serial Converter

The parallel-to-serial converter is comprised of two 8-bit parallel registers. The first register latches the data from the PIN[7:0] bus on the rising edge of PICLK. The second register is a parallel loadable shift register which takes its parallel input from the first register.

The load signal, which latches the data from the parallel to the serial shift register, has a fixed relationship to PCLK. If PICLK is tied to PCLK, the PIN[7:0] data latched into the parallel register will meet the timing specifications with respect to the load signal. If PICLK is not tied to PCLK, the delay must meet the timing requirements.

Redundant Outputs

Two high-speed differential outputs are provided for each channel. This enables each channel to drive a primary and secondary switch fabric for SONET applications in which redundancy is required to achieve higher reliability.

Routing of Signals for Channel-Lock Operation

When operating in the Channel Lock (CH_LOCK) Mode, the user must ensure that the path length of the four high-speed serial data signals are matched to within ±3 ns of delay. Failure to meet this requirement may result in bit errors in the received data or in byte misalignment.

Table 3. Reference Jitter Limits

Maximum Reference Clock Jitter in 12 kHz to 5 MHz Band	Operating Mode
14 ps rms	STS–12

The following figures illustrate the broad range of transmit data clocking options supported by the S3038.

Figure 7 demonstrates the flexibility afforded by the S3038. A low jitter reference is provided directly to the S3038 at either 1/8 or 1/16 the serial data rate. This ensures minimum jitter in the synthesized clock used for serial data transmission. A system clock output at the 32-bit parallel rate, PCLK, is derived from the PLL and provided to the upstream circuit as a system clock. This clock can be buffered as required without concern about added delay. There is no phase requirement placed upon PCLK and the PICLKx clock, which is provided back to the S3038, other than that they remain within ±3 ns of the phase relationship established at reset.

The S3038 also supports the traditional REFCLK clocking and is illustrated in Figure 8. This approach imposes significant challenges in maintaining timing margins on the designer.

Figure 7. PIN Data Clocking with PICLK

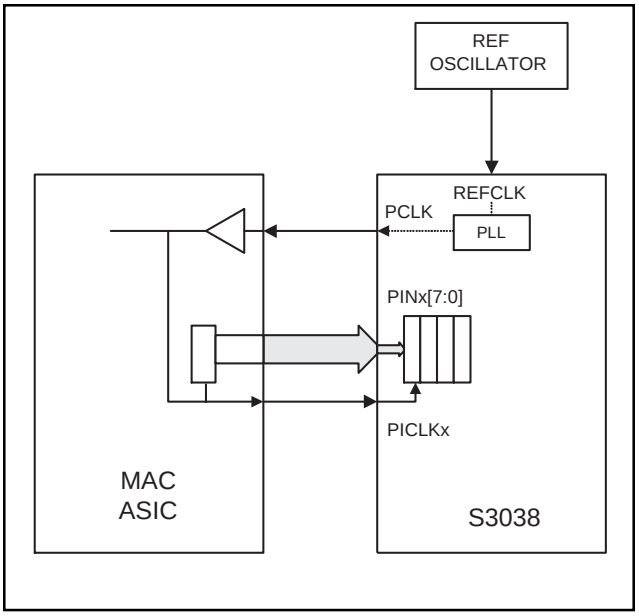
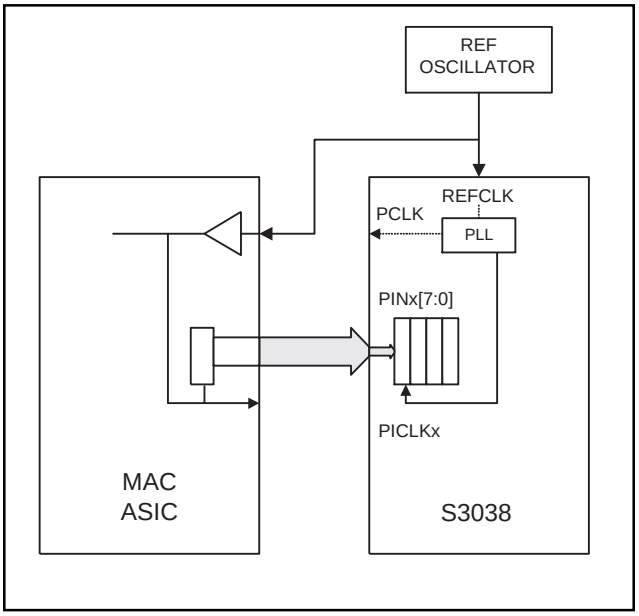


Figure 8. REFCLK Forward PIN Clocking



RECEIVER OPERATION

The S3038 quad transceiver chip provides the first stage of digital processing of a receive SONET STS-12 bit-serial stream. It converts the bit-serial 622.08 Mbps data stream into a 77.76 Mbyte/sec 8-bit parallel data format.

Data Input

Two differential receivers are provided for each channel of the S3038. This supports switching between redundant switch fabrics for SONET applications. A select signal RSDSEL is provided for each channel to control the selection of primary or secondary inputs. In addition, each channel supports a diagnostic loopback mode in which the serial data from the transmitter replaces external serial data. The loopback functions for all four channels is controlled by a single Diagnostic Loopback Enable (DLEB) signal.

Clock recovery is performed on the incoming scrambled NRZ data stream. A 77.76 MHz reference clock is required for phase locked loop start-up and proper operation under loss of signal conditions. An integral prescaler and phase locked loop circuit is used to multiply this reference to the nominal bit rate.

A loopback mode is provided for diagnostic loopback (transmitter to receiver).

Clock Recovery

Clock recovery generates a clock that is at the same frequency as the incoming data bit rate at the RSD input or, in loopback, the transmitter data output. The clock is phase aligned by a Phase Locked Loop (PLL) so that it samples the data in the center of the data eye pattern.

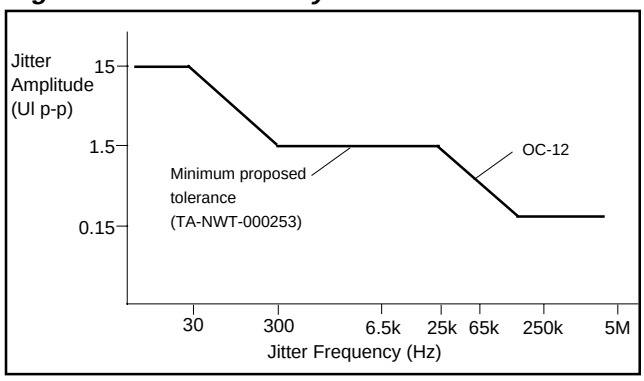
The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency discriminator. Output pulses from the discriminator indicate the required direction of phase corrections. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock.

Frequency stability without incoming data is guaranteed by an alternate reference input (REFCLK) that the PLL locks onto when data is lost. If the frequency of the incoming signal varies by greater than the value stated in Table 11 with respect to REFCLK, the PLL will be declared out of lock, and the PLL will lock to the reference clock. The assertion of LOS will also cause an out of lock condition.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal.

The total loop dynamics of the clock recovery PLL yield a jitter tolerance which exceeds the minimum tolerance proposed for SONET equipment by the Bellcore TA-NWT-000253 standard, shown in Figure 9.

Figure 9. Clock Recovery Jitter Tolerance



Frame and Byte Boundary Detection

The frame and byte boundary detection circuitry searches the incoming data for three consecutive A1 bytes followed immediately by three consecutive A2 bytes. Framing pattern detection is enabled and disabled by the Out-Of-Frame (OOF) input. Detection is enabled by a rising edge on OOF, and remains enabled for the duration that OOF is set High. It is disabled when a framing pattern is detected and OOF is no longer set High. When the framing pattern detection is enabled, the framing pattern is used to locate byte and frame boundaries in the incoming data stream (RSD or looped transmitter data). The timing generator block takes the located byte boundary and uses it to block the incoming data stream into bytes for output on the parallel output data bus (POUT[7:0]). The frame boundary is reported on the Frame Pulse (FP) output when any 48-bit pattern matching the framing pattern is detected on the incoming data stream. When the framing pattern detection is disabled, the byte boundary is frozen to the location found when detection was previously enabled. Only framing patterns aligned to the fixed byte boundary are indicated on the FP output.

The probability that random data in an STS-12 stream will generate the 48-bit framing pattern is extremely small. It is highly improbable that a mimic pattern would occur within one frame of data. Therefore, the time to match the first frame pattern and to verify it with down-stream circuitry, at the next occurrence of the pattern, is expected to be less than the required 250 µs, even for extremely high bit error rates.

Once down-stream overhead circuitry has verified that frame and byte synchronization are correct, the OOF input can be set low to disable the frame search process from trying to synchronize to a mimic frame pattern

Serial-to-Parallel Converter

The serial-to-parallel converter consists of three 8-bit registers. The first is a serial-in, parallel-out shift register, which performs serial to parallel conversion clocked by the clock recovery block. The second is an 8-bit internal holding register, which transfers data from the serial to parallel register on byte boundaries as determined by the frame and byte boundary detection block. On the falling edge of the free running POCLK, the data in the holding register is transferred to an output holding register which drives POUT[7:0].

The delay through the serial-to-parallel converter can vary from 1.5 to 3.5 byte periods (12 to 28 serial bit periods) measured from the first bit of an incoming byte to the beginning of the parallel output of that byte. The variation in the delay is dependent on the alignment of the internal parallel load timing, which is synchronized to the data byte boundaries, with respect to the falling edge of POCLK, which is independent of the byte boundaries. The advantage of this serial to parallel converter is that POCLK is neither truncated nor extended during reframe sequences.

OTHER OPERATING MODES

Diagnostic Loopback

When the Diagnostic Loopback Enable (DLEB) input is active, a loopback from the transmitter to the receiver at the serial data rate can be set up for diagnostic purposes. The differential serial output data from the transmitter is routed to the serial-to-parallel block in place of the normal data stream (RSD). DLEB has precedence over SDTTL.

Forward Clocking

For 77.76 MHz reference operation, the S3038 operates in the forward clocking mode. The PLL locks the PCLK output of the transmitter section to the REFCLK with a fixed and repeatable phase relation. This allows the transmitter data source to also be the timing source for the serial clock synthesis.

The rising edge of PCLK is locked to the rising edge of REFCLK, with a maximum delay of 8 to 10 nsec due to the PCLK TTL output driver.

Reset

The RESET signal initializes the internal counters, in addition, the rising edge on OOF is required after RESET to initialize the chip.

Table 4. Transmitter Input Signals Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
PINA0 PINA1 PINA2 PINA3 PINA4 PINA5 PINA6 PINA7	TTL	I	P12 R12 T13 T12 U13 P11 R11 T11	Transmit Data for Channel A. Parallel data on this bus is clocked in on the rising edge of PICLKA or REFCLK.
PICLKA	TTL	I	U12	Transmit Data Clock A. This signal is used to clock data on PINA[7:0]. This signal can also be used to clock data on PINB[7:0], PINC[7:0] and PIND[7:0].
PINB0 PINB1 PINB2 PINB3 PINB4 PINB5 PINB6 PINB7	TTL	I	R15 P14 T15 R14 U17 U16 P13 T14	Transmit Data for Channel B. Parallel data on this bus is clocked in on the rising edge of PICLKA, PICLKB or REFCLK.
PICLKB	TTL	I	R13	Transmit Data Clock B. This signal is used to clock data on PINB[7:0].
PINC0 PINC1 PINC2 PINC3 PINC4 PINC5 PINC6 PINC7	TTL	I	M15 N16 M14 R17 P16 N15 T17 N14	Transmit Data for Channel C. Parallel data on this bus is clocked in on the rising edge of PICLKA, PICLKC or REFCLK.
PICLKC	TTL	I	P15	Transmit Data Clock C. This signal is used to clock data on PINC[7:0].
PIND0 PIND1 PIND2 PIND3 PIND4 PIND5 PIND6 PIND7	TTL	I	L17 K16 K15 K14 M17 L16 M16 L15	Transmit Data for Channel D. Parallel data on this bus is clocked in on the rising edge of PICLKA, PICLKD, or REFCLK.
PICLKD	TTL	I	L14	Transmit Data Clock D. This signal is used to clock data on PIND[7:0].

Table 5. Transmitter Output Signals Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
TSDA0P TSDA0N	Diff. LVPECL	O	A17 B17	Primary high speed serial outputs for Channel A.
TSDA1P TSDA1N	Diff. LVPECL	O	E14 D16	Secondary high speed serial outputs for Channel A.
TSDB0P TSDB0N	Diff. LVPECL	O	C17 D17	Primary high speed serial outputs for Channel B.
TSDB1P TSDB1N	Diff. LVPECL	O	F14 F15	Secondary high speed serial outputs for Channel B.
TSDC0P TSDC0N	Diff. LVPECL	O	F16 E17	Primary high speed serial outputs for Channel C.
TSDC1P TSDC1N	Diff. LVPECL	O	G15 G14	Secondary high speed serial outputs for Channel C.
TSDD0P TSDD0N	Diff. LVPECL	O	F17 G17	Primary high speed serial outputs for Channel D.
TSDD1P TSDD1N	Diff. LVPECL	O	H14 H15	Secondary high speed serial outputs for Channel D.
PCLK	TTL	O	J14	TTL output clock at the parallel data rate. This clock is provided for use by the up-stream circuitry.

Table 6. Transmitter Control Signals Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
CH_LOCK	TTL	I	E4	Channel Lock. Parallel input mode control. Active High. When active, this signal locks all four channels together.
TMODE	TTL	I	B13	Transmit Mode Control. When TMODE is Low, REFCLK is used to clock data on PINx[7:0]. When TMODE is High, PICLKx is used to clock data into the S3038. In channel lock mode, all four channels are clocked by PICLKA. In independent mode (CHAN-LOCK LOW) each channel is clocked by its respective PICLK.
CLKSEL	TTL	I	C12	REFCLK Select input. This signal configures the PLL for the appropriate REFCLK frequency. When CLKSEL = 0, the REFCLK frequency should equal the 32-bit parallel rate. When CLKSEL = 1, the REFCLK frequency should be 1/2 the parallel data rate.
REFCLK	TTL	I	H17	Reference clock used for the transmit VCO and as a frequency check for the clock recovered from the receiver serial data. REFCLK can also be used to clock the input data of all four channels.
RESET	TTL	I	C15	When Low, the S3038 is held in reset. The receiver PLL is forced to lock to the REFCLK. The FIFO's are initialized on the rising edge of RESET. When High, the S3038 operates normally.

Note: All inputs have internal pull-up networks.

Table 7. Receiver Output Signals Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
POUTA0 POUTA1 POUTA2 POUTA3 POUTA4 POUTA5 POUTA6 POUTA7	TTL	O	J1 J3 J2 H1 H2 H3 F1 G2	Channel A Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of POCLKAP.
FPA	TTL	O	F2	Frame Pulse. A High on this output indicates that valid data has been detected and is present on the Parallel Data Output POUTA[7:0].
POCLKAP POCLKAN	TTL	O	K2 K1	Receive Data Clock. Parallel receive data, POUTA[7:0], are valid on the rising edge of POCLKAP.
POUTB0 POUTB1 POUTB2 POUTB3 POUTB4 POUTB5 POUTB6 POUTB7	TTL	O	R1 P1 M3 N2 M2 N1 L2 M1	Channel B Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of POCLKBP.
FPB	TTL	O	L1	Frame Pulse. A High on this output indicates that valid data has been detected and is present on the Parallel Data Output POUTB[7:0].
POCLKBP POCLKBN	TTL	O	U1 T1	Receive Data Clock. Parallel receive data, POUTB[7:0] are valid on the rising edge of POCLKBP.
POUTC0 POUTC1 POUTC2 POUTC3 POUTC4 POUTC5 POUTC6 POUTC7	TTL	O	R7 R6 T5 U3 T4 R5 U2 T3	Channel C Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of POCLKCP.
FPC	TTL	O	R2	Frame Pulse. A High on this output indicates that valid data has been detected and is present on the Parallel Data Output POUTC[7:0].
POCLKCP POCLKCN	TTL	O	U5 U4	Receive Data Clock. Parallel receive data, POUTC[7:0] are valid on the rising edge of POCLKCP.

Table 7. Receiver Output Signals Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
POUTD0 POUTD1 POUTD2 POUTD3 POUTD4 POUTD5 POUTD6 POUTD7	TTL	O	U11 R10 U9 R9 T9 U8 U7 T8	Channel D Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of POCLKDP.
FPD	TTL	O	U6	Frame Pulse. A High on this output indicates that valid data has been detected and is present on the Parallel Data Output POUTD[7:0].
POCLKDP POCLKDN	TTL	O	T10 U10	Receive Data Clock. Parallel receive data, POUTD[7:0] are valid on the rising edge of POCLKDP.

Table 8. Receiver Input Signals Pin Assignment and Description

Pin Name	Level	I/O	Pin #	Description
RSDA0P RSDA0N	Diff. LVPECL	I	D5 C5	Primary differential LVPECL compatible inputs for channel A. RSDA0P is the positive input, RSDA0N is the negative. Internally biased to VDD-1.3V for AC coupled applications.
RSDA1P RSDA1N	Diff. LVPECL	I	D4 B3	Secondary differential LVPECL compatible inputs for channel A. RSDA1P is the positive input, RSDA1N is the negative. Internally biased to VDD-1.3V for AC coupled applications.
RSDASEL	TTL	I	A3	Channel A input select control. Low selects input RSDA0, High selects RSDA1. (Internal pull-up when not connected.)
RSDB0P RSDB0N	Diff. LVPECL	I	C6 B5	Primary differential LVPECL compatible inputs for channel B. RSDB0P is the positive input, RSDB0N is the negative. Internally biased to VDD-1.3V for AC coupled applications.
RSDB1P RSDB1N	Diff. LVPECL	I	C7 D7	Secondary differential LVPECL compatible inputs for channel B. RSDB1P is the positive input, RSDB1N is the negative. Internally biased to VDD-1.3V for AC coupled applications.
RSDBSEL	TTL	I	A5	Channel B input select control. Low selects input RSDB0, High selects RSDB1. (Internal pull-up when not connected.)
RSDC0P RSDC0N	Diff. LVPECL	I	A10 B9	Primary differential LVPECL compatible inputs for channel C. RSDC0P is the positive input, RSD is the negative. Internally biased to VDD-1.3V for AC coupled applications.
RSDC1P RSDC1N	Diff. LVPECL	I	A8 A9	Secondary differential LVPECL compatible inputs for channel C. RSDC1P is the positive input, RSDC1N is the negative. Internally biased to VDD-1.3V for AC coupled applications.
RSDCSEL	TTL	I	C9	Channel C input select control. Low selects input RSDC0, High selects RSDC1. (Internal pull-up when not connected.)
RSDD0P RSDD0N	Diff. LVPECL	I	C10 D10	Primary differential LVPECL compatible inputs for channel D. RSDD0P is the positive input, RSDD0N is the negative. Internally biased to VDD-1.3V for AC coupled applications.
RSDD1P RSDD1N	Diff. LVPECL	I	C11 B12	Secondary differential LVPECL compatible inputs for channel D. RSDD1P is the positive input, RSDD1N is the negative. Internally biased to VDD-1.3V for AC coupled applications.
RSDDSEL	TTL	I	B11	Channel D input select control. Low selects input RSDD0, High selects RSDD1. (Internal pull-up when not connected.)
OOFA OOFB OOFC OOFD	LVTTL	I	U14 T16 P17 K17	Out of frame indicator used to enable framing pattern detection logic in the S3038. The framing pattern detection logic is enabled by a rising edge on OOF, and remains enabled until frame boundary is detected or when OOF is set low, whichever is longer. OOF is an asynchronous signal with a minimum pulse width of one POCLK period. Rising edge on OOF is required after RESET to initialize the chip.
SDTTLA SDTTLB SDTTLC SDTTLD	LVTTL	I	U15 R16 N17 J16	LVTTL Signal Detect. Active High (logic 1). When SDTTL is inactive, the data on the RSDP/N pins will be internally forced to a constant zero. When SDTTL is active, data on the RSDP/N pins will be processed normally.

Table 9. Receiver Control Signals Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
DLEB	TTL	I	D14	Diagnostic Loopback Enable. When Low, input source is determined by the RSDSEL for each channel. When High, the serial output for each channel is looped back to its input. TSD0XP/N and TSD1XP/N are squelched when DLEB = HIGH.

Table 10. Power and Ground Pin Assignments

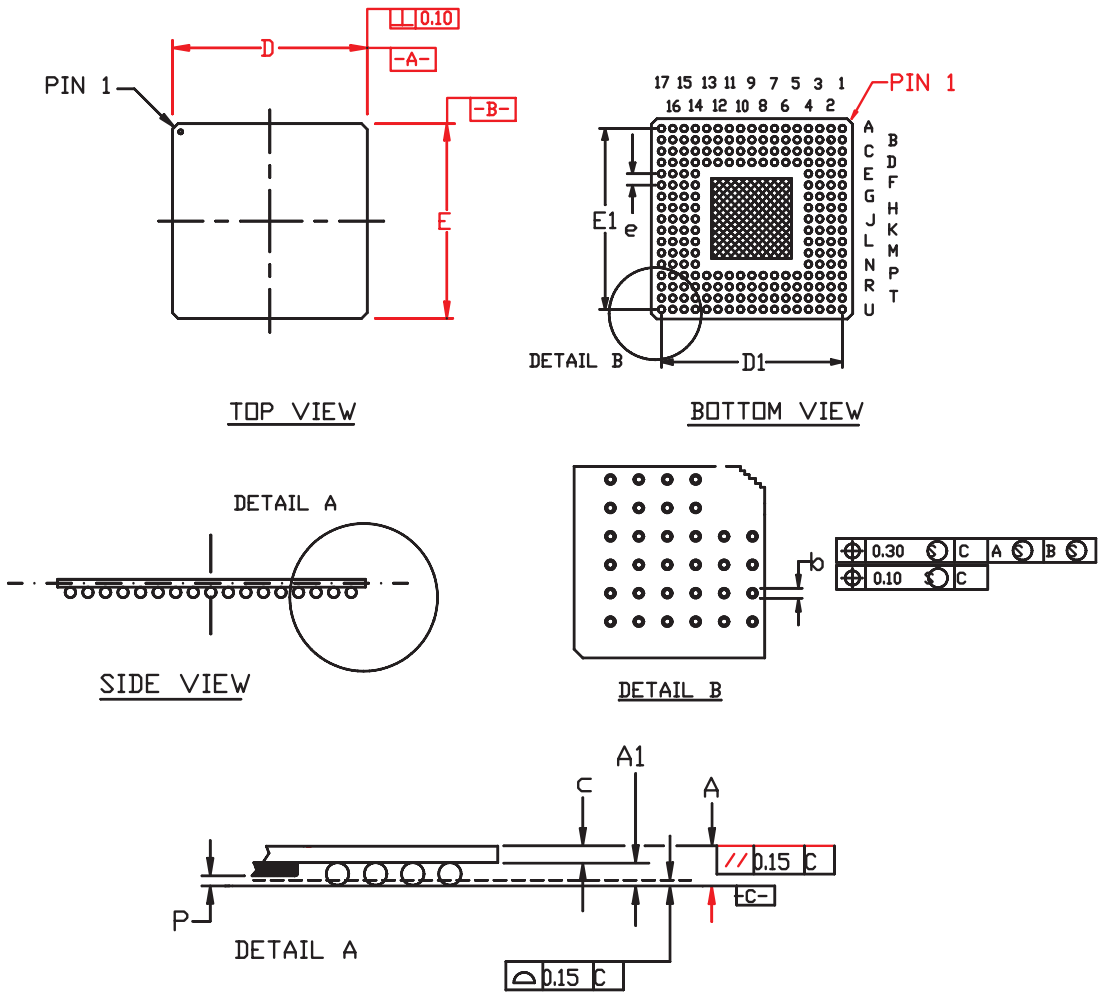
Pin Name	Aliases	No. Signals	Pin #	Description
AVDD	VDDAx	5	A1 A6 C8 A13 A16	Analog Power (VDD) low noise.
AVSS	VSSAx	5	C4 B7 B8 D11 B15	Analog Ground (VSS).
VDD	VDDx	5	B4 B6 D9 A12 A15	Power for high speed circuitry (VDD).
VSS	VSSx VSSSUBx	10	A2 A4 D6 A7 D8 A11 B10 C13 A14 B14	Ground for high speed circuitry (VSS).
PVDD	PECLPWR	4	D15 E15 E16 G16	PECL Power (VDD).
PVSS	PECLGND	1	C16	PECL Ground (VSS).
DVDD	DIGPWR DIGPWR1	9	B1 B2 C2 D3 D12 E3 L4 J17 P9	Core circuitry power (VDD).
DVSS	DIGGND DIGGND1 DIGGNDS	10	B16 C1 D2 C3 R3 F4 N4 J15 H16 P10	Core circuitry ground (VSS).
TVDD	TTLPWR	8	E1 N3 G4 H4 K4 P5 P7 P8	Power for TTL I/O (VDD).
TVSS	TTLGND	10	D1 E2 F3 L3 J4 M4 P4 R4 P6 R8	Ground for TTL I/O (VSS).
Total Pwr/Gnd		67		
NC		8	G1 G3 K3 P2 P3 T2 T6 T7	Not connected.
CAP1 CAP2		2	D13 C14	Pins for external loop filter capacitor and resistors. See Figure 20.

Figure 10. Quad Transceiver Pinout-Bottom View

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U
1	AVDD	DVDD	DVSS	TVSS	TVDD	POUTA6	NC	POUTA3	POUTA0	POCLKAN	FPB	POUTB7	POUTB5	POUTB1	POUTB0	POCLKBN	POCLKBP
2	VSS	DVDD	DVDD	DVSS	TVSS	FPA	POUTA7	POUTA4	POUTA2	POCLKAP	POUTB6	POUTB4	POUTB3	NC	FPC	NC	POUTC6
3	RSDASEL	RSDA1N	DVSS	DVDD	DVDD	TVSS	NC	POUTA5	POUTA1	NC	TVSS	POUTB2	TVDD	NC	DVSS	POUTC7	POUTC3
4	VSS	VDD	AVSS	RSDA1P	CH_LOCK	DVSS	TVDD	TVDD	TVSS	TVDD	DVDD	TVSS	DVSS	TVSS	TVSS	POUTC4	POCLKCN
5	RSDBSEL	RSDB0N	RSDA0N	RSDA0P										TVDD	POUTC5	POUTC2	POCLKCP
6	AVDD	VDD	RSDB0P	VSS										TVSS	POUTC1	NC	FPD
7	VSS	AVSS	RSDB1P	RSDB1N										TVDD	POUTC0	NC	POUTD6
8	RSDC1P	AVSS	AVDD	VSS										TVDD	TVSS	POUTD7	POUTD5
9	RSDC1N	RSDC0N	RSDCSEL	VDD										DVDD	POUTD3	POUTD4	POUTD2
10	RSDC0P	VSS	RSDD0P	RSDD0N										DVSS	POUTD1	POCLKDP	POCLKDN
11	VSS	RSDDSEL	RSDD1P	AVSS										PINA5	PINA6	PINA7	POUTD0
12	VDD	RSDD1N	CLKSEL	DVDD										PINA0	PINA1	PINA3	PICLKA
13	AVDD	TMODE	VSS	CAP1										PINB6	PICLKB	PINA2	PINA4
14	VSS	VSS	CAP2	DLEB	TSDA1P	TSDB1P	TSDC1N	TSDD1P	PCLK	PIND3	PICLKD	PINC2	PINC7	PINB1	PINB3	PINB7	OOFA
15	VDD	AVSS	RESET	PVDD	PVDD	TSDB1N	TSDC1P	TSDD1N	DVSS	PIND2	PIND7	PINC0	PINC5	PICLKC	PINB0	PINB2	SDTTLA
16	AVDD	DVSS	PVSS	TSDA1N	PVDD	TSDC0P	PVDD	DVSS	SDTTLD	PIND1	PIND5	PIND6	PINC1	PINC4	SDTTLB	OOFB	PINB5
17	TSDA0P	TSDA0N	TSDB0P	TSDB0N	TSDC0N	TSDD0P	TSDD0N	REFCLK	DVDD	OOFD	PIND0	PIND4	SDTTLC	OOFC	PINC3	PINC6	PINB4

S3038
208 TBGA
Bottom View

Figure 11. 208 TBGA Package



DIMENSIONS (are in millimeters)

UNIT	A	A_1	D	D_1	E	E_1	P	b	c	e
MIN	1.45	0.60	22.80	20.32 BSC.	22.80	20.32 BSC.		0.65	0.85	1.27 BSC.
NOM	1.55	0.65	23.00		23.00			0.75	0.90	
MAX	1.65	0.70	23.20		23.20		0.25	0.85	0.95	

Thermal Management

Max Package Power	Θja (Still Air)	Θjc
3.4 W	14˚ C/W	0.8˚ C/W

Table 11. Performance Specifications

Parameter	Min	Typ	Max	Units	Condition
Nominal VCO Center Frequency		622.08		MHz	
Data Output Jitter **STS-12** –38.88 MHz Ref.Clk. –77.76 MHz Ref Clk.			0.01 0.0075	UI (rms)	rms jitter, in lock
Reference Clock Frequency Tolerance*	-20		+20	ppm	Required to meet SONET output frequency specification
OC-12/STS-12 Capture Range Lock Range		±200 ±12%		ppm	With respect to fixed reference frequency
Acquisition Lock Time			16	µsec	Minimum transition density of 20% With device already powered up and valid ref. clk.
Reference Clock Input Duty Cycle	30		70	%	
Reference Clock Rise & Fall Times			2.0	ns	20% to 80% of amplitude
Frequency difference at which the PLL goes out of lock (REFCLK compared to the divided down VCO clock)	250	290	330	ppm	
Frequency difference at which the receive PLL goes into lock (REFCLK compared to the divided down VCO clock)	250	290	330	ppm	
Maximum run length of serial data input before out of lock is declared	80		1000	UI	No transitions on RSDP/N.
OC-12/STS-12 Jitter Tolerance	0.4			UI	Sinusoidal input jitter. Amplitude on SERDATI/P data inputs from 12 kHz to 5 MHz.

* Noise on REFCLK should be less than 14 ps rms in a jitter frequency band from 12 kHz to 5 MHz.

Table 12. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature	-65		150	˚C
Voltage on VDD with respect to GND	-0.5		+7.0	V
Voltage on any TTL Input Pin	-0.5		3.47	V
Voltage on any LVPECL Input Pin	0		VDD	V
TTL Output Sink Current			8	mA
TTL Output Source Current			8	mA
High speed LVPECL Output Source Current			50	mA
ESD Sensitivity[1]	1500			V

1. Human body model.

Table 13. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	0		70	˚C
Junction Temperature Under Bias			130	˚C
Voltage on TTLVDD, ECLVDD,ECLIOVDD, and AVDD with respect to GND/VSS	3.135	3.3	3.465	V
Voltage on any TTL Input Pin	0		3.465	V
Voltage on any LVPECL Input Pin	VDD -2V		VDD	V
Voltage on TTL Data Pin	0		3.465	V

Table 14. Reference Clock Requirements

Parameters	Description	Min	Max	Units	Comments
FT	Frequency Tolerance	-100	+100	ppm	
TD_{1-2}	Symmetry	40	60	%	Duty Cycle at 50% pt.
T_{RCR}, T_{RCF}	REFCLK Rise and Fall Time		2	ns	20% - 80%.

Table 15. TTL Input/Output DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Comments
V_{OH}	Output High Voltage (TTL)	2.4	2.8	VDD	V	VDD = min I_{OH} = -4mA
V_{OL}	Output Low Voltage (TTL)	GND	.025	0.5	V	VDD = min I_{OL} = 4mA
V_{IH}	Input High Voltage (TTL)	2.0			V	
V_{IL}	Input Low Voltage (TTL)	GND		0.8	V	
I_{IH}	Input High Current (TTL)			40	µA	V_{IN} = 2.4V, VDD = max
I_{IL}	Input Low Current (TTL)			600	µA	V_{IN} = 2.4V, VDD = max
I_{CC}	Supply Current		825	980	mA	1010 Pattern.
P_D	Power Dissipation		2.7	3.4	W	1010 Pattern.
V_{DIFF}	Min. differential input voltage swing for differential LVPECL inputs	150		1300	mV	See Figure 12.
ΔV_{OUT}	Serial Output Voltage Swing (single-ended)	600		1600	mV	50Ω to VDD -2.0V
C_{IN}	Input Capacitance			3	pF	

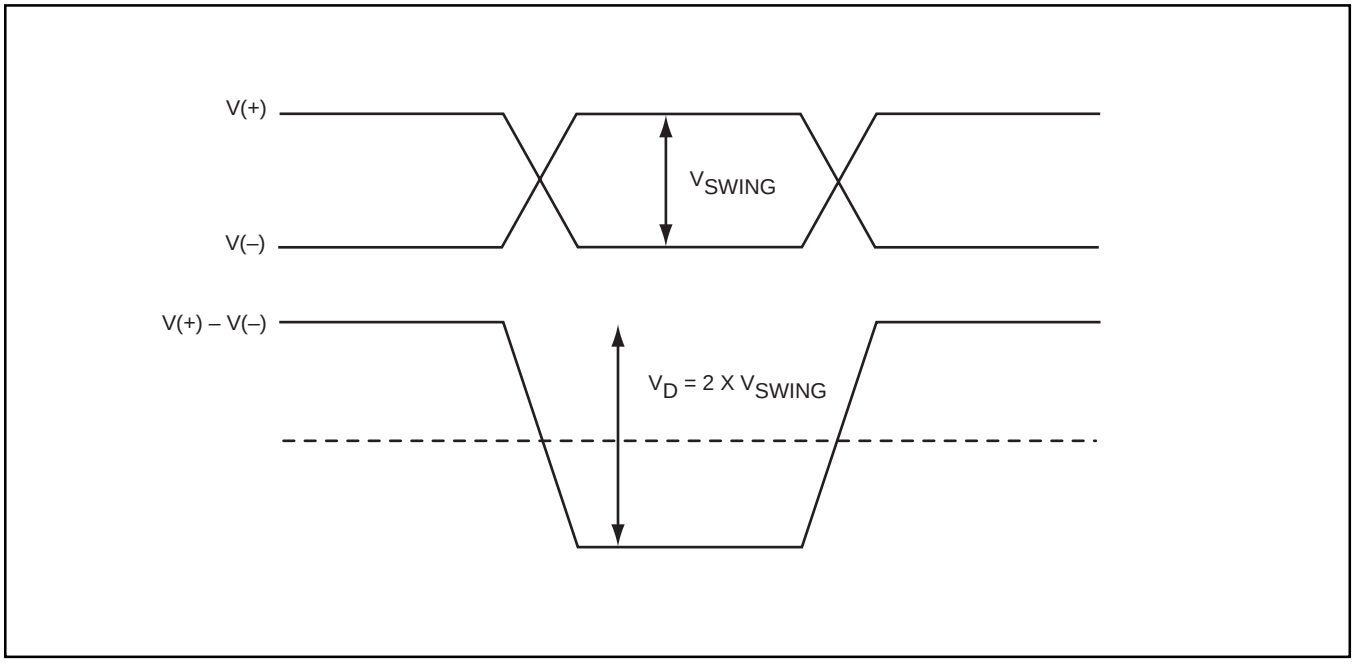
Table 16. Transmit Signals Characteristics

Parameters	Description	Min	Max	Units	Comments
Total Jitter	Serial Data Output Jitter (p-p)		192	ps	Peak-to-peak, tested on a sample basis. Measured with a 2^7 -1 pattern.
T_{SDR}, T_{SDF}	Serial Data Rise and Fall Time		350	ps	20% to 80% tested on a sample basis. Measured with 10 pF load.

Table 17. Receive Signal Characteristics

Parameters	Description	Min	Max	Units	Comments
Input Sensitivity	Swing required on input to reliably recover data	100		mV	
T_{SDR}, T_{SDF}	Serial Data Rise and Fall Time		500	ps	20% to 80% tested on a sample basis.

Figure 12. Differential Voltage



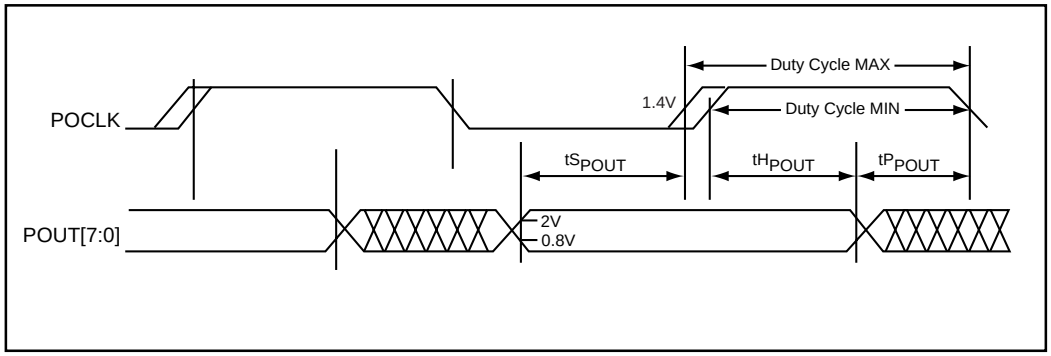
Note: V(+) – V(-) is the algebraic difference of the input signals.

Table 18. Receiver Timing (See Figure 13)

Symbol	Description	Min	Max	Units	Comments
	POCLK Duty Cycle	40	60	%	
	POCLK Rise/Fall Time		3	ns	
tS_{POUT}	Data Setup w.r.t. POCLK	3		ns	
tH_{POUT}	Data Hold Time w.r.t. POCLK	3		ns	
tP_{POUT}	POCLK Low to POUTx[7:0] valid	-2	2	ns	

1. All AC measurements are made from the reference level of the clock 1.4V to the valid input or output data level (0.8 or 2V).

Figure 13. Receiver Output Timing Diagram



Notes on Output Timing:

1. Output propagation delay time of LVTTL outputs is the time in nanoseconds from the 1.4V point of the reference signal to the valid input or output data level (0.8V or 2V).
2. Maximum output propagation delays of LVTTL outputs are measured with a 10 pF load on the outputs.
3. Output propagation delay time of high speed LVPECL outputs is the time in nano seconds from the cross-over point of the reference signal to the cross-over point of the output.

Table 19. PCLK Timing

Symbol	Description	Min	Max	Units	Comments
tD_{PCLK}	Delay from REFCLK to PCLK	2	7.5	ns	CLKSEL = 0
tD_{PCLK}	Delay from REFCLK to PCLK	2	7.5	ns	CLKSEL = 1

Figure 14. PCLK Timing (See Table 19)

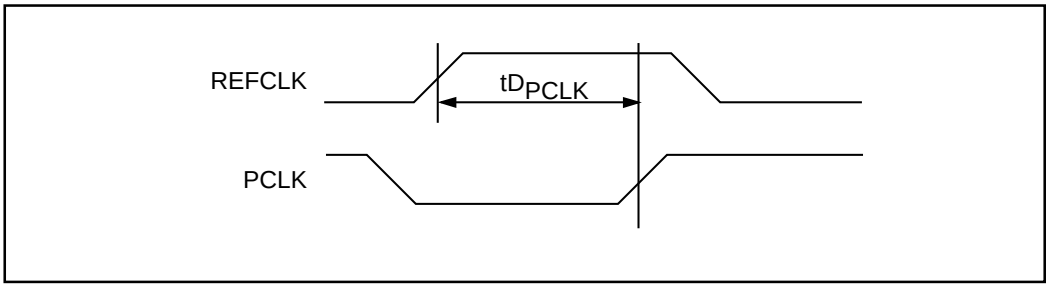


Figure 15. Transmitter Timing (Normal or Channel Lock Mode, TMODE = 0)

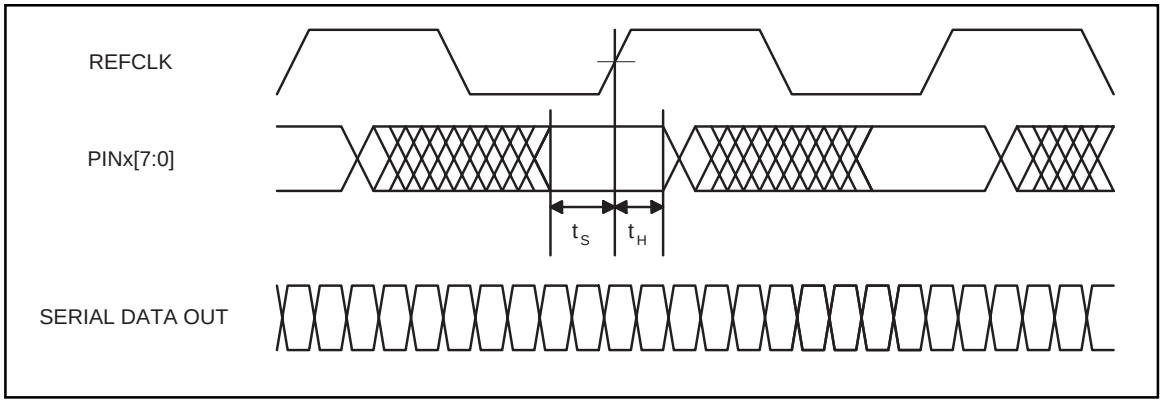


Table 20. S3038 Transmitter Timing (Normal or Channel Lock Mode, TMODE = 0)

Parameters	Description	Min	Max	Units	Conditions
t_S	Data Setup w.r.t. ↑ REFCLK	0.5	-	ns	See Note 1.
t_H	Data Hold w.r.t. ↑ REFCLK	1.5	-	ns	

1. All AC measurements are made from the reference voltage level of the clock (1.4V) to the valid input or output data levels (0.8V or 2.0V).

Figure 16. Transmitter Timing (Normal or Channel Lock Mode TMODE = 1)

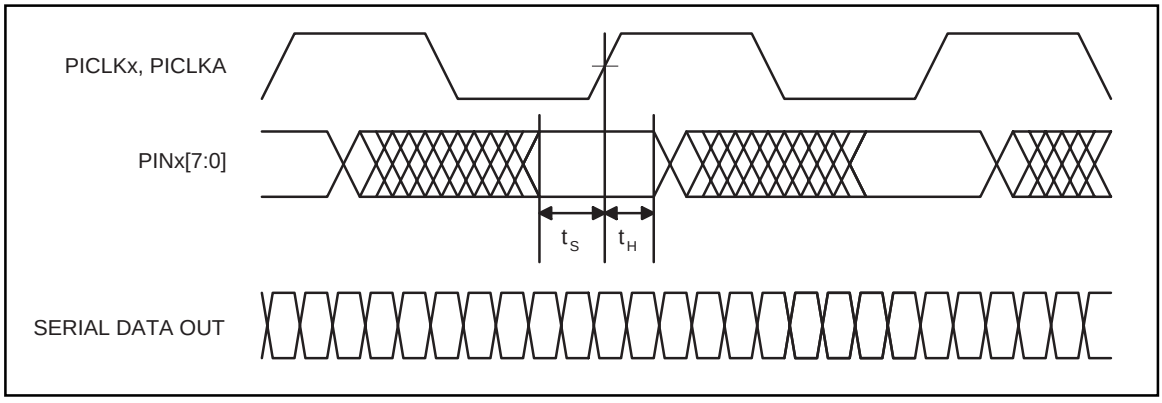


Table 21. S3038 Transmitter Timing (Normal or Channel Lock Mode, TMODE = 1)

Parameters	Description	Min	Max	Units	Conditions
t_S	Data Setup w.r.t. ↑ PICLK	1	-	ns	See Note 1.
t_H	Data Hold w.r.t. ↑ PICLK	0.5	-	ns	

1. All AC measurements are made from the reference voltage level of the clock (1.4V) to the valid input or output data levels (0.8V or 2.0V).

Table 22. Power and Ground Application Information

Function	Names on Master Pinout	Pin Name	Instructions
Analog	VDDA	AVDD	Connect to low noise or filtered 3.3V supply. Provide local HF bypassing to A-VSS. Use dual (0.1µF, 100 pF) bypassing.
	VSSA	AVSS	Connect to ground plane.
High Speed	VDD	VDD	Low impedance connection to 3.3V. Provide local bypassing to GND plane. Use dual (0.1µF, 100 pF) bypassing.
	VSS VSSSUB	VSS	Connect to ground plane.
PECL I/O	PECLPWR	PVDD	Provide low impedance connection to 3.3V. Provide local bypassing to GND plane. Use dual (0.1µF, 100 pF) bypassing.
	PECLGND	PVSS	Connect to ground plane.
Core	DIGPWR	DVDD	Provide low impedance connection to 3.3V. Provide local bypassing using 0.1µF capacitors.
	DIGGND	DVSS	Connect to ground plane.
TTL I/O	TTLPWR	TVDD	Connect to 3.3V power plane. Provide local bypassing using 0.1µF capacitors.
	TTLGND	TVSS	Connect to ground plane.
Logic Level	NA	PWR	Logic connection to VDD. No bypassing necassary.
	NA	GND	logic connection to VSS.

RECEIVER FRAMING

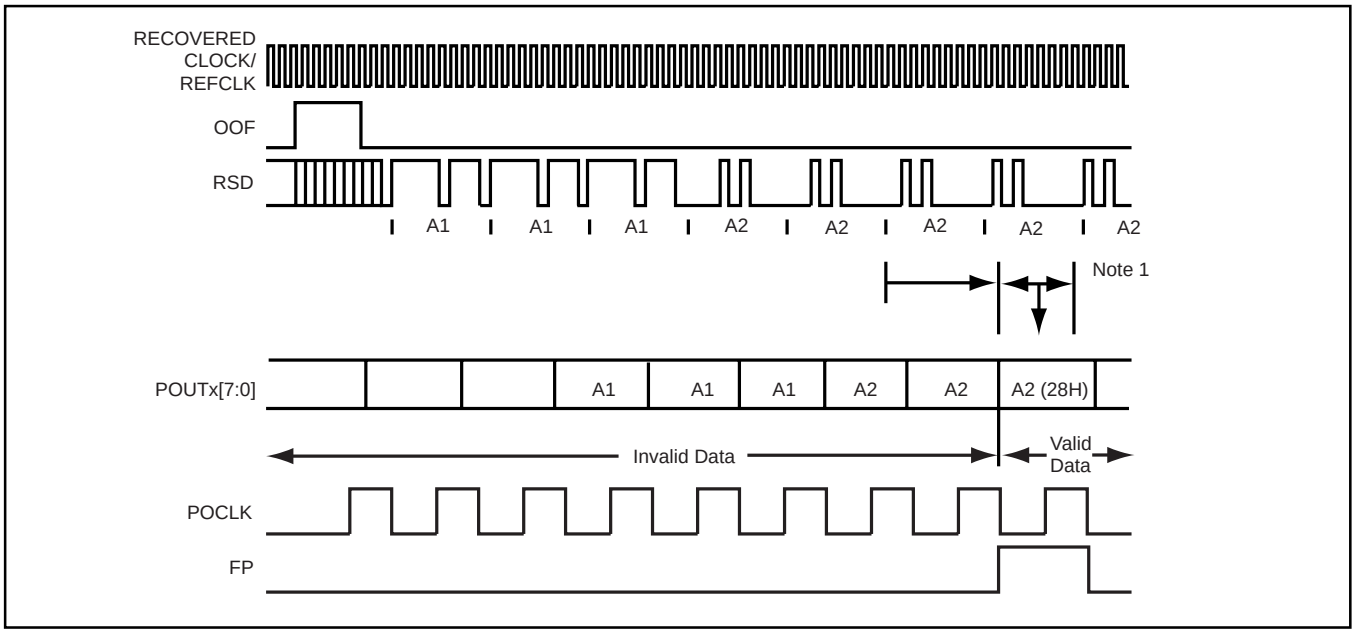
Figure 17 shows a typical reframe sequence in which a byte realignment is made. The frame and byte boundary detection is enabled by the rising edge of OOF and remains enabled while OOF is high. Both boundaries are recognized upon receipt of the third A2 byte which is the first data byte to be reported with the correct byte alignment on the outgoing data bus (POUTx[7:0]). Concurrently, the frame pulse is set high for one POCLK cycle.

When interfacing with a section terminating device, the OOF input remains high for one full frame after the first frame pulse while the section terminating device verifies internally that the frame and byte alignment are correct, as shown in Figure 17. Since at least one framing pattern has been detected since the rising edge of OOF, boundary detection is disabled when OOF is set low.

The frame and byte boundary detection block is activated by the rising edge of OOF, and stays active until the first FP pulse or until OOF goes low, whichever occurs last. Figure 18 shows a typical OOF timing pattern which occurs when the S3038 is connected to a down stream section terminating device. OOF remains high for one full frame after the first FP pulse. The frame and byte boundary detection block is active until OOF goes low.

Figure 19 shows the frame and byte boundary detection activation by a rising edge of OOF, and deactivated by the first FP pulse.

Figure 17. Frame and Byte Detection



NOTE 1: Range of input to output delay can be 1.5 to 2.5 POCLK cycles.

Figure 18. OOF Operation Timing with PM5312 STTX or PM5355 SUNI-622

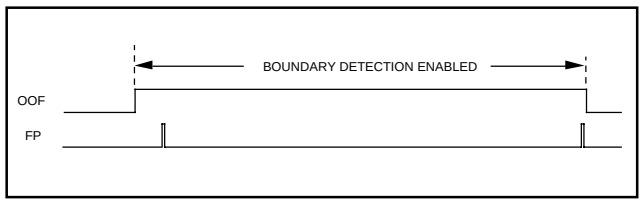


Figure 19. Alternate OOF Timing

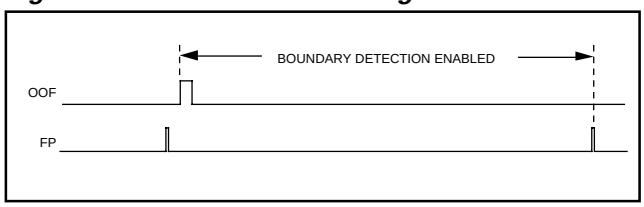


Figure 20. External Loop FIlter

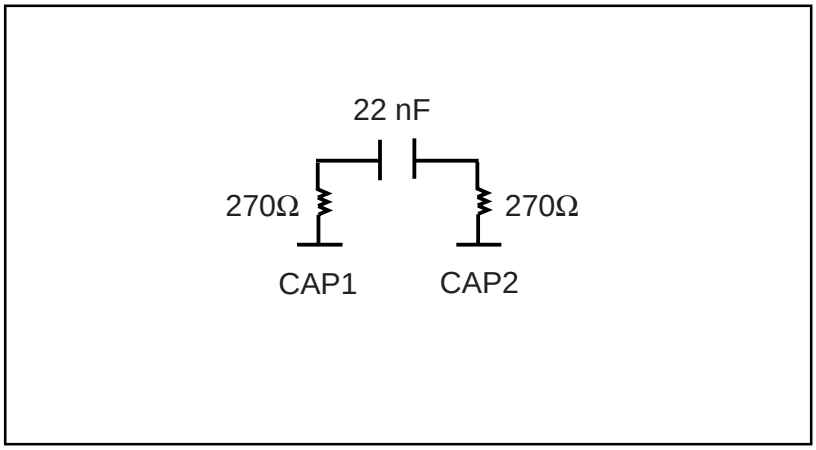


Figure 21. Serial Output Load

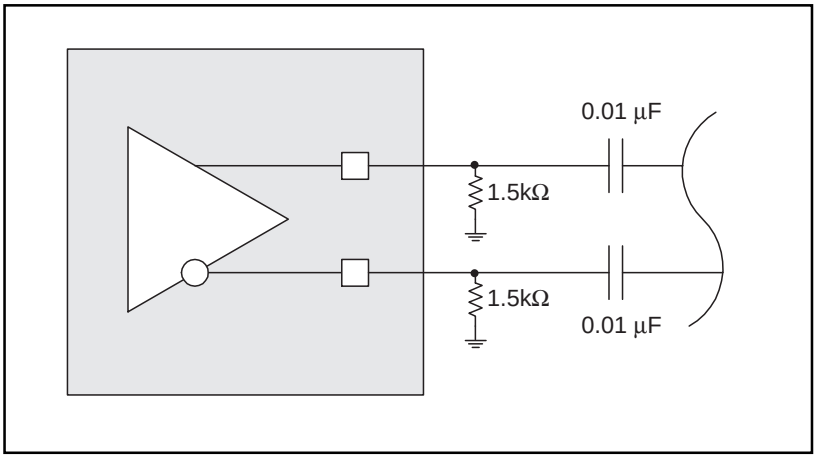
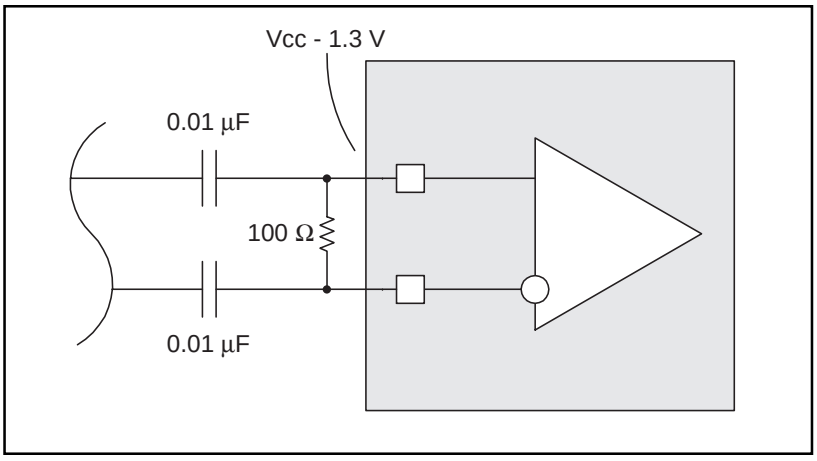
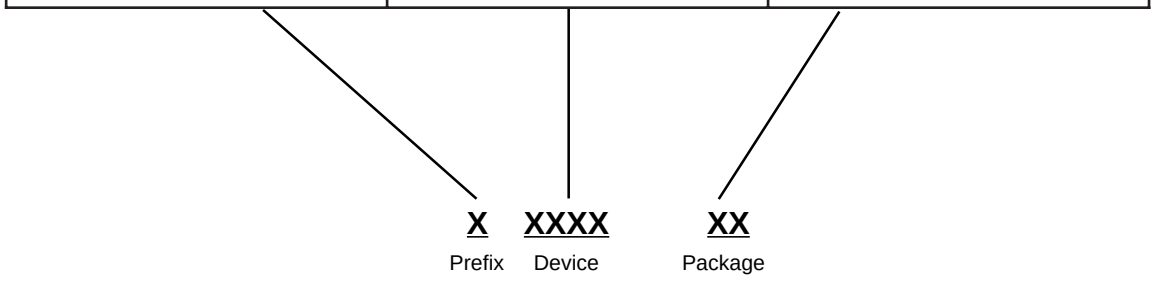


Figure 22. High Speed Differential Inputs



Ordering Information

PREFIX	DEVICE	PACKAGE
S – Integrated Circuit	3038	TB – 208 TBGA



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