Preliminary Data Sheet, DS 2, Nov. 2001

TE3-FALC

T3/E3 Framer & Line Interface for ATM, Frame Relay & PPP/IP

PEF 3460 E Version 1.1

Wired Communications

Infineon technologies

Never stop thinking.

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Revision History: **2001-11-30** DS 2

Previous Version: 2001-05-09, DS 1

Page (previous Version)	Page (current Version)	Subjects (major changes since last revision)
28	13	Changed recommended connection for pin RSVD_F1 from "unconnected" to "pull-down resistor required". This is to ensure the correct T3/E3 line coding.

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Preface

This Preliminary Data Sheet provides a complete reference for hardware and software design with "T3/E3 Framer & Line Interface for ATM, Frame Relay & PPP/IP" TE3-FALC (PEF 3460 E).

Note: Some features mentioned in this document are options for future firmware enhancements and not supported with the current release of firmware. These options are marked with a preceding "✧" symbol.

The document is organized as follows:

- **Chapter 1, Overview**
  Gives a general description of the product and its family, lists the key features, and presents some typical applications.

- **Chapter 2, Pin Descriptions**
  Lists pin locations with associated signals, categorizes signals according to function, and describes signals.

- **Chapter 3, Functional Description**
  Contains a block diagram and provides a brief description of the functional blocks.

- **Chapter 4, Operational Description**
  Describes the operational states of the device like reset, boot procedures, initialization and power-down.

- **Chapter 5, Hardware Interface Description**
  Provides a detailed description of all external hardware interfaces and their characteristics.

- **Chapter 6, Software Interface Description**
  Describes the application programmer's interface (API) and gives detailed reference information about the supported message catalog.

- **Chapter 7, Electrical Characteristics**
  Lists all DC and AC characteristics of the hardware interfaces including interface timings.

- **Chapter 8, Test Configurations**
  Provides information about various test configurations that simplify hardware and software design, like boundary scan.

- **Chapter 9, Package Outlines**
  Technical drawing of the package including all relevant dimensions.

Related Documentation

This document refers to the following international standards (in alphabetical/numerical order):

ANSI T1.107-1995 section 9 (DS3 framing)

ANSI T1.231-1997 section 7 (DS3 performance monitoring)

ANSI T1.404-1994 (DS3)

ANSI T1.646-1995 (DS3, esp. PLCP mapping)

ATMF af-phy-0034.000, Aug. 1995 (E3 UNI)

ATMF af-phy-0039.000, Jun. 1995 (UTOPIA Level 2)

ATMF af-phy-0054.000, Jan. 1996 (PLCP and direct ATM mapping into DS3)

ATMF UNI 3.1, Sep. 1994 (User-Network Interface)

ETSI ETS 300 166, Aug. 1993

ETSI TBR24, Jul. 1997 (E3)

FRF.14 (Physical Layer Interface Implementation Agreement)

IEEE 1149.1 (TAP controller, boundary scan)

IETF RFC1661 (The Point-to-Point Protocol PPP)

IETF RFC1662 (PPP in HDLC-like framing)

IETF RFC2496 (Definition of Managed Object for the DS3/E3 Interface Type)

ITU-T G.703 (T3/E3 Physical Interface)

ITU-T G.704, section 2.5 (DS3 framing)

ITU-T G.775 (DS3 alarm handling)

ITU-T G.783

ITU-T G.804 (PLCP and direct ATM mapping)

ITU-T G.823, Feb. 1999 (E3 Jitter/Wander)

ITU-T G.824, Mar. 1993 (T3 Jitter/Wander)

ITU-T G.832 (E3 framing)

ITU-T I.432.1 (ATM TC-sublayer)

ITU-T O.151, Oct. 1992 (Error Performance Measurement)

ITU-T O.153, Oct. 1992 (Error Performance Measurement)

ITU-T Q.921 (HDLC)

MIL-STD 883D (ESD requirements)

SATURN Group POS-PHY Level 2, Dec. 1998

Telcordia GR-499-CORE, Dec. 1998

1 Overview

The TE3-FALC is a complete solution for a T3/E3 broadband interface. It includes DS3/E3 framing, analogue line interface, two jitter attenuators and the mapping of ATM or HDLC-framed PPP. The TE3-FALC also integrates a µController which is running the device driver and gathering statistics in accordance with the relevant managed MIB objects.

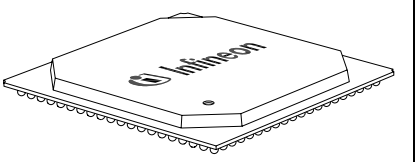
On line side the TE3-FALC interfaces to a 75 ohm co-axial cable via transformers. Highly accurate analogue pulse shaping removes the need to measure cable length and set the Line Build Out.

On the system side, industry standard UTOPIA, UTOPIA-L2X and POS-PHY interface as well as a serial clock/data port are provided. This allows the TE3-FALC to be connected to a wide array of Layer 2/3 & 4 network processors.

T3/E3 Framer & Line Interface for ATM, Frame Relay & PPP/IP **PEF 3460 E**
TE3-FALC

Version 1.1

1.1 Features



PBGA-272-4

General Features

- Integrated T3/E3 LIU for recovery of analog signals from the line and the transmission of signals onto the line via a transformer.
- Flexible main clock input accepting any frequency between 4 and 52 MHz.
- Integrated transmit and receive jitter attenuators
- Integrated transmit clock multiplier to enable a wide number of transmit reference clocks (optional) to be used from 8 kHz to 52 MHz
- Integrated receive clock multiplier to enable a wide number of receive reference clocks (optional) to be used from 8 kHz to 52 MHz
- Integrated receive reference clock multiplier
- DS3 M23 and C-Bit Parity framer with overhead bit processing.
- E3 G.832 framer with overhead byte processing.
- Integrated Bit Error Rate Tester (BERT)
- ATM TC layer allowing the direct mapping/extraction of ATM cells into/from the DS3 or E3 frame.
- ATM DS3 PLCP function allowing the mapping of ATM cells into the DS3 frame using the PLCP sub-frame.
- Single channel HDLC controller allowing the mapping/extraction of bit or byte mapped HDLC encapsulated packet from either the DS3 or E3 frame
- Flexible 16/8-bit Packet Stream Interface (PSI) allowing connection to industry standard UTOPIA, UTOPIA-L2X and POS-PHY interfaces.
- Integrated micro-controller with associated boot loader ROM and code/data RAM to allow low level drivers to be run on chip to reduce the software required to control the device and homologation time.
- Integrates a 16/8-bit switchable Intel or Motorola style microprocessor interface.
- JTAG boundary scan according to IEEE 1149.1 (5 pins).
- 0.18 µm, 1.8 V low power core technology

Type	Package
PEF 3460 E	PBGA-272-4

- I/Os are 3.3 V tolerant and have 3.3 V driving capability
- Package PBGA-272-4 (27mm x 27mm; pitch 1.27mm)
- Full scan path and BIST of on-chip RAMs for production test
- Estimated power consumption: < 1500 mW

Analog Interface

- Supports clock recovery on B3ZS and HDB3 line coding.
- Meets jitter input tolerance according to GR-499-CORE (Cat. 1 & 2), ITU-T G.823, G.824 and ETSI TBR24.
- Meets jitter output requirements according to GR-499-CORE and ETSI TBR24.
- Performs jitter attenuation of receive clock when in loop timed mode for terminal applications in compliance to GR-499-CORE and TBR24.
- Pulse shaper meets templates according to ANSI T1.102 & 404, GR-499-CORE, ITU-T G.703.
- Single RC interface to transformer for both T3 and E3.
- Provides PLL for transmit clock duty cycle correction.
- Provides LOS detection for both T3 (ANSI T1.231) and E3 (G.775)
- Identical performance to Infineon’s PEF 3452 TE3-LIU.

DS3/E3 Framer

- DS3 M23 framer in accordance with ANSI T1.107 and T1.404.
- E3 framer in accordance with G.832.
- DS3 support for C-Bit Parity operation and clear channel mode.
- Detection of OOF, LOF, AIS, RDI/FERF alarms. Counting of OOF events, parity errors and far end errors as required in ATMF and IETF MIB.
- Automatic insertion of RDI/FERF on correct received alarm status. Generation and insertion of FEBE on received parity errors.
- DS3 C-Bit Parity detection by AIC monitoring; counting and processing of the FEAC and maintenance data link channel.
- E3 G.832 TR byte (16 byte Trail Trace) processing and generation. MA byte multi-frame synchronization, synchronization status nibble extraction and insertion.
- Gathers statistics in accordance with RFC 2496 'Managed Objects for DS3/E3 Interface Type'.
- Bypass modes supported to bypass both Framer and Cell/Packet processor.

ATM/PPP Protocol Processor

- Transmit Cell Processing:
  - ✧Extraction of ATM cells on pre-set VPI/VCI[1)].
  - ✧Optional on-the-fly checking of CRC-10 or AAL5 CRC-32 and length fields for extracted cells[1)].
  - Supports ATM cell payload scrambling, header check sequence generation, idle cell generation as per ITU-T I.432.
  - Mapping of ATM cells into E3 and DS3 frame as per G.804.
  - Generation of DS3 PLCP frame and mapping of ATM cell stream into PLCP frame as per ATMF UNI 3.1.

- Receive Cell Processing:
  - Optional termination of PLCP frame for DS3, extraction of ATM cell stream from PLCP frame or directly from DS3 or E3 frame.
  - Supports cell payload de-scrambling, header check sequence verification, idle cell filtering and performance monitoring.
  - ✧Insertion of ATM cells in the direction of the UTOPIA port[1)].
  - ✧Optional generation of CRC-10 or AAL5 CRC-32 field for inserted cells[1)].

- Transmit Packet Processing:
  - ✧Extraction of in-band messaging packets on packet header[1)].
  - ✧On-the-fly checking of CRC and length fields for extracted packets[1)].
  - ✧Insertion of PPP packets into data stream[1)].
  - Supports HDLC Flag, CRC-16/32 and idle sequence generation. Abort generation for under-run conditions.
  - Optional PPP Address-and-Control-Field compression supported.
  - Mapping of HDLC data stream directly into DS3 or E3 frame.

- Receive Packet Processing:
  - Extraction of HDLC data stream from DS3 or E3 frame.
  - Detection and removal of HDLC flags, checks for Abort sequence and optional checking of length and CRC-16/32 field.
  - Optional PPP Address-and-Control-Field compression supported.
  - ✧Insertion of in-band messaging packets in the direction of the POS-PHY/UTOPIA-L2X port. Generation of CRC and length field for inserted packets[1)].

[1)] This is an option which is not available with the current firmware release.

System Interface

- UTOPIA Interface
  - 8/16-bit interface running up to 50 MHz.
  - Compliant to ATMF Utopia Level 2.
  - 16 Cell FIFO in both transmit and receive directions, ✧programmable FIFO depth[1)].
- POS-PHY Interface
  - Dual mode 8/16-bit interface running up to 50 MHz.
  - Compliant to POS-PHY Level 2.
  - Programmable burst size up to 64 bytes.
  - 896 byte FIFO in both transmit and receive directions, ✧programmable FIFO depth[1)].
- UTOPIA-L2X Interface
  - 8/16-bit interface running up to 50 MHz.
  - Based on UTOPIA Level 2 interface, extended for packet transfer capability.
  - Programmable chunk size of 16 ... 64 bytes.
  - 896 byte FIFO in both transmit and receive directions, ✧programmable FIFO depth[1)].
- Serial Bitstream Interface
  - Serial clock master and data interface for access to the DS3/E3 framer.
  - Serial clock slave and data interface for access to the cell/packet processor.

Microprocessor Interface

- 8/16-bit microprocessor slave interface.
- Multi-master access to external FLASH/EPROM when device is configured to boot independently.
- Eight configurable I/O ports that can be used to control LED's, provide boot up information or control external circuitry.

General

- JTAG
- Enables Boundary Scan Test Support (IEEE 1149.1) for low-cost product development.

Applications

- 3rd Generation Mobile Basestations etc.
- DSLAMs
- Multiservice Access Switches
- Edge Routers

1) This is an option which is not available with the current firmware release.

1.2 Logic Symbol

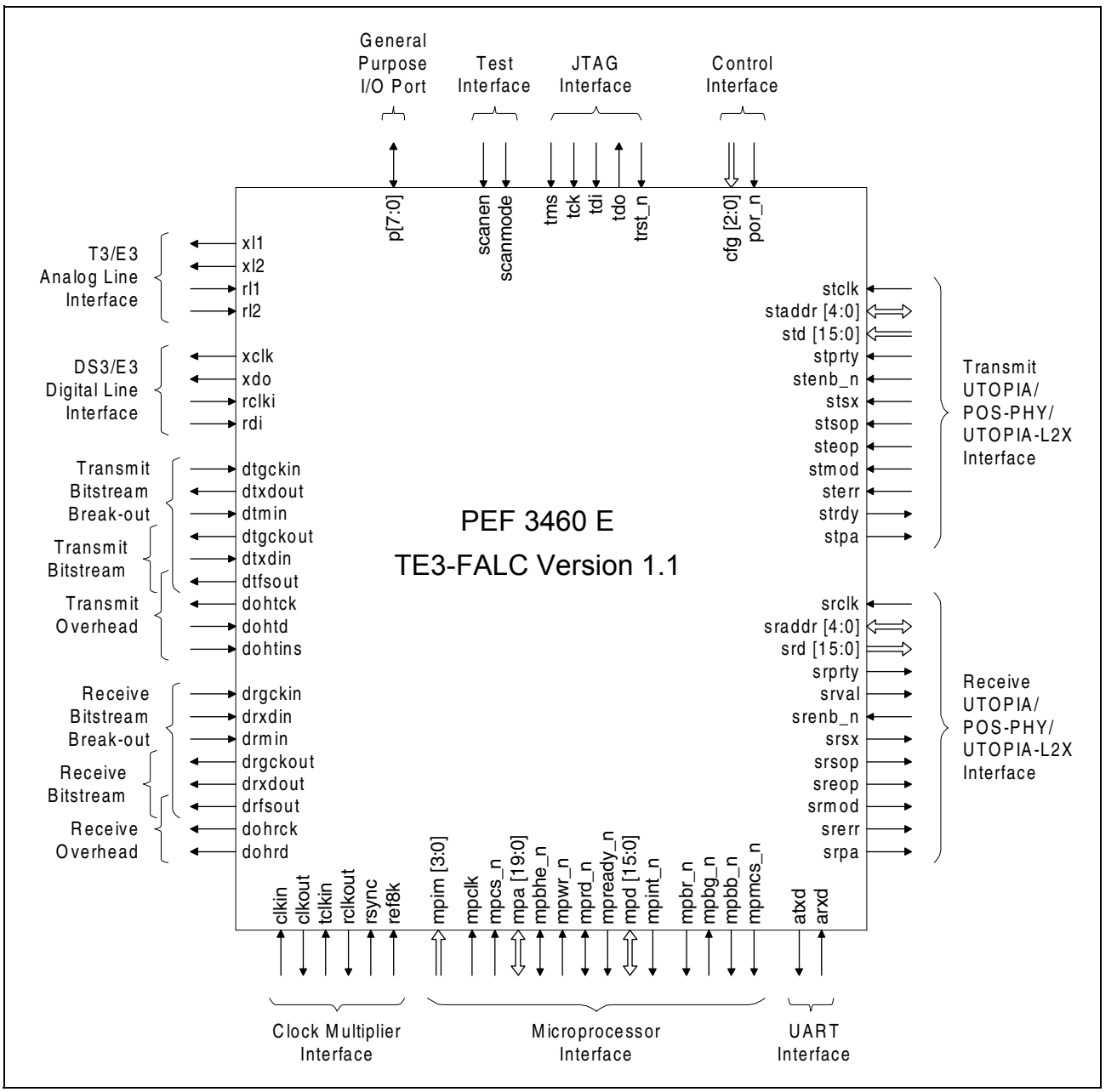


Figure 1 Logic Symbol

1.3 Minimum System

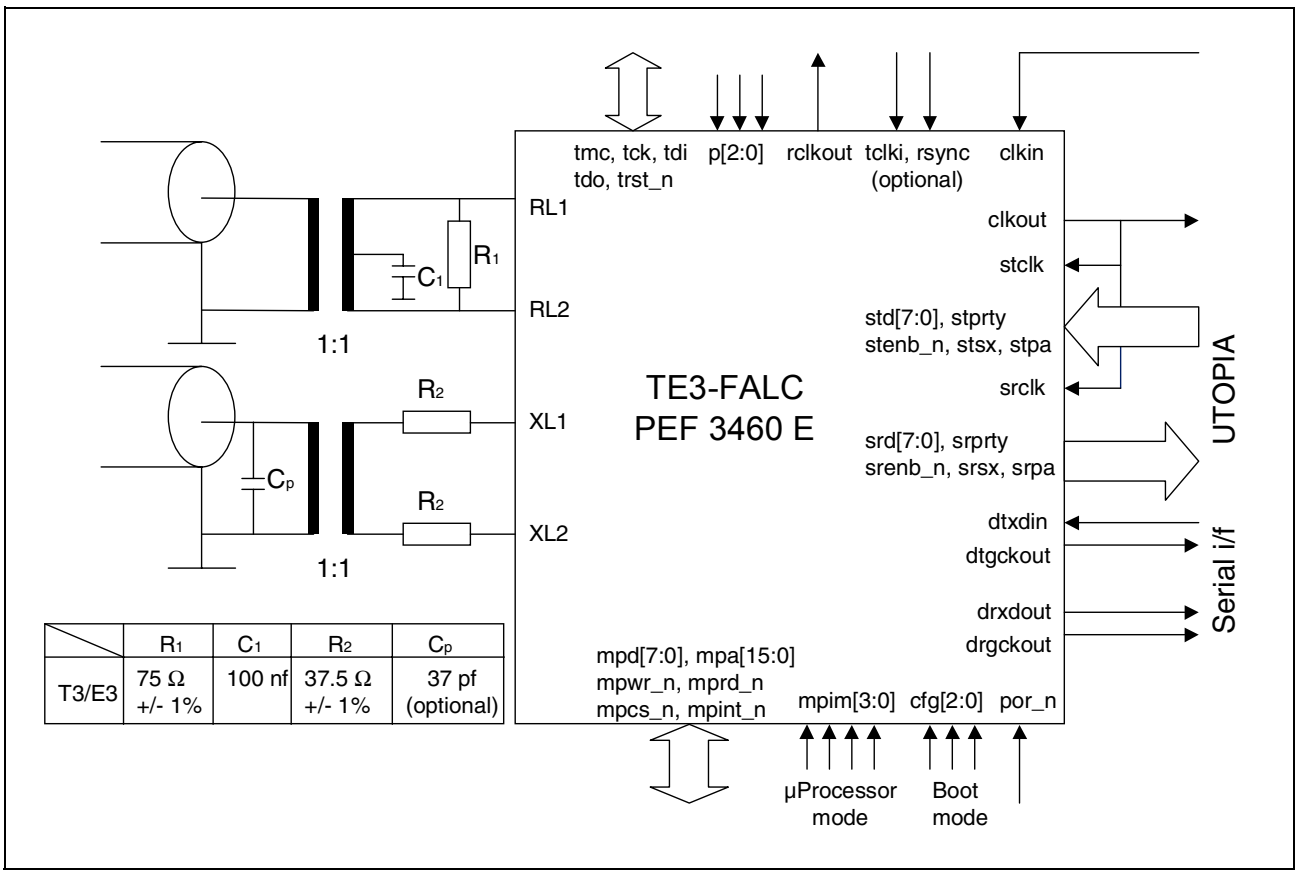


Figure 2 TE3-FALC Minimum System (UTOPIA or Serial Interface)

The above diagram shows the minimum system connectivity for the TE3-FALC showing all required signals to operate the device either with an UTOPIA interface or a serial interface. The TE3-FALC can operate from a single reference clock, CLKIN, and support software switching between T3 and E3 without any hardware change. When using a POS-PHY or UTOPIA-L2X interface the TE3-FALC is also able to switch between mapping ATM cells to PPP packets without any hardware change. Unused pins should be either left unconnected or tied to their inactive state as recommended in the pin description tables.

There are three hardware configuration selection pin groups. The first is P[2:0] which select the frequency range of CLKIN. The second is MPIM[3:0] which selects the type of microprocessor mode being used and the third, CFG[2:0], selecting the start up boot mode.

1.4 Typical Applications

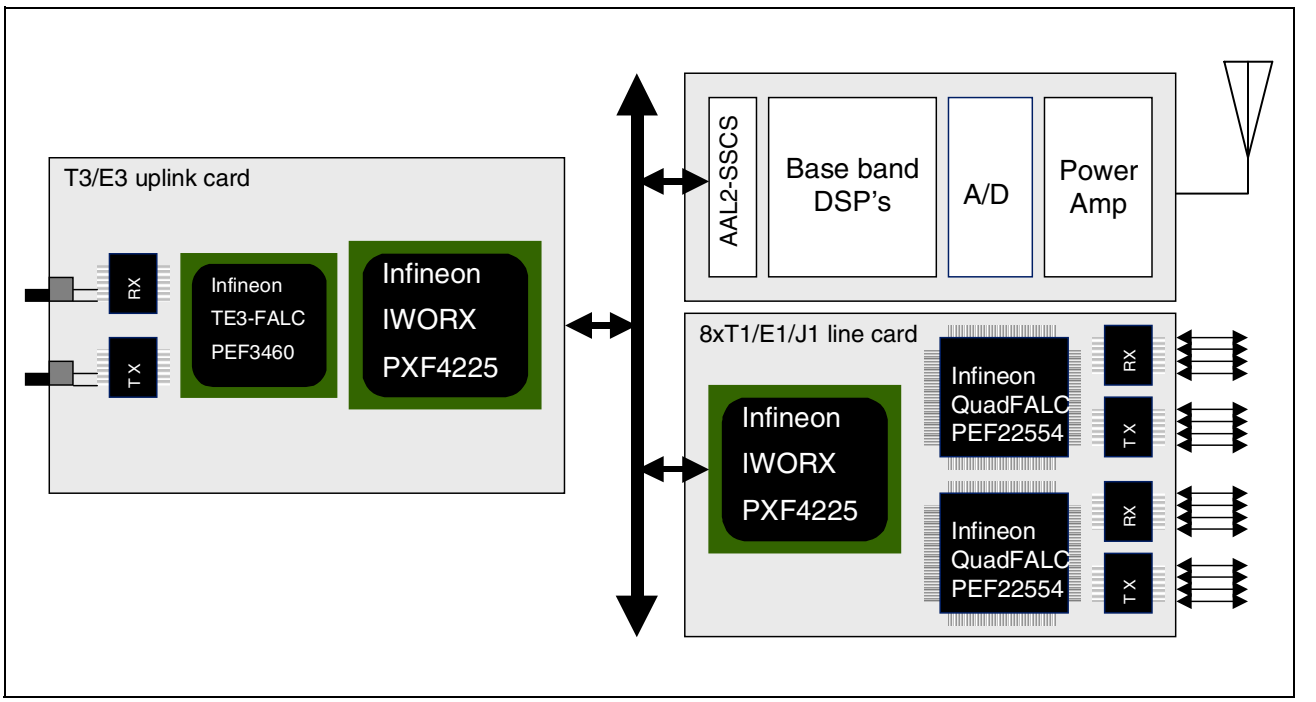


Figure 3 3G Mobile Base Station (AAL1/AAL2/AAL5)

The above diagram shows an application where the TE3-FALC provides the T3/E3 high speed WAN connection of a 3G Base stations, via point-point micro-wave equipment or SDH/SONET Optical transmission. Along with the very high integration (LIU, DJAT, Framer) the ability of the TE3-FALC to support both ATM and PPP/IP enables a single network interface to be designed that support today's ATM based networks and future proposed IP based networks.

The TE3-FALC compliments Infineon's IWORX device and QuadFALC. The IWORX provides a complete solution for AAL2 CPS, Traffic Management (CBR, VBR-rt etc.), I.610 OAM, Address Translation and IMA which is required for E1/T1 ATM based 3G Network interfaces. The IWORX also supports AAL1 allowing 2G equipment with TDM interfaces (Abis) to be connected to a 3G core network. The IWORX can also connect to other PHY devices like TE3-FALC via a second UTOPIA port. The QuadFALC framer and line interface component fulfills all required interfacing for four analog E1/T1/J1 lines. The powerful clocking options of QuadFALC have been included in TE3-FALC as well.

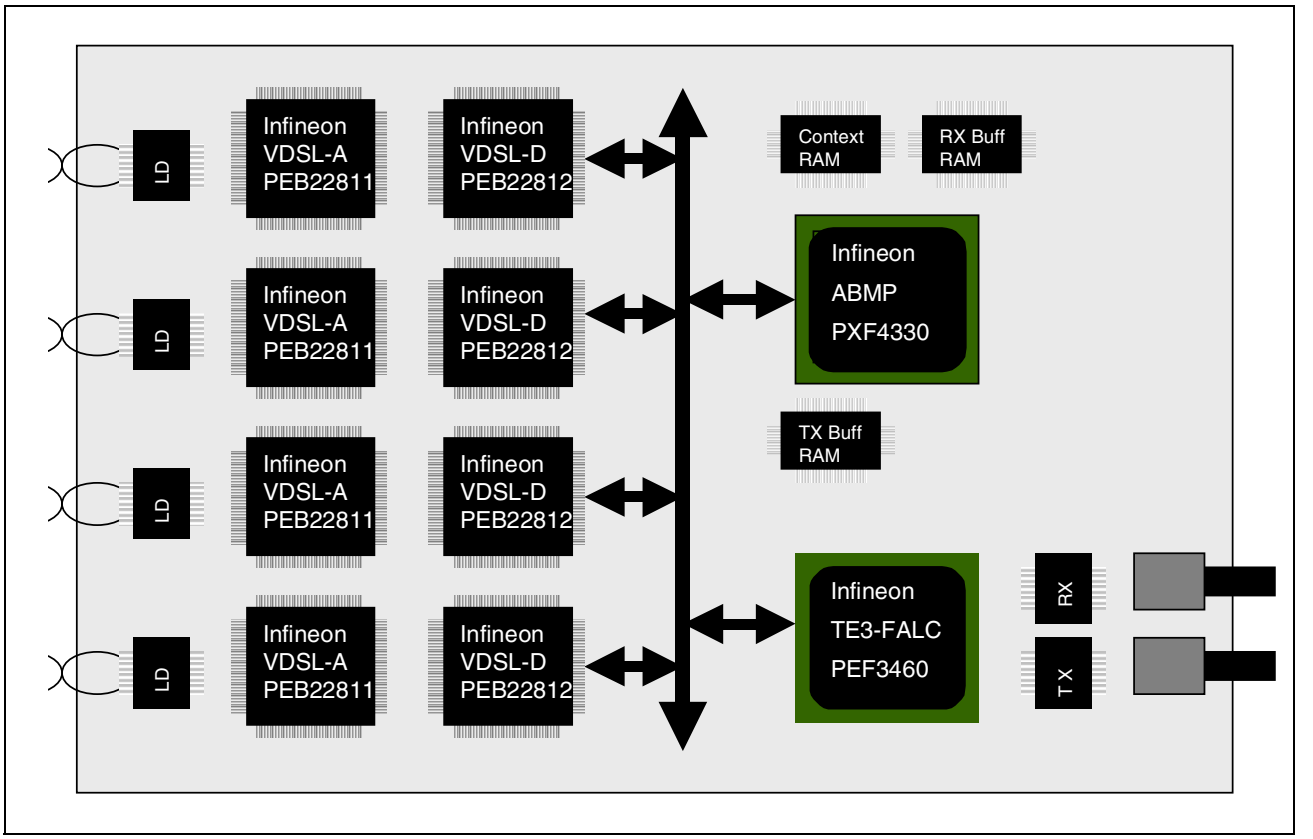


Figure 4 Customer based MDU with T3/E3 uplink

The above diagram shows an example of a four port Multi Dwelling Unit (MDU). The TE3-FALC provides the high speed connection to the core via SDH/SONET transmission equipment, the ABMP provides both traffic management and switching functionality.

The TE3-FALC supports not only ATM but also Frame Relay and PPP/IP which are popular alternatives for high speed links especially for equipment delivering Frame Relay over DSL or 10BaseS Ethernet. Integrated digital jitter attenuators enable the equipment to be in loop-timed mode and the integrated LIU supports plug and play installation for T3 (no requirement to measure cable length and set Line Build Out on the transmit pulse)

The ABMP provides full traffic management and switching for up to 31 UTOPIA L2 ports, it provides CBR, VBR-rt, VBR-nrt, ABR and UBR classes and supports IP Diffserv over ATM. Support of MPLS Label Switch Router (LSR) functionality is enabled with the support of VC-merging. Additional Infineon devices can be used along side the ABMP to add I.610 OAM (PXB 4340 AOP) and I.371 Policing and Address Translation (PXB 4350 ALP)

The VDSL transceivers solution from Infineon (PEB 22811 & PEB 22812) connect to the ABMP via a UTOPIA L2 interface. These interfaces can be exchanged for ADSL or G.SHDSL interfaces also available from Infineon.

2 Pin Descriptions

Table 1 gives an overview about the pin utilization per interface. Beyond the signal count of these interfaces there is a variety of test signals, which is made available either directly (using dedicated pins) or multiplexed with existing signal I/O pins. These test signals are not shown in Table 1. For complete pinning information, including multiplexed signals, driver strengths, pull-ups/pull-downs, refer to the following sections, which cover all pins.

Table 1 External Interfaces

Interface	Function	Signal Count
T3/E3 Analog Line Interface	Transmit tip/ring, receive tip/ring	4
DS3/E3 Digital Line Interface	Transmit and receive clock/data	4
DS3/E3 Bitstream and Overhead Access Interface	Optional access to DS3/E3 overhead and/or payload data (9 transmit, 8 receive pins)	17
Clock Multiplier Interface	Clock supplies and clock outputs	6
System Interface (UTOPIA / POS-PHY / UTOPIA-L2X)	Cell and packet based streaming interface. 16 bit data, 5 bit address per direction	62
Microprocessor Interface	Microprocessor interface in Intel/ Motorola format. 16 bit data, 20 bit address	52
JTAG Interface	Provides access to boundary scan	5
Control Interface	Reset, boot configuration	6
General Purpose I/O Port	General purpose I/O pins	8
UART Interface	Asynchronous TX and RX line	2
Test Interface	Test pins for manufacturer use only	2
Debug Interface (Reserved)		19

2.1 Pin Diagram

(top view)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	VSS	VDD	clkout	VDDPLL	mpim1	RSVD	mpready_n	mpwr_n	mpmcs_n	mpa16	mpa15	mpa12	mpa8	mpa5	VDD	mpd15	mpd12	mpd11	mpd6	mpd5
B	RSVD	ref8k	rsync	clkin	mpint_n	mpim0	mpbhe_n	VDD	mpbr_n	mpa17	mpa13	mpa11	mpa7	mpa4	mpa2	mpd14	mpd8	mpd7	mpd4	mpd2
C	N.C.	RSVD	N.C.	rclkout	core_ratio	mpim3	mpcs_n	mprd_n	mpbg_n	mpa18	mpa14	mpa10	mpa6	mpa3	mpa0	mpd13	mpd9	mpd3	mpd1	sterr
D	N.C.	RSVD	RSVD	VSS	tclkin	VDDP	mpim2	VSS	mpbb_n	mpa19	VDDP	mpa9	VSS	mpa1	VDDP	mpd10	VSS	mpd0	VDD	steop
E	N.C.	N.C.	N.C.	RSVD	*Clock Multiplier Interface*					*Microprocessor Interface*							mpclk	stmod	strdy	stenb_n
F	RSVD	RSVD	RSVD	VDDP													VDDP	stsop	RSVD	stpa
G	VDD	rdi	rclki	RSVD													stsx	RSVD	staddr0	staddr1
H	VDDA	xclk	xdo	VSS	*T3/E3 Line Interface*												VSS	staddr2	staddr3	VDD
J	xl1	VDDA	RSVD	RSVD					VSS	VSS	VSS	VSS					staddr4	RSVD	stprty	std0
K	rl1	xl2	N.C.	VDDP					VSS	VSS	VSS	VSS			*Streaming Interface*		std1	std2	std3	std4
L	rl2	VDDA	VDDA	VDD					VSS	VSS	VSS	VSS			*(UTOPIA / POS-PHY / UTOPIA-L2X)*		VDDP	std6	std7	std5
M	VDD	N.C.	dtgckin	dtxdout	*Bitstream and Overhead Access Interface*				VSS	VSS	VSS	VSS					std11	std10	std9	std8
N	VDD	dtxdin	dtfsout	VSS													VSS	std13	VDD	std12
P	dtmin	dtgckout	dohtd	drxdout													srd14	stclk	std15	std14
R	dohtck	dohtins	drxdin	VDDP													VDDP	srd13	srd15	srclk
T	drgckin	drfsout	drgckout	scanmode	*Test Pins*		*Config & Misc Pins*			*Debug Pins (reserved)*							srd7	srd10	srd11	srd12
U	drmin	dohrck	scanen	VSS	arxd	VDDP	p6	VSS	RSVD	VDDP	RSVD	RSVD	VSS	srenb_n	VDDP	sraddr4	VSS	srd6	VDD	srd9
V	dohrd	tdo	tck	atxd	p2	p5	cfg1	RSVD	RSVD	RSVD	RSVD	RSVD	srerr	srsop	RSVD	sraddr1	RSVD	srd1	srd5	srd8
W	tdi	tms	VDD	RSVD	p3	p7	cfg2	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	sreop	srsx	srpa	sraddr2	srprty	srd2	srd4
Y	trst_n	por_n	p0	p1	p4	cfg0	RSVD	RSVD	VDD	RSVD	RSVD	RSVD	RSVD	srmod	srval	VDD	sraddr0	sraddr3	srd0	srd3

Figure 5 Pin Configuration PBGA-272-4 Package

2.2 Pin Definitions and Functions

The following tables contain the pin information. The 1st column contains the ball number, the 2nd the pin name.

The 3rd column describes if it is an input (I), output (O) or bidirectional (I/O) pin. If it's an output or I/O the 4th column lists the driver strength. Strengths of the different driver types are specified in **Chapter 7.4**.

The 5th column lists if the pin has an internal pull-up PU or an internal pull-down PD. Strengths of the pull-up/pull-down transistors are specified in **Chapter 7.4**. To override an internal pull-up (pull-down), connect an external pull-down (pull-up) resistor of 10 kΩ to the corresponding pin.

The last column contains a short description of the pin function.

Signal Type Definitions:

I	**Input** is a standard input-only signal.
O	**Totem Pole Output** is a standard active driver.
I/O	**I/O** is a bidirectional input/output pin.

Signal Type Attributes:

t/s	**Tri-State capability**: The corresponding pin gets tri-stated during operation.
o/d	**Open Drain** allows multiple devices to share as a wire-OR. A pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.

Signal Name Conventions:

RSVD_n **Reserved Pin n**
Such pins are bonded with silicon and are for vendor specific use only. Reserved pins shall be left unconnected unless stated different in the pin description tables below.

Note: The signal type definition specifies the functional usage of a pin. This does not necessarily reflect the implementation of a pin, e.g. a pin defined of signal type 'Input' may be implemented with a bidirectional pad.

2.2.1 T3/E3 Analog Line Interface

Table 2 T3/E3 Analog Line Interface

Ball No.	Name	In/Out	Driver	Pullup/ -down	Function
J1	XL1	O (analog)			**Transmit Line 1 (ring)** Analog output to the external transformer (transmit bipolar ring). XL1 can be switched into inactive mode.
K2	XL2	O (analog)			**Transmit Line 2 (tip)** Analog output to the external transformer (transmit bipolar tip). XL2 can be switched into inactive mode.
K1	RL1	I (analog)			**Line Receiver 1 (ring)** Analog input from the external transformer (receive bipolar ring). The signal at RL1 must be coded according to B3ZS or HDB3.
L1	RL2	I (analog)			**Line Receiver 2 (tip)** Analog input from the external transformer (receive bipolar tip). The signal at RL1 must be coded according to B3ZS or HDB3.
F3	RSVD_F3	I		PU	
G4	RSVD_G4	I		PU	
J4	RSVD_J4	O (analog)			
J3	RSVD_J3	I/O (analog)			*A pull-down resistor is required for this pin.*
C2	RSVD_C2	O	D		
F2	RSVD_F2	I		PU	
F1	RSVD_F1	I		PU	*A pull-down resistor is required for this pin.*

2.2.2 DS3/E3 Digital Line Interface

Table 3 DS3/E3 Digital Line Interface

Ball No.	Name	In/Out	Driver	Pullup / -down	Function
G3	RCLKI	I		PU	**Digital Receive Clock** RDI data is clocked in with this clock
G2	RDI	I		PU	**Digital Receive Data Input** NRZ coded data is expected on this pin
H2	XCLK	O	D		**Digital Transmit Clock**
H3	XDO	O	D		**Digital Transmit Data Output** NRZ coded data is output on this pin
B1	RSVD_B1	O	D		
D2	RSVD_D2	O			
D3	RSVD_D3	O			
E4	RSVD_E4	O			

2.2.3 DS3/E3 Bitstream and Overhead Access Interface

Table 4 DS3/E3 Bitstream and Overhead Access Interface

Ball No.	Name	In/Out	Driver	Pullup / -down	Function
M3	DTGCKIN	I		PD	**Transmit Payload Gapped Clock In**
M4	DTXDOUT	O	E		**Transmit Payload Data Out**
N2	DTXDIN	I		PD	**Transmit Payload Data In**
N3	DTFSOUT	O	E		**Transmit Frame Start Marker Out**
P1	DTMIN	I		PD	**Transmit Payload Marker In**
P2	DTGCKOUT	O	E		**Transmit Payload Gapped Clock Out**

Table 4 DS3/E3 Bitstream and Overhead Access Interface (cont'd)

Ball No.	Name	In/Out	Driver	Pullup / -down	Function
R1	DOHTCK	O	E		**Transmit Overhead Gapped Clock Out**
P3	DOHTD	I		PD	**Transmit Overhead Data In**
R2	DOHTINS	I		PD	**Transmit Overhead Insertion Marker**
T1	DRGCKIN	I		PD	**Receive Payload Gapped Clock In**
P4	DRXDOUT	O	E		**Receive Payload Data Out**
R3	DRXDIN	I		PD	**Receive Payload Data In**
T2	DRFSOUT	O	E		**Receive Frame Start Marker Out**
U1	DRMIN	I		PD	**Receive Payload Marker In**
T3	DRGCKOUT	O	E		**Receive Payload Gapped Clock Out**
U2	DOHRCK	O	E		**Receive Overhead Gapped Clock Out**
V1	DOHRD	O	E		**Receive Overhead Data Out**

2.2.4 Clock Multiplier Interface

Table 5 Clock Multiplier Interface

Ball No.	Name	In/Out	Driver	Pullup / -down	Function
C5	CORE_ RATIO	I		PU	**Core Clock Ratio** '0' : Core Clock = 2 × System Clock '1' : Core Clock = System Clock For some service upgrades it might be required that the on-chip microprocessor runs at double speed. *Recommendation for board layout: provide soldering pad for pull-down resistor that can optionally be equipped.*
B4	CLKIN	I		PU	**Main Input Clock** This clock input drives the PLL which generates internal clocks. In this case the clock can have a range of 4 ... 52 MHz. Optionally this input, internally divided by 2, can directly be used as system clock. Pins P[2:0] have to be configured depending on the CLKIN frequency, see **Table 12**.
A3	CLKOUT	O	B		**Global Clock Output** This programmable clock signal can output any one of the internal clocks, divided by an arbitrary factor.
D5	TCLKIN	I		PU	**Transmit Clock Input** Optionally this input can be used as source for the transmit line clock. **Transmit Reference Clock** Optionally this clock with a range of 8 kHz to 52 MHz can be used as a reference clock for the transmit DJAT PLL.

Table 5 Clock Multiplier Interface (cont'd)

Ball No.	Name	In/Out	Driver	Pullup / -down	Function
C4	RCLKOUT	O	D		**Recovered Line Clock Output** This pin can be programmed to output the recovered receive clock (direct or via DJAT), divided by an arbitrary factor.
B3	RSYNC	I		PU	**Receive Reference Clock** Optionally this clock with a range of 8 kHz to 52 MHz can be used as a reference clock for the receive DJAT PLL.
B2	REF8K	I		PU	**PLCP 8 kHz Reference Clock**

2.2.5 System Interface (UTOPIA / POS-PHY / UTOPIA-L2X)

These pins carry different signals depending on the interface mode. Please refer to **Table 31** and **Table 32** for the corresponding signal naming.

Table 6 System Interface Receive (UTOPIA/POS-PHY/UTOPIA-L2X)

Ball No.	Name	In/Out	Driver	Pullup / -down	Function
R20	SRCLK	I			**Receive Clock**
Y17	SRADDR0	I			**UTOPIA Receive Address** *A pull-down resistor is required for unused address pins, especially in UTOPIA Level 1 mode, where no address is defined!*
V16	SRADDR1	I			
W17	SRADDR2	I			
Y18	SRADDR3	I			
U16	SRADDR4	I			
V17	RSVD_V17	I			*A pull-down resistor is required for this pin.*

Table 6 System Interface Receive (UTOPIA/POS-PHY/UTOPIA-L2X) (cont'd)

Ball No.	Name	In/Out	Driver	Pullup / -down	Function
Y19	SRD0	O	C		**Receive Data (8-/16-bit mode)** Least significant byte [7:0] in 16-bit mode. Receive data [7:0] in 8-bit mode.
V18	SRD1	O	C		
W19	SRD2	O	C		
Y20	SRD3	O	C		
W20	SRD4	O	C		
V19	SRD5	O	C		
U18	SRD6	O	C		
T17	SRD7	O	C		
V20	SRD8	O	C		**Receive Data (16-bit mode only)** Most significant byte [15:8] in 16-bit mode.
U20	SRD9	O	C		
T18	SRD10	O	C		
T19	SRD11	O	C		
T20	SRD12	O	C		
R18	SRD13	O	C		
P17	SRD14	O	C		
R19	SRD15	O	C		
W18	SRPRTY	O	C		**Receive Parity**
Y15	SRVAL	O	C		**Receive Data Valid**
U14	$\overline{\text{SRENB}}$	I			**Receive Enable**
W15	SRSX/SRSOC	O	C		**Receive Start Of Cell / Chunk**
V14	SRSOP	O	C		**Receive Start Of Packet**
W14	SREOP	O	C		**Receive End Of Packet**
Y14	SRMOD	O	C		**Receive Modulo Byte Count**
V13	SRERR	O	C		**Receive Error**
W16	SRPA	O	C		**Receive Cell / Packet Available**
V15	RSVD_V15	O	C		

Table 7 System Interface Transmit (UTOPIA/POS-PHY/UTOPIA-L2X)

Ball No.	Name	In/Out	Driver	Pullup / -down	Function
P18	STCLK	I			**Transmit Clock**
G19	STADDR0	I			**Transmit Address** *A pull-down resistor is required for unused address pins, especially in UTOPIA Level 1 mode, where no address is defined!*
G20	STADDR1	I			
H18	STADDR2	I			
H19	STADDR3	I			
J17	STADDR4	I			
J18	RSVD_J18	I			*A pull-down resistor is required for this pin.*
J20	STD0	I			**Transmit Data (8-/16-bit mode)** Least significant byte [7:0] in 16-bit mode. Transmit data [7:0] in 8-bit mode.
K17	STD1	I			
K18	STD2	I			
K19	STD3	I			
K20	STD4	I			
L20	STD5	I			
L18	STD6	I			
L19	STD7	I			
M20	STD8	I			**Transmit Data (16-bit mode only)** Most significant byte [15:8] in 16-bit mode. *A pull-up resistor is required for these pins in 8-bit mode.*
M19	STD9	I			
M18	STD10	I			
M17	STD11	I			
N20	STD12	I			
N18	STD13	I			
P20	STD14	I			
P19	STD15	I			
J19	STPRTY	I			**Transmit Parity** *A pull-up resistor is required for this pin if parity check is not used.*
E20	$\overline{\text{STENB}}$	I			**Transmit Enable**

Table 7 System Interface Transmit (UTOPIA/POS-PHY/UTOPIA-L2X) (cont'd)

Ball No.	Name	In/Out	Driver	Pullup / -down	Function
G17	STSX/STSOC	I			**Transmit Start Of Cell / Chunk** *A pull-down resistor is required for this pin in POS-PHY mode.*
F18	STSOP	I			**Transmit Start Of Packet** *A pull-down resistor is required for this pin in UTOPIA mode.*
D20	STEOP	I			**Transmit End Of Packet** *A pull-down resistor is required for this pin in UTOPIA mode.*
E18	STMOD	I			**Transmit Modulo Byte Count** *A pull-down resistor is required for this pin in UTOPIA mode.*
C20	STERR	I			**Transmit Error** *A pull-down resistor is required for this pin in UTOPIA mode and if transmit error signalling is not used.*
E19	STRDY	O	C		**Transmit Ready**
F20	STPA	O	C		**Transmit Cell / Packet Available**
F19	RSVD_F19	O	C		
G18	RSVD_G18	O	C		

2.2.6 Microprocessor Interface

These pins carry different signals depending on the interface mode. Please refer to **Table 33** for the corresponding signal naming.

Table 8 Microprocessor Interface

Ball No.	Name	In/Out	Driver	Pullup / -down	Function
B6	MPIM0	I		PD	**MPI Mode (1:0)** '00' = reserved. '10' = Intel demux mode '01' = Motorola synchronous '11' = Motorola asynchronous
A5	MPIM1	I		PU	

Table 8 Microprocessor Interface (cont'd)

Ball No.	Name	In/Out	Driver	Pullup / -down	Function
D7	MPIM2	I		PD	**MPI Mode #2** This mode pin is reserved and should be left unconnected.
C6	MPIM3	I		PD	**MPI Mode #3** '0' = 16-bit data bus width '1' = 8-bit data bus width
A6	MPIM4	I/O	D	PU	**MPI Mode #4** '0' = Host processor is little endian '1' = Host processor is big endian *This pin has no function in V1.1 of TE3-FALC. In future revisions it shall redundantize access to register* ***MCR (page 82)****. For backward compatibility, the setting via register MCR is still possible.*
E17	MPCLK	I		PU	**MPI Clock** (Motorola sync)
C7	$\overline{\text{MPCS}}$	I		PU	**Slave Chip Select**
C15	MPA0	I/O	D		**Address Bus** For slave accesses to the TE3-FALC (input address), only lines MPA[15:0] need to be connected. Slave access including the lines MPA[19:16] is provided for manufacturer use only. For TE3-FALC master read accesses (output address) to an optional boot EPROM lines MPA[16:0] are available which limits the loadable firmware image to 128 kB in size.
D14	MPA1	I/O	D		
B15	MPA2	I/O	D		
C14	MPA3	I/O	D		
B14	MPA4	I/O	D		
A14	MPA5	I/O	D		
C13	MPA6	I/O	D		
B13	MPA7	I/O	D		
A13	MPA8	I/O	D		
D12	MPA9	I/O	D		
C12	MPA10	I/O	D		
B12	MPA11	I/O	D		
A12	MPA12	I/O	D		
B11	MPA13	I/O	D		
C11	MPA14	I/O	D		
A11	MPA15	I/O	D		

Table 8 Microprocessor Interface (cont'd)

Ball No.	Name	In/Out	Driver	Pullup / -down	Function
A10	MPA16	I/O	D		*A pull-down resistor is required for unused address pins.*
B10	MPA17	I/O	D		
C10	MPA18	I/O	D		
D10	MPA19	I/O	D		
B7	$\overline{\text{MPBHE}}$ $\overline{\text{MPBLE}}$ MPTSIZ0	I/O	D		**Byte High Enable** (Intel) *A pull-up resistor is required for this pin in 8-bit mode.* **Byte Low Enable** (Motorola async) *A pull-up resistor is required for this pin in 8-bit mode.* **Transfer Size 0** (Motorola sync) In 16-bit Motorola sync mode, only 16-bit accesses are supported. *A pull-up resistor is required for this pin in 8-bit mode.*
A8	$\overline{\text{MPWR}}$ MPR/$\overline{\text{W}}$	I/O	D		**Write Strobe** (Intel) **Read/$\overline{\text{Write}}$ Select** (Motorola)
C8	$\overline{\text{MPRD}}$ $\overline{\text{MPDS}}$ $\overline{\text{MPTS}}$	I/O	D		**Read Strobe** (Intel) **Data Strobe** (Motorola async) **Transfer Start** (Motorola sync)
A7	$\overline{\text{MPREADY}}$ $\overline{\text{MPDTACK}}$ $\overline{\text{MPTA}}$	O (t/s)	D		**Ready** (Intel) **Transfer Ack** (Motorola async) **Transfer Ack** (Motorola sync)
D18	MPD0	I/O	D		**Data Bus, Low Byte** (8-/16-bit mode)
C19	MPD1	I/O	D		
B20	MPD2	I/O	D		
C18	MPD3	I/O	D		
B19	MPD4	I/O	D		
A20	MPD5	I/O	D		
A19	MPD6	I/O	D		
B18	MPD7	I/O	D		

Table 8 Microprocessor Interface (cont'd)

Ball No.	Name	In/Out	Driver	Pullup / -down	Function
B17	MPD8	I/O	D		**Data Bus, High Byte** (16-bit mode only) *A pull-up resistor is required for these pins in 8-bit mode.*
C17	MPD9	I/O	D		
D16	MPD10	I/O	D		
A18	MPD11	I/O	D		
A17	MPD12	I/O	D		
C16	MPD13	I/O	D		
B16	MPD14	I/O	D		
A16	MPD15	I/O	D		
B5	$\overline{\text{MPINT}}$	O, o/d	D		**Interrupt Output** The interrupt pin can be programmed to be open drain or push/pull active high or low.
A9	$\overline{\text{MPMCS}}$	O	D		**Master Chip Select** Only needed if the EPROM boot function is used.
B9	$\overline{\text{MPBR}}$ MPHOLD	O	D		**Bus Request** (Motorola) Only needed if the EPROM boot function is used and multiple masters share the bus. **Bus Hold Request** (Intel) Only needed if the EPROM boot function is used and multiple masters share the bus.

Table 8 Microprocessor Interface (cont'd)

Ball No.	Name	In/Out	Driver	Pullup / -down	Function
C9	$\overline{\text{MPBG}}$ MPHLDA	I			**Bus Grant** (Motorola) Only needed if the EPROM boot function is used. If TE3-FALC is the only bus master, this input shall be connected to the $\overline{\text{MPBR}}$ output. *A pull-up resistor is required for this pin if unused.* **Bus Hold Acknowledge** (Intel) Only needed if the EPROM boot function is used. If TE3-FALC is the only bus master, this input shall be connected to the MPHOLD output. *A pull-down resistor is required for this pin if unused.*
D9	$\overline{\text{MPBB}}$	O (o/d)	D		**Bus Busy** (Motorola) Only needed if the EPROM boot function is used. *A pull-up resistor is required for this pin.*

2.2.7 JTAG Interface

Table 9 JTAG Interface

Ball No.	Name	In/Out	Driver	Pullup / -down	Function
V2	TDO	O	E		**Test Access Port Data Out**
W1	TDI	I		PU	**Test Access Port Data In**
V3	TCK	I		PU	**Test Access Port Clock**
W2	TMS	I		PU	**Test Access Port Mode Select**
Y1	$\overline{\text{TRST}}$	I		PU	**Test Access Port Reset**

2.2.8 Debug Interface (Reserved)

This debug interface is for manufacturer use only. Pins can be left unconnected.

Table 10 Debug Interface

Ball No.	Name	In/Out	Driver	Pullup / -down	Function
V8	RSVD_V8	I		PU	
W8	RSVD_W8	I		PU	
Y8	RSVD_Y8	O	C		
U9	RSVD_U9	O	C		
V9	RSVD_V9	O	C		
W9	RSVD_W9	O	C		
W10	RSVD_W10	O	C		
V10	RSVD_V10	O	C		
Y10	RSVD_Y10	O	C		
Y11	RSVD_Y11	O	C		
W11	RSVD_W11	O	C		
V11	RSVD_V11	O	C		
U11	RSVD_U11	O	C		
Y12	RSVD_Y12	O	C		
W12	RSVD_W12	O	C		
V12	RSVD_V12	O	C		
U12	RSVD_U12	O	C		
Y13	RSVD_Y13	O	C		
W13	RSVD_W13	O	C		

2.2.9 Control Interface

Table 11 Control Interface

Ball No.	Name	In/Out	Driver	Pullup / -down	Function
Y2	$\overline{\text{POR}}$	I			**Power-On Reset** The power-on reset should be active as long as the supply voltage has not yet stabilized.
W4	RSVD_W4	I/O (o/d)	E	PU	
Y6	CFG0	I		PU	**Boot Mode Configuration** Pins CFG[2:0] define the boot procedure for TE3-FALC's on-chip microprocessor. '001' : boot from external host via DCI (default). '011' : boot from external EPROM (TE3-FALC is master) others reserved.
V7	CFG1	I		PD	
W7	CFG2	I		PD	
Y7	RSVD_Y7	I		PU	

2.2.10 General Purpose I/O Port

Table 12 General Purpose I/O Port

Ball No.	Name	In/Out	Driver	Pullup / -down	Function
Y3	P0	I/O	E	PU	**PLL Clock Base** Depending on the clock frequency supplied to pin CLKIN set pins P(2:0) to ’000’ : reserved. ’001’ : reserved. ’010’ : 4 MHz < CLKIN ≤ 8 MHz ’011’ : 8 MHz < CLKIN ≤ 16 MHz ’100’ : 16 MHz < CLKIN ≤ 32 MHz ’101’ : 32 MHz < CLKIN ≤ 52 MHz ’110’ : reserved. ’111’ : Analog PLL bypassed; system clock is CLKIN/2. *Recommendation for board layout: provide soldering pads for pull-down resistors that can optionally be equipped.* **General Purpose I/O Port** After boot process, each of these pins can be independently configured.
Y4	P1	I/O	E	PU	
V5	P2	I/O	E	PU	
W5	P3	I/O	E	PU	**General Purpose I/O Port** Each of these pins can be independently configured.
Y5	P4	I/O	E	PU	
V6	P5	I/O	E	PU	
U7	P6	I/O	E	PU	
W6	P7	I/O	E	PU	

2.2.11 UART Interface

Table 13 UART Interface

Ball No.	Name	In/Out	Driver	Pullup / -down	Function
V4	ATXD	O	E		**Asynchronous Transmit Data**
U5	ARXD	I		PU	**Asynchronous Receive Data**

2.2.12 Test Interface

Table 14 Test Interface

Ball No.	Name	In/Out	Driver	Pullup / -down	Function
T4	SCANMODE	I			**Scan Mode** Test pin for manufacturer use only. Connect to V_{SS}.
U3	SCANEN	I			**Scan Enable** Test pin for manufacturer use only. Connect to V_{SS}.

2.2.13 Power Supply

Table 15 Power Supply

Ball No.	Name	Function
A1, D4, D8, D13, D17, H4, H17, N4, N17, U4, U8, U13, U17, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12	V_{SS}	**Common Ground Rail**
A2, N1, Y16, U19, N19, H20, D19, A15, B8, Y9, W3, L4, G1, M1	V_{DD}	**Core Power Supply, 1.8 V**
D6, D11, D15, F4, F17, K4, L17, R4, R17, U6, U10, U15	V_{DDP}	**I/O Power Supply, 3.3 V**
A4	V_{DDPLL}	**Analog PLL Power Supply, 3.3 V** Supply for PLL in Clocking Unit
L2, L3, H1, J2	V_{DDA}	**Analog LIU Power Supply, 3.3 V**

2.2.14 No Connect Pins

Table 16 No Connect Pins

Ball No.	Name	Function
C1, C3, D1, E1, E2, E3, K3, M2	NC_C1, NC_C3, ..., NC_M2	**No Connect Pins** Such pins are not bonded with the silicon. No-Connect pins might be used for additional functionality in later versions of the device. Leaving them unconnected will guarantee hardware compatibility to later device versions.

3 Functional Description

3.1 Functional Overview

3.2 Block Diagram

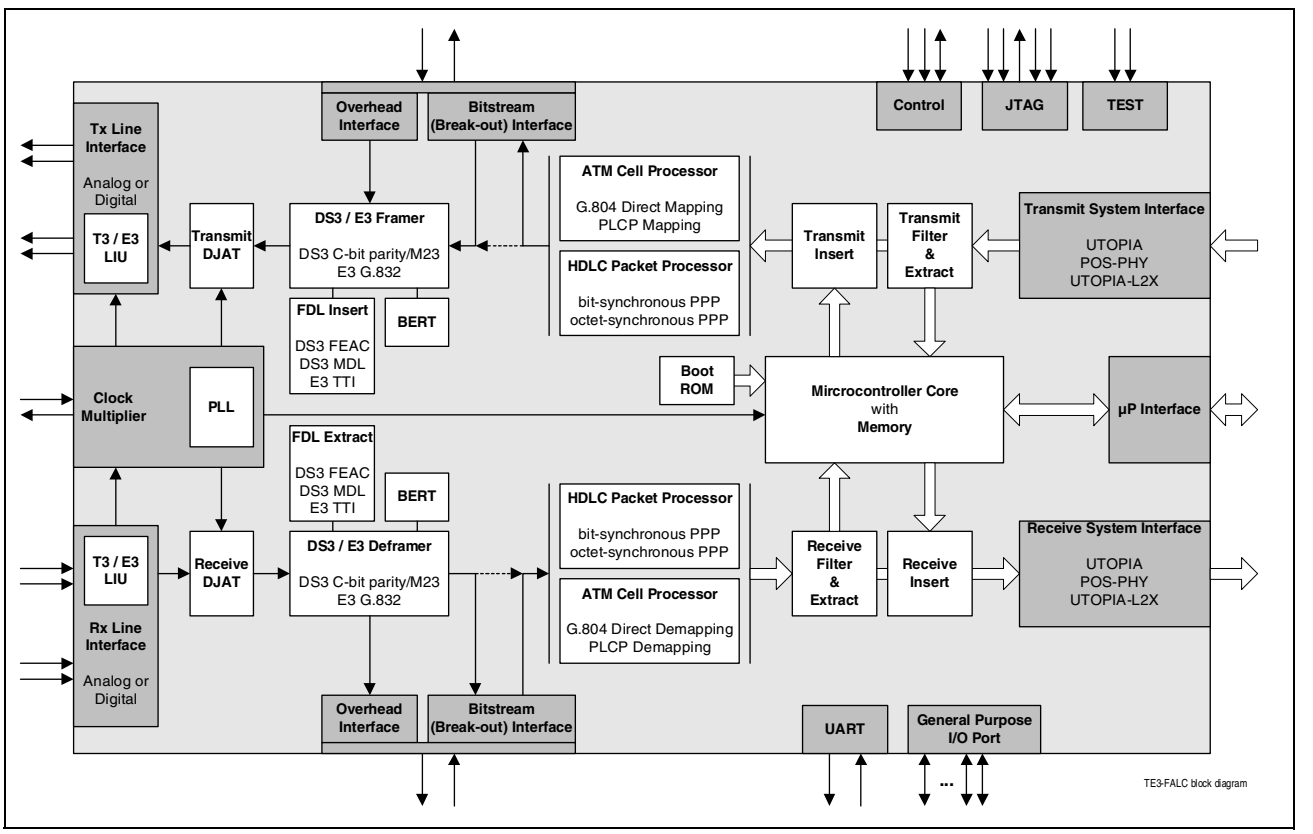


Figure 6 TE3-FALC Block Diagram

3.3 Functional Blocks

The functional blocks described in this section are shown as white boxes in the block diagram, **Figure 6**.

For a description of the external hardware interfaces shown as greyed boxes in the above block diagram refer to **“Hardware Interface Description” on Page 56**.

3.3.1 Analog T3/E3 Line Interface Unit (LIU)

This contains analog and digital functional blocks, which are configured and controlled via software.

The main interfaces are

- Receive Line Interface

- Transmit Line Interface

The main internal functional blocks are

- Analog line receiver with noise & crosstalk filter, equalizer network and clock/data recovery
- Analog line driver with programmable pulse shaper
- Central clock generation module
- Maintenance functions (e.g. loop switching local or remote)

3.3.2 Jitter Attenuator (DJAT)

3.3.2.1 Receive DJAT

The receive jitter attenuator is placed in the receive path. The working clock is an internally generated high frequency clock based on the clock provided on pin CLKIN. The jitter attenuator meets the E3 requirements of G.823 and ETSI TBR24 and DS3 requirements of GR-499-CORE. The internal PLL circuitry generates a "jitter-free" output clock which is directly dependent on the phase difference of the incoming clock and the jitter attenuated clock. The receive jitter attenuator can be synchronized either on the extracted receive clock RCLK or on a programmable receive reference clock, between 52 MHz and 8 kHz clock, provided on pin RSYNC. The jitter attenuated clock can be output on pin RCLKOUT and optionally divided down to an 8 kHz clock. The receive jitter attenuator circuitry attenuates the incoming jittered clock starting at 20 Hz jitter frequency with 20 dB per decade fall-off. Wander with a jitter frequency below 20 Hz is passed un-attenuated. ✧A holdover mode or a center mode is possible in case of lost reference clock[1)]. The RX DJAT center mode clock frequency is derived from CLKIN. The intrinsic jitter in the absence of any input jitter is < 0.06 UI.

3.3.2.2 Transmit DJAT

The transmit jitter attenuator circuitry generates a "jitter-free" transmit clock and meets the following requirements for E3: ETSI TBR24 and DS3: GR-499-CORE. The TX DJAT circuitry works internally with the same high frequency clock as the receive jitter attenuator. It synchronizes either to the transmit reference clock provided on pin TCLKIN, or the clock recovery PLL output, or to the RX DJAT output clock (remote loop/ loop-timed). ✧A holdover mode or a center mode is possible in case of lost reference clock[1)]. The TX DJAT center mode clock frequency is derived from CLKIN.

The TX DJAT attenuates the incoming clock jitter starting at 20 Hz with 20 dB per decade fall-off. Wander with a jitter frequency below 20 Hz is passed transparently.

1) This is an option which is not available with the current firmware release.

The jitter attenuated clock is output on pin XCLK. ✧The transmit jitter attenuator can be disabled[1]. In that case data is read from the transmit elastic buffer with the clock sourced on pin TCLKIN (34 MHz for E3 or 45 MHz for DS3).

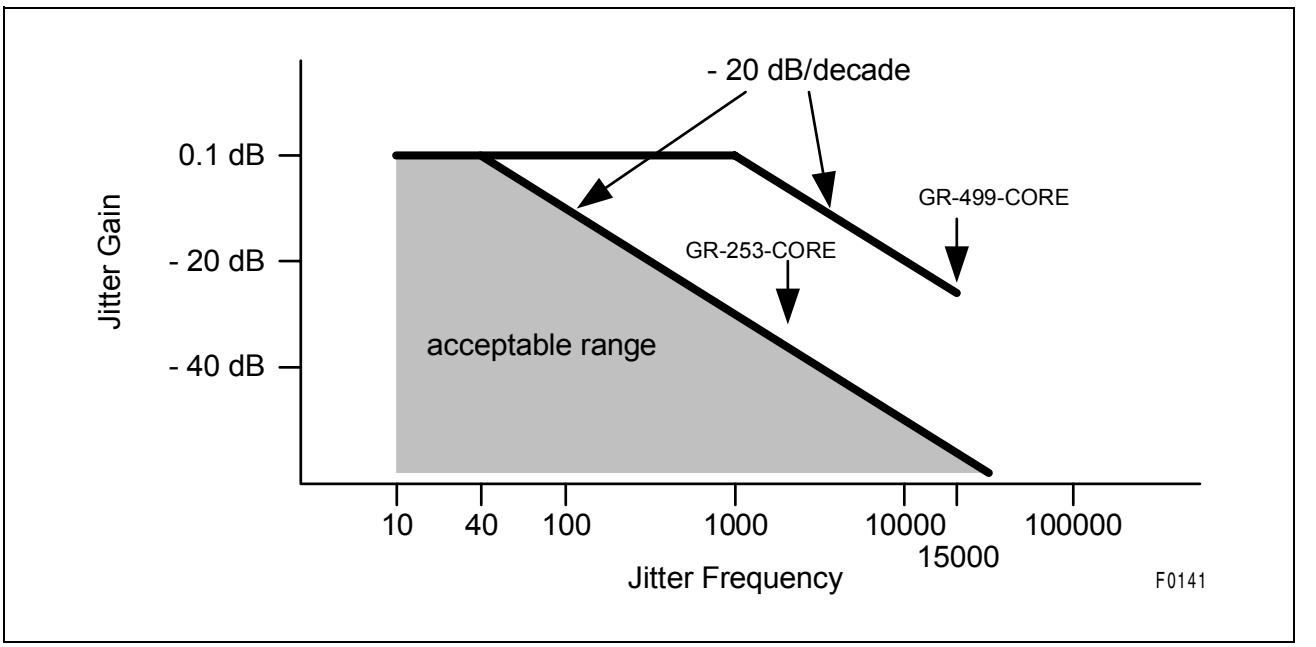


Figure 7 Jitter Attenuation Characteristic

Intrinsic Jitter

The TE3-FALC transmit PLL generates an output jitter which fulfills the requirements as specified in **Table 17** below.

Table 17 Transmit Output Jitter

Specification	Measurement Filter Bandwidth		Output Jitter[1]
	Lower Cutoff	Upper Cutoff	
GR-499-CORE (DS3)	10 Hz	300 kHz	< 1.0 UI_{PP}
			< 0.3 UI_{rms}
ANSI T1.404 (DS3)	10 Hz	400 kHz	< 0.5 UI_{PP}
	30 kHz	400 kHz	< 0.05 UI_{PP}
ETSI TBR24 (E3)	100 Hz	800 kHz	< 0.4 UI_{PP}
	10 kHz	800 kHz	< 0.15 UI_{PP}

1) Measured with maximum input jitter applied (see **Figure 20**).

1) This is an option which is not available with the current firmware release.

3.3.2.3 RX and TX Jitter Attenuator Buffer

The TE3-FALC has two jitter attenuator buffers, one for transmit direction and one for receive. The buffer length is 64 bit. The buffers can be used if the line clock and the framer clock are different, e.g. in case the RX DJAT output clock is used as receive framer clock. As the TE3-FALC is a terminating device, it is normally not necessary to use the dejittered clock for the receive framer and ✧the RX buffer can be bypassed[1)].

The buffers are useful for remote loops with jitter attenuation and if the bitstream access ports should have a dejittered clock.

3.3.3 Line Coding

In E3 applications the HDB3 coding is provided for the data received from the ternary interface. In DS3 mode the B3ZS code is supported. All code violations are detected and indicated.

3.3.3.1 B3ZS Code

In the B3ZS line code each block of three consecutive zeros is replaced by either of two replacements codes which are B0V and 00V, where B represents a pulse which applies to the bipolar rule ("+1" or "-1") and V represents a bipolar violation (two consecutive "+1" or "-1" bits). The replacement code is chosen in a way that there is an odd number of valid B pulses between consecutive V pulses to avoid the introduction of a DC component into the analog signal.

3.3.3.2 HDB3 Code

In the HDB3 line code each block of four consecutive zeros is replaced by either of two replacements codes which are B00V and 000V, where B represents a pulse which applies to the bipolar rule ("+1" or "-1") and V represents a bipolar violation (two consecutive "+1" or "-1" bits). The replacement code is chosen in a way that there is an odd number of valid B pulses between consecutive V pulses to avoid the introduction of a DC component into the analog signal.

3.3.4 DS3 Framer

The DS3 framer can be operated in two application modes:

- C-bit parity format
- M23 multiplex format

Optionally the TE3-FALC can automatically detect the application mode by observing the Application Identification Channel (AIC bit in C-bit parity = C_{11} bit in M23 multiplex mode).

1) This is an option which is not available with the current firmware release.

In both modes, full payload rate format is supported, i.e. the data blocks [84] carry one continuous data stream.

3.3.4.1 M23 Multiplex Format

The framing structure of the M23 multiplex signal is shown in **Table 18**. Each DS3 multiframe consists of 7 subframes and each subframe of eight blocks. One block consists of 85 bits, where the first bit is the overhead (OH) bit and the remaining 84 bits are the information bits.

Table 18 DS3 M23 Multiplex Frame Structure

	Sub-frame	Block 1 through 8 of a Subframe							
		1	2	3	4	5	6	7	8
DS3- Multiframe	1	X [84]	F_1 [84]	C_{11} [84]	F_0 [84]	C_{12} [84]	F_0 [84]	C_{13} [84]	F_1 [84]
	2	X [84]	F_1 [84]	C_{21} [84]	F_0 [84]	C_{22} [84]	F_0 [84]	C_{23} [84]	F_1 [84]
	3	P [84]	F_1 [84]	C_{31} [84]	F_0 [84]	C_{32} [84]	F_0 [84]	C_{33} [84]	F_1 [84]
	4	P [84]	F_1 [84]	C_{41} [84]	F_0 [84]	C_{42} [84]	F_0 [84]	C_{43} [84]	F_1 [84]
	5	M_0 [84]	F_1 [84]	C_{51} [84]	F_0 [84]	C_{52} [84]	F_0 [84]	C_{53} [84]	F_1 [84]
	6	M_1 [84]	F_1 [84]	C_{61} [84]	F_0 [84]	C_{62} [84]	F_0 [84]	C_{63} [84]	F_1 [84]
	7	M_0 [84]	F_1 [84]	C_{71} [84]	F_0 [84]	C_{72} [84]	F_0 [84]	C_{73} [84]	F_1 [84]

F_0 , F_1 - Frame Alignment Pattern

F_0 and F_1 form the frame alignment pattern. Each DS3 frame consists of 28 F-bits, four per subframe in block 2, 4, 6 and 8. F_0 and F_1 form the pattern '1001'. This pattern is repeated in every subframe.

M_0 , M_1 - Multiframe Alignment Signal

M_0 and M_1 form the multiframe alignment signal. The M-bit is contained in the OH-bit of the first block in subframe 5, 6 and 7. The multiframe alignment signal is '010'.

C_{11} ..C_{73} - Stuffing Indicators

The C-bits control the bit stuffing procedure of the multipexed DS2 signals. Since TE3-FALC only processes the unchannelized DS3 signal, DS2 stuffing does not apply and these bits are set to ’1’.

P - Even Parity

The P-bits contain parity information and are automatically calculated as even parity on all information bits of the previous DS3 frame.

X

The X-bits are used for transmission of asynchronous in-service messages (Remote Defect Indications, RDI). Both X-bits carry the identical value and do not change more than once every second.

[84] - DS3 Information Data

These bits represent an information data block, which consists of 84 bits.

3.3.4.2 C-bit Parity Format Specifics

The framing structure of the C-bit parity format is shown in **Table 19**. The assignment of the information bits [84] is identical to the M23 multiplex format, but the function of the C-bits is redefined for path maintenance and data link channels.

Table 19 DS3 C-bit Parity Frame Structure

	Sub-frame	Block 1 through 8 of a Subframe															
		1		2		3		4		5		6		7		8	
DS3- Multiframe	1	X	[84]	F_1	[84]	AIC	[84]	F_0	[84]	N_r	[84]	F_0	[84]	FEAC	[84]	F_1	[84]
	2	X	[84]	F_1	[84]	DL	[84]	F_0	[84]	DL	[84]	F_0	[84]	DL	[84]	F_1	[84]
	3	P	[84]	F_1	[84]	CP	[84]	F_0	[84]	CP	[84]	F_0	[84]	CP	[84]	F_1	[84]
	4	P	[84]	F_1	[84]	FEBE	[84]	F_0	[84]	FEBE	[84]	F_0	[84]	FEBE	[84]	F_1	[84]
	5	M_0	[84]	F_1	[84]	DL_t	[84]	F_0	[84]	DL_t	[84]	F_0	[84]	DL_t	[84]	F_1	[84]
	6	M_1	[84]	F_1	[84]	DL	[84]	F_0	[84]	DL	[84]	F_0	[84]	DL	[84]	F_1	[84]
	7	M_0	[84]	F_1	[84]	DL	[84]	F_0	[84]	DL	[84]	F_0	[84]	DL	[84]	F_1	[84]

N_r

Reserved. Set to '1' in transmit direction.

AIC - Application Identification Channel

TE3-FALC can automatically select the DS3 application (C-Bit Parity or M23 mode) by evaluating the AIC bit.

DL_t - Path Maintenance Data Link Channel

The terminal-to-terminal path maintenance data link (MDL) uses the HDLC protocol. Access to the MDL channel is provided.

DL

Reserved. Set to '1' in transmit direction.

FEAC - Far End Alarm and Control Channel

The alarm or status information of a far end terminal is sent back over the Far End Alarm and Control channel. Messages are sent in bit oriented mode (→BOM). Access to the FEAC channel is provided.

DS3 line loopback requests are also detected and generated by TE3-FALC through the FEAC channel.

FEBE - Far End Block Error

The Far End Block Error bits indicate a CP-bit parity error or a framing error. They are used to monitor the performance of a DS3 signal. Upon detection of either error in the incoming data stream the FEBE-bits are set automatically to '000' in the outgoing direction. Received far end block errors are counted.

CP - Path Parity

The CP-bits are used to carry path parity information and are set to the same value as the P-bits. In receive direction the CP-bits are checked against the calculated parity and differences are counted.

3.3.4.3 Alarm Indication Signal (AIS), Idle Signal

Alarm Indication Signal or Idle signal is declared, when the selected signal format was received with less than 8/15 bit errors for at least one multiframe.

The alarm indication signal can be selected as:

- Unframed all '1's
- Framed '1010' sequence, starting with a binary '1' after each OH-bit. C-bits are set to '0'. X-bits are checked as '1' (✧X-bit check can be disabled[1)]).

The idle signal is a

- Framed '1100' sequence, starting with a binary '11' after each OH-bit. C-bits are set to '0' in M-subframe 3. X-bits are checked as '1' (✧X-bit check can be disabled[1)]).

In transmit direction the alarm indication signal or idle signal will be generated according to the selected signal format.

3.3.4.4 Loss of Signal

Loss of signal defect is declared, when the incoming data stream contains more than 1022 consecutive '0's. Loss of signal defect is removed, when two or more ones are detected in the incoming data stream.

1) This is an option which is not available with the current firmware release.

3.3.4.5 Performance Measurement

The following conditions are counted:

- Line code violations
- Excessive zeros
- P-bit errors, CP-bit errors
- Framing bit errors
- Far end block errors
- OOF defects
- LOS defects
- Remote Defect Indications (RDI)
- Errored Seconds (far-end and near-end)

3.3.5 E3 Framer (G.832)

The E3 framing structure is shown in **Table 20**. Each E3 frame consists of 9 rows with 59 columns each. The frame consists of 7 overhead bytes and 530 bytes information data.

Table 20 E3 Frame Structure (G.832)

59 columns

9 rows		
	FA1	FA2
	EM	
	TR	
	MA	
	NR	[530 bytes]
	GC	

FA1, FA2 - Frame Alignment Octets

FA1 and FA2 form the frame alignment pattern, with A1 = 11110110_2 and A2 = 00101000_2 ($F628_H$).

EM - Error Monitoring

This byte is allocated for error monitoring using a BIP-8 code with even parity. The BIP-8 is calculated over all bits, including the overhead bits, of the previous 125 µs frame. The computed BIP-8 is placed in the EM byte of the current 125 µs frame.

TR - Trail Trace

This byte is used to repetitively transmit a trail access point identifier (16-byte frame format) so that a trail receiving terminal can verify its continued connection to the intended transmitter. TE3-FALC provides insert and extract access to the TR channel.

MA - Maintenance and Adaptation Byte

RDI	REI	Payload Type [2:0]	MFI[1:0]	SSM

The Remote Defect Indication bit (RDI) is processed by the TE3-FALC.

The Remote Error Indication bit (REI) is set to '1' and sent back to the remote trail termination if one or more errors were detected by the BIP-8, and is otherwise set to zero.

The Payload Type is coded as follows:

Table 21 E3 Payload Type Coding

Code	Payload Type
000	Unequipped
001	Equipped, non-specific
010	ATM
011	SDH TU-12s

Bit SSM represents a Synchronization Status Message which is transferred in a four-frame multiframe, MSB-first. The phase of the multiframe is determined by the value of the Multiframe Identifier (MFI) bits with the sequence 00_2, 01_2, 10_2, 11_2, 00_2, ...

✧Optionally the E3 framer can be switched into a non-multiframe mode[1)]. In that case the MFI field is ignored.

NR - Network Operator Channel

This channel is allocated for maintenance purposes. Its transparency from Trail termination to Trail termination is not guaranteed. ✧TE3-FALC optionally provides insert and extract access to this byte[1)].

GC - General Purpose Communications Channel

This channel is allocated for maintenance purposes. ✧TE3-FALC optionally provides insert and extract access to this byte[1)].

1) This is an option which is not available with the current firmware release.

3.3.5.1 Performance Measurement

The following conditions are counted:

- Line code violations
- BIP-8 errors
- Framing bit errors
- Remote error indications (REI)
- OOF defects
- LOS defects
- Remote Defect Indications (RDI)
- Errored Seconds (far-end and near-end)

3.3.6 DS3/E3 Bit Error Rate Test (BERT) Unit

The bit error rate test unit of the TE3-FALC incorporates a test pattern generator and a test pattern synchronizer which can be assigned to the DS3 or the E3 framer. Controlled by a set of messages it can generate and synchronize to polynomial pseudorandom test patterns or repetitive fixed length test patterns.

In pseudorandom test mode the receiver tries to achieve synchronization to a test pattern which satisfies the programmed receiver polynomial. In fixed pattern mode it synchronizes to a repetitive pattern with a programmable length. An all '1' pattern or an all '0' pattern, which satisfies this condition, is flagged. Measurement intervals as well as receiver synchronization can be controlled by the user. When a test is finished an interrupt is generated and the bit count and the bit error count are readable.

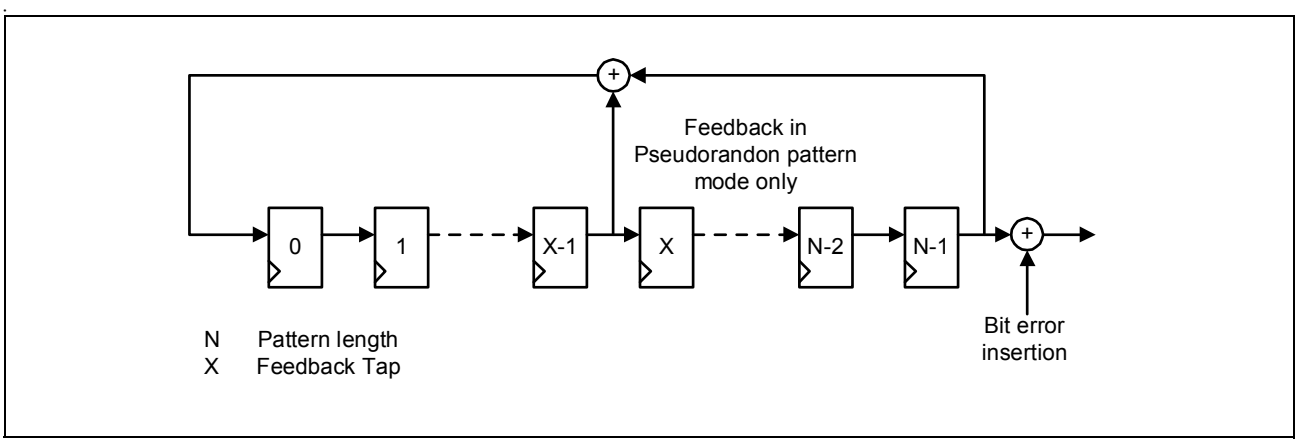


Figure 8 Pattern Generator

Bit Error Insertion

The test unit provides the optional capability to insert bit errors in the range of 10^{-7} (1 error in 10.000.000 bits) up to 10^{-1} bit errors (1 error in 10 bits).

3.3.7 ATM Cell Processor and PLCP

The cell processor performs the mapping and de-mapping of ATM cells from the G.832 E3 Frame, DS3 Frame and DS3-PLCP Frame. The mapping and de-mapping follows the requirements described in G.804.

The self-synchronizing payload scrambler with the generator polynom $X^{43} + 1$ can optionally be enabled.

Transmit

In the transmit direction ATM cells from the internal FIFO are taken, a valid HEC is calculated and written into the cell header.

In order to maintain a constant flow of back-to-back cells, IDLE cells are automatically inserted when no cells are available from the internal FIFO.

ATM cells are mapped byte-synchronously into both the E3 G.832 frame and the PLCP sub-frame. Nibble-aligned mapping is used for the DS3 frame option.

Receive

In receive direction the ATM cells are either extracted directly from the E3 or DS3 frame or from the PLCP frame. When extracting cells directly from the E3/DS3 frame, cell boundaries are found by using the HCS. The state transition diagram for cell delineation is shown in **Figure 9**.

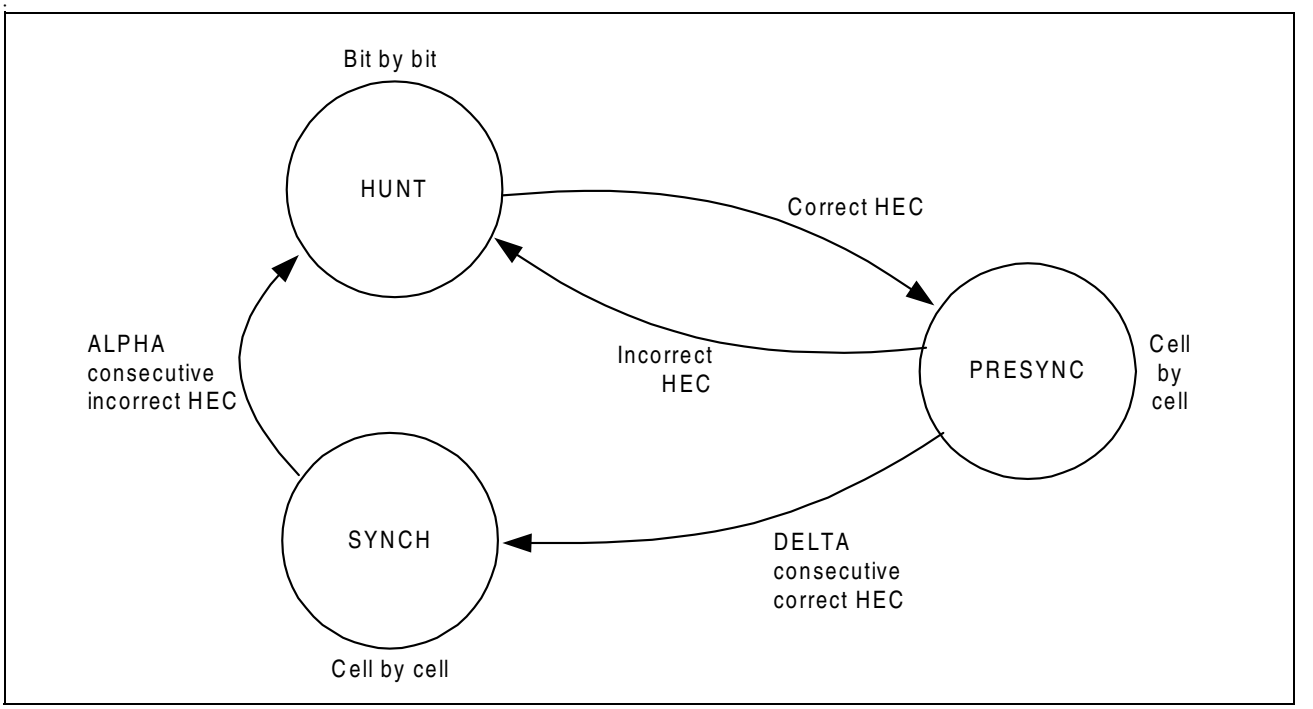


Figure 9 ATM Cell Delineation State Diagram

As indicated in the state diagram it requires the number of DELTA consecutive cells with correct HEC to transition from the PRESYNC state to the SYNCH state. Also, only a sequence of ALPHA consecutive cells with incorrect HEC can bring the ATM cell processor back to HUNT state. The values ALPHA and DELTA are configurable.

Single bit errors in the ATM header can be corrected using the Header Error Correction mechanism. IDLE cells are detected and discarded within the cell processor.

3.3.7.1 PLCP Mapping

The TE3-FALC supports mapping of ATM cells via PLCP layer into a DS3 envelope according to standards ATM Forum af-phy-0054.000 and ANSI T1.646-1995.

Table 22 DS3 PLCP Frame Structure

Framing		POI	POH	Payload	
A1	A2	P11	Z6	ATM Cell 1	
A1	A2	P10	Z5	ATM Cell 2	
...	...	...	...	...	
A1	A2	P7	Z2	ATM Cell 5	
A1	A2	P6	Z1	ATM Cell 6	
A1	A2	P5	F1	ATM Cell 7	
A1	A2	P4	B1	ATM Cell 8	
A1	A2	P3	G1	ATM Cell 9	
A1	A2	P2	M2	ATM Cell 10	
A1	A2	P1	M1	ATM Cell 11	
A1	A2	P0	C1	ATM Cell 12	Trailer (m bits)

The PLCP frame rate is 125 µs. The PLCP overhead octets are described in the following:

A1, A2 - Frame Alignment Octets

A1 and A2 form the frame alignment pattern, with A1 = 11110110_2 and A2 = 00101000_2 ($F628_H$).

F1 - User Channel

F1 is the user channel. ✧TE3-FALC provides optional extract and insert access for this channel[1)].

[1)] This is an option which is not available with the current firmware release.

B1 - Bit Interleaved Parity

The B1 octet contains the bit interleaved parity information (BIP-8) calculated over a 12 times 54 octet structure consisting of the POH field and the associated ATM cells of the previous PLCP frame.

G1

The G1 octet contains path status information.

FEBE[3:0]	RAI	X[2:0]

The Far End Block Error (FEBE[3:0]) field indicates the number (0 to 8) of BIP-8 errors detected in the previous frame at the far end.

The Remote Alarm Indication (RAI, "yellow alarm") indicates that the far end declared Out-of-Frame.

✧The three X-bits can optionally be accessed[1)].

M1, M2 - Control Octets

By default, these octets are zero. ✧Optional access to the control octets is provided[1)].

C1 - Cycle/Stuff Counter

This cycle/stuff counter indicates the number of trailing nibbles, i.e. the length of the PLCP frame. In order to get the PLCP frame nibble-aligned to the DS3 frame (both are running asynchronous to each other), stuffing is applied after the 12th ATM cell using a trailer of various length. A stuffing opportunity occurs every third PLCP frame:

The value of the C1 field shall be

- FF_H in the first PLCP frame, indicating a trailer length of 13 nibbles,
- 00_H in the second PLCP frame, indicating a trailer length of 14 nibbles,
- 66_H (or 99_H) in the third PLCP frame, indicating a trailer length of 13 nibbles (or 14 nibbles, i.e. stuffing!)

Z1..Z6 - Growth Octets

These growth octets are reserved for future use and are all zeros.

1) This is an option which is not available with the current firmware release.

P0..P11 - Path Overhead Identifier (POI) Octets

The Path Overhead Identifier (POI) octets mark the individual path overhead (POH) octets.

Table 23 Path Overhead Identifier (POI) Codes

POI	POI Code	Associated POH Octet
P11	$00101100_2 = 2C_H$	Z6
P10	$00101001_2 = 29_H$	Z5
P9	$00100101_2 = 25_H$	Z4
P8	$00100000_2 = 20_H$	Z3
P7	$00011100_2 = 1C_H$	Z2
P6	$00011001_2 = 19_H$	Z1
P5	$00010101_2 = 15_H$	F1
P4	$00010000_2 = 10_H$	B1
P3	$00001101_2 = 0D_H$	G1
P2	$00001000_2 = 08_H$	M2
P1	$00000100_2 = 04_H$	M1
P0	$00000001_2 = 01_H$	C1

Note: In TE3-FALC, the ATM cell delineation algorithm is always underlying the PLCP cell mapping. These sequential cell delineation processes lead to an increased overall synchronization time.

3.3.7.2 Performance Measurement

The TE3-FALC offers a set of counters

- transmitted and received user cells
- transmitted and received idle cells
- HEC errors
- HEC corrections
- OCD events
- PLCP BIP-8 errors
- PLCP framing errors
- PLCP far end block errors
- PLCP OOF defects
- PLCP Remote Alarm Indications (RAI)

3.3.8 HDLC Packet Processor

The HDLC packet processor implements HDLC framing and supports the Point-to-Point Protocol (PPP) with its bit-synchronous and octet-synchronous mapping options.

Opening Flag	PPP Address	PPP Control	PPP PID	LLC Data	CRC	Closing Flag
$7E_H$	FF_H	03_H	16 bit	>= 0 bits	16/32 bit	$7E_H$

Figure 10 PPP in HDLC-like Framing

The frame[1] begin and frame end synchronization is performed with the flag character $7E_H$ ($0111\ 1110_2$). Shared opening and closing flag is supported in receive direction and can be programmed for transmit direction. Shared '0' bit between closing and opening flags is understood by the receiver in bit-synchronous HDLC operation.

The following CRC modes are supported:

- 16 bit CRC $1+x^5+x^{12}+x^{16}$
- 32 bit CRC $1+x+x^2+x^4+x^5+x^7+x^8+x^{10}+x^{11}+x^{12}+x^{16}+x^{22}+x^{23}+x^{26}+x^{32}$

Optionally CRC transfer and check can be disabled. The interframe-time fill pattern can be programmed to either flags ($7E_H$) or all ones indicating idle.

3.3.8.1 PPP Header Operations

When using the standard PPP in HDLC-like framing, the Address and Control fields contain the hexadecimal values FF_H and 03_H respectively.

PPP Filtering

✧An optional filter, that passes only receive packets starting with the PPP header FF-03 is provided[2]. Other packets are not forwarded to system side in that case.

Address-and-Control-Field Compression

If Address-and-Control-Field compression (RFC1662, chapter 3) is enabled, PPP packets on the line are transferred without the PPP Address and Control fields FF-03.

In transmit direction TE3-FALC checks if the first two bytes delivered from system side contain FF-03, and if so, these are omitted. Any packet header not starting with FF-03 is assumed to be compressed already and is transmitted unmodified.

On reception, the Address and Control fields are decompressed by examining the first two octets. If they contain the values FF_H and 03_H, they are assumed to be the Address

1) Both terms "frame" and "packet" are used further on. When describing HDLC framing functions, "frame" is the preferred term; a PPP datagram is referred as "packet".
2) This is an option which is not available with the current firmware release.

and Control fields. If not, it is assumed that the fields were compressed and were not transmitted. Towards the system side, the bytes FF-03 are added to front if they were not present on the line.

When other Address or Control field values than FF-03 are in use, Address-and-Control-Field-Compression must not be negotiated.

3.3.8.2 Performance Measurement

The TE3-FALC offers a set of counters:

- transmitted and received bytes
- transmitted and received valid and errored packets
- underflown and overflown packets
- too long, too short packets
- CRC errored packets
- misaligned packets
- bad PPP address fields and bad PPP control fields

4 Operational Description

4.1 Operational Overview

4.2 Operating States

This chapter shall guide the designer through the initial steps of activating and configuring the TE3-FALC.

4.2.1 Reset

Global Hardware Reset

A Global Reset of the device can be issued on hardware level by assering pin $\overline{\text{POR}}$, where the provided reset signal is not required to be synchronous to any clock. After this type of reset the on-chip boot strap loader starts loading a new firmware image from the origin defined with the boot configuration pins.

Global Software Reset

Also on software level a Global Device Reset can be issued via message **CMD_RESET_DEVICE** (page 99). All internal modules are set back to reset state, just the configuration of the Device Control Interface (DCI, see **Chapter 6.1** for details) remains unchanged.

A parameter selects whether the firmware image shall be reloaded or the current image shall be re-used.

4.2.2 Boot Process

The firmware upload can be performed in two ways. The firmware image data is read autonomously by TE3-FALC (acting as bus master) out of an attached EPROM or image data can be written to the device by issuing a set of boot messages via the Device Control Interface DCI.

4.2.2.1 Boot via Device Control Interface (DCI)

Figure 11 lists the individual actions user software has to take for booting via DCI (see **Chapter 6.1** for details).

After internal initialization the device is ready to boot. If internal initialization was successful the **NFC_DCI_ACCESSIBLE** (page 49) notification is written into the low priority egress queue (LPQOUT). At this point in time the interrupt system is not yet enabled, thus the LPQOUT queue needs to be polled.

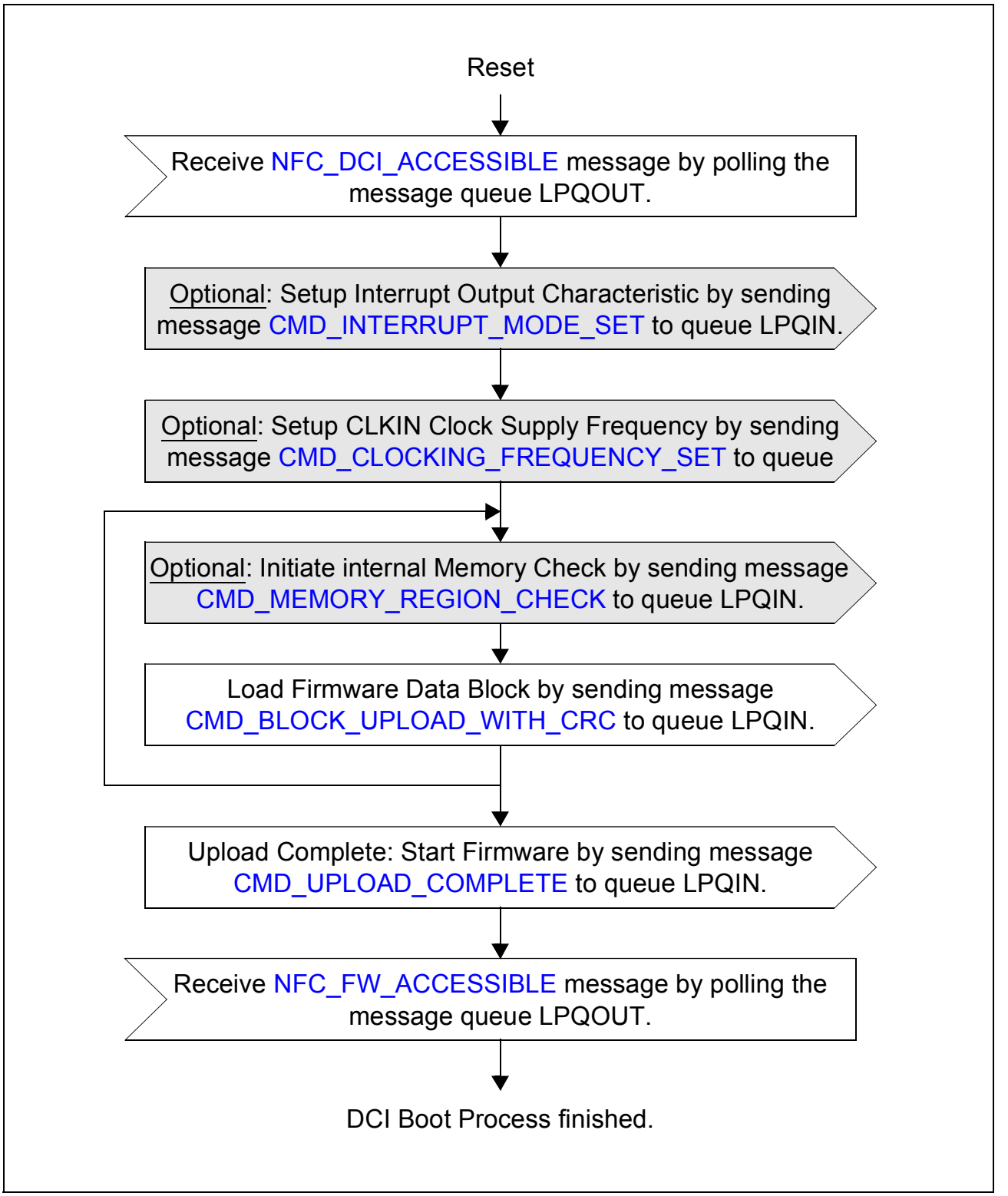
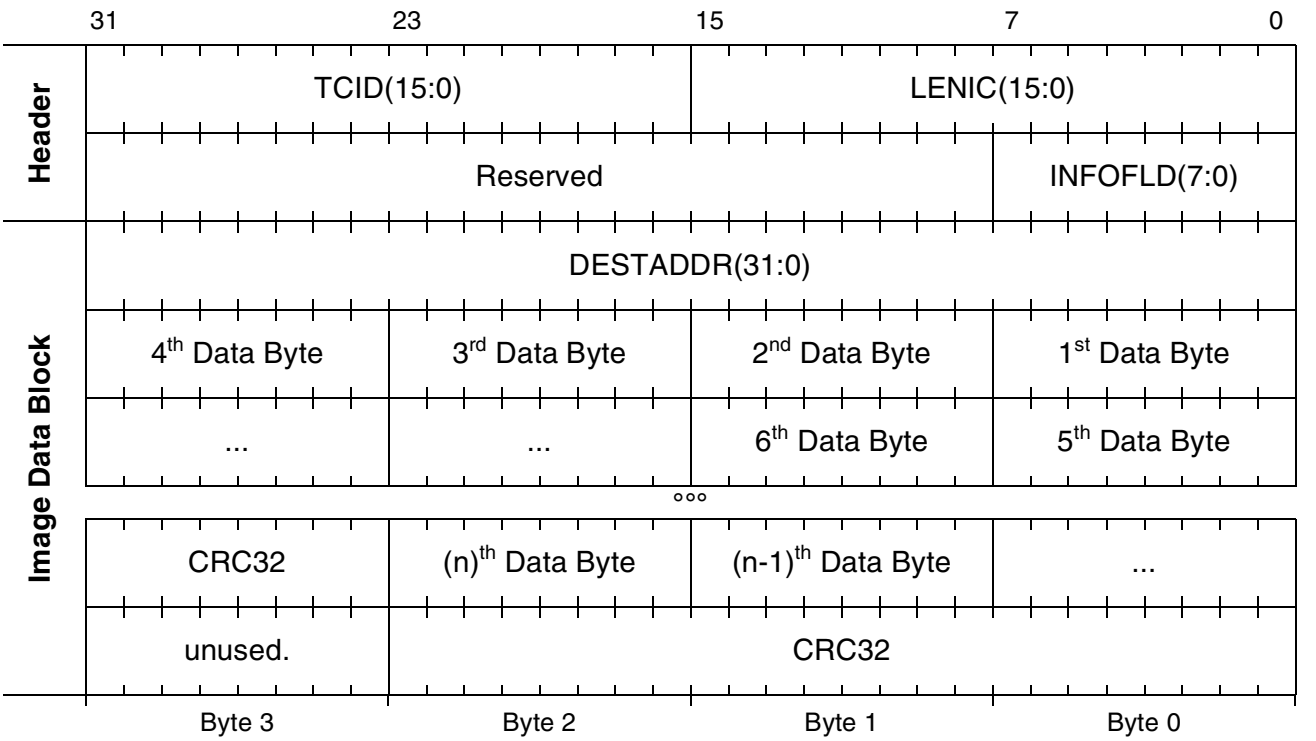


Figure 11 DCI Boot Process

Upload of firmware is performed with cyclic redundancy check (CRC32). The generator polynomial used for CRC32 check is:

$1 + x^1 + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$

Table 24 Upload Image Data



A block of image data as shown in **Table 24** is to be written into the DCI memory area. The usable address range is 8000_H to $FF80_H$.

The length indicator (LENIC) includes the whole block size, including header, data field and CRC32 field. Its value should be (n + 16) with n > 0 being the number of bytes to be transferred.

The block format includes the internal destination address DESTADDR(31:0) for this block.

Note that the parameter data format during boot deviates from the parameter array format described in **Chapter 6.2.2.2**.

A block transfer starts after writing the **CMD_BLOCK_UPLOAD_WITH_CRC** (page 49) command into the low priority ingress queue (LPQIN).

To indicate that the upload of firmware is completed, the **CMD_UPLOAD_COMPLETE** (page 49) command must be written into the low priority ingress queue (LPQIN). After receiving this message the TE3-FALC starts running off the loaded firmware image. The fact that firmware started successfully is indicated with the **NFC_FW_ACCESSIBLE** (page 94) which can be read from queue LPQOUT.

Note: The following messages are only applicable for the boot process, i.e. until message **NFC_FW_ACCESSIBLE** (page 94) is sent out by TE3-FALC.

Notification ID: **NFC_DCI_ACCESSIBLE**

This message reports the successful initialization of the Device Control Interface (DCI) after reset. When receiving this message the interface is ready to interchange information. As long as the firmware is not uploaded, only boot messages can be interchanged via the Low Priority Queue In (LPQIN) and the Low Priority Queue OUT (LPQOUT). All other messages are acknowledged with with the Return Code "Message Denied".

Output Parameters	*none*

Command ID: **CMD_BLOCK_UPLOAD_WITH_CRC**

This message causes the firmware to load new image data via DCI. The image data is loaded sequentially in blocks assigned to each CMD_BLOCK_UPLOAD_WITH_CRC message. The data is stored in the code memory. In parallel a checksum is calculated. After storing the block of image data, the checksum is verified and the result is indicated to the host in the Return Code (RC) of the **ACK_BLOCK_UPLOAD_WITH_CRC** message.

Input Parameters
Block of Upload Image Data as shown in **Table 24**.

Command ID: **CMD_UPLOAD_COMPLETE**

This message is used to identify the end of firmware upload process. After receiving this message the TE3-FALC starts with the firmware specific configuration. If the configuration is finished the **NFC_FW_ACCESSIBLE** (page 94) message is sent to the host.

Input Parameters
32-bit Program Start Pointer (PSP)

Optional Boot Messages

The following messages are optional and can be used as needed to improve the standard (minimum) boot process described above. Note that after the boot process messages **CMD_SPECIFY_CLOCKS** (page 94) and **CMD_SET_INTERRUPT_MODE** (page 96) are available for analog functionality as the following boot messages **CMD_CLOCKING_FREQUENCY_SET** and **CMD_INTERRUPT_MODE_SET**.

Command ID: **CMD_MEMORY_REGION_CHECK**

This message is used to initiate a memory check. The memory check is non-destructive, i.e. after the check is complete, the original values are restored.
The following memory address regions can be checked with this message:

Memory	Start Address	End Address
Code/Data Section	C000 1000_H	C001 $FFFC_H$
Message Queues	DF00 8000_H	DF00 $9FFC_H$

Input Parameters *(each parameter is a 32-bit value)*		
Start Address	*32-bit address*	Word aligned start address of the memory region.
End Address	*32-bit address*	Word aligned end address of the memory region.
0000 0001_H	*32-bit value*	This fixed 32-bit value must be appended for proper operation.

Command ID: **CMD_CLOCKING_FREQUENCY_SET**

This optional message is used to set the TE3-FALC internal system clock to a fixed frequency in the range 58 to 60 MHz.
PLL multiplicator and divisor parameters are calculated from the clock frequency value passed as input parameter to this message (2^{nd} stage PLL programming). The settings configured with port pins P2, P1 and P0 (1^{st} stage PLL programming) are overwritten.

Input Parameters
32-bit value carrying the CLKIN frequency in Hertz (Hz). The allowed range is 4,000,000 Hz (003D 0900_H) to 52,000,000 Hz (0319 7500_H).

Command ID: **CMD_INTERRUPT_MODE_SET**

The external interrupt pin characteristic is configurable with this meassage. By default the interrupt output is disabled.
For interrupt driven download, the interrupt mask register INTMSK (see **Page 84**) must be programmed.

Note: Interrupts INTREG:HPQINSA and INTREG:LPQINSA are not available during download!

Input Parameters *(each parameter is a 32-bit value)*		
Interrupt Port Config	INT_DISABLE INT_OPEN_DRAIN INT_HIGH INT_LOW	Interrupt output is disabled (tri-state). Interrupt output is open-drain. Interrupt output is push/pull, active high. Interrupt output is push/pull, active low.
0000 0000_H	*32-bit value*	This fixed 32-bit value must be appended for proper operation.
0000 $001F_H$	*32-bit value*	This fixed 32-bit value must be appended for proper operation.

4.2.2.2 Boot from EPROM

No host action is required for booting from an external EPROM. After reset, the TE3-FALC autonomously starts loading the provided firmware image. After load is complete, firmware starts running and indicates to the host that it is ready to receive messages via the DCI interface by sending the notification **NFC_FW_ACCESSIBLE** (page 94) to the queue LPQOUT. The boot process is visualized in **Figure 12**.

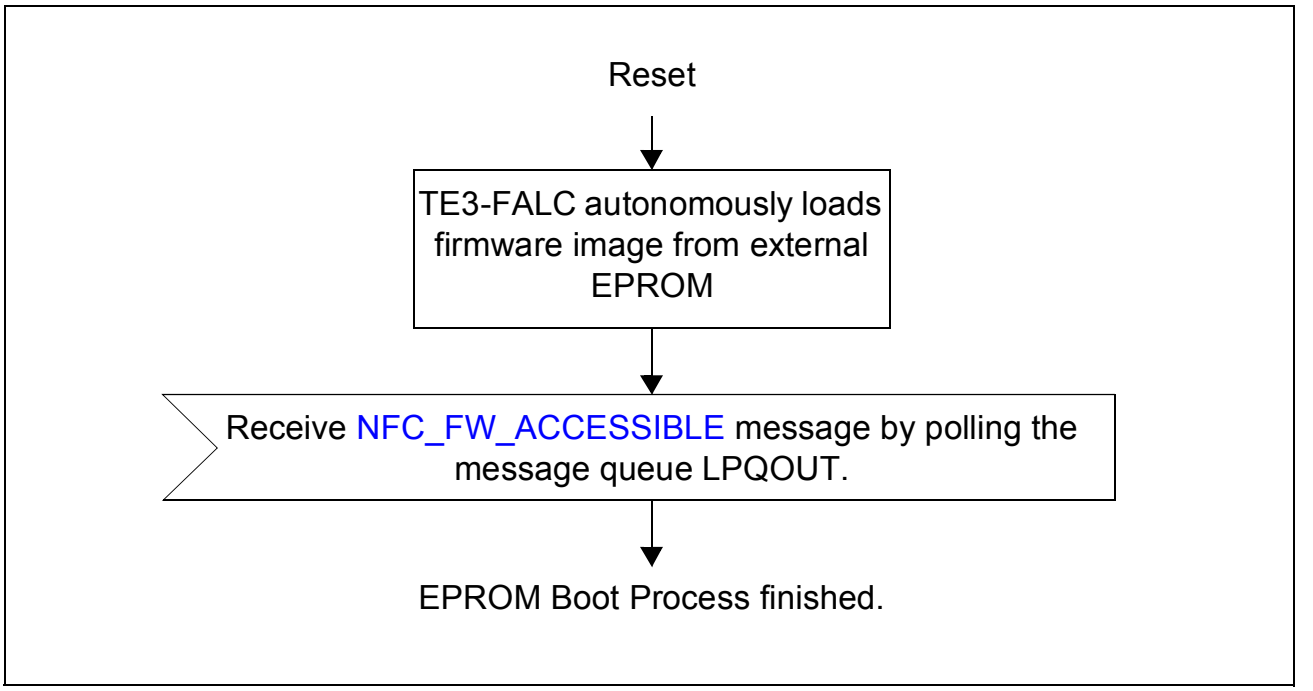


Figure 12 EPROM Boot Process

4.2.3 Initialization

After the boot process is completed, as indicated with the notification message **NFC_FW_ACCESSIBLE** (page 94), a few initialization messages need to be sent to TE3-FALC's ingress queue LPQIN.

The first steps of the initialization procedure shown in **Figure 13** are configuration of the TE3-FALC interrupt output pin characteristic via the **CMD_SET_INTERRUPT_MODE** (page 96) message (unless device polling is the preferred method) and specification of input and output frequencies of the clocks used in the system surrounding TE3-FALC with message **CMD_SPECIFY_CLOCKS** (page 94).

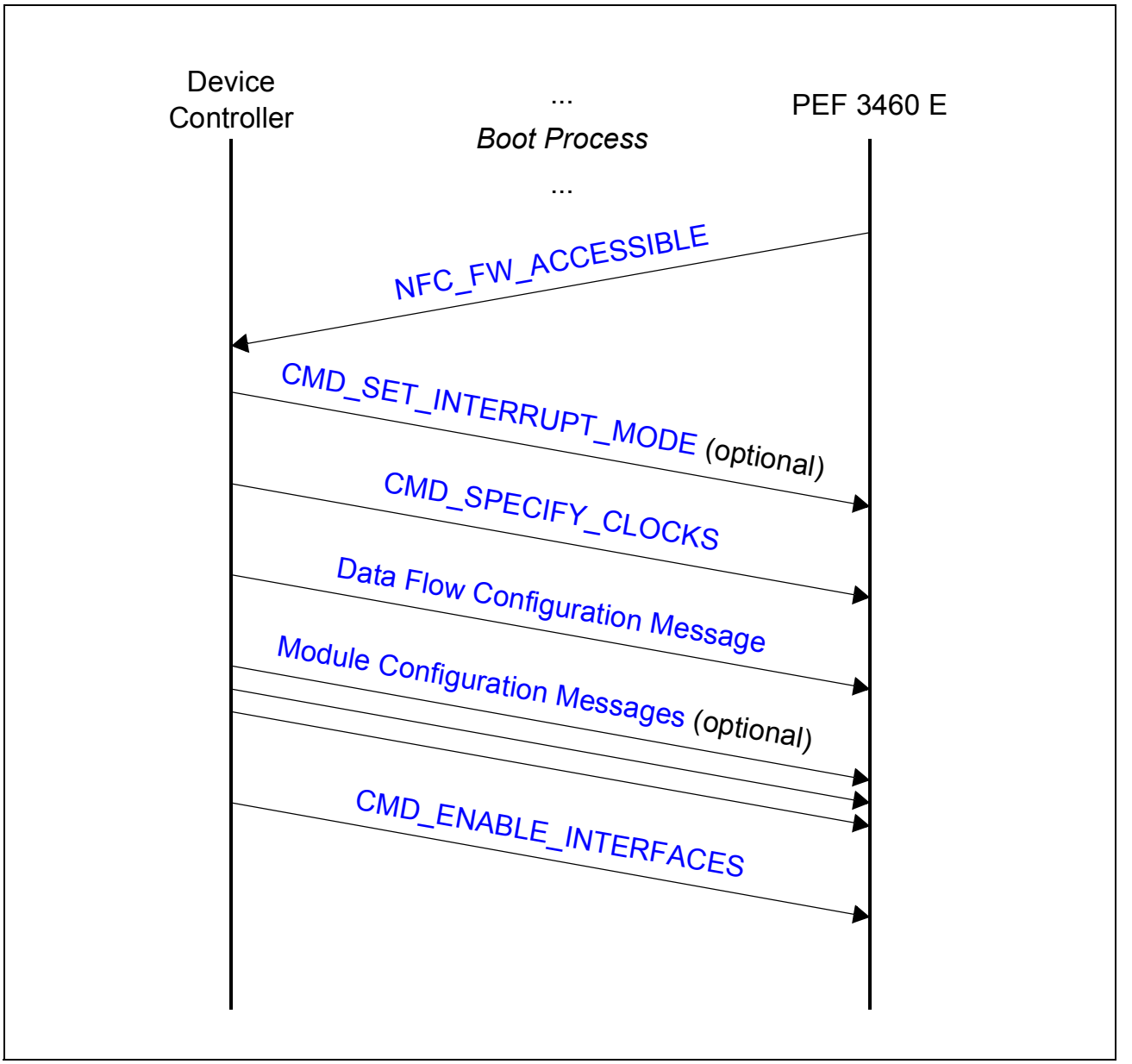


Figure 13 Minimum Initialization Message Flow

As an option, the RX PLL and TX PLL transitioning to their LOCK state can be monitored through notifications **NFC_PLL_LOCKED** (page 95) and **NFC_PLL_UNLOCKED** (page 95). These notifications must first be enabled by using the message **CMD_SET_NFC_ALM_MODE** (page 96).

The next initialization step is to select a **Data Flow Configuration Message** (page 100) from the ones listed in **Table 39**. All internal modules that are part of the selected data flow do contain default settings which apply in most cases. If the desired module settings deviate from the default setting, **Module Configuration Messages** (page 113) can be sent to individual TE3-FALC modules.

Now configuration of the data flow is complete and the line and system side interfaces shall be enabled with the **CMD_ENABLE_INTERFACES** (page 112) message.

4.2.4 Test Loops

The TE3-FALC supports a number of test loops as shown in **Figure 14**. If a Remote Loop and a Local Loop shall be enabled simultaneously, it must be ensured that no "infinite loop" is established (e.g. Local Line loop and Remote Line loop exclude each other since data would circle within the →LIU).

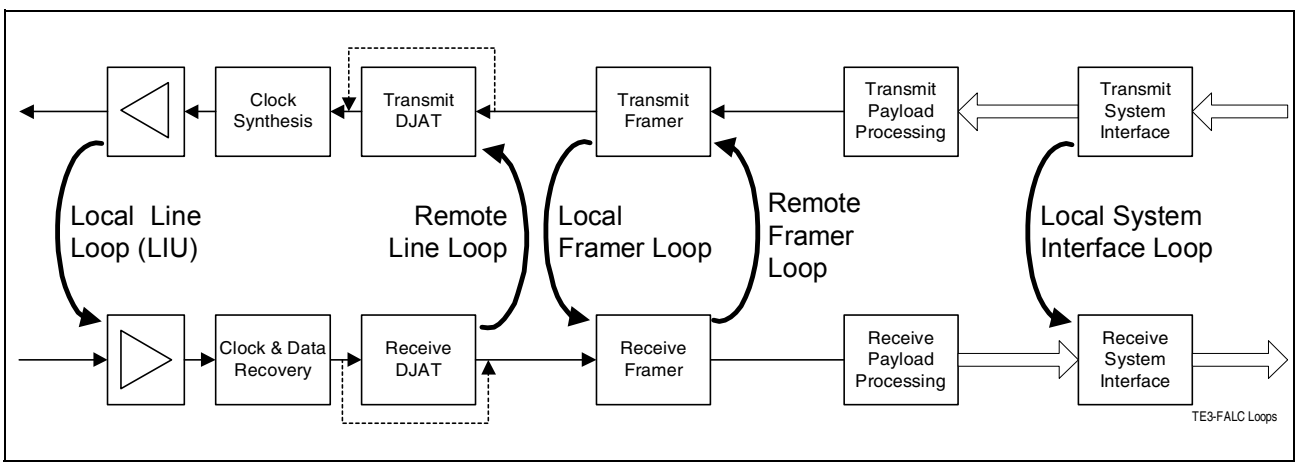


Figure 14 TE3-FALC Test Loops

Each of the shown loops can individually be enabled or disabled using the command message **CMD_SET_LOOP** (page 97).

Local Line Loop (LIU)

The local line loopback mode disconnects the receive lines RL1/2 from the receiver. Instead of the signals coming from the line, data provided by the transmit framer is routed through the analog receiver back to the receive framer interface. The transmit bit stream is sent to the transmit line unchanged.

Note: Enabling a local line loop usually invokes an out-of-frame error until the receiver resynchronizes to the new framing.

Remote Line Loop

In the remote loopback mode the clock and data recovered from the line inputs RL1/2 are routed back to the line outputs XL1/2. As in normal mode, data is also sent to the receive framer. The recovered receive clock is used to drive the transmit pulse shaper, optionally dejittered via transmit DJAT.

Local Framer Loop

The local framer loopback mode disconnects the receive data to the framer. Instead of the signals coming from the →LIU, data provided by the transmit framer is routed back to the receive framer. The transmit clock is used for the receive path. As in normal mode, transmit data is sent to the LIU. Optionally, AIS can be sent towards LIU, which does not influence the looped data.

✧Remote Framer Loop[1)]

In the remote loopback mode, data passes the receive framer and gets then looped back to the transmit framer. Receive data towards the system side is disconnected. The recovered receive clock is used for the transmit path, optionally dejittered via transmit DJAT.

Local System Interface Loop

The local system interface loop mode disconnects the complete transmit and receive line side. The line transmitter sends the AIS pattern.

Receive backpressure via signal $\overline{\text{SRENB}}$ is not supported. The transmit and receive system clock must be equal.

1) This is an option which is not available with the current firmware release.

5 Hardware Interface Description

5.1 T3/E3 Analog Line Interface

5.1.1 Receiver Application

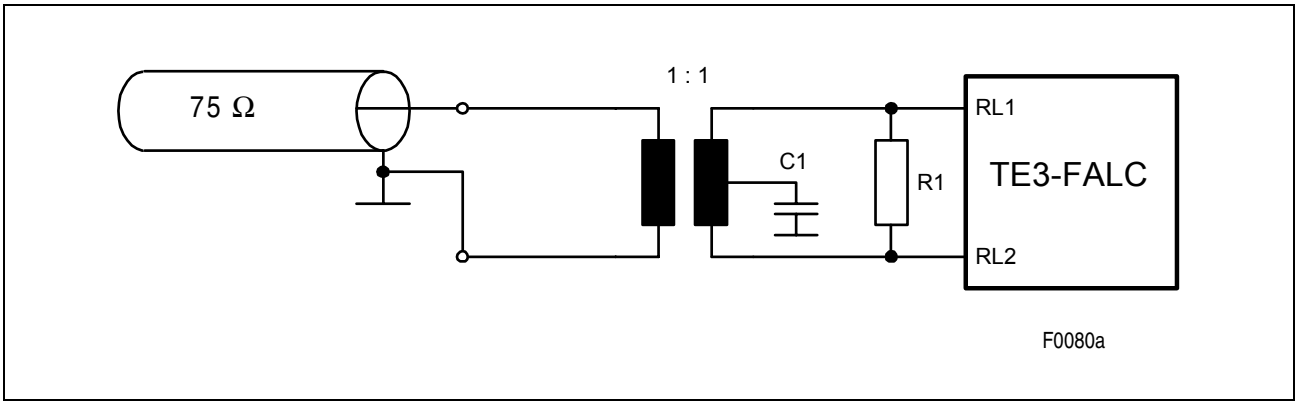


Figure 15 Standard Receiver Configuration

Table 25 External Component Values for Receiver

Parameter	Characteristic Line Impedance [Ω]	
	DS3	E3
	75	
R_1 (± 1 %) [Ω]	75	
C_1 (± 20 %) [nF]	100	
$t_2 : t_1$	1 : 1	

The external components are the same for DS3 and E3 applications.

5.1.1.1 Line Monitoring Application

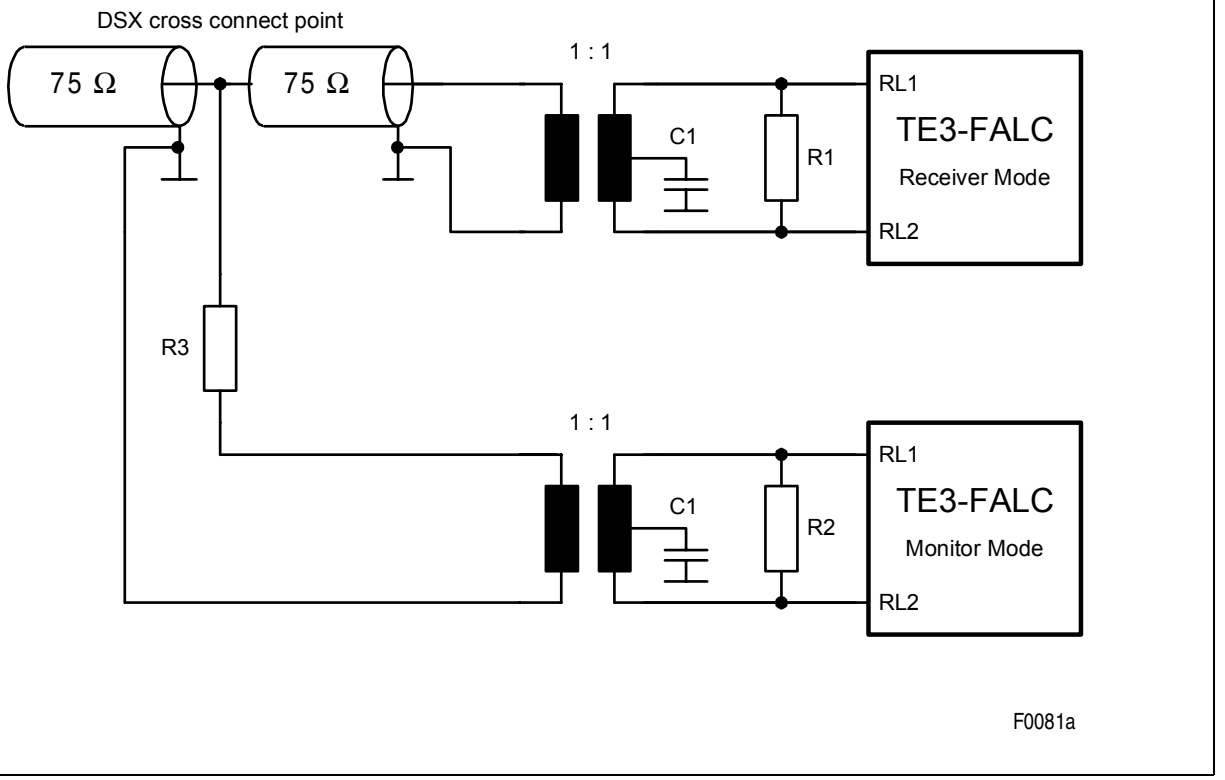


Figure 16 DS3 Line Monitoring

Table 26 External Component Values for DS Line Monitoring

Parameter	Values
R_1 (± 1 %) [Ω]	75
R_2 (± 1 %) [Ω]	47
R_3 (± 1 %) [Ω]	470
C_1 (± 20 %) [nF]	100
$t_2 : t_1$	1 : 1

The external components are according to ANSI T1.102 Annex B. The dimensions given above lead to a signal level at the monitor device input of approximately -20 dB below the level at the receiver device.

Similar configurations using the line monitoring mode are possible in E3 applications.

5.1.2 Receive Line Interface

The receive line interface consists of a pre-amplifier, a noise and crosstalk filter, a variable gain amplifier (VGA) and an equalizer followed by the clock and data recovery.

The noise and crosstalk filter reduces distortions within the incoming analog signal. The VGA amplifies the analog signal and the equalizer compensates the frequency dependent line attenuation. Digital signal levels are formed within the retiming block of the clock and data recovery.

Receive return loss requirements of ITU-T G.703 are fulfilled as required for E3 operation.

Table 27 E3 Receive Return Loss

Frequency Range		Return Loss
from [kHz]	to [kHz]	[dB]
860	1720	12
1720	34368	18
34368	51550	14

The equalizer contains an additional 20 dB gain stage, which is used in line monitoring mode to amplify resistively attenuated signals.

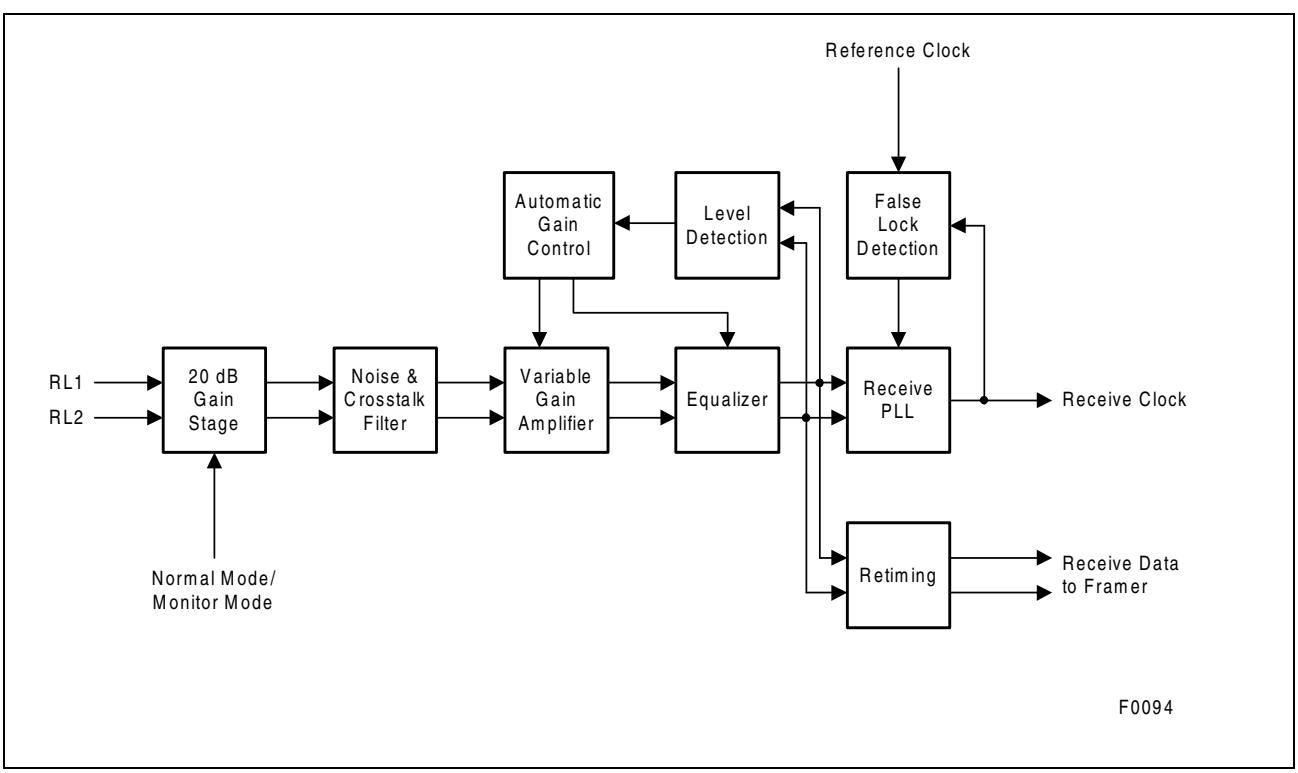


Figure 17 Receive Clock System

5.1.3 Receive Clock and Data Recovery

The receive clock and data recovery extracts the route clock from the digital data stream and converts the data stream into a dual rail bit stream. The clock and data recovery needs a reference clock to keep the PLL stable during times without data signal at RL1/ RL2. The receive clock is recovered of the signal provided on RL1/RL2 and has a duty cycle close to 50 %. The PLL reference clock is generated internally without the need for external components.

5.1.4 Receive Analog LOS

If the TE3-FALC is in E3 mode, the receive line interface includes the alarm detection for analog loss of signal (LOS). In T3/DS3 mode, the LOS definition is based on digital input levels. Digital LOS detection is a function of the DS3 framer.

Analog LOS is detected, if the signal level on pins RL1/2 drops below a fixed level ("B") for a certain period. Loss of signal level "B" is defined to be between 15 and 35 dB below normal signal level "A". If the signal exceeds 35 dB for 175 contiguous pulse periods (10 ≤ N ≤ 255), analog LOS defect is indicated.

Analog LOS defect is cleared, if the signal exceeds a threshold of 15 dB below nominal level for 175 contiguous pulse periods (10 ≤ N ≤ 255). See ITU-T G.775 for reference.

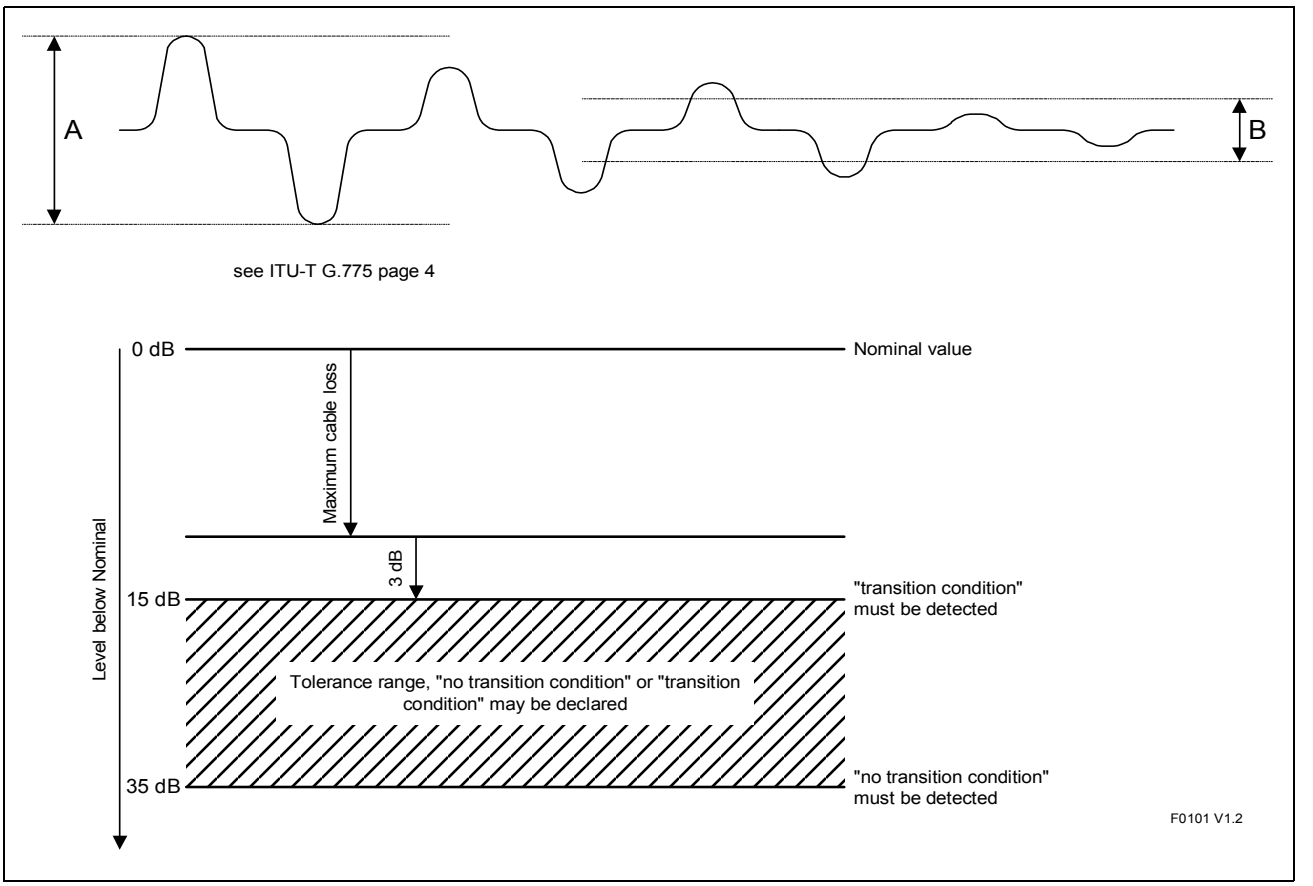


Figure 18 E3 Analog Loss of Signal (LOS) Definition

5.1.5 Receive Jitter Tolerance

The TE3-FALC receiver's tolerance to input jitter complies to and exceeds the relevant international standards. Especially the requirements of Telcordia GR-499-CORE (DS3), ITU-T G.824 (DS3) and ITU-T G.823 (E3) are fulfilled and exceeded. **Figure 19** and **Table 28** show the different input jitter specifications. Low frequency jitter is called "wander", where the defined border between jitter and wander is 10 Hz for DS3 and E3.

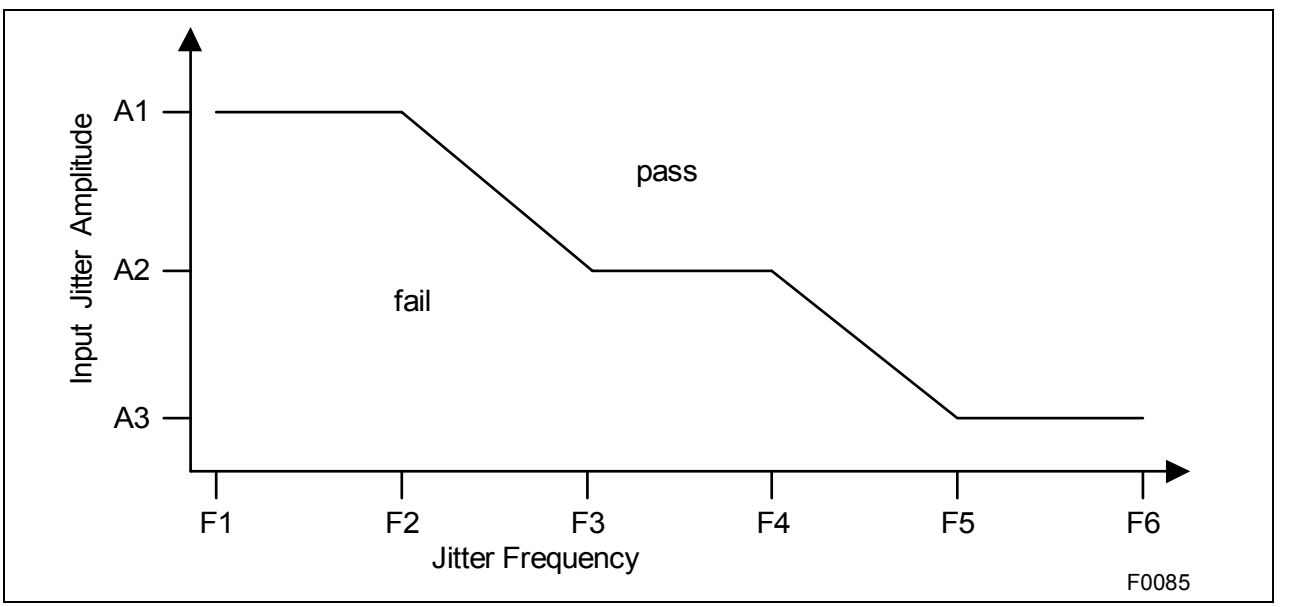


Figure 19 Jitter Tolerance Principle

Table 28 Input Jitter Requirements

Reference	A1	A2	A3	F1	F2	F3	F4	F5	F6
	[UI_{PP}]			[Hz]					
GR-499-CORE, Category I	5	0.1	not def.	10	2300	60 × 10^3	300 × 10^3	not def.	not def.
GR-499-CORE, Category II	10	0.3	not def.	10	669	22.3 × 10^3	300 × 10^3	not def.	not def.
ITU-T G.823 & ETSI TBR24	1.5	0.15	not def.	100	1000	10 × 10^3	800 × 10^3	not def.	not def.
ITU-T G.824	18 µs	5	0.1	not def.	1.2 × 10^{-5}	10	600	30 × 10^3	400 × 10^3

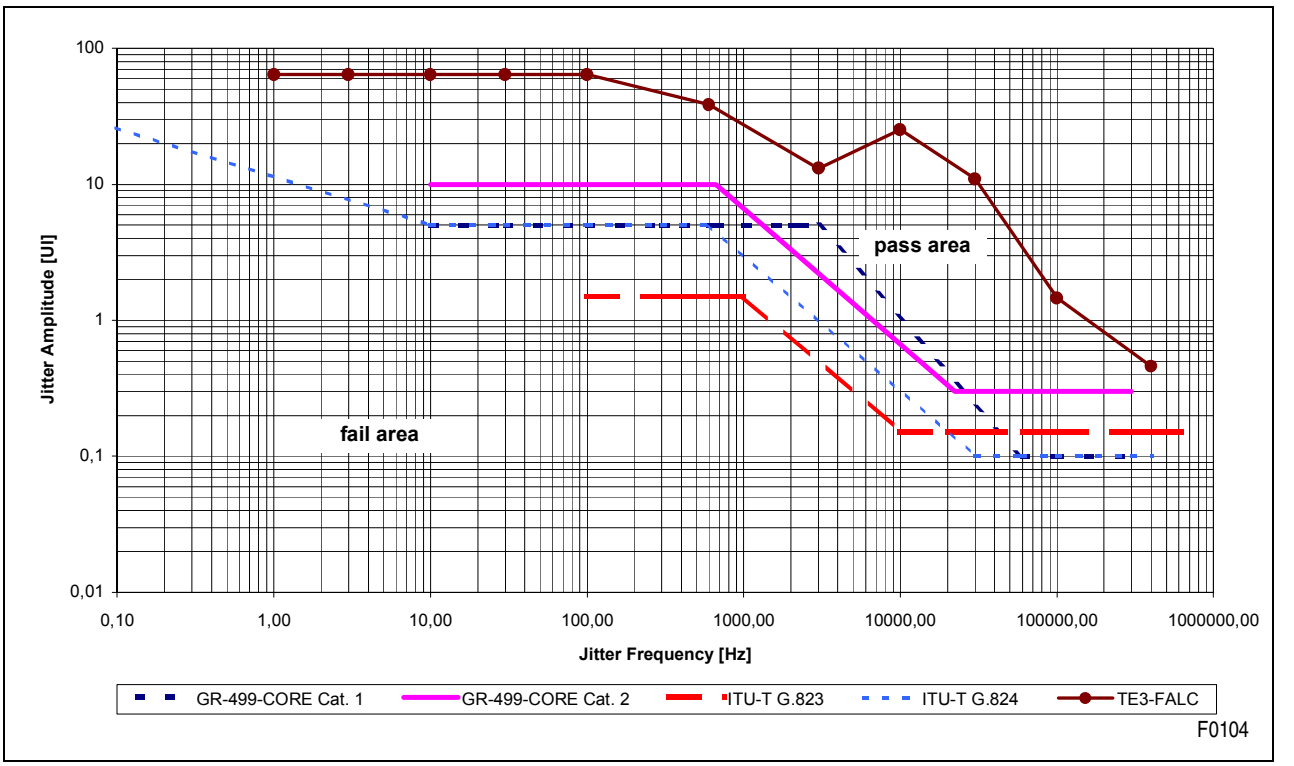


Figure 20 Jitter Tolerance

GR-499-CORE Jitter Tolerance Requirements (DS3)

The input jitter tolerance is defined as the minimum amplitude of sinusodial jitter at a given frequency that when modulating the signal at an equipment input port results in more than 2 errored seconds in a 30-second measurement interval. Requirements on input jitter tolerances are then given in terms of a jitter tolerance mask, which represents the minimum acceptable jitter tolerances for a specified range of jitter frequencies.

There are two different jitter tolerance masks defined for Category I (SONET interfaces) and Category II (non-SONET interfaces) equipment.

5.1.6 Transmitter Application

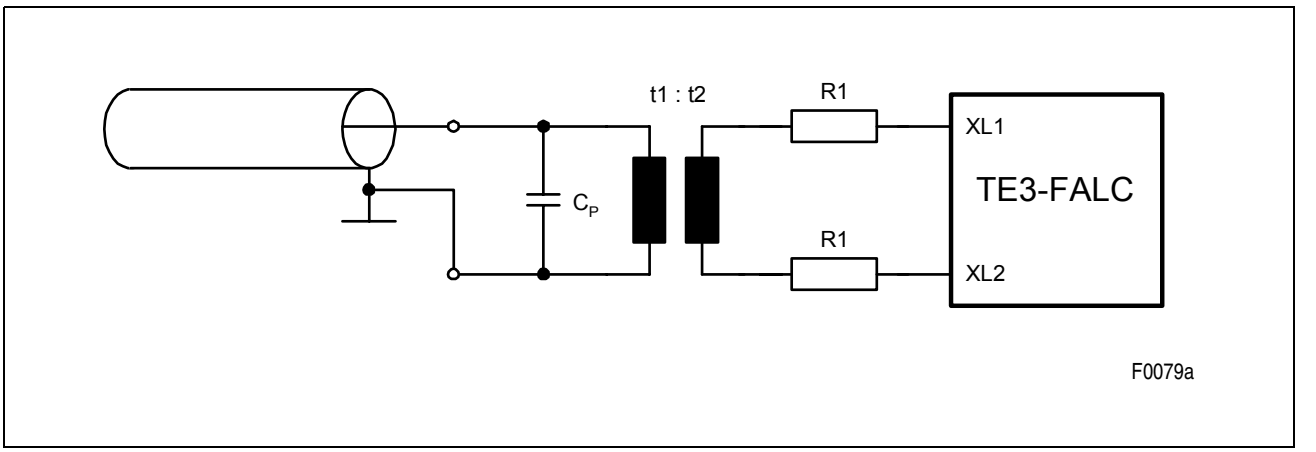


Figure 21 Transmitter Configuration

Table 29 External Component Values for Transmitter

Parameter	Characteristic Line Impedance [Ω]	
	DS3	E3
	75	
R_1 (± 1 %) [Ω]	37.5[1)]	
C_p [pF]	37[2)]	
$t_2 : t_1$	1 : 1	

1) This value refers to an ideal transformer without any parasitics. Any transformer resistance or other parasitic resistances have to be taken into account when calculating the final value for the output serial resistors.

2) This value includes all parisitic capacitances on the secondary side of the transformer.

The external components are the same for DS3 and E3 applications. Transmit return loss requirements for E3 defined in ETS 300 166 are fulfilled. Pulse mask requirements according to ANSI T1.102 (at cross connect point, up to 450 ft.) are fulfilled.

Note: An additional capacitor on the primary or secondary side of the transformer may be required in some DS3 applications to improve the pulse mask, if the parasitic capacitances of the PCB are very small.

Table 30 E3 Transmit Return Loss

Frequency Range		Return Loss[1)]
from [kHz]	to [kHz]	[dB]
860	1720	6
1720	51550	8

1) measured with an unframed PRBS 2^{15}-1 pattern

5.1.7 Transmit Pulse Shaper

The internal pulse shaper generates the required pulse shapes for E3 and DS3 signals according to ANSI T1.102, T1.404, Telcordia GR-499-CORE and ITU-T G.703).

The specific pulse mask is fulfilled at the crossconnect point at a distance of 0 to 450 ft. to the transmitter (DS3 requirement).

The maximum line length between a TE3-FALC transmitter and TE3-FALC receiver is 1100 ft. for a coaxial cable of AT&T type 728A, 734A or 734D.

5.2 DS3/E3 Digital Line Interface

The T3/E3 LIU can be bypassed and a digital clock and data interface can be provided via pins RDI, RCLKI, XCLK and XDO. This interface enables TE3-FALC to be connected to an external clock recovery circuit used for transmitting DS3/E3 over fiber or for connection to a DS3/E3 mapping device.

5.3 DS3/E3 Overhead, Bitstream and Payload Access Interface

The TE3-FALC provides serial access to the DS3/E3 frame overhead which enables proprietary framing formats or insertion/extraction of reserved overhead bits (named "Overhead Interface", see **Figure 22**). Once this interface is enabled, DS3/E3 frame overhead data can be extracted on the receive side at all times. Transmit overhead bits get overwritten whenever the DOHTINS signal is active (high) at the corresponding bit position. The first overhead bit is marked with the frame sync marker.

The TE3-FALC supports two serial payload interfaces, the first allows the TE3-FALC to act as a pure framer and provides clock, frame pulse and data signals for an external controller to map protocols, such as HDLC, into the frame (named "Bitstream Interface", see **Figure 22**). The second serial payload interface allows the data to and from the ATM cell processor or HDLC controller of the TE3-FALC to be accessed externally.

The latter two interfaces can be used together to provide a break in the TE3-FALC datapath (named "Bitstream Break-out", see **Figure 22**) to allow for external proprietary sub-rate framing to performed, such as those used for Subrate T3.

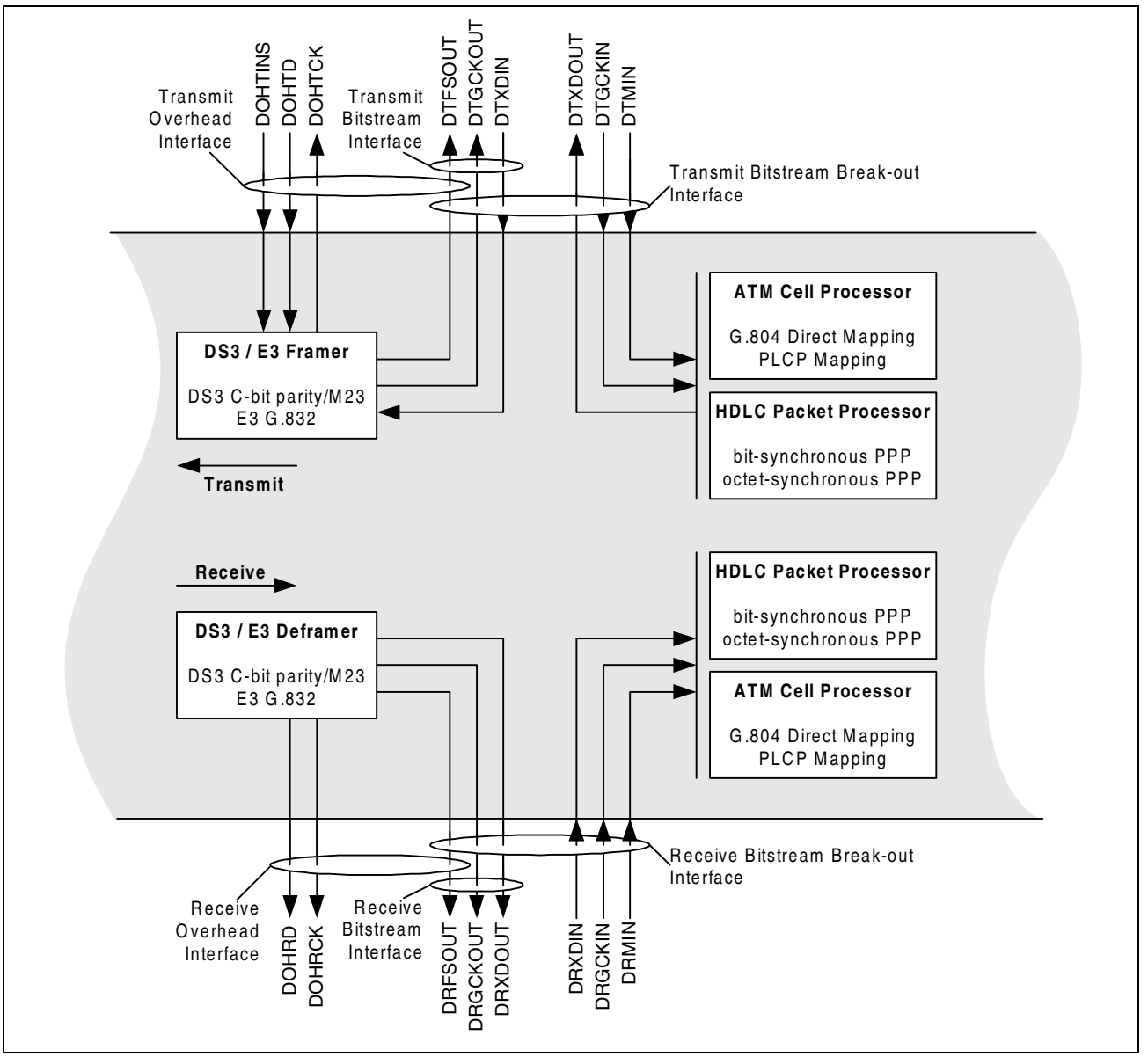


Figure 22 Overhead, Bitstream and Break-out Interface

Both overhead and bitstream interface share common frame sync markers. The signal timing is shown in **Figure 23** for the receive side and in **Figure 24** for the transmit side.

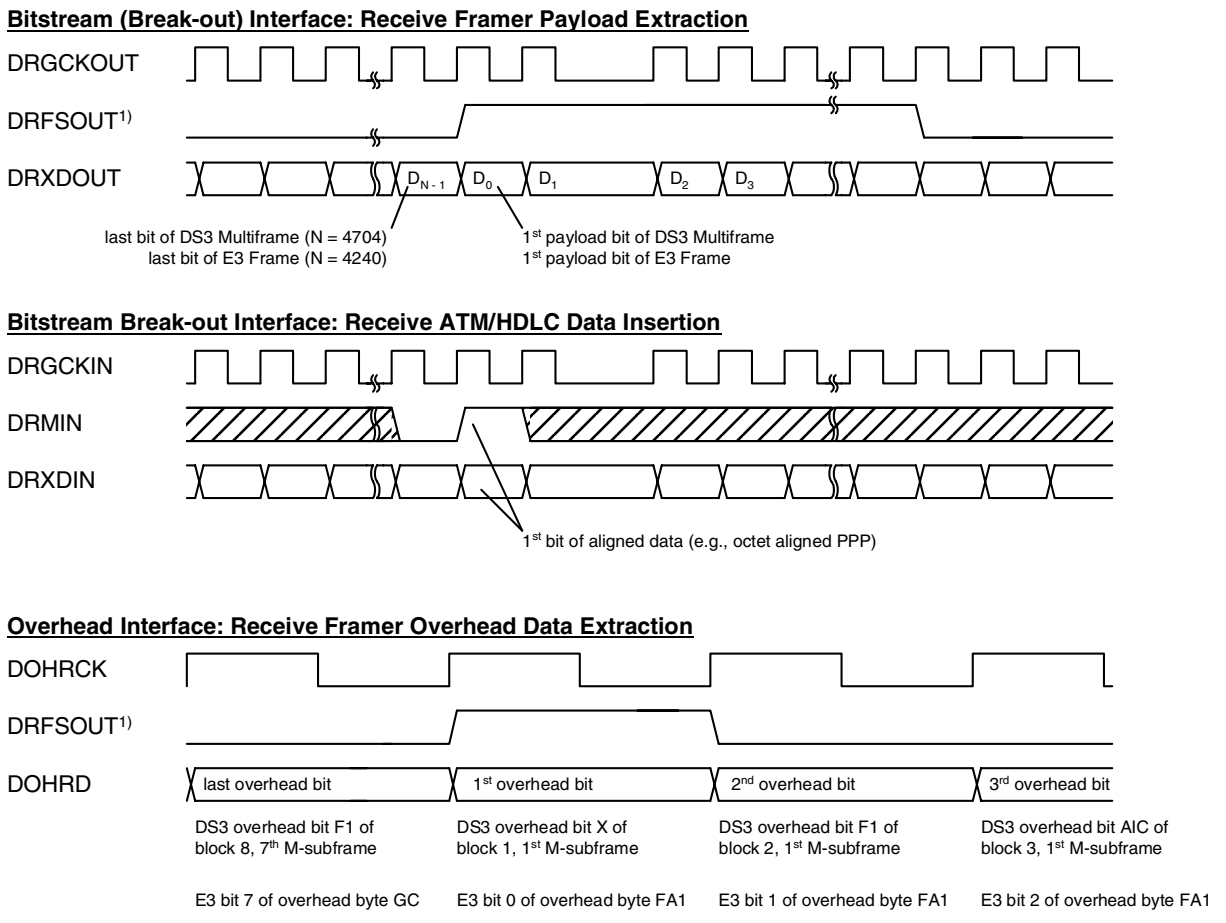


Figure 23 Receive Overhead, Bitstream and Break-out Interface Timing

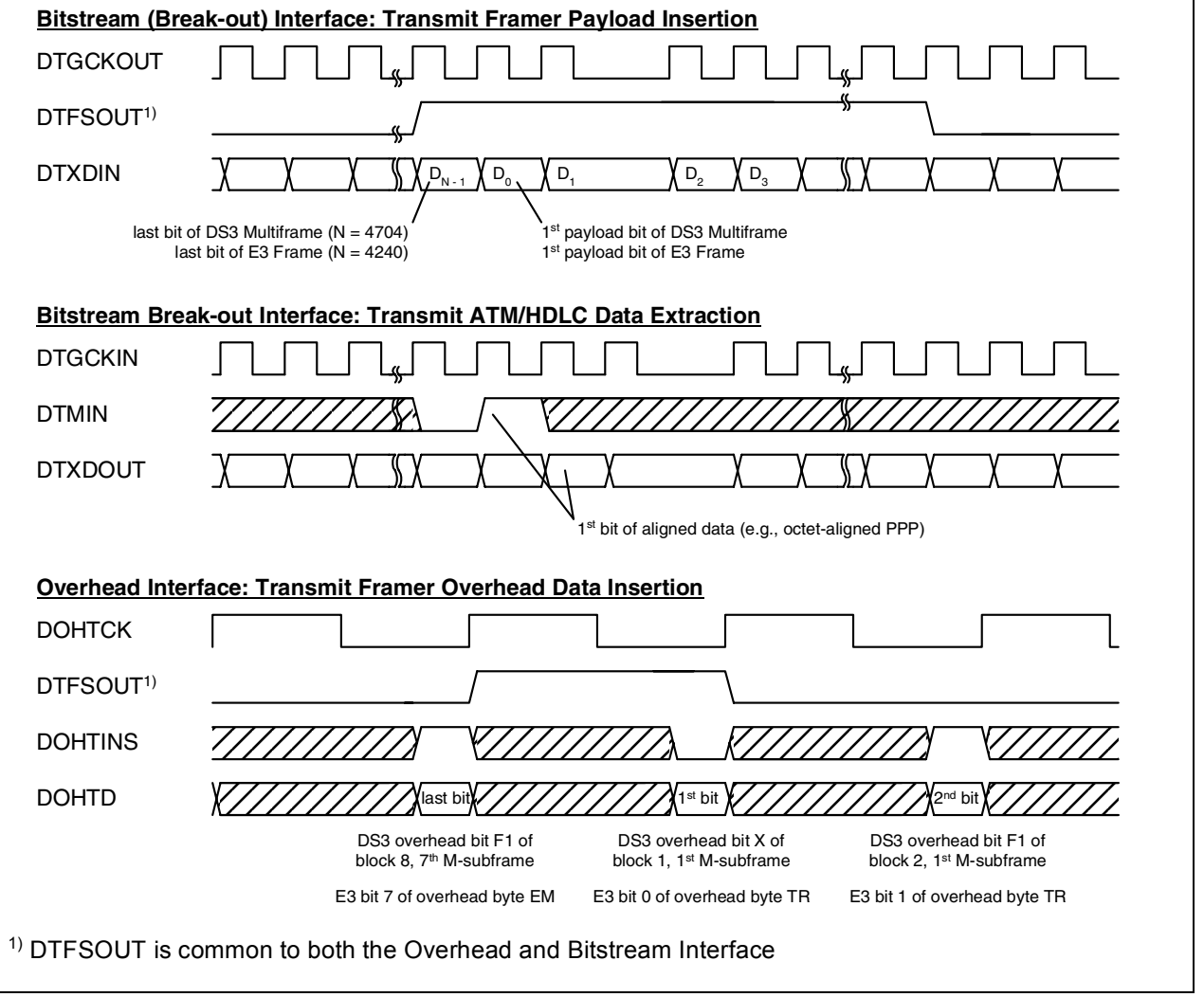


Figure 24 Transmit Overhead, Bitstream and Break-out Interface Timing

5.4 Clock Multiplier Interface

The TE3-FALC integrates PLL's to enable the generation of T3/E3 line rate clocks for use in both transmit and receive directions. The TE3-FALC requires only a single clock, CLKIN, which can vary between 4 MHz to 52 MHz, the frequency range is selected by setting pins P0, P1 and P2 (1st stage PLL programming) with fine tuning via internal registers (2nd stage PLL programming). All required clocks can be generated via CLKIN, this includes transmit line clock, receive reference clock, high speed clocks for the TX and RX DJAT's, internal logic and also a programmable output clock CLKOUT which can be used by the system (e.g. for UTOPIA clock).

TCLKIN is the optional transmit reference clock, this clock can be the reference for the TX DJAT PLL or be used as the exact transmit clock (bypass the DJAT PLL). The reference clock for the TX DJAT PLL can vary between 8 kHz and 52 MHz.

RSYNC is the optional receive reference clock, the TE3-FALC can use this clock during LOS conditions for a reference to the RX DJAT PLL. The reference clock for the RX DJAT PLL can vary between 8 kHz and 52 MHz. The clock recovery PLL uses a reference clock derived from CLKIN in case of LOS conditions.

✧REF8K is an optional 8 kHz input used to synchronize the PLCP sub-frame inside a DS3 frame; it does not need to be synchronous with TCLKIN[1)].

The TE3-FALC monitors clock activity on TCLKIN and RSYNC and can switch back to internally generated clocks, this provides the ability for the TE3-FALC to continue operating (e.g. to enable AIS transmission) when the central clock unit of a system fails or is removed.

Two clock outputs are provided: CLKOUT and RCLKOUT.

CLKOUT is a programmable general purpose clock, e.g. for UTOPIA clock.

RCLKOUT is the recovered line clock, this clock can be taken directly from the clock recovery unit and in this case is the line rate clock (34 or 45 MHz) with jitter. Optionally the RCLKOUT can pass through the RX DJAT PLL and to provide a smooth reference clock that can be divided down from the line clock by a arbitary factor (e.g to give an 19.44 MHz, 2.048 MHz or 8 kHz reference). The RX DJAT also provide optional holdover for RCLKOUT during LOS rather than switching back to the receive reference clock.

5.5 System Interface (UTOPIA / POS-PHY / UTOPIA-L2X)

The system side of the TE3-FALC implements a streaming interface which represents a superset of the industry standard interfaces:

– UTOPIA
– POS-PHY
– UTOPIA-L2X

The TE3-FALC acts as slave on these interfaces.

UTOPIA-L2X ("UTOPIA Level 2 with packet eXtension") interface supports the transfer of variable size packets in form of segments (chunks). POS-PHY interface also supports the transfer of variable size packets and mainly differs in the signalling.

Standard UTOPIA is considered a sub-mode of the packet oriented modes, with the assumption that an ATM cell is a fixed size packet with a length of 53 bytes (8-bit UTOPIA interface) or 27 words (16-bit UTOPIA interface).

The data bus can be configured to be 8-bit or 16-bit wide in all interface modes (although 8-bit bus width is not standardised in POS-PHY Level 2). The data format is big endian

1) Firmware option. TE3-FALC uses by default a fixed PLCP stuffing sequence which results in a nominal frame rate of 7.999848 kHz in DS3 master timed mode. In DS3 loop-timed mode, the recovered 8 kHz from the receiver is used as PLCP transmit reference.

and the parity calculated over the data bus lines is odd. The size of the chunks is programmable.

The signals listed in **Table 31** and **Table 32** cover the functionality of the UTOPIA / UTOPIA-L2X / POS-PHY interface signals. These tables shall be used as a reference.

Table 31 Receive UTOPIA / POS-PHY / UTOPIA-L2X Interface Signals

TE3-FALC Signal	I/O	Function	UTOPIA	POS-PHY	UTOPIA-L2X
SRCLK	I	Receive Clock	RxClk	RFCLK	RCLK
SRADDR [4:0]	I	Receive Poll Address	RxAddr [4:0]	RADR [4:0]	RADDR [4:0]
SRD[15:0]	O	Receive Data D15-D0	RxData [15:0]	RDAT [15:0]	RD [15:0]
SRPRTY	O	Receive Parity	RxPrty	RPRTY	RPRTY
$\overline{\text{SRENB}}$	I	Receive Enable	$\overline{\text{RxEnb}}$	$\overline{\text{RENB}}$	$\overline{\text{RENB}}$
SRVAL	O	Receive Data Valid	-	RVAL	-
SRSX	O	Receive Start of Cell/Chunk	RxSoc	-	RSX
SRSOP	O	Receive Start of Packet	-	RSOP	RSOP
SREOP	O	Receive End Of Packet	-	REOP	REOP
SRMOD	O	Receive Modulo Count	-	RMOD	RMOD
SRERR	O	Receive Error	-	RERR	RERR
SRPA	O	Receive Pkt./Cell Avail. – Polled Status – Direct Status	 RxClav $\overline{\text{RxClav}}$/ $\overline{\text{RxEmpty}}$	 PRPA DRPA	 RPA RPA

Table 32 Transmit UTOPIA / POS-PHY / UTOPIA-L2X Interface Signals

TE3-FALC Signal	I/O	Function	UTOPIA	POS-PHY	UTOPIA-L2X
STCLK	I	Transmit Clock	TxClk	TFCLK	TCLK
STADDR [4:0]	I	Transmit Poll Address	TxAddr [4:0]	TADR [4:0]	TADDR [4:0]
STD[15:0]	I	Transmit Data D15-D0	TxData [15:0]	TDAT [15:0]	TD [15:0]
STPRTY	I	Transmit Parity	TxPrty	TPRTY	TPRTY
$\overline{\text{STENB}}$	I	Transmit Enable	$\overline{\text{TxEnb}}$	$\overline{\text{TENB}}$	$\overline{\text{TENB}}$

Table 32 Transmit UTOPIA / POS-PHY / UTOPIA-L2X Interface Signals (cont'd)

TE3-FALC Signal	I/O	Function	UTOPIA	POS-PHY	UTOPIA-L2X
STSX	I	Transmit Start of Transfer/ Cell	TxSoc	*pull-down*	TSX
STSOP	I	Transmit Start Of Packet	*pull-down*	TSOP	TSOP
STEOP	I	Transmit End Of Packet	*pull-down*	TEOP	TEOP
STMOD	I	Transmit Modulo Count	*pull-down*	TMOD	TMOD
STERR	I	Transmit Error	*pull-down*	TERR	TERR
STRDY	O	Transmit Ready	-	STPA	-
STPA	O	Transmit Pkt./Cell Avail. – Polled Status – Direct Status	 TxClav TxClav/ $\overline{\text{TxFull}}$	 PTPA DTPA	 TPA TPA

5.5.1 UTOPIA Interface Option

For a description of the UTOPIA Level 2 interface protocol refer to ATM-Forum specification af-phy-0039.000. Regarding the TE3-FALC interface signals consider the following:

- Packet signals SOP, EOP, ERR and MOD are not used. The corresponding transmit inputs shall be pulled down to V_{SS} level, corresponding receive outputs can be left unconnected.
- SRSX/STSX are equivalent to the UTOPIA start of cell signals RxSoc/TxSoc.
- SRPA/STPA are equivalent to the UTOPIA cell-available signals RxClav/TxClav.

Optional UTOPIA Settings

- Bus Width
  - 8-bit
  - 16-bit
- Handshake
  - Cell-level handshake
  - Octet-level handshake
- Status Indication
  - MPHY polling mode
  - Direct status indication
- Bus Configuration
  - Multiple PHY devices (tri-state bus)
  - Single PHY, point-to-point connection (outputs do not tri-state)
- Parity Check

– Parity check enabled.
  Parity-errored cells are discarded within transmit buffer.
– Parity check disabled

UTOPIA Cell Format

For 16-bit UTOPIA interface the 54-octet cell format is used, with big endian byte arrangement. For 8-bit UTOPIA interface the 53-octet cell format applies. The following structures show the supported cell formats.

54-octet Format

D15 D8	D7 D0
H1	H2
H3	H4
UDF1[1)]	UDF2[1)]
P1	P2
:	:
P47	P48

53-octet Format

D7 D0
H1
H2
H3
H4
UDF[1)]
P1
:
P48

[1)] User Defined Field; this field is not evaluated by the TE3-FALC.

5.5.2 POS-PHY Interface Option

The POS-PHY Level 2 interface has been defined by the SATURN group. For a description of the interface protocol refer to the POS-PHY Level 2 specification. The TE3-FALC signals SRSX/STSX are unused; the transmit input STSX should be pulled down to V_{SS} level, SRSX can be left unconnected.

Optional POS-PHY Settings

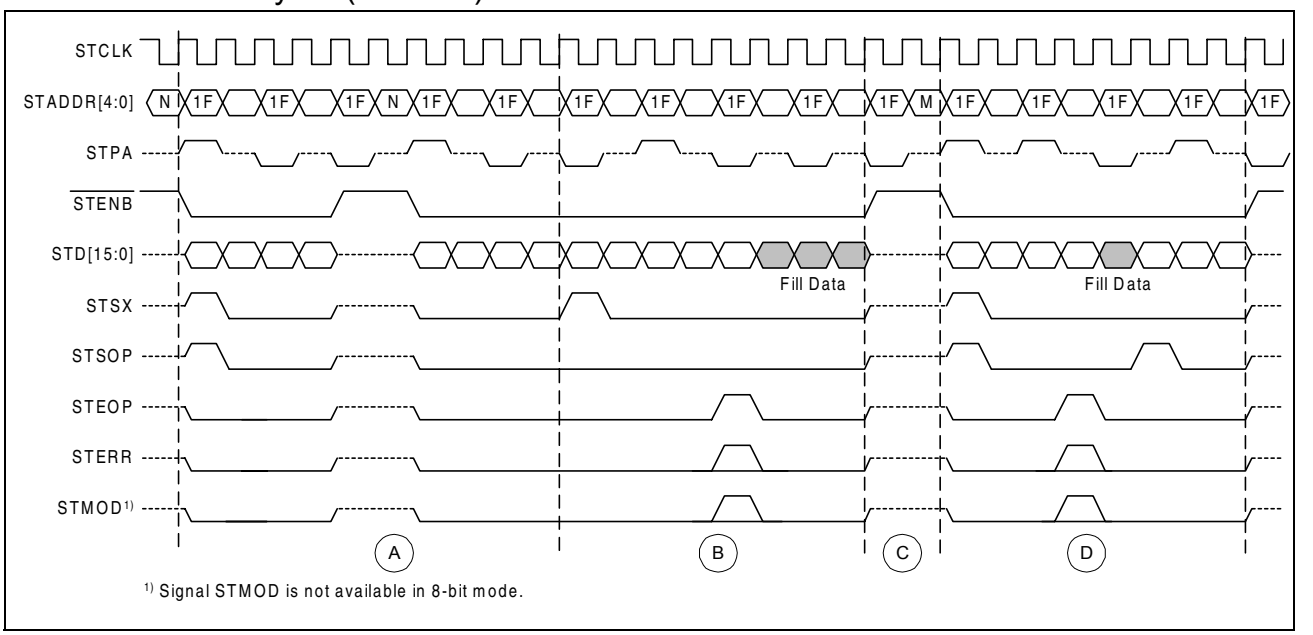
- Bus Width
  – 8-bit
  – 16-bit
- Status Indication
  – Packet level mode
  – Byte level mode
- Bus Configuration
  – Multiple PHY devices (tri-state bus)
  – Single PHY, point-to-point connection (outputs do not tri-state)
- Parity Calculation

– Odd or Even parity generation/check
  Short parity-errored packets are discarded within transmit buffer.
  Long parity-errored packets are aborted on the line.
– Parity check disabled

5.5.3 UTOPIA-L2X Interface Option

UTOPIA-L2X Transmit

Following diagram shows an example of packet oriented transmit data transfer with a chunk size of 16 bytes (8 words):



The channel polling and selection using the address bus STADDR[4:0] and the enable signal STENB is identical to the UTOPIA-L2 mechanism (UTOPIA signals named TxAddr[4:0] and TxEnb). In the section (A), PHY N is selected with STENB transitioning from high to low. The first word of the chunk transfer is indicated with an active STSX signal. The active STSOP signal indicates that this chunk is the start of a packet.

In the middle of this chunk transfer two wait states are inserted by the higher-layer device by deasserting the STENB signal. Note that correct PHY address N must be present on the address bus before STENB is asserted again.

Section (B) contains the second chunk belonging to the packet started in (A). Before this chunk transfer completes, the STEOP signal gets active indicating the last word transfer for the current packet. Data between the STEOP marker and the following STSOP marker (fill data) is disregarded by the PHY.

TMOD asserted along with STEOP indicates that the packet has an odd byte count. In that case valid data is only located on lines STD[15:8] (big endianess).

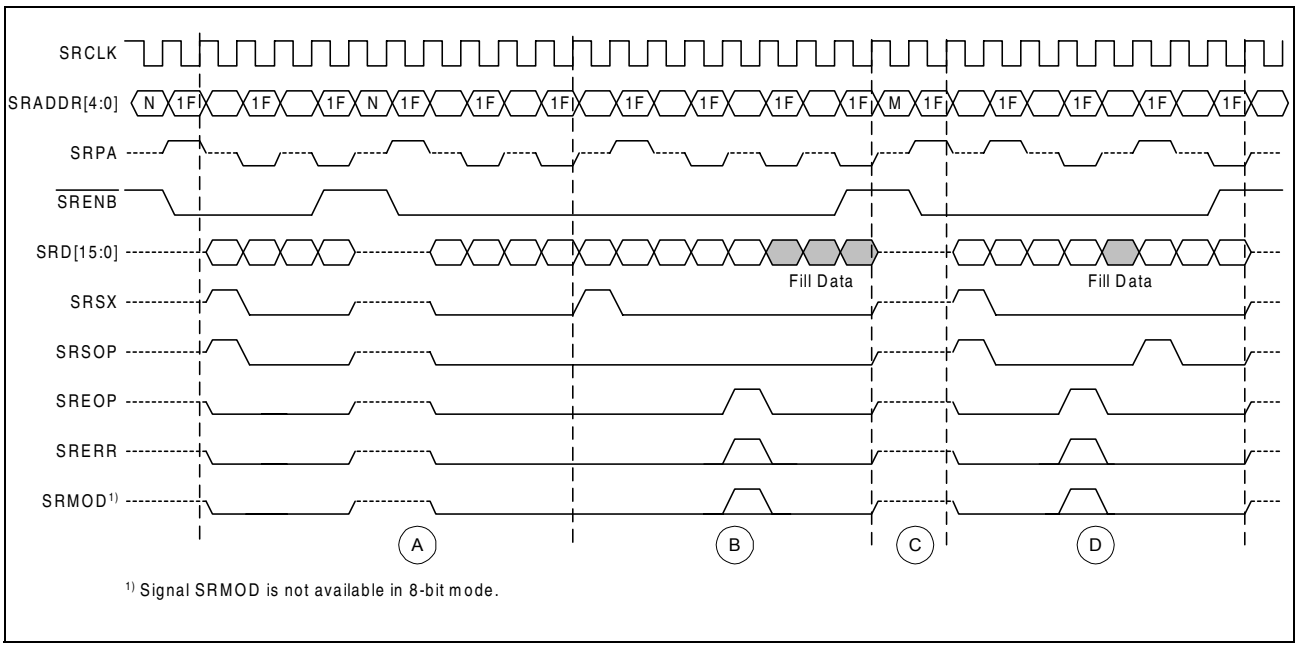
The higher-layer device has the possibility to invalidate a packet sent to the TE3-FALC by asserting the STERR line along with STEOP. In case of HDLC/PPP protocol this leads to the well defined abort sequence.

In section (C), PHY M gets selected for the next chunk transfer.

Chunk (D) carries one complete (short) packet and the start of another packet for the same PHY M. Again, data between STEOP and STSOP marker is disregarded.

UTOPIA-L2X Receive

The receive UTOPIA-L2X interface works analogue to the transmit interface. The function of signals SRADDR, SRPA, SRENB, SRD, SRPRTY (not in the diagram) SRSX, SRSOP, SREOP and SRMOD is the same.



Signal SRERR asserted along with SREOP indicates that the received packet was errored and thus has to be discarded. The cause for the error is coded in an error status byte ERRSTA which is copied to both the upper and the lower byte of the last 16-bit word transfer (with SRERR asserted).

Receive Error Status Word (ERRSTA)

7	6	5	4	3	2	1	0
0	MAXFL	RFO	CRC	ILEN	RAB	0	0

RAB	Receive Abort
ILEN	Illegal length (octet boundary error, for bit-synchronous HDLC only)
CRC	CRC Error
RFO	Receive FIFO Overflow
MAXFL	Maximum Frame Length exceeded (limit programmable)

Optional UTOPIA-L2X Settings

- Bus Width
  - 8-bit
  - 16-bit
- Chunk Size
  - Programmable to 16 .. 64 bytes (multiple of 4 bytes)
- Status Indication
  - MPHY polling mode
  - Direct status indication
- Bus Configuration
  - Multiple PHY devices (tri-state bus)
  - Single PHY, point-to-point connection (outputs do not tri-state)
- Parity Check
  - Parity check enabled.
    Short-parity errored packets are discarded within transmit buffer.
    Long-parity errored packets are aborted on the line.
  - Parity check disabled

5.6 Microprocessor Interface

The microprocessor interface (MPI) can be configured to asynchronous Intel or Motorola like handshake, the Motorola mode offers additionally a synchronous interface option with MPC860 compatible handshake. The multiplexing of pins for the three interface options is shown in **Table 33**.

Table 33 Intel/Motorola Pin Correspondence

Intel	Motorola	
Demux Mode (= Pin Name)	**Asynchronous Mode**	**Synchronous Mode**
MPIM[1:0] = 10	MPIM[1:0] = 11	MPIM[1:0] = 01
$\overline{\text{MPCS}}$		
MPA[19:0]		
$\overline{\text{MPBHE}}$	$\overline{\text{MPBLE}}$	MPTSIZ0
$\overline{\text{MPWR}}$	MPR/$\overline{\text{W}}$	
$\overline{\text{MPRD}}$	$\overline{\text{MPDS}}$	$\overline{\text{MPTS}}$
$\overline{\text{MPREADY}}$	MPDTACK	MPTA
MPD[15:0]		

For timing diagrams showing read and write accesses for the three interface configurations refer to **Chapter 7.5.1**.

5.6.1 Slave Accesses (Device Configuration/Control)

Communication with the TE3-FALC is done via MPI slave accesses according to the message based Device Control Interface (DCI, refer to **Chapter 6.1** for details). Internal data structures are 32-bit wide, and in general 32-bit words (→DWORD) have to "tunnel" through the low pin-count MPI with 16- or 8-bit data bus width.

5.6.1.1 Byte Mapping in 8-bit Mode

Table 5-1 and **Table 5-2** provide a reference for the mapping of accesses in 8-bit MPI mode to the TE3-FALC's internal 32-bit data structures.

Table 5-1 8-bit Intel Mode

A1	A0	32-bit word internal to TE3-FALC			
		31 24	23 16	15 8	7 0
0	0				MPD[7:0]
0	1			MPD[7:0]	
1	0		MPD[7:0]		
1	1	MPD[7:0]			

Table 5-2 8-bit Motorola Mode

A1	A0	32-bit word internal to TE3-FALC			
		31 24	23 16	15 8	7 0
0	0	MPD[7:0]			
0	1		MPD[7:0]		
1	0			MPD[7:0]	
1	1				MPD[7:0]

5.6.1.2 Byte Mapping in 16-bit Mode

Table 5-3, **Table 5-4** and **Table 5-5** provide a reference for the mapping of accesses in 16-bit MPI mode to the TE3-FALC's internal 32-bit data structures. Note that in synchronous 16-bit Motorola mode no byte accesses are supported.

Table 5-3 16-bit Intel Mode

$\overline{BHE}$	A1	A0	32-bit word internal to TE3-FALC			
			31 24	23 16	15 8	7 0
0	0	0			MPD[15:8]	MPD[7:0]
0	1	0	MPD[15:8]	MPD[7:0]		

Table 5-3 16-bit Intel Mode (cont'd)

$\overline{BHE}$	A1	A0	32-bit word internal to TE3-FALC 31 24 23 16 15 8 7 0			
1	0	0				MPD[7:0]
0	0	1			MPD[15:8]	
1	1	0		MPD[7:0]		
0	1	1	MPD[15:8]			
1	X	1	not allowed			

Table 5-4 16-bit Asynchronous Motorola Mode

$\overline{BLE}$	A1	A0	32-bit word internal to TE3-FALC 31 24 23 16 15 8 7 0			
0	0	0	MPD[15:8]	MPD[7:0]		
0	1	0			MPD[15:8]	MPD[7:0]
1	0	0	MPD[15:8]			
0	0	1		MPD[7:0]		
1	1	0			MPD[15:8]	
0	1	1				MPD[7:0]
1	X	1	not allowed			

Table 5-5 16-bit Synchronous Motorola Mode

TSIZ0	A1	A0	32-bit word internal to TE3-FALC 31 24 23 16 15 8 7 0			
0	0	0	MPD[15:8]	MPD[7:0]		
0	1	0			MPD[15:8]	MPD[7:0]
1	X	X	not allowed			

5.6.2 Master Accesses (8-Bit EPROM Load Function)

TE3-FALC performs master read accesses to an external EPROM/EEPROM/Flash during the boot process if an appropriate boot configuration is selected via pins CFG[2:0]. The addressable range is 128 kB using address lines A[16:0].

Prior to a read access the TE3-FALC arbitrates for bus mastership. Both Intel and Motorola arbitration mechanisms are implemented, **Table 34** gives an overview of the pin correspondence in both modes:

Table 34 Intel/Motorola Master Pin Correspondence

Intel MPIM[1:0] = 10 or MPIM[1:0] = 00	Motorola MPIM[1:0] = 11 or MPIM[1:0] = 01
$\overline{\text{MPMCS}}$	
MPA[16:0]	
$\overline{\text{MPRD}}$	$\overline{\text{MPDS}}$
MPD[7:0]	
MPHOLD	$\overline{\text{MPBR}}$
MPHLDA	$\overline{\text{MPBG}}$
unused	$\overline{\text{MPBB}}$

5.6.2.1 Arbitration Intel Mode

Figure 25 explains the arbitration in Intel mode. The TE3-FALC starts arbitration by asserting the MPHOLD signal[1]. As soon as the module gets access to the bus via MPHLDA it begins the bus transaction. The signal MPHOLD remains active until the transaction is finished. It is ensured that no bus signal is driven by MPI master when MPHOLD gets inactive.

The maximum count of consecutive read accesses without new bus arbitration is 16; the MPHLDA is required to go inactive after each transaction. If TE3-FALC is the only bus master, the MPHOLD output should be connected to the MPHLDA input.

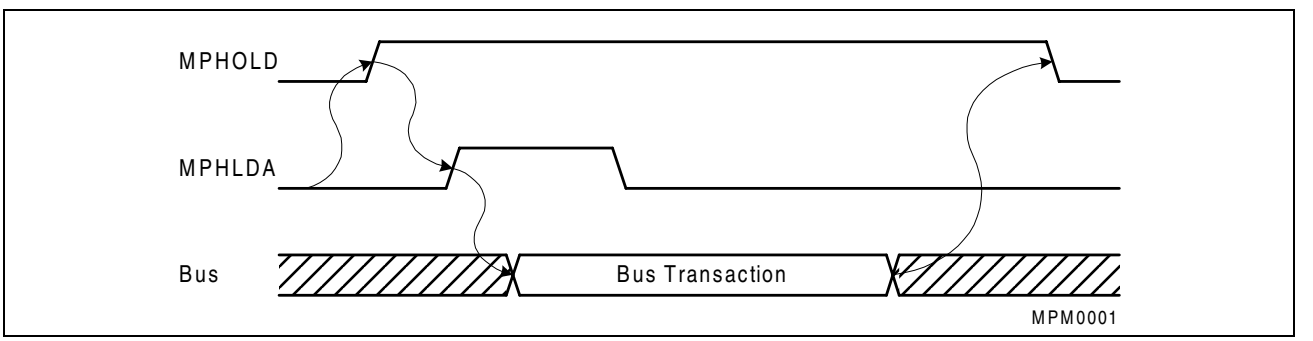


Figure 25 Intel Arbitration

[1] Input MPHLDA is required to be inactive, otherwise TE3-FALC will not start arbitration.

5.6.2.2 Arbitration Motorola Mode

Figure 26 shows the arbitration in Motorola mode. The MPI master starts arbitration by asserting the MPBR signal (low). After receiving an bus grant MPBG the MPI master has to wait until MPBB becomes or is inactive (high). Now it activates the MPBB signal and begins the bus transaction. The signal MPBB remains active until the transaction is finished. It is ensured that no bus signal is driven by MPI master when MPBB gets inactive.

The maximum count of read accesses without new bus arbitration is 16; the MPBG is required to go inactive after each transaction. If TE3-FALC is the only bus master, the MPBR output should be connected to the MPBG input.

The signal MPBB is an open drain signal; only the low phase is driven.

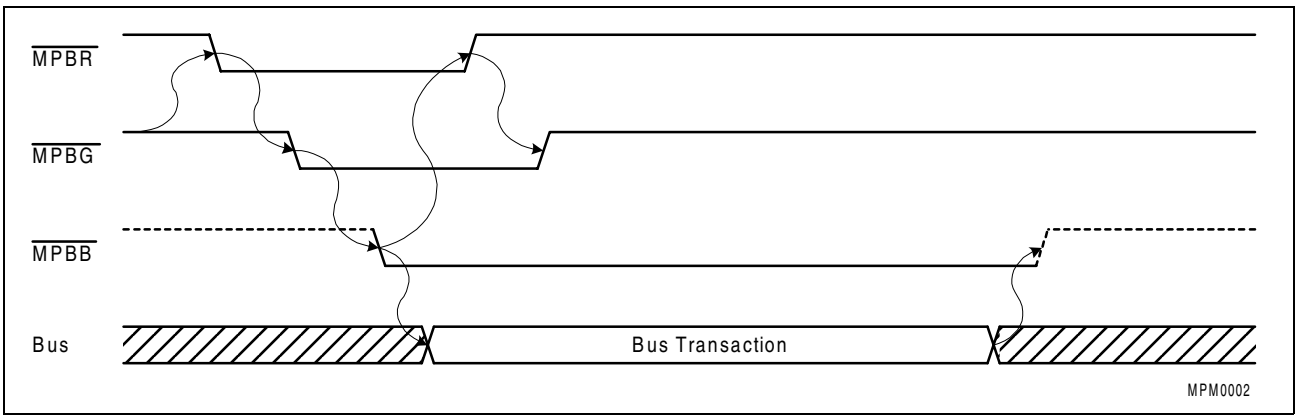


Figure 26 Motorola Arbitration

5.6.2.3 Master Read Access

Figure 27 illustrates a read access. The TE3-FALC as a master can do read accesses only, with a data bus width of 8-bit.

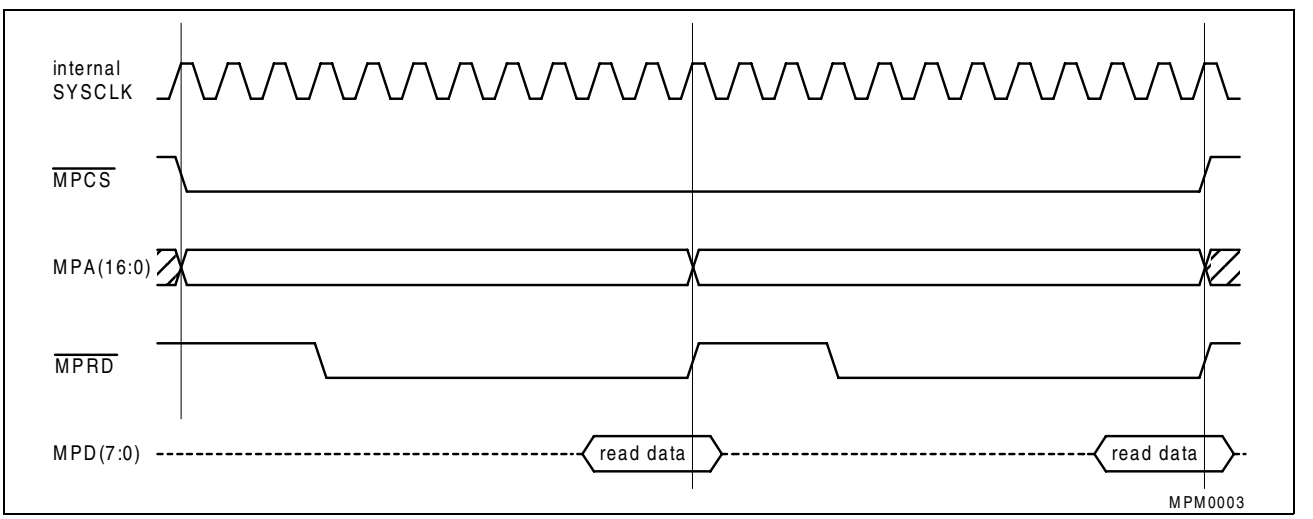


Figure 27 Master Read Access

After the TE3-FALC is granted to access the bus, the address and the $\overline{\text{MPCS}}$ signal are driven synchronously to the internal system clock (SYSCLK). After three system clock cycles the $\overline{\text{MPRD}}$ signal is activated. The $\overline{\text{MPRD}}$ signal can be used as output enable at the EPROM. 17 system clock cycles later the read data is expected to be valid and is registered in. The next read cycle can follow directly. If after 20 system clock cycles no more internal read request comes up, the TE3-FALC relinquishes the microprocessor bus.

5.7 JTAG Interface

A Test Access Port (TAP) with boundary scan operation is implemented according to IEEE 1149.1. For details refer to **Chapter 8.1** on **Page 170**.

5.8 Control Interface

Power-On Reset

Setting the external input pin $\overline{\text{POR}}$ to 0 resets the complete chip with new image download. This is an asynchronous reset.

Boot Mode Configuration

The 3 pins CFG[2:0] exist for configuration of the boot mode.

For boot operation via the message based Device Control Interface (DCI), pins (CFG2, CFG1, CFG0) should be set to (0, 0, 1).

To boot from an external EPROM, pins (CFG2, CFG1, CFG0) should be set to (0, 1, 1).

Any other settings are for debug purpose or future use.

5.9 General Purpose I/O Port

The general purpose I/O port comprises two functions:

PLL Frequency Programming

At the beginning of the boot process, right after reset, the input levels on pins P2, P1 and P0 are used to roughly program the on-chip PLL such that it generates a system clock of 25 to 50 MHz derived from the provided clock CLKIN.

Note: Wrong PLL frequency programming might lead to internal overclocking and can thus influence the reliablitiy of the device’s operation!

Table 35 PLL Frequency Programming

P2, P1, P0	CLKIN Clock Supply Frequency
000_2	*Reserved.*
001_2	*Reserved.*
010_2	4 MHz < CLKIN ≤ 8 MHz
011_2	8 MHz < CLKIN ≤ 16 MHz
100_2	16 MHz < CLKIN ≤ 32 MHz
101_2	32 MHz < CLKIN ≤ 52 MHz
110_2	*Reserved.*
111_2	Analog PLL bypassed; system clock is CLKIN divided by 2.

The appropriate pin coding shall be realized with external pull-up / pull-down resistors.

General Purpose Input/Output Function

During operation, pins P0 to P7 are used as general purpose inputs and outputs. Optionally an internal pull-up or pull-down transistor can be enabled which eliminates the need for an external resistor.

5.10 UART Interface

✧The UART interface is available for debug purposes. The output can be monitored via a terminal with following settings:

- 9600 bit/s
- 1 Start bit
- 8 Data bits
- No Parity
- 1 Stop bit

6 Software Interface Description

6.1 Device Control Interface (DCI)

The Device Control Interface (DCI) is built to make the configuration and controlling of the device easier and more comfortable. The DCI is a dual-ported Memory- and Register-Area which is accessible for the user.

Table 36 TE3-FALC Memory Map

	Address		Comment
DCI Memory Area (32 kB)	$FFFF_H$ $A000_H$	reserved	
	$9FFF_H$ 9000_H	Egress Buffer for Parameter Arrays	TE3-FALC is responsible for memory management.
	$8FFF_H$ 8000_H	Ingress Buffer for Parameter Arrays	User is responsible for memory management.
DCI Register Area	$7FFC_H$	MCR	MPI Control Register
	$7FF8_H$ 0294_H	reserved	
	0290_H	HPQIN_CNT	Access to High/Low Priority Ingress/ Egress Message Queues. 32-bit wide Message Actuators are exchanged here.
	0280_H	HPQIN message queue	
	0270_H	LPQIN_CNT	
	0260_H	LPQIN message queue	
	0250_H	HPQOUT_CNT	
	0240_H	HPQOUT message queue	
	0230_H	LPQOUT_CNT	
	0220_H	LPQOUT message queue	
	0134_H	DCIERR	DCI Error Indicatior Register
	0014_H	INTMSK	Interrupt Mask Register
	0010_H	INTREG	Interrupt Status Register
	0000_H	reserved	

This interface decouples the internal functional blocks from the external microprocessor bus. The RAM data width is 32 bits, the depth is 8192 words, resulting in an overall size of 32 kBytes. **Table 36** shows how memory and register areas are mapped to the 16-bit addressable range of the TE3-FALC.

The memory regions to be accessed by the host processor during normal operation are shown as white areas.

Message Queues

The DCI manages four message queues (LPQOUT, HPQOUT, LPQIN, HPQIN) which are accessible from the internal and from the external bus for read and write, with the external access having the higher priority.

The width of the message words is 32 bits. TE3-FALC only allows 16- or 8-bit accesses to these 32-bit structures. Thus, one byte of the 32-bit word is configured as an "indicator" byte. Writing to the indicator byte of a 32-bit word increments the write pointer, reading the indicator byte increments the read pointer (destructive read/write), while reading or writing other bytes of a word does not influence the pointers. Thus the message queue indicator byte should be read/written last (see **Table 37**).

A level counter (LPQOUT_CNT, HPQOUT_CNT, LPQIN_CNT, HPQIN_CNT) indicates how many words are stored inside the message queue. The counter is incremented with every indicator byte write and is decremented with every indicator byte read. This counter is stored in a read only register and this register is accessible from both sides. In case of reading an empty queue, all zeros get returned. In case of writing to a full queue the written word is discarded.

Table 37 8-/16-bit Accesses to an Internal 32-bit Word

		8-bit Access		16-bit Access		
A[1:0]		Motorola	Intel		Motorola	Intel
00	1st	Byte 3	Byte 0	1st	Byte 3 Byte 2	Byte 1 Byte 0
01	2nd	Byte 2	Byte 1			
10	3rd	Byte 1	Byte 2	2nd	Byte 1 Byte 0	Byte 3 Byte 2
11	4th	Byte 0	Byte 3			

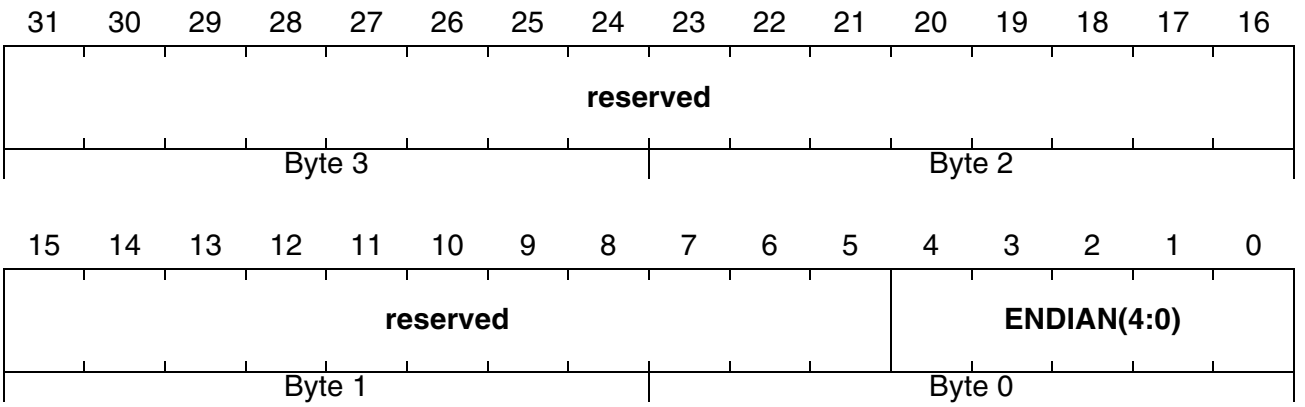
Internal 32-bit Word	Byte 3	Byte 2	Byte 1	Byte 0

Indicator Byte for INTREG Indicator Byte for Message Queues

The MPI Control Register MCR allows to configure the indicator bytes mentioned above, depending on the endianess of the host processor. This register should only be

programmed with a Read-Modify-Write sequence to preserve control information within the bits marked as "reserved".

MCR
MPI Control Register **rd/wr** **Reset value: 0000 00x0$_H$**
Address: 7FFC$_H$



MCR Register Bits:

ENDIAN (4:0) **Host Processor Endianess**
The code entered in this bit field defines the indicator bytes settings required for the host processor's endianess. Codes other than listed are reserved.

07_H Little Endian (Intel-like addressing)

19_H Big Endian (Motorola-like addressing)

Note: To evaluate the host processor's addressing scheme it might be helpful to initiate a 32-bit read access to TE3-FALC address 0008_H which holds the unique value 0000 3802_H.

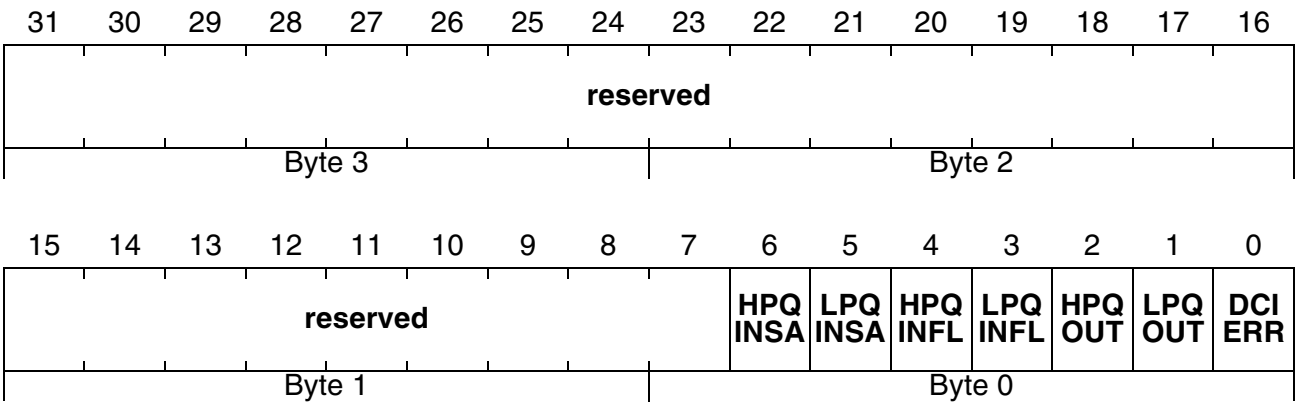
Interrupt Registers

The DCI can assert the external interrupt pin $\overline{\text{MPINT}}$ to notify the host processor that messages in outgoing queues are ready to be read. The interrupt pin $\overline{\text{MPINT}}$ can be programmed to be open drain or push/pull active high or active low.

32-bit wide interrupt status (INTREG) and interrupt mask (INTMSK) registers are provided. Since TE3-FALC only allows 16- or 8-bit accesses, a shadow register is implemented. One byte of the INTREG register bytes is the indicator byte (destructive read). This byte must be accessed first (see **Table 37**). At that moment the interrupt status register is copied to the shadow register and then cleared. All other read accesses to the interrupt status register not accessing the indicator byte are served by the shadow register.

In case bit INTREG:DCIERR was read as ’1’, the DCIERR register must be read too, in order to clear its status bits.

INTREG
Interrupt Status Register **rd only** **Reset value: 0000 0000$_H$**
Address: 0010$_H$



INTREG Register Bits:

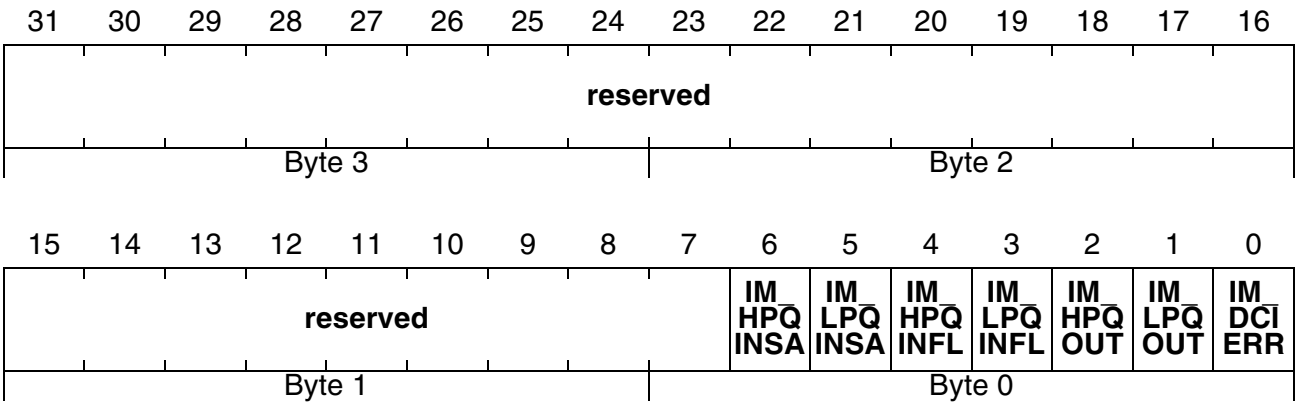
DCIERR **DCI Error**
This bit indicates that a Queue-Overflow happened for at least one queue. The error details must be read from register DCIERR.

LPQOUT **Egress Low/High Priority Queue Interrupt**
HPQOUT This bit indicates that at least one new message is waiting to be read by the host from the corresponding egress queue.

LPQINFL **Ingress Low/High Priority Queue Full Interrupt**
HPQINFL This bit indicates that the corresponding ingress queue is full, i.e. the next write access might lead to an overflow.

LPQINSA **Ingress Low/High Priority Queue Space Available Interrupt**
HPQINSA This bit indicates that the corresponding ingress queue has space available again, i.e. the host can continue writing to this queue.
This interrupt occurs only if the full-condition was reached before (see LPQINFL/HPQINFL) and the amount of queued messages fell back to four.

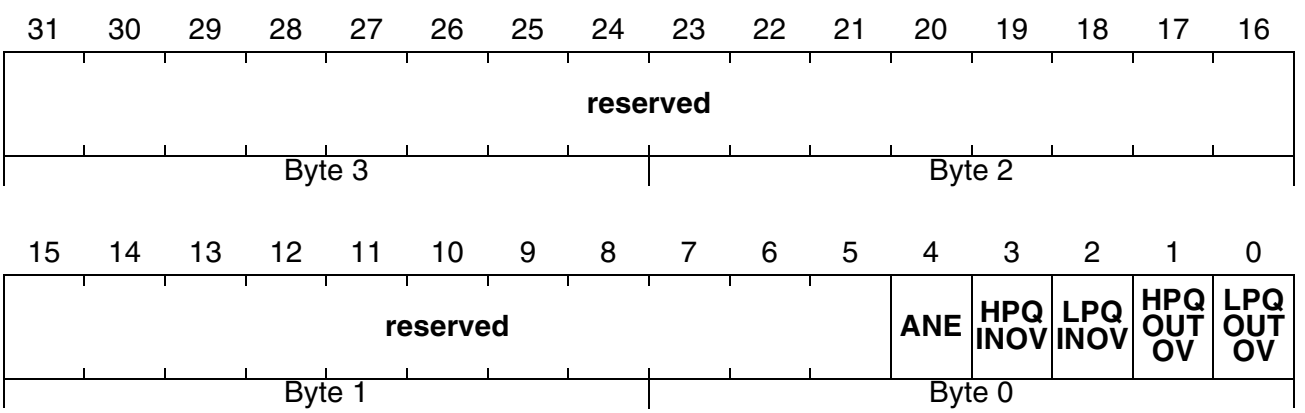
INTMSK
Interrupt Mask Register **rd/wr** **Reset value: FFFF FFFF$_H$**
Address: 0014$_H$



INTMSK Register Bits:

Each bit in this register masks the $\overline{\text{MPINT}}$ interrupt generation for the corresponding interrupt status bit of register INTREG. This does not prevent the interrupt status bit from being set to ’1’ if the corresponding interrupt event occurs.

DCIERR
DCI Error Indicator Register **rd only** **Reset value: 0000 0000$_H$**
Address: 0134$_H$



Note: In case of an INTREG:DCIERR interrupt, this register must be read to clear the interrupt!

DCIERR Register Bits:

LPQOUTOV
HPQOUTOV **Egress Low/High Priority Queue Overflow Error**
This bit indicates that the corresponding egress queue experienced an overflow error and at least one message got lost. The host processor should read the corresponding egress queue at a higher rate, or the amount of egress messages should be reduced.

LPQINOV
HPQINOV **Ingress Low/High Priority Queue Overflow Error**
This bit indicates that the corresponding ingress queue experienced an overflow error and at least one mesaage got lost. The host processor should limit the ingress message flow by evaluating the interrupt status bits INTREG:LPQINFL and INTREG:HPQINFL.

ANE **Access to Non-Existent Address**
This bit indicates that the host attempted to access an address which is out of the allowed range (see **Table 36** for valid addresses).

6.2 Introduction to Message Catalog

This document describes the TE3-FALC Message Catalog used at the USER message interface via the Dual Port SRAM or via ✧ in-band ATM cells/PPP packets.

6.2.1 Message Types

There are specific message types for different needs. The structure of the messages (as described in the following chapter) is common to all types, only the message identifier (MSGID) differs.

There are five general message types:

- Command (CMD)
- Progress Indication (PRG)
- Acknowledgement (ACK)
- Notification (NFC)
- Alarm (ALM)

The dependency between different message types is shown below. Grey arrows mark optional messages.

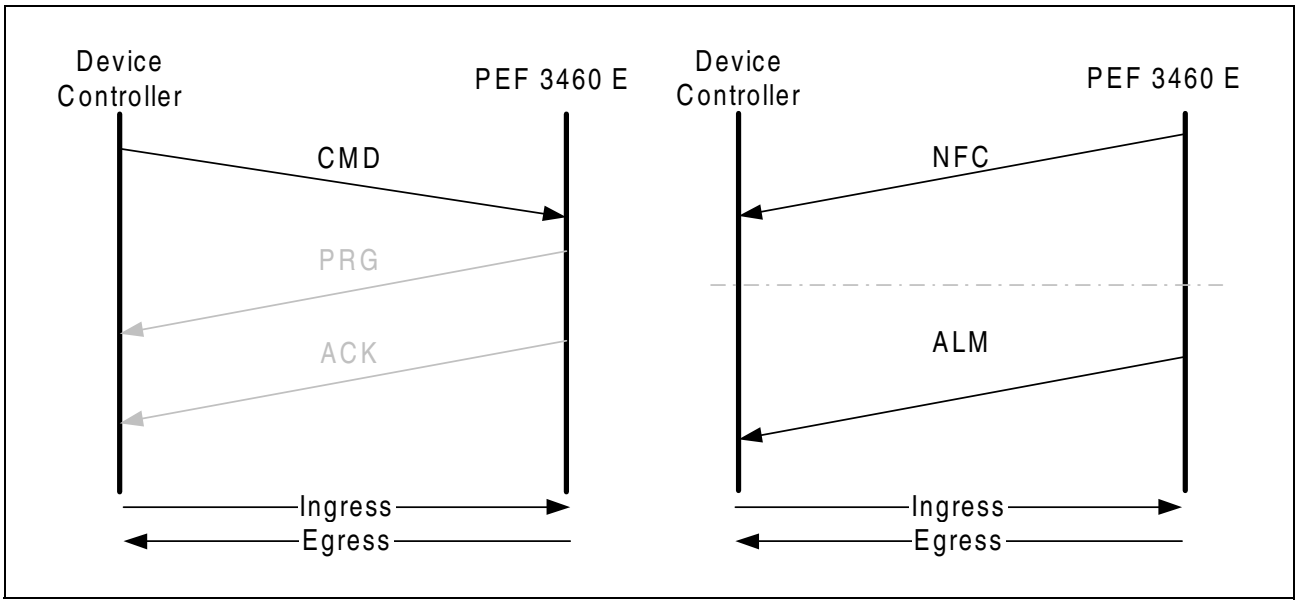


Figure 28 Dependency between different message types

Command Messages

Command Messages are used for configuring or controlling the TE3-FALC. The direction of command messages is always towards the device (ingress).

Commands can either be sent in format MAT 1-1 or MAT 2-1 (refer to **Chapter 6.2.2.1**).

Progress-Indication Message

The Progress-Indication message is a reaction of the device to a received Command message. A Progress-Indication message indicates the processing of the respective Command message. It is sent after the device has read the entire parameter array so that the parameter array can be used again. A Transaction Correlation ID (TCID) is used to get the match between the sent Command message and the received Progress-Indication message. The Transaction Correlation ID is returned unmodified from the TE3-FALC.

Progress-Indication messages could either be sent of format MAT 1-2 or MAT 2-2.

Acknowledge Message

The Acknowledgement message is returned by the device after processing of the Command message completed. The Acknowledgement message also contains a Transaction Correlation ID and a Message ID to recover the relation to the corresponding Command message.

Acknowledgement messages could either be sent of format MAT 1-2 or MAT 2-2.

Notification Message

Notification messages are sent from the TE3-FALC to the external controller if a special internal event occurs. Every Notification message has to be enabled by the user software before.

Within a notification message the transaction correlation identifier TCID is always zero. Determination is only done with the message identifier MSGID.

Notification messages could either be sent of format MAT 1-1 or MAT 2-1. In both cases the P-Flag and A-Flag are not used and should be ignored by the receiver of this message.

Alarm Message

Alarm messages are sent from the TE3-FALC to the external controller if a user definable alarm occurs. Every Alarm-Message has to be enabled before.

Within an alarm message the transaction correlation identifier TCID is always set to zero.

Alarm messages could either be sent of format MAT 1-1 or MAT 2-1. In both cases the P-Flag and A-Flag are not used and should be ignored by the receiver of this message.

6.2.2 General Message Structures

A message consists of a 32-bit message actuator (MAT) and an optional parameter array. Message actuators of type MAT 1-1 and MAT 1-2 do carry a pointer MSGPT to an associated parameter array, message actuators of type MAT 2-1 and MAT 2-2 do not.

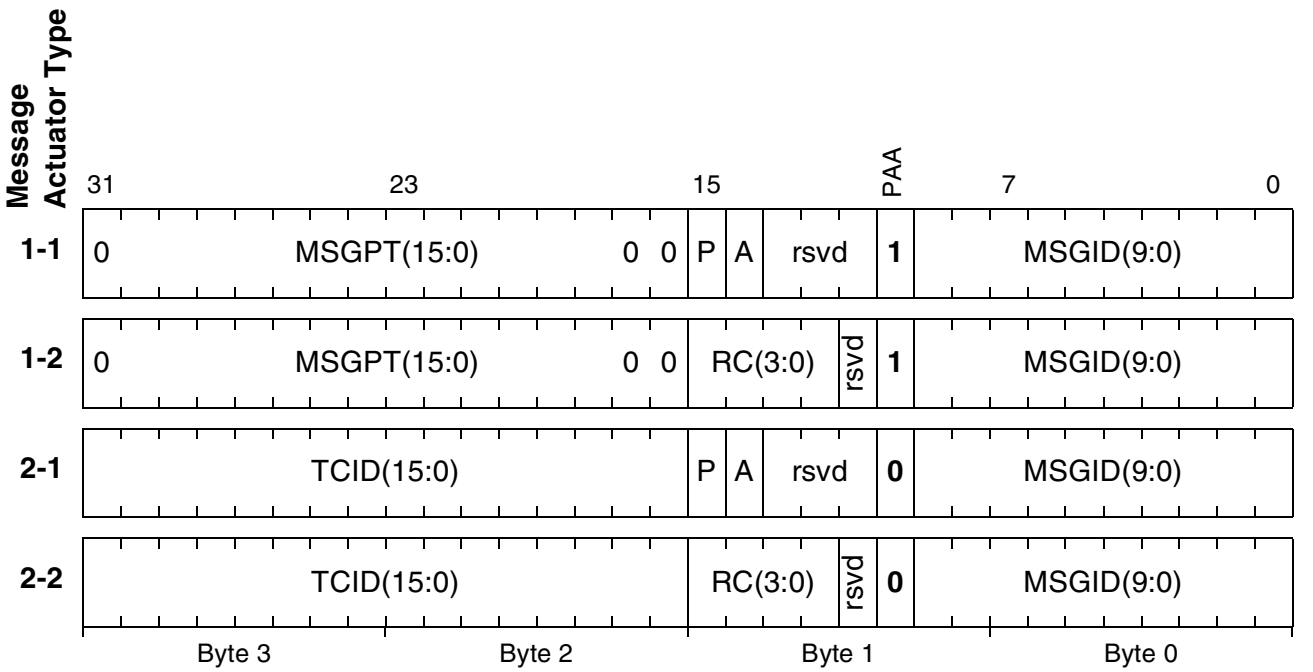
First the parameter array has to be set up in the related memory buffer before the message actuator is written into the message queue.

6.2.2.1 Message Actuators

An MAT 1-1 or MAT 2-1 actuator contains a progress-indication flag (P-Flag) and an acknowledgement flag (A-Flag). If the progress-indication flag is set, a progress-indication message is generated by the device after the appropriate parameter array has ben read. If the acknowledgement-flag is set, an acknowledgement message is generated after the received message is finally processed.

The MAT 1-2 or MAT 2-2 actuator contains a return code (RC) and is used for progress-indication and acknowledgement messages. The return code indicates whether the corresponding command message has been processed successfully or not.

To distinguish between the different messages, the actuator contains a 10-bit message identifier field MSGID.



Message Actuator Fields

MSGID (9:0) Message Identifier
This unique value is to distinguish between the different messages used within the system.

PAA Parameter Array Attached
This is to distinguish between messages with and without attached parameter array. It defines how the bits (31:16) of the message actuator are to be interpreted.

- 0 No parameter array attached. Bits (31:16) are interpreted as Transaction Correlation ID TCID(15:0).
- 1 Parameter array attached. Bits (31:16) are interpreted as pointer MSGPT(15:0) to this parameter array.

A-Flag Acknowledgement Flag
This flag is only valid within command messages. It decides whether an acknowledgement shall be generated when the command has been processed.

- 0 No acknowledgement message is desired for the command message.
- 1 Send acknowledgement message after the processing of this command message is finished.

Message Actuator Fields (cont'd)

P-Flag Progress-Indication Flag
This flag is only valid within command messages. It decides whether a progress-indication message shall be generated when the command including its optional parameter array has been read. This indication can be used to free the memory space acquired by this command (actuator and parameter set).

- 0 No progress-indication message is desired for this command message.
- 1 Send progress-indication message after the command including its optional parameter array has been read.

RC(3:0) Return Code
This field is only valid within acknowledgement messages. It indicates the status of the acknowledged command message.

- 0000_2 positive acknowledgement
- 0001_2 negative acknowledgement
- 0010_2 message denied (MSGID of command not valid)
- 0011_2 parameter mismatch, parameter out of range
- 0100_2 parameter mismatch, configuration invalid
- 0101_2 parameter array mismatch
- 0110_2 resource occupied
- 0111_2 mandatory parameter(s) missing
- others *Reserved.*

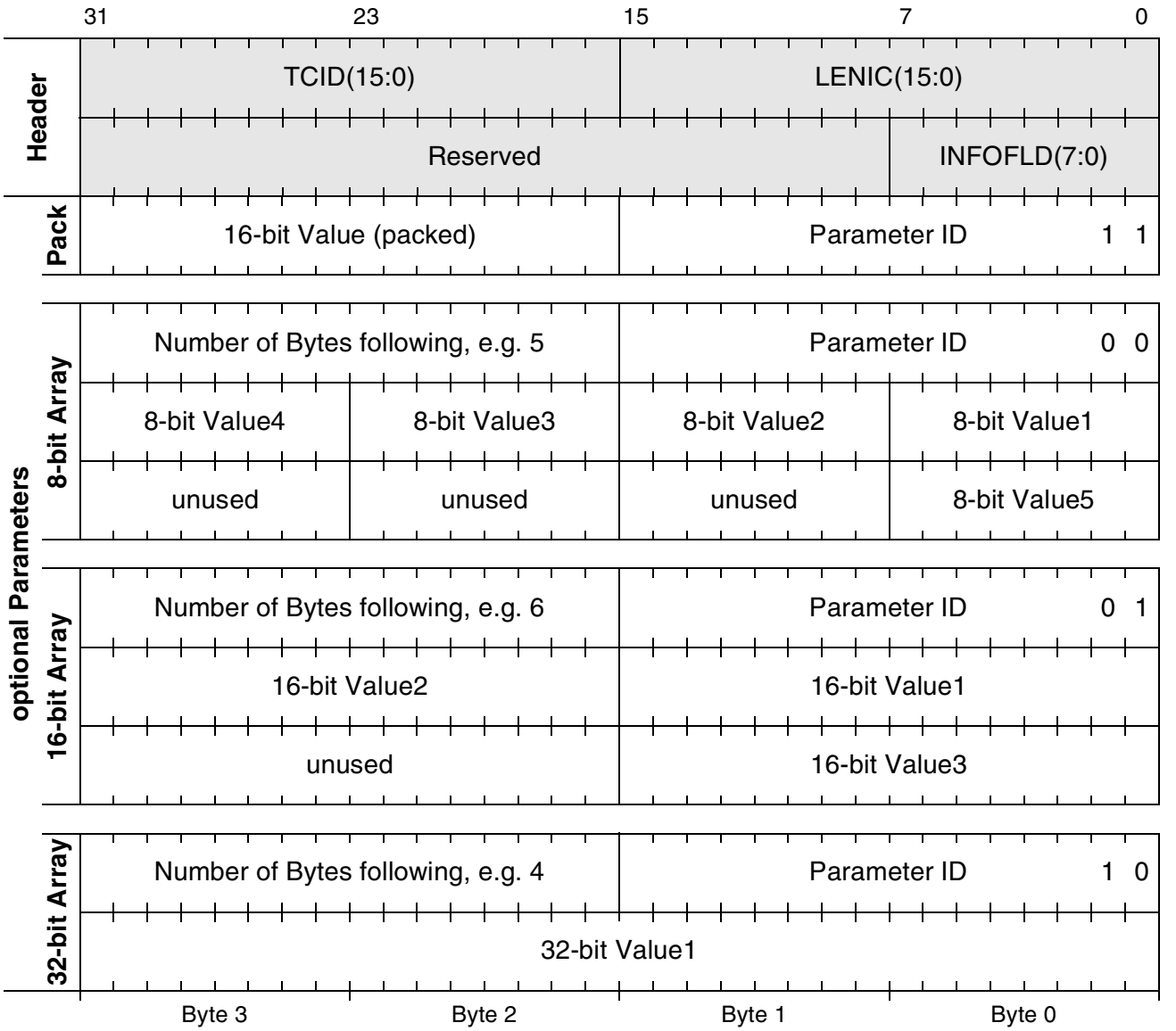
MSGPT (15:0) Message Pointer
16-bit pointer to the appropriate parameter array (located in in-/egress buffer, depends on message direction). This pointer must be 32-bit aligned, thus bits MSGPT(1:0) must be zero.

TCID (15:0) Transaction Correlation Identifier
This user definable value is used to get the match between the sent Command message and the received Progress-Indication or Acknowledgement message. The Transaction Correlation ID is returned unmodified from the TE3-FALC.

6.2.2.2 Optional Parameter Array

The parameter array (see **Table 38**) has variable length. Therefore every parameter array has its own header (shaded fields).

Table 38 Parameter Array Structure



Note: This parameter array format is not suited for DCI boot messages as described in **Chapter 4.2.2.1**.

Parameter Array Fields

LENIC (15:0) Length Indicator
The length indicator (LENIC) represents the size (in number of bytes) of the complete parameter array, including its 8-byte header.

0 No progress-indication message is desired for this command message.

1 Send progress-indication message after the command including its optional parameter array has been read.

TCID (15:0) Transaction Correlation Identifier
This field has the same meaning as the TCID(15:0) field in the message actuator (refer to **Page 89**).

INFOFLD (7:0) Information Field
The INFOFLD is used for memory management.
It marks the parameter array “valid” or “invalid”. If the parameter array has been marked “invalid” the associated memory area can be re-used. The user always has to set the INFOFLD to “valid” when writing a parameter array to the ingress buffer in DCI memory. The device sets the INFOFLD “invalid” after the parameter array has been read from the internal processor and the user can use the memory region that was allocated by this parameter array again.
The same applies to the opposite direction, i.e. for egress messages with associated output parameters the user has to set the INFOFLD to “invalid” as soon as the parameters have been read.

Parameter Array Fields (cont'd)

Param. ID (15:0) Parameter ID
Parameters consist of a 16-bit Parameter ID and one or more associated Values. The list of optional parameters is processed as long as the defined length (LENIC) of the parameter array is reached. The lower two bits of the parameter ID define the type of this parameter:

...11_2 Packed Parameter
A single 32-bit unit is consumed by this parameter type. The lower 16 bits contain the parameter ID, thus a field of 16-bit width remains which is used for the parameter value.

...00_2 Parameter Array of 8-bit Values
The 16-bit field following the parameter ID contains the count of 8-bit values (bytes) attached to this parameter.

...01_2 Parameter Array of 16-bit Values
The 16-bit field following the parameter ID contains the length information of this parameter in number of bytes. If *n* 16-bit values are attached, the byte count is $2 \times n$ bytes.

...10_2 Parameter Array of 32-bit Values
The 16-bit field following the parameter ID contains the length information of this parameter in number of bytes. If *n* 32-bit values are attached, the byte count is $4 \times n$ bytes.

If an optional parameter is not supplied, the value of this parameter stays unchanged. In case a parameter was never set by user software, a reset value is applied which is highlighted (underlined) in the message descriptions.

6.3 Message Catalog

The below example of a command and corresponding acknowledge message show the structure of message descriptions used in the following chapters.

Command ID: CMD_EXAMPLE_MSGID

A brief description of the message is posted here.

Input Parameters (optional)

Parameter ID	Value	Description
$PARAMETER\_ID_P$	_VALUE1 _VALUE2	Value 1 of the optional parameter. Value 2 of the optional parameter (the underline marks it as default value).

Acknowledgement ID: ACK_EXAMPLE_MSGID

This acknowledgement is sent out when the command **CMD_EXAMPLE_MSGID** has been processed.

Output Parameters

Parameter ID	Value	Description
$PARAMETER\_ID_{32}$	*32-bit field*	This is a 32-bit Value

All parameters consist of a 16-bit Parameter ID in capital letters (example: "PARAMETER_ID") and a 16-bit Value (example: "PARAMETER_ID_VALUE1" or "PARAMETER_ID_VALUE2"). The default value for each optional input parameter is underlined.

The type of each parameter is indicated with the appended index: ’P’ (packed), ’8’ (8-bit array), ’16’ (16-bit array) or ’32’ (32-bit array). Refer to **Chapter 6.2.2.2** for details.

When developing software for the TE3-FALC it is recommended to use the predefined value names (in capital letters), e.g. in a C-header file.

6.3.1 Device Maintenance Messages

Notification ID: NFC_FW_ACCESSIBLE

This notification is sent to the host after receipt firmware boot and initialization was completed successfully. The attached output parameters identify the hardware and firmware version ID of the device (see **CMD_GET_VERSION_ID** (page 97) for encoding).
This notification is enabled by default and can not be disabled.

Output Parameters

Parameter ID	Value	Description
$HW\_VERSION\_ID_{32}$	32-bit value	Hardware version ID
$FW\_VERSION\_ID_{32}$	32-bit value	Firmware version ID

Command ID: CMD_SPECIFY_CLOCKS

This message causes the firmware to set the internal clocks of the device. The frequency of an input clock is used to calculate the Clock Multiplication Factor for raising input clock to high frequency master clock, and the Clock Division Factor for generating the desired clock (e.g., Line Speed clock) from high frequency master clock.
The parameter for CLKIN frequency is mandatory.
This message should be the first message sent to TE3-FALC.

Note: Wrong PLL frequency programming might lead to internal overclocking and can thus influence the reliablitiy of the device's operation!

Input Parameters (optional)

Parameter ID	Value	Description
$CLK\_FRQ\_CLKIN_{32}$	*32-bit field*	Value providing the CLKIN input frequency in Hz (4,000,000 to 52,000,000 Hz).
$CLK\_SRC\_TCLKIN_{P}$	_DIRECT	TCLKIN is used directly as transmit clock.
	_VIA_PLL	The transmit PLL can derive the target transmit clock frequency from the clock provided on pin TCLKIN. In this case the TCLKIN frequency must be specified with parameter CLK_FRQ_TCLKIN.
	If the transmit master clock shall be derived from CLKIN, the clock input TCLKIN is not used and this parameter is not relevant.	

Command ID: **CMD_SPECIFY_CLOCKS** (cont'd)

$CLK\_FRQ\_TCLKIN_{32}$	*32-bit field*	Optional value providing the TCLKIN input frequency in Hz (8,000 to 52,000,000 Hz).
$CLK\_FRQ\_RSYNC_{32}$	*32-bit field*	Optional value providing the RSYNC input frequency in Hz (8,000 to 52,000,000 Hz).
$CLK\_FRQ\_CLKOUT_{32}$	*32-bit field*	Optional value providing the CLKOUT output frequency in Hz. Default value zero means this clock output is disabled.
$CLK\_SRC\_RCLKOUT_P$	_DIRECT	The recovered receive clock is directly output on pin RCLKOUT.
	_VIA_PLL	The receive PLL can derive the frequency programmed with CLK_FRQ_RCLKOUT from the recovered receive clock and provide it on pin RCLKOUT.
$CLK\_FRQ\_RCLKOUT_{32}$	*32-bit field*	Optional value providing the RCLKOUT output frequency in Hz. Default value zero means this clock output is disabled.

Notification ID: **NFC_PLL_LOCKED**

After power up the internal PLLs are in the unlocked state. If all clocking setting are applied, the internal PLLs shall reach the locked state. This is reported by this message.
To enable this notification use message **CMD_SET_NFC_ALM_MODE** (page 96).

Output Parameters

Parameter ID	Value	Description
$INTERNAL\_PLL_P$	_RX	RX PLL entered Locked state
	_TX	TX PLL entered Locked state

Notification ID: **NFC_PLL_UNLOCKED**

If an internal PLL switched from the locked state into the unlocked state this message will be generated.
To enable this notification use message **CMD_SET_NFC_ALM_MODE** (page 96).

Notification ID: **NFC_PLL_UNLOCKED** (cont'd)

Output Parameters

Parameter ID	Value	Description
$INTERNAL\_PLL_P$	_RX	RX PLL entered Unlocked state
	_TX	TX PLL entered Unlocked state

Command ID: **CMD_SET_INTERRUPT_MODE**

With this command the output characteristics of the interrupt output pin $\overline{\text{MPINT}}$ can be programmed. Interrupt sources are determined by reading register **INTREG** (page 83). Interrupt events can be masked via register **INTMSK** (page 84).

Input Parameters (optional)

Parameter ID	Value	Description
$INT\_PORT\_CFG_P$	_DISABLE	Interrupt output is disabled (tri-state).
	_OPEN_DRAIN	Interrupt output is open-drain.
	_ACT_HIGH	Interrupt output is push/pull, active high.
	_ACT_LOW	Interrupt output is push/pull, active low.

Command ID: **CMD_SET_NFC_ALM_MODE**

This command assigns the selected notification or alarm message to one of the outgoing message queues (LPQOUT, HPQOUT) at the user interface. Assigning NOQOUT inhibits sending out a message to the user interface.

Input Parameters (optional)

Parameter ID	Value	Description
$MSG\_TO\_HPQOUT_P$	*16-bit field*	10-bit message identifier MSGID(9:0) of the Alarm or Notification that shall be assigned to high priority egress queue.
$MSG\_TO\_LPQOUT_P$	*16-bit field*	10-bit message identifier MSGID(9:0) of the Alarm or Notification that shall be assigned to low priority egress queue.
$MSG\_TO\_NOQOUT_P$	*16-bit field*	10-bit message identifier MSGID(9:0) of the Alarm or Notification that shall not be assigned to any egress queue, i.e. Alarm/ Notification generation is suppressed.

Note: The above input parameters can be issued multiple times. That way it is possible to e.g. enable a group of alarm messages by issuing this message CMD_SET_NFC_ALM_MODE only once.

Command ID: CMD_SET_LOOP

This message causes the firmware to activate or deactivate a specific data path loop. For details on provided loop options refer to **Chapter 4.2.4**.

Input Parameters (optional)

Parameter ID	Value	Description
$LOOP\_LOCAL_P$	_LIU	Local Line Loop (LIU)
	_FRAMER	Local Framer Loop
	_SYSIF	Local System Interface Loop
	_OFF	No Local Loop
$LOOP\_REMOTE_P$	_LIU	Remote Line Loop (LIU)
	_FRAMER	✧Remote Payload Loop (Framer)[1)]
	_OFF	No Remote Loop

1) This is an option which is not available with the current firmware release.

Command ID: CMD_GET_VERSION_ID

This message initiates the firmware to send the device hardware version ID and firmware version ID.

The hardware version ID is decoded from the 32-bit hexadecimal HW_VERSION_ID as follows:

<as_digit[19:16]> . <as_digit[15:12]> – <as_alpha[11:8]><as_digit[7:4]><as_digit[3:0]>

E.g., HW_VERSION_ID = $00011A11_H$ reads as "V1.1-A11" and means Hardware Version 1.1, Build A11.

The firmware version ID is maintained by the firmware in a constant data type and is decoded from the 32-bit hexadecimal FW_VERSION_ID as follows:

Firmware Build: *<as_digit[23:20]>.<as_digit[19:16]>*
Feature Set: *<as_digit[15:13]>.<as_digit[12:6]>*
Development Step: *<as_digit[5:0]>*

E.g., FW_VERSION_ID = 00212041_H means Firmware Build 2.1, Feature Set 1.1, Development Step 1.

Command ID: **CMD_GET_VERSION_ID** (cont'd)

Input Parameters	*none*

Acknowledgement ID: **ACK_GET_VERSION_ID**

This acknowledgement is sent to the host after receipt of the **CMD_GET_VERSION_ID** message to identify the hardware and firmware version of the device.

Output Parameters

Parameter ID	Value	Description
$HW\_VERSION\_ID_{32}$	32-bit value	Hardware version ID
$FW\_VERSION\_ID_{32}$	32-bit value	Firmware version ID

Command ID: **CMD_SELF_DIAGNOSTICS**

This commands triggers the execution of the device-selftest. The result of the device selftest is returned to the user via the standard acknowledge message.
Because the execution of this command is service disruptive a subsequent device reset with initialization is mandatory.

Input Parameters	*none*

Acknowledgement ID: **ACK_SELF_DIAGNOSTICS**

This message is sent to the user to provide the results of the self-diagnostics run after requested so by the host via **CMD_SELF_DIAGNOSTICS** message.

Output Parameters

Parameter ID	Value	Description
$TEST\_RESULT_P$	_OK	The self-test has been executed successfully.
	_FAIL	One or more tests failed.
$ERROR\_CODE_P$	*16-bit field*	Manufacturer specific error code.

Command ID: **CMD_RESET_DEVICE**

This message causes the firmware to perform a reset of the TE3-FALC. All hardware modules are reset. All interrupts except for DCI interrupts are disabled.
For details on the boot process refer to **Chapter 4.2.2**.

Input Parameters (optional)

Parameter ID	Value	Description
$REBOOT\_SOURCE_P$	_CURR_IMAGE _PRESET	Reboot from current image. Load new image according to preset Hardware Boot Selection and reboot.

6.3.2 Data Flow Configuration Message

The configuration process should be hierarchical. A *Data Flow Configuration Function* selects a specific data flow between the system side and the line side of the TE3-FALC device. According to the selected data flow all involved modules are configured by module specific configuration functions. A number of default settings are applied which can individually be changed by **Module Configuration Messages** (page 113).

After configuration is completed, the interfaces can be enabled with the **CMD_ENABLE_INTERFACES** (page 112) command.

All applicable types of data flow are listed in **Table 39**. The left column (Type of Data Flow) identifies the selected type of data flow, whereas the other columns identify the module specific operating modes.

Table 39 Supported Operational Modes

Type of Data Flow (Command Message)	LIU	Framer [1]	FDL/ TTI	PLCP	G.804	PPP	System side Interface [2]
ATM - G.832 - E3 (CMD_SET_ATM_E3G832_E3)	E3	E3 G.832	TTI	n.a.	G.804	n.a.	UTOPIA/ POS-PHY/ UTOPIA-X
ATM DS3 T3 (CMD_SET_ATM_DS3_T3)	T3	DS3	FEAC MDL	n.a.	G.804	n.a.	UTOPIA/ POS-PHY/ UTOPIA-X
ATM - PLCP - DS3 - T3 (CMD_SET_ATM_PLCP_DS3_T3)	T3	DS3	FEAC MDL	PLCP	G.804	n.a.	UTOPIA/ POS-PHY/ UTOPIA-X
PPP - G.832 - E3 (CMD_SET_PPP_E3G832_E3)	E3	E3 G.832	TTI	n.a.	n.a.	PPP	POS-PHY/ UTOPIA-X
PPP - DS3 - T3 (CMD_SET_PPP_DS3_T3)	T3	DS3	FEAC MDL	n.a.	n.a.	PPP	POS-PHY/ UTOPIA-X
ATM - E3 (CMD_SET_ATM_E3)	E3	bypass	n.a.	n.a.	G.804	n.a.	UTOPIA/ POS-PHY/ UTOPIA-X
ATM - T3 (CMD_SET_ATM_T3)	T3	bypass	n.a.	n.a.	G.804	n.a.	UTOPIA/ POS-PHY/ UTOPIA-X
PPP - E3 (CMD_SET_PPP_E3)	E3	bypass	n.a.	n.a.	n.a.	PPP	POS-PHY/ UTOPIA-X
PPP - T3 (CMD_SET_PPP_T3)	T3	bypass	n.a.	n.a.	n.a.	PPP	POS-PHY/ UTOPIA-X

Table 39 Supported Operational Modes (cont'd)

Type of Data Flow (Command Message)	LIU	Framer [1]	FDL/ TTI	PLCP	G.804	PPP	System side Interface [2]
ATM - G.832 (CMD_SET_ATM_E3G832)	bypass	E3 G.832	TTI	n.a.	G.804	n.a.	UTOPIA/ POS-PHY/ UTOPIA-X
ATM - DS3 (CMD_SET_ATM_DS3)	bypass	DS3	FEAC MDL	n.a.	G.804	n.a.	UTOPIA/ POS-PHY/ UTOPIA-X
ATM - PLCP - DS3 (CMD_SET_ATM_PLCP_DS3)	bypass	DS3	FEAC MDL	PLCP	G.804	n.a.	UTOPIA/ POS-PHY/ UTOPIA-X
PPP - G.832 (CMD_SET_PPP_E3G832)	bypass	E3 G.832	TTI	n.a.	n.a.	PPP	POS-PHY/ UTOPIA-X
PPP - DS3 (CMD_SET_PPP_DS3)	bypass	DS3	FEAC MDL	n.a.	n.a.	PPP	POS-PHY/ UTOPIA-X
✧ ATM Transparent (CMD_SET_ATM_TRANS)	bypass	bypass	n.a.	n.a.	G.804	n.a.	UTOPIA/ POS-PHY/ UTOPIA-X
✧ PPP Transparent (CMD_SET_PPP_TRANS)	bypass	bypass	n.a.	n.a.	n.a.	PPP	POS-PHY/ UTOPIA-X
✧ Bitstream G.832 E3 (CMD_SET_BIT_E3G832_E3)	E3	E3 G.832	TTI	not used			Bitstream Access
✧ Bitstream - DS3 - T3 (CMD_SET_BIT_DS3_T3)	T3	DS3	FEAC MDL	not used			Bitstream Access
✧ Bitstream - E3 (CMD_SET_BIT_E3TRANS_E3)	E3	bypass	n.a.	not used			Bitstream Access
✧ Bitstream - T3 (CMD_SET_BIT_DS3TRANS_T3)	T3	bypass	n.a.	not used			Bitstream Access
✧ Bitstream - G.832 (CMD_SET_BIT_E3G832)	bypass	E3 G.832	TTI	not used			Bitstream Access
✧ Bitstream - DS3 (CMD_SET_BIT_DS3)	bypass	DS3	FEAC MDL	not used			Bitstream Access
✧ Bitstream Transparent (CMD_SET_BIT_TRANS)	bypass	bypass	n.a.	not used			Bitstream Access

[1] For DS3 modes, the framer evaluates the AIC bit to dynamically select C-bit parity or M23 unchannelized mode

[2] One of the alternative system side interface configurations can be selected at configuration time

Command ID: **CMD_SET_ATM_E3G832_E3**
Command ID: **CMD_SET_ATM_E3G832**

Message CMD_SET_ATM_E3G832_E3 sets up the path
System Interface <=> G.804 <=> E3:G.832 <=> E3 LIU.
Message CMD_SET_ATM_E3G832 sets the same data path with digital line interface:
System Interface <=> G.804 <=> E3:G.832.

Input Parameters (optional)

Parameter ID	Value	Description
$LINE\_TIMING_P$	_MASTER_INT	E3 Line internal Master timing (CLKIN)
	_MASTER_EXT	E3 Line external Master timing (TCLKIN)
	_LOOP	E3 Line Loop timing
$SYSIF\_MODE_P$	_UTOPIA_L1	UTOPIA Level 1 mode
	_UTOPIA_L2	UTOPIA Level 2 mode
	_POSPHY_L2	POS-PHY Level 2 mode
	_UTOPIA_L2X	UTOPIA Level 2 eXtended mode
$SYSIF\_WIDTH_P$	_8BIT	8 bit data bus width
	_16BIT	16 bit data bus width
$SYSIF\_ADDR_P$	*16-bit field*	PHY address (0 to 30). Default is 0.
$SYSIF\_STATUS_P$	_POLLING	MPHY Polling
	_DIRECT_IND	Direct Status Indication

Default Settings *(These settings can be modified by Module Configuration Messages)*

E3 Framer	• SSM pattern is disabled (set to 0000_2). • Payload Type field set to 'ATM'
ATM Processor	• Payload Scrambling enabled • Header Correction enabled • ALPHA = 7, DELTA = 6
Serial Data Access	• E3 Bitstream Breakout interface disabled • E3 Overhead Access interface disabled
Data Buffers	• Burst-/Chunksize set to 64 bytes (only for POS-PHY / UTOPIA-L2X) • Forward Threshold set to 64 bytes (only for POS-PHY / UTOPIA-L2X)
System Interface	• Cell-Level handshake (UTOPIA only) / Packet-Level handshake (POS-PHY only) • Tri-statable bus, allows configuration with multiple PHYs • Parity check enabled

Command ID: **CMD_SET_ATM_DS3_T3**
Command ID: **CMD_SET_ATM_DS3**

Message CMD_SET_ATM_DS3_T3 sets up the data path
System Interface <=> G.804 <=> DS3 <=> T3 LIU.
Message CMD_SET_ATM_DS3 sets the same data path with digital line interface:
System Interface <=> G.804 <=> DS3.

Input Parameters (optional)

Parameter ID	Value	Description
$LINE\_TIMING_P$	_MASTER_INT	T3 Line internal Master timing (CLKIN)
	_MASTER_EXT	T3 Line external Master timing (TCLKIN)
	_LOOP	T3 Line Loop timing
$SYSIF\_MODE_P$	_UTOPIA_L1	UTOPIA Level 1 mode
	_UTOPIA_L2	UTOPIA Level 2 mode
	_POSPHY_L2	POS-PHY Level 2 mode
	_UTOPIA_L2X	UTOPIA Level 2 eXtended mode
$SYSIF\_WIDTH_P$	_8BIT	8 bit data bus width
	_16BIT	16 bit data bus width
$SYSIF\_ADDR_P$	*16-bit field*	PHY address (0 to 30). Default is 0.
$SYSIF\_STATUS_P$	_POLLING	MPHY Polling
	_DIRECT_IND	Direct Status Indication

Default Settings *(These settings can be modified by Module Configuration Messages)*

DS3 Framer	• Auto sensing of application via AIC channel (C-Bit Parity / M23 unchannelized mode) • AIS signal defined as 101010_2... sequence.
ATM Processor	• Payload Scrambling enabled • Header Correction enabled • Direct Mapping (ALPHA = 7, DELTA = 6)
Serial Data Access	• DS3 Bitstream Breakout interface disabled • DS3 Overhead Access interface disabled
Data Buffers	• Burst-/Chunksize set to 64 bytes (only for POS-PHY / UTOPIA-L2X) • Forward Threshold set to 64 bytes (only for POS-PHY / UTOPIA-L2X)
System Interface	• Cell-Level handshake (UTOPIA only) / Packet-Level handshake (POS-PHY only) • Tri-statable bus, allows configuration with multiple PHYs • Parity check enabled

Command ID: **CMD_SET_ATM_PLCP_DS3_T3**
Command ID: **CMD_SET_ATM_PLCP_DS3**

Message CMD_SET_ATM_PLCP_DS3_T3 sets up the data path
System Interface <=> G.804 <=> PLCP <=> DS3 <=> T3 LIU.
Message CMD_SET_ATM_PLCP_DS3 sets the same data path with digital line i/f:
System Interface <=> G.804 <=> PLCP <=> DS3.

Input Parameters (optional)

Parameter ID	Value	Description
$LINE\_TIMING_P$	_MASTER_INT	T3 Line internal Master timing (CLKIN)
	_MASTER_EXT	T3 Line external Master timing (TCLKIN)
	_LOOP	T3 Line Loop timing
$SYSIF\_MODE_P$	_UTOPIA_L1	UTOPIA Level 1 mode
	_UTOPIA_L2	UTOPIA Level 2 mode
	_POSPHY_L2	POS-PHY Level 2 mode
	_UTOPIA_L2X	UTOPIA Level 2 eXtended mode
$SYSIF\_WIDTH_P$	_8BIT	8 bit data bus width
	_16BIT	16 bit data bus width
$SYSIF\_ADDR_P$	*16-bit field*	PHY address (0 to 30). Default is 0.
$SYSIF\_STATUS_P$	_POLLING	MPHY Polling
	_DIRECT_IND	Direct Status Indication

Default Settings *(These settings can be modified by Module Configuration Messages)*

DS3 Framer	• Auto sensing of application via AIC channel (C-Bit Parity / M23 unchannelized mode) • AIS signal defined as 101010_2... sequence.
ATM Processor	• PLCP mapping • Payload Scrambling enabled • Header Correction enabled
Serial Data Access	• DS3 Bitstream Breakout interface disabled • DS3 Overhead Access interface disabled
Data Buffers	• Burst-/Chunksize set to 64 bytes (only for POS-PHY / UTOPIA-L2X) • Forward Threshold set to 64 bytes (only for POS-PHY / UTOPIA-L2X)
System Interface	• Cell-Level handshake (UTOPIA only) / Packet-Level handshake (POS-PHY only) • Tri-statable bus, allows configuration with multiple PHYs • Parity check enabled

Command ID: **CMD_SET_PPP_E3G832_E3**
Command ID: **CMD_SET_PPP_E3G832**

Message CMD_SET_PPP_E3G832_E3 sets up the data path
System Interface <=> PPP <=> E3:G.832 <=> E3 LIU.
Message CMD_SET_PPP_E3G832 sets the same data path with digital line interface:
System Interface <=> PPP <=> E3:G.832.

Input Parameters (optional)

Parameter ID	Value	Description
$LINE\_TIMING_P$	_MASTER_INT	E3 Line internal Master timing (CLKIN)
	_MASTER_EXT	E3 Line external Master timing (TCLKIN)
	_LOOP	E3 Line Loop timing
$SYSIF\_MODE_P$	_POSPHY_L2	POS-PHY Level 2 mode
	_UTOPIA_L2X	UTOPIA Level 2 eXtended mode
$SYSIF\_WIDTH_P$	_8BIT	8 bit data bus width
	_16BIT	16 bit data bus width
$SYSIF\_ADDR_P$	*16-bit field*	PHY address (0 to 30). Default is 0.
$SYSIF\_STATUS_P$	_POLLING	MPHY Polling
	_DIRECT_IND	Direct Status Indication

Default Settings *(These settings can be modified by Module Configuration Messages)*

E3 Framer	• SSM pattern is disabled (set to 0000_2). • Payload Type field set to 'non-specific'
PPP Processor	• Bit-synchronous PPP mode • 16-bit CRC • Shared Flag between two frames • Address/Control-Field Compression disabled
Serial Data Access	• E3 Bitstream Breakout interface disabled • E3 Overhead Access interface disabled
Data Buffers	• Burst-/Chunksize set to 64 bytes • Forward Threshold set to 64 bytes
System Interface	• Packet-Level handshake (POS-PHY only) • Tri-statable bus, allows configuration with multiple PHYs

Command ID: **CMD_SET_PPP_DS3_T3**
Command ID: **CMD_SET_PPP_DS3**

Message CMD_SET_PPP_DS3_T3 sets up the data path
System Interface <=> PPP <=> DS3 <=> T3 LIU.
Message CMD_SET_PPP_DS3 sets the same data path with digital line interface:
System Interface <=> PPP <=> DS3.

Input Parameters (optional)

Parameter ID	Value	Description
$LINE\_TIMING_P$	_MASTER_INT	T3 Line internal Master timing (CLKIN)
	_MASTER_EXT	T3 Line external Master timing (TCLKIN)
	_LOOP	T3 Line Loop timing
$SYSIF\_MODE_P$	_POSPHY_L2	POS-PHY Level 2 mode
	_UTOPIA_L2X	UTOPIA Level 2 eXtended mode
$SYSIF\_WIDTH_P$	_8BIT	8 bit data bus width
	_16BIT	16 bit data bus width
$SYSIF\_ADDR_P$	*16-bit field*	PHY address (0 to 30). Default is 0.
$SYSIF\_STATUS_P$	_POLLING	MPHY Polling
	_DIRECT_IND	Direct Status Indication

Default Settings *(These settings can be modified by Module Configuration Messages)*

DS3 Framer	• Auto sensing of application via AIC channel (C-Bit Parity / M23 unchannelized mode) • AIS signal defined as 101010_2... sequence.
PPP Processor	• 16-bit CRC • Shared Flag between two frames • Address/Control-Field Compression disabled
Serial Data Access	• DS3 Bitstream Breakout interface disabled • DS3 Overhead Access interface disabled
Data Buffers	• Burst-/Chunksize set to 64 bytes • Forward Threshold set to 64 bytes
System Interface	• Packet-Level handshake (POS-PHY only) • Tri-statable bus, allows configuration with multiple PHYs

Command ID: **CMD_SET_ATM_E3**

This message sets up the path
System Interface <=> G.804 <=> E3 LIU ,
with the E3 G.832 framer being bypassed.

Input Parameters (optional)

Parameter ID	Value	Description
$LINE\_TIMING_P$	_MASTER_INT	E3 Line internal Master timing (CLKIN)
	_MASTER_EXT	E3 Line external Master timing (TCLKIN)
	_LOOP	E3 Line Loop timing
$SYSIF\_MODE_P$	_UTOPIA_L1	UTOPIA Level 1 mode
	_UTOPIA_L2	UTOPIA Level 2 mode
	_POSPHY_L2	POS-PHY Level 2 mode
	_UTOPIA_L2X	UTOPIA Level 2 eXtended mode
$SYSIF\_WIDTH_P$	_8BIT	8 bit data bus width
	_16BIT	16 bit data bus width
$SYSIF\_ADDR_P$	*16-bit field*	Physical address (0 to 30). Default is 0.
$SYSIF\_STATUS_P$	_POLLING	MPHY Polling
	_DIRECT_IND	Direct Status Indication

Default Settings *(These settings can be modified by Module Configuration Messages)*

ATM Processor	• Payload Scrambling enabled • Header Correction enabled • ALPHA = 7, DELTA = 6
Serial Data Access	• E3 Bitstream Breakout interface disabled
Data Buffers	• Burst-/Chunksize set to 64 bytes (only for POS-PHY / UTOPIA-L2X) • Forward Threshold set to 64 bytes (only for POS-PHY / UTOPIA-L2X)
System Interface	• Cell-Level handshake (UTOPIA only) / Packet-Level handshake (POS-PHY only) • Tri-statable bus, allows configuration with multiple PHYs • Parity check enabled

Command ID: **CMD_SET_ATM_T3**

This message sets up the path
System Interface <=> G.804 <=> T3 LIU ,
with the T3 framer being bypassed.

Input Parameters (optional)		
Parameter ID	Value	Description
$LINE\_TIMING_P$	_MASTER_INT	T3 Line internal Master timing (CLKIN)
	_MASTER_EXT	T3 Line external Master timing (TCLKIN)
	_LOOP	T3 Line Loop timing
$SYSIF\_MODE_P$	_UTOPIA_L1	UTOPIA Level 1 mode
	_UTOPIA_L2	UTOPIA Level 2 mode
	_POSPHY_L2	POS-PHY Level 2 mode
	_UTOPIA_L2X	UTOPIA Level 2 eXtended mode
$SYSIF\_WIDTH_P$	_8BIT	8 bit data bus width
	_16BIT	16 bit data bus width
$SYSIF\_ADDR_P$	*16-bit field*	PHY address (0 to 30). Default is 0.
$SYSIF\_STATUS_P$	_POLLING	MPHY Polling
	_DIRECT_IND	Direct Status Indication

Default Settings *(These settings can be modified by Module Configuration Messages)*	
ATM Processor	• Payload Scrambling enabled • Header Correction enabled • Direct Mapping (ALPHA = 7, DELTA = 6)
Serial Data Access	• DS3 Bitstream Breakout interface disabled
Data Buffers	• Burst-/Chunksize set to 64 bytes (only for POS-PHY / UTOPIA-L2X) • Forward Threshold set to 64 bytes (only for POS-PHY / UTOPIA-L2X)
System Interface	• Cell-Level handshake (UTOPIA only) / Packet-Level handshake (POS-PHY only) • Tri-statable bus, allows configuration with multiple PHYs • Parity check enabled

Command ID: **CMD_SET_PPP_E3**

This message sets up the data path
System Interface <=> PPP <=> E3 LIU ,
with the E3 G.832 framer being bypassed.

Input Parameters (optional)

Parameter ID	Value	Description
$LINE\_TIMING_P$	_MASTER_INT	E3 Line internal Master timing (CLKIN)
	_MASTER_EXT	E3 Line external Master timing (TCLKIN)
	_LOOP	E3 Line Loop timing
$SYSIF\_MODE_P$	_POSPHY_L2	POS-PHY Level 2 mode
	_UTOPIA_L2X	UTOPIA Level 2 eXtended mode
$SYSIF\_WIDTH_P$	_8BIT	8 bit data bus width
	_16BIT	16 bit data bus width
$SYSIF\_ADDR_P$	*16-bit field*	PHY address (0 to 30). Default is 0.
$SYSIF\_STATUS_P$	_POLLING	MPHY Polling
	_DIRECT_IND	Direct Status Indication

Default Settings *(These settings can be modified by Module Configuration Messages)*

PPP Processor	• 16-bit CRC • Shared Flag between two frames • Address/Control-Field Compression disabled
Data Buffers	• Burst-/Chunksize set to 64 bytes • Forward Threshold set to 64 bytes
System Interface	• Packet-Level handshake (POS-PHY only) • Tri-statable bus, allows configuration with multiple PHYs

Command ID: **CMD_SET_PPP_T3**

This message sets up the data path
System Interface <=> PPP <=> T3 LIU ,
with the DS3 framer being bypassed.

Input Parameters (optional)

Parameter ID	Value	Description
$LINE\_TIMING_P$	_MASTER_INT	T3 Line internal Master timing (CLKIN)
	_MASTER_EXT	T3 Line external Master timing (TCLKIN)
	_LOOP	T3 Line Loop timing
$SYSIF\_MODE_P$	_POSPHY_L2	POS-PHY Level 2 mode
	_UTOPIA_L2X	UTOPIA Level 2 eXtended mode
$SYSIF\_WIDTH_P$	_8BIT	8 bit data bus width
	_16BIT	16 bit data bus width
$SYSIF\_ADDR_P$	*16-bit field*	PHY address (0 to 30). Default is 0.
$SYSIF\_STATUS_P$	_POLLING	MPHY Polling
	_DIRECT_IND	Direct Status Indication

Default Settings *(These settings can be modified by Module Configuration Messages)*

PPP Processor	• 16-bit CRC • Shared Flag between two frames • Address/Control-Field Compression disabled
Data Buffers	• Burst-/Chunksize set to 64 bytes • Forward Threshold set to 64 bytes
System Interface	• Packet-Level handshake (POS-PHY only) • Tri-statable bus, allows configuration with multiple PHYs

Command ID: **CMD_SET_BIT_E3G832_E3**
Command ID: **CMD_SET_BIT_E3G832**

Message CMD_SET_BIT_E3G832_E3 sets up a serial E3 framer + E3 LIU data path Bitstream Interface <=> E3:G.832 <=> E3 LIU.
Message CMD_SET_BIT_E3G832 sets this data path without E3 LIU (pure E3 framer): Bitstream Interface <=> E3:G.832.

Input Parameters (optional)

Parameter ID	Value	Description
$LINE\_TIMING_P$	_MASTER_INT	E3 Line internal Master timing (CLKIN)
	_MASTER_EXT	E3 Line external Master timing (TCLKIN)
	_LOOP	E3 Line Loop timing

Default Settings *(These settings can be modified by Module Configuration Messages)*

E3 Framer	• SSM pattern is disabled (set to 0000_2). • Payload Type field set to 'non-specific'

Command ID: **CMD_SET_BIT_DS3_T3**
Command ID: **CMD_SET_BIT_DS3**

Message CMD_SET_BIT_DS3_T3 sets up a serial DS3 framer + T3 LIU data path Bitstream Interface <=> DS3 <=> T3 LIU.
Message CMD_SET_BIT_DS3 sets this data path without T3 LIU (pure DS3 framer): Bitstream Interface <=> DS3.

Input Parameters (optional)

Parameter ID	Value	Description
$LINE\_TIMING_P$	_MASTER_INT	T3 Line internal Master timing (CLKIN)
	_MASTER_EXT	T3 Line external Master timing (TCLKIN)
	_LOOP	T3 Line Loop timing

Default Settings *(These settings can be modified by Module Configuration Messages)*

DS3 Framer	• Auto sensing of application via AIC channel (C-Bit Parity / M23 unchannelized mode) • AIS signal defined as 101010_2... sequence.

6.3.3 Interfaces Control Messages

Command ID: **CMD_ENABLE_INTERFACES**

This message controls enabling and disabling of both line interface (digital or analog) and system side interface (UTOPIA, POS-PHY or Bitstream).
Also the bitstream break-out and DS3/E3 framer overhead access interfaces (see **Chapter 5.3**) are controlled by this message.
Prior to this command, the data flow and the interfaces must be configured properly.

Input Parameters (optional)

Parameter ID	Value	Description
IF_SYSTEM_P	_DISABLE	Disable system side interface.
	_ENABLE	Enable system side interface.
IF_LINE_P	_DISABLE	Disable line side interface.
	_ENABLE	Enable line side interface.
$IF\_BREAKOUT_P$	_DISABLE	Disable serial bitstream break-out.
	_ENABLE	Enable serial bitstream break-out between DS3/E3 framer and ATM/HDLC protocol processor.
	This option is not available in data flow configurations with system side interface set to "Bitstream Access".	
$IF\_OVERHEAD_P$	_DISABLE	Disable DS3/E3 framer overhead access interface.
	_ENABLE	Enable DS3/E3 framer overhead access interface.

6.3.4 Module Configuration Messages

Command ID: CMD_CFG_LIU

This message causes the firmware to configure the Line Interface Unit (LIU).

Input Parameters (optional)

Parameter ID	Value	Description
$LIU\_AMPLIFIER_P$	_NORMAL	Normal amplifier setting.
	_MONITOR	Monitor mode: additional 20 dB gain stage at RL1/RL2 activated.
$LIU\_TRANSMIT_P$	_DISABLE	Transmitter disabled.
	_ENABLE	Transmitter enabled.

Command ID: CMD_CFG_DJAT

This message causes the firmware to configure the Digital Jitter Attenuators.

Input Parameters (optional)

Parameter ID	Value	Description
$DJAT\_RECEIVE_P$	_DISABLE	Receive DJAT disabled.
	_ENABLE	Receive DJAT enabled.
$DJAT\_RX\_REF_P$	_RSYNC	Receive DJAT uses clock provided on pin RSYNC.
	_RSYNC_PLL	Receive DJAT uses clock from receive PLL; PLL sourced by RSYNC.
	_RCLK_PLL	Receive DJAT uses clock from receive PLL; PLL sourced by recovered route clock[1)].
$DJAT\_RX\_LOSMODE_P$	_AUTO_REF	TE3-FALC automatically switches to the highest prio clock available to source the receive PLL: (Prio1) recovered route clock → (Prio2) pin RSYNC → (Prio3) derived from CLKIN, center mode.
	_HOLDOVER	In case of loss of receive PLL reference clock, the last PLL clock is held. Intrinsic jitter increases.
	_CENTER	In case of loss of receive PLL reference clock, the PLL gets sourced by CLKIN.

Command ID: **CMD_CFG_DJAT** (cont'd)

DJAT_TRANSMIT$_P$	_DISABLE	Transmit DJAT disabled.
	_ENABLE	Transmit DJAT enabled.
DJAT_TX_LOSMODE$_P$	_AUTO_REF	TE3-FALC automatically switches to the highest prio clock available to source the transmit PLL: (Prio1) recovered route clock → (Prio2) pin TCLKIN → (Prio3) derived from CLKIN, center mode.
	_HOLDOVER	In case of loss of transmit PLL reference clock, the last PLL clock is held. Intrinsic jitter increases.
	_CENTER	In case of loss of transmit PLL reference clock, the PLL gets sourced by CLKIN.

1) In digital line interface mode, the clock on pin RCLKI is used as reference instead.

Command ID: **CMD_CFG_DS3_FRAMER**

This message causes the firmware to configure the DS3 framer. The DS3 framer is configured in C-Bit Parity mode by default. If the M23 mode is sensed from the far end, a M23 indication message **NFC_DS3_FRAMER_MODE** (page 115) is sent to the host.

Input Parameters (optional)

Parameter ID	Value	Description
DS3F_MODE$_P$	_AUTOSENSE	Automatically sense C-Bit Parity mode or M23 mode via the AIC channel
	_CBIT_PARITY	Select C-Bit Parity mode
	_M23	Select M23 unchannelized mode
	_BYPASS	Bypass DS3 framer
	Setting the DS3F_MODE parameter forces the DS3 framer to start a new search for the framing pattern (reframe).	

Command ID: **CMD_CFG_DS3_FRAMER** (cont'd)

DS3F_AIS_PATTERN$_P$	_TOGGLE	AIS pattern is 101010_2... between overhead bits, C-bits all zeros, X-bits all ones (standard)
	_ALL_ONES	AIS pattern is unframed all ones
DS3F_F_REFRAME$_P$	_3_OF_8	New F-frame search when 3 out of 8 contiguous F bits are in error.
	_3_OF_16	New F-frame search when 3 out of 16 contiguous F bits are in error.
DS3F_M_REFRAME$_P$	_DISABLE	No new F-frame search due to M-bit errors, only for F-bit errors
	_2_OF_4	New F-frame search if M-bit errors are detected in 2 out of 4 consecutive M-frames.
	_3_OF_4	New F-frame search if M-bit errors are detected in 3 out of 4 consecutive M-frames.

Notification ID: **NFC_DS3_FRAMER_MODE**

This message notificates to the host, that the C-Bit Parity mode (AIC signal is set to 1) or the M23 mode has been detected (AIC signal is random 1s and 0s) on the DS3 interface. It is only generated if the DS3 framer auto sensing mode is selected. Auto sensing is inhibited by TE3-FALC during times where AIS is received.
To enable this notification use message **CMD_SET_NFC_ALM_MODE** (page 96).

Output Parameters

Parameter ID	Value	Description
DS3F_MODE$_P$	_CBIT_PARITY _M23	Sensed C-Bit Parity mode via AIC signal. Sensed M23 unchannelized mode via AIC signal.

Command ID: **CMD_CFG_E3_FRAMER**

This message causes the firmware to configure the E3 framer.

Input Parameters (optional)

Parameter ID	Value	Description
$E3F\_MODE_P$	_G832	Select E3 framing according to ITU-T G.832.
	_BYPASS	Bypass E3 framer.
	Setting the E3F_MODE parameter forces the E3 framer to start a new search for the framing pattern (reframe).	

Command ID: **CMD_CFG_HDLC_PROCESSOR**

This message causes the firmware to configure the HDLC Module.

Input Parameters (optional)

Parameter ID	Value	Description
$HDLC\_MODE_P$	_BIT_HDLC	Bit-synchronous HDLC operation
	_BIT_PPP	Bit-synchronous PPP operation[1].
	_BYTE_PPP	Byte-synchronous PPP operation. Setting not valid for DS3 flows.
	_TRANSP	Transparent mode: No flags, no CRC, no bit/byte stuffing.
$HDLC\_CRC\_MODE_P$	_CRC16	Select CRC-16 generation/check.
	_CRC32	Select CRC-32 generation/check.
	_NOCRC	Disable CRC generation/check.
$HDLC\_SHARED\_FLG_P$	_DISABLE	Disable shared flag transmission.
	_ENABLE	Enable shared flag transmission.
$HDLC\_IFTF_P$	_FLAGS	Inter-frame time fill pattern is HDLC flags.
	_ALL_ONES	Inter-frame time fill pattern is continuous ones.
$HDLC\_MAX\_FRMLEN_P$	*16-bit field*	Maximum Frame Length in number of bytes (1 to 8187 bytes). Calculation accounts all bytes between start and end flag excluding the CRC field. When programming to zero, the Maximum Frame Length check is disabled.
$HDLC\_MIN\_FRMLEN_P$	*16-bit field*	Minimum Frame Length in number of bytes (1 to 64 bytes). A frame is considered invalid when the number of bytes received is less than this specified length. Calculation accounts all bytes between start and end flag, excluding CRC. When programming to zero, minimum frame length check is disabled.
$PPP\_COMPRESS_P$	_NONE	No compression of Address/Control-field.
	_ADR_CTRL	Enable compressed Address/Control field.
	Only applicable for PPP modes.	

[1] In case of inter-frame time fill set to 'continuous ones', the minimum number of idle ones between two frames is 7 in bit-synchronous HDLC mode, 15 in bit-synchronous PPP mode.

Command ID: **CMD_CFG_ATM_PROCESSOR**

This message causes the firmware to configure the G.804 Module.

Input Parameters (optional)

Parameter ID	Value	Description
$ATM\_MAPPING_P$	_DIRECT _PLCP	Direct mapped ATM. PLCP mapped ATM. Setting only available with DS3 flow.
$ATM\_SCRAMBLING_P$	_DISABLE _ENABLE	Disable ATM payload scrambling. Enable ATM payload scrambling acc. to I.432.1.
$ATM\_HEAD\_CORR_P$	_DISABLE _ENABLE	Disable header error correction. Enable single-bit header error correction.
ATM_ALPHA_P	*16-bit field*	Determines the transition conditions (number of consecutive incorrect HECs) from SYNCH to HUNT state in the cell delineation state diagram (1 to 31). Default is 7.
ATM_DELTA_P	*16-bit field*	Determines the transition conditions (number of consecutive correct HECs) from PRESYNC to SYNCH state in the cell delineation state diagram (1 to 31). Default is 6.

Command ID: **CMD_CFG_SYSIF**

This message causes the firmware to configure the System Interface.

Input Parameters (optional)

Parameter ID	Value	Description
$SYSIF\_MODE_P$	_UTOPIA_L1	UTOPIA Level 1 mode
	_UTOPIA_L2	UTOPIA Level 2 mode
	_POSPHY_L2	POS-PHY Level 2 mode
	_UTOPIA_L2X	UTOPIA Level 2 eXtended mode
$SYSIF\_WIDTH_P$	_8BIT	8 bit data bus width
	_16BIT	16 bit data bus width
$SYSIF\_ADDR_P$	*16-bit field*	PHY address (0 to 30). Default is 0.
	Not applicable for UTOPIA Level 1 mode.	
$SYSIF\_STATUS_P$	_POLLING	MPHY Polling
	_DIRECT_IND	Direct Status Indication
	Not applicable for UTOPIA Level 1 mode.	
$SYSIF\_CHUNK\_SIZE_P$	*16-bit field*	UTOPIA-L2X Chunk Size: The UTOPIA-L2X Chunk Size is programmable between 16 and 128 bytes, in multiples of 4. Default: 64 bytes. POS-PHY-L2 Burst Size: The POS-PHY burst size is programmable between 4 and 256 bytes, in multiples of 4. Default: 64 bytes.
	Not applicable for UTOPIA Level 1 / Level 2 mode.	
$SYSIF\_PARITY\_CHK_P$	_DISABLE	Parity checking across the transmit input data bus is disabled.
	_ENABLE	Parity checking across the transmit input data bus is enabled. Parity errored transmit cells/packets are discarded.

Command ID: **CMD_CFG_SYSIF** (cont'd)

$SYSIF\_PARITY_P$	_ODD	Calculated parity over data bus is Odd.
	_EVEN	Calculated parity over data bus is Even.
$SYSIF\_OUTPUTS_P$	_TRISTATE	Outputs tri-state during idle times. This is the recommended setting.
	_DRIVING	Outputs do not tri-state. This is only applicable for a point-to-point connection.
$SYSIF\_HANDSHAKE_P$	_PKT_CELL	Packet (POS-PHY) / Cell (UTOPIA) Level handshake
	_BYTE	Byte (POS-PHY) / Octet (UTOPIA) Level handshake
	Not applicable for UTOPIA Level 2 eXtended mode.	

Command ID: **CMD_CFG_BUFFERS**

This message causes the firmware to configure the Data Buffers.
The forward threshold parameter has no relevance for ATM operation.

Input Parameters (optional)

Parameter ID	Value	Description
BUF_SIZE_P	*16-bit field*	✧Buffer Size. The buffer size can be programmed in multiples of 64-byte blocks[1]. The lower limit is 2 blocks (128 bytes). The upper limit is 14 blocks (896 bytes).
$BUF\_FW\_THRESH_P$	*16-bit field*	Forward Threshold (not for ATM cells). In order to prevent transmit underrun situations, data is no earlier forwarded to the protocol processor than the forward threshold has been reached, i.e. the amount of data bytes reaches this programmed value (4 to 308 bytes, in multiples of 4). Short packets that do not reach the threshold are forwarded as soon as the packet end is stored in the buffer. Default setting is 64 bytes.

[1] This is an option which is not available with the current firmware release.

Command ID: **CMD_CFG_GPIO**

This message causes the firmware to configure the General Purpose I/O port pins.

Input Parameters (optional)		
Parameter ID	Value	Description
$GPIO\_0\_CTRL_P$	_IN	Input Pin
	_IN_PU	Input Pin with internal Pull-Up
	_IN_PD	Input Pin with internal Pull-Down
	_OUT	Output Pin (Push/Pull)
	_OUT_OD	Output Pin (Open Drain)
	_LED_STATUS	Configurable Status Output (Push/Pull). The condition that leads to activation (high level) of this pin is programmable with parameter GPIO_0_LED_STAT.
$GPIO\_1\_CTRL_P$	*as above*	*analog to GPIO Pin 0 above*
...	...	...
$GPIO\_7\_CTRL_P$	*as above*	*analog to GPIO Pin 0 above*
$GPIO\_ALL\_CTRL_P$	*as above*	This option allows to configure all 8 port pins at the same time.
$GPIO\_0\_LED\_STAT_{32}$	*32-bit field*	This 32-bit field is only evaluated if option GPIO_0_CTRL_LED_STATUS from above is selected. For the 32-bit value refer to **ACK_GET_STATUS** (page 143). If a combination of several indications/ failures is entered, the LED status output is the OR function of the respective bits. Default: $0000\ 0800_H$ (Out Of Service)
$GPIO\_1\_LED\_STAT_{32}$	*32-bit field*	Default: $0040\ 0000_H$ (Local Loop)
$GPIO\_2\_LED\_STAT_{32}$	*32-bit field*	Default: $0000\ 0080_H$ (Remote Loop)
$GPIO\_3\_LED\_STAT_{32}$	*32-bit field*	Default: $0002\ 0000_H$ (OOF Defect)
$GPIO\_4\_LED\_STAT_{32}$	*32-bit field*	Default: $0000\ 0001_H$ (No Alarm)
$GPIO\_5\_LED\_STAT_{32}$	*32-bit field*	Default: $0004\ 0000_H$ (RDI Defect)
$GPIO\_6\_LED\_STAT_{32}$	*32-bit field*	Default: $0008\ 0000_H$ (LOS Defect)
$GPIO\_7\_LED\_STAT_{32}$	*32-bit field*	Default: $0001\ 0000_H$ (AIS Defect)

Command ID: **CMD_READ_GPIO**

This message causes the firmware to perform a read access to the General Purpose I/O port pins.

Input Parameters	*none*

Acknowledgement ID: **ACK_READ_GPIO**

Returned input level of the GPIO port after requested by the host via message **CMD_READ_GPIO**.

Output Parameters

Parameter ID	Value	Description
$GPIO\_VALUE_P$	*16-bit field*	Current input level of the 8 GPIO port pins (including those configured as outputs).

Command ID: **CMD_WRITE_GPIO**

This message causes the firmware to perform a write access to the General Purpose I/O port pins.

Input Parameters (optional)

Parameter ID	Value	Description
$GPIO\_VALUE_P$	*16-bit field*	The lower 8-bit value gets mapped to the 8 port pins. Individual bits can get masked with parameter GPIO_MASK. Default is 00_H.
$GPIO\_MASK_P$	*16-bit field*	This bit mask defines which of the GPIO output ports get overwritten and which ones do not. A ’1’ at the corresponding bit postion enables overwriting. Default is FF_H.

6.3.5 Link Maintenance Messages

6.3.5.1 TTI Support (E3/G.832)

The firmware synchronizes to the Trail Trace Identifier (TTI) as specified in G.832 Annex A and checks and generates the CRC-7 checksums. TTI data are not generated or evaluated by the firmware but passed through the user interface. The received TTI is compared against a user-supplied TTI, and deviations are reported. The 16-byte frame format is shown in **Table 40**.

Table 40 TTI Message - 16-Byte Frame Format

	MSB	LSB
Byte 1	1[1)]	CRC-7 (over previous frame) [2)]
Byte 2	0	7-bit Character
Byte 3	0	7-bit Character
	...	...
Byte 16	0	7-bit Character

1) Frame Start Marker; must be set to '1' in transmit direction

2) If in transmit direction automatic CRC-7 generation is enabled, set these 7 bits to '0'.

Command ID: CMD_CFG_TTI_CHANNEL

This message causes the firmware to start or stop receiving TTI data. The TTI transmitter is always active.

Input Parameters (optional)

Parameter ID	Value	Description
$TTI\_RX\_CHNG\_CNT_P$	*16-bit field*	Number of repetitions (3 to 15) of new valid TTI before a change is accepted/ reported. Default is 3.
$TTI\_TX\_DATA_8$	*16 × 8-bit array*	16 bytes of new Transmit TTI Data (includes CRC)
$TTI\_CRC\_GENERATE_P$	_DISABLE _ENABLE	Disable CRC-7 checksum generation. Enable CRC-7 checksum generation. This is valid for both receive and transmit TTI.
$TTI\_RX\_CMP\_DATA_8$	*16 × 8-bit array*	16 bytes of new Receive TTI Data to compare with (includes CRC)

Notification ID: **NFC_TTI_RX_DATA_CHANGE**

This message indicates to the host that TTI data different from the data set by message **CMD_CFG_TTI_CHANNEL** was received.
To enable this notification use message **CMD_SET_NFC_ALM_MODE** (page 96).

Output Parameters

Parameter ID	Value	Description
$TTI\_RX\_STATUS_P$	_MATCH	New received TTI data matches preset receive data, including correct CRC.
	_MISMATCH	New received TTI data does not match preset receive data but has correct CRC.
	_INVALID	Received TTI data is invalid (CRC errors and/or invalid data format).
$TTI\_RX\_DATA_8$	*16 × 8-bit array*	16 bytes of new Receive TTI Data (includes CRC)

6.3.5.2 Payload Type (PTY) Support (E3/G.832)

Command ID: **CMD_CFG_PTY_CHANNEL**

This message causes the firmware to start or stop evaluating the received PTY field and sets the transmit and receive Payload Type field. The PTY transmitter is always active. Note that the Payload Type field is also set with the data path configuration messages.

Input Parameters (optional)

Parameter ID	Value	Description
$PTY\_RX\_CHNG\_CNT_P$	*16-bit field*	Number of repetitions (3 to 15) of new valid PTY before a change is accepted/ reported. Default is 3.
$PTY\_TX\_FIELD_P$	_UNEQUIPPED	Set transmit Payload Type field to 'unequipped'.
	_NONSPECIFIC	Set transmit Payload Type field to 'equipped, non-specific'.
	_ATM	Set transmit Payload Type field to 'ATM'.
	_SDH_TU12	Set transmit Payload Type field to 'SDH TU 12s'.
$PTY\_RX\_CMP\_FIELD_P$	_UNEQUIPPED	Set expected receive Payload Type field to 'unequipped'.
	_NONSPECIFIC	Set expected receive Payload Type field to 'equipped, non-specific'.
	_ATM	Set expected receive Payload Type field to 'ATM'.
	_SDH_TU12	Set expected receive Payload Type field to 'SDH TU 12s'.

Notification ID: **NFC_PTY_RX_DATA_CHANGE**

This message indicates to the host that a PTY field different from the field set by message **CMD_CFG_PTY_CHANNEL** was received.

Output Parameters

Parameter ID	Value	Description
$PTY\_RX\_STATUS_P$	_MATCH	New received PTY data matches preset receive data.
	_MISMATCH	New received PTY data does not match preset receive data.
	_UNSTABLE	Received PTY data is unstable.
$PTY\_RX\_FIELD_P$	_UNEQUIPPED	Received Payload Type field is ’unequipped’.
	_NONSPECIFIC	Received Payload Type field is ’equipped, non-specific’.
	_ATM	Received Payload Type field is ’ATM’.
	_SDH_TU12	Received Payload Type field is ’SDH TU 12s’.

6.3.5.3 SSM Nibble Support (E3/G.832)

Command ID: **CMD_CFG_SSM_CHANNEL**

This message causes the firmware to start or stop receiving SSM nibble data. The SSM transmitter is always active.

Input Parameters (optional)

Parameter ID	Value	Description
$SSM\_RX\_CHNG\_CNT_P$	*16-bit field*	Sets the number of repetitions of new valid SSM before a change is accepted/ reported.
$SSM\_TX\_DATA_P$	*16-bit field*	Transmit SSM nibble data (4-bits)
$SSM\_RX\_CMP\_DATA_P$	*16-bit field*	Expected receive SSM nibble data (4-bits)

Notification ID: **NFC_SSM_RX_DATA_CHANGE**

This message indicates to the host that SSM data different from the data set by message **CMD_CFG_SSM_CHANNEL** was received.
To enable this notification use message **CMD_SET_NFC_ALM_MODE** (page 96).

Output Parameters

Parameter ID	Value	Description
$SSM\_RX\_DATA_P$	*16-bit field*	Receive SSM nibble data (4-bits)
$SSM\_RX\_STATUS_P$	_MATCH	New received SSM data matches preset receive data.
	_MISMATCH	New received SSM data does not match preset receive data.
	_UNSTABLE	Received SSM data is unstable.

6.3.5.4 MDL Support (DS3)

Three bits C-Bits per multiframe (DL_t bits) are used for the MDL channel (Path Maintenance Data Link). An HDLC controller processes these bits, checks and generates CRC16 checksums, adds and detects HDLC frame delimiting flags etc.

The HDLC idle pattern when no data are transmitted is the HDLC flag (01111110).

Received and transmitted frames are not generated or evaluated by the firmware but passed through the user interface.

Command ID: CMD_CFG_MDL_CHANNEL

This message causes the firmware to configure the MDL controller.

Input Parameters (optional)

Parameter ID	Value	Description
$MDL\_RECEIVE_P$	_DISABLE	Disable MDL Receive Channel.
	_ENABLE	Enable MDL Receive Channel. Make sure that the **NFC_MDL_RX_DATA** (page 129) notification gets enabled too.
$MDL\_TRANSMIT_P$	_DISABLE	Disable MDL Transmit Channel.
	_ENABLE	Enable MDL Transmit Channel.
$MDL\_MAX\_FRM\_LEN_P$	*16-bit field*	Maximum Frame Length (1 to 256 octets)
$MDL\_RX\_ERR\_RPT_P$	_DISABLE	Errored MDL data gets discarded without notification to the user.
	_ENABLE	The notification **NFC_MDL_RX_DATA** (page 129) gets sent for both valid and errored MDL data.

Command ID: CMD_SET_MDL_TX_DATA

This message causes the firmware to transmit MDL data.

Input Parameters (optional)

Parameter ID	Value	Description
$MDL\_TX\_DATA_8$	*n × 8-bit array (1 ≤ n ≤ 256)*	Transmit MDL data (maximum length as specified via message **CMD_CFG_MDL_CHANNEL**)

Notification ID: **NFC_MDL_RX_DATA**

This message notifies the host about new receive MDL data. Along with the MDL data, the parameter MDL_RX_STATUS indicates whether the received HDLC frame is valid or not.
To enable this notification use message **CMD_SET_NFC_ALM_MODE** (page 96).

Output Parameters

Parameter ID	Value	Description
$MDL\_RX\_DATA_8$	*n × 8-bit array (1 ≤ n ≤ 256)*	Receive MDL data (maximum length as specified via message **CMD_CFG_MDL_CHANNEL**)
$MDL\_RX\_STATUS_P$	_VALID_FRAME	Valid Frame
	_CRC_ERR	CRC error
	_ABORT_ERR	Aborted frame
	_MAXFL_ERR	Frame exceeded maximum length
	_MINFL_ERR	Frame too short
	_ILEN_ERR	Frame length not multiple of 8 bits

6.3.5.5 FEAC Support (DS3)

The firmware synchronizes to the 8-ones bit pattern in the FEAC codes delivered by the hardware. **Table 41** and **Table 42** list the FEAC codes supported by the TE3-FALC firmware, according to ANSI T1.107-1995 (Figures 23 and 24). The unassigned codes listed in ANSI T1.107-1995 Table 25 are not supported by the TE3-FALC firmware.

The rightmost bit of each codeword is transmitted first. Specific codewords are transmitted continuously for the duration of the alarm or status condition, or for a minimum of n codeword repetitions (n is programmable), whichever is longer. When no alarm or status condition is being transmitted, the FEAC code contains all ones.

Table 41 FEAC Alarm and Status Codes

Alarm / Status Codes	ID	Code Word	(Hex)	Prio Code
DS3 equiment failure (SA)	_DS3_SA	0 011001 0 11111111	32_H	38_H
DS3 Loss of Signal (LOS)	_DS3_LOS	0 001110 0 11111111	$1C_H$	30_H
DS3 Out-of-Frame	_DS3_OOF	0 000000 0 11111111	00_H	28_H
DS3 AIS received	_DS3_AIS	0 010110 0 11111111	$2C_H$	20_H
DS3 IDLE received	_DS3_IDLE	0 011010 0 11111111	34_H	18_H
DS3 equiment failure (NSA)	_DS3_NSA	0 001111 0 11111111	$1E_H$	10_H
Common equipment failure (NSA)	_COM_NSA	0 011101 0 11111111	$3A_H$	08_H
No FEAC Code	_NONE	1 111111 1 11111111	FF_H	00_H

The DS3 line loopback codes consist of a sequence of two FEAC codewords (see **Table 42**). These codewords are sent sequentially, each with the programmed repetition count (inifinite repetition count is not allowed). This ensures that no gap occurs between the 2 codewords.

Table 42 FEAC Loopback Control Codes

Loopback Control Codes	ID	Code Word	(Hex)	Prio Code
DS3 Line loopback activate	_DS3_LP_ON[1)]	0 011011 0 11111111	36_H	40_H
		0 000111 0 11111111	$0E_H$	40_H
DS3 Line loopback deactivate	_DS3_LP_OFF[2)]	0 011011 0 11111111	36_H	40_H
		0 011100 0 11111111	38_H	40_H

1) The corresponding 16-bit parameter value of this code sequence is $8F40_H$

2) The corresponding 16-bit parameter value of this code sequence is $B940_H$

Command ID: **CMD_SET_FEAC_CODE**

This message causes the firmware to transmit the FEAC code word followed by the DS3 line code word acc. to ANSI T1.107-1995.

Input Parameters (optional)

Parameter ID	Value	Description
$FEAC\_CODEWORD_P$	_DS3_SA	DS3 equiment failure (Service Affecting)
	_DS3_LOS	DS3 Loss of Signal LOS
	_DS3_OOF	DS3 Out-of-Frame
	_DS3_AIS	DS3 AIS received
	_DS3_IDLE	DS3 IDLE Signal received
	_DS3_NSA	DS3 equiment failure (Non-Service Affecting)
	_COM_NSA	Common equipment failure (Non-Service Affecting)
	_DS3_LP_ON	DS3 Line Loopback activate
	_DS3_LP_OFF	DS3 Line Loopback deactivate
	_NONE	No valid FEAC code to be transmitted
	other 16-bit value	High byte is the actual FEAC code (excluding FF_H), low byte defines priority of this code. Refer to **Table 41** and **Table 42** for the predefined code words with their priority code.
$FEAC\_CODE\_CNT_P$	*16-bit field*	Repetition Counter for FEAC code word (10 to 65535). Progamming to zero leads to infinite repetition count. Default is 10.

Notification ID: **NFC_FEAC_LOOP_STATUS**

This message indicates to the host, that the loop status changed, indicated via FEAC channel.
To enable this notification use message **CMD_SET_NFC_ALM_MODE** (page 96).

Output Parameters

Parameter ID	Value	Description
$FEAC\_DS3\_LOOP_P$	_INACTIVE	DS3 Line loopback is inactive.
	_ACTIVE	DS3 Line loopback is active.

6.3.6 Alarm Messages

6.3.6.1 Framer LOS Detection (Loss of Signal)

Alarm ID: **ALM_FRM_LOS_DEFECT**

An LOS defect occurs when the TE3-FALC does not detect the expected signal type on the line.
In DS3 mode, LOS defects are integrated to generate an LOS failure after 2.5 sec.
To enable this alarm use message **CMD_SET_NFC_ALM_MODE** (page 96).

Output Parameters		
Parameter ID	Value	Description
$FRM\_LOS\_DEFECT_P$	_DECLARED	LOS defect has been declared
	_CLEARED	LOS defect has been cleared
Firmware Actions		
Actions when declared	– Declare RDI to far end (if enabled) – Increment LOS counter – Activate LOS LED (if enabled) – Start integration for LOS Failure (DS3 only)	
Actions when cleared	– Clear RDI to far end – Deactivate LOS LED (if enabled) – Stop integration for LOS Failure (DS3 only)	

Alarm ID: **ALM_FRM_LOS_FAILURE**

This alarm notifies about both declaring and clearing a Loss of Signal (LOS) failure. It is only supported in DS3 mode.
To enable this alarm use message **CMD_SET_NFC_ALM_MODE** (page 96).

Output Parameters		
Parameter ID	Value	Description
$FRM\_LOS\_FAILURE_P$	_DECLARED	LOS failure has been declared since LOS defect persisted for 2.5 sec.
	_CLEARED	LOS failure has been cleared since the last 10.0 sec had no LOS defects.
Firmware Actions		
Actions when declared	– Start transmission of the FEAC code 'DS3 LOS' to the far end (if enabled), unless a higher priority FEAC code needs to be sent	
Actions when cleared	– Stop transmission of the FEAC code 'DS3 LOS'	

6.3.6.2 Framer OOF/LOF Detection (Out of Frame, Loss of Frame)

Alarm ID: **ALM_FRM_OOF_DEFECT**

This alarm notifies about both declaring and clearing a Out-of-Frame (OOF) defect. An OOF defect is indicated by the framer if several F- and M-bit errors are detected. In DS3 mode, OOF defects are integrated to generate an LOF failure after 2.5 sec.
To enable this alarm use message **CMD_SET_NFC_ALM_MODE** (page 96).

Output Parameters		
Parameter ID	Value	Description
$FRM\_OOF\_DEFECT_P$	_DECLARED	OOF defect has been declared.
	_CLEARED	OOF defect has been cleared.
Firmware Actions		
Actions when declared	– Declare RDI to far end (if enabled) – Incremet OOF counter – Activate OOF LED (if enabled) – Start integration for LOF Failure (DS3 only)	
Actions when cleared	– Clear RDI to far end – Deactivate OOF LED (if enabled) – Stop integration for LOF Failure (DS3 only)	

Alarm ID: **ALM_FRM_LOF_FAILURE**

This alarm notifies about both declaring and clearing a Loss of Frame (LOF) failure. It is only supported in DS3 mode.
To enable this alarm use message **CMD_SET_NFC_ALM_MODE** (page 96).

Output Parameters		
Parameter ID	Value	Description
$FRM\_LOF\_FAILURE_P$	_DECLARED	LOF failure has been declared since OOF defect persisted for 2.5 sec.
	_CLEARED	LOF failure has been cleared since the last 10.0 sec had no OOF defects.
Firmware Actions		
Actions when declared	– Start transmission of the FEAC code 'DS3 out-of-frame' to the far end (if enabled), unless a higher priority FEAC code needs to be sent	
Actions when cleared	– Stop transmission of the FEAC code 'DS3 out-of-frame'	

6.3.6.3 Framer AIS/IDLE Detection (Alarm Indication, DS3 Idle Signal)

Alarm ID: **ALM_FRM_AIS_DEFECT**

An AIS defect is declared when the AIS pattern is received from the far end. In DS3 mode, AIS defects are monitored to generate an AIS failure after 2.5 sec.
To enable this alarm use message **CMD_SET_NFC_ALM_MODE** (page 96).

Output Parameters		
Parameter ID	Value	Description
$FRM\_AIS\_DEFECT_P$	_DECLARED	AIS defect has been declared.
	_CLEARED	AIS defect has been cleared.
Firmware Actions		
Actions when declared	– Declare RDI to far end (if enabled) – Activate AIS LED (if enabled) – Start integration for AIS Failure (DS3 only)	
Actions when cleared	– Clear RDI to far end – Deactivate AIS LED (if enabled) – Stop integration for AIS Failure (DS3 only)	

Alarm ID: **ALM_FRM_AIS_FAILURE**

This alarm notifies about both declaring and clearing an AIS failure. It is only supported in DS3 mode.
To enable this alarm use message **CMD_SET_NFC_ALM_MODE** (page 96).

Output Parameters		
Parameter ID	Value	Description
$FRM\_AIS\_FAILURE_P$	_DECLARED	AIS failure has been declared since AIS defect persisted for 2.5 sec.
	_CLEARED	AIS failure has been cleared since the last 10.0 sec had no AIS defects.
Firmware Actions		
Actions when declared	– Start transmission of the FEAC code 'DS3 AIS Received' to the far end (if enabled), unless a higher priority FEAC code needs to be sent	
Actions when cleared	– Stop transmission of the FEAC code 'DS3 AIS Received'	

Alarm ID: **ALM_FRM_IDLE_RECEIVED**

This alarm is generated if the DS3 Idle Signal is detected on the receive line. The Idle Signal is defined as a 1100_2... inside the DS3 payload. This message is supported in DS3 mode only.
To enable this alarm use message **CMD_SET_NFC_ALM_MODE** (page 96).

Output Parameters		
Parameter ID	Value	Description
$FRM\_IDLE\_RCVD_P$	_DECLARED	DS3 Idle is being received.
	_CLEARED	No DS3 Idle is received.

Firmware Actions	
Actions when declared	– Start transmission of the FEAC code 'DS3 IDLE Received' to the far end (if enabled), unless a higher priority FEAC code needs to be sent
Actions when cleared	– Stop transmission of the FEAC code 'DS3 IDLE Received'

6.3.6.4 Framer AIS/IDLE Generation (Alarm Indication, DS3 Idle Signal)

Command ID: **CMD_FRM_TX_AIS_IDLE**

With this message the transmit signal can be set to AIS or Idle (DS3 only). In DS3 mode, the AIS signal definition can be programmed with message **CMD_CFG_DS3_FRAMER** (page 114).

Input Parameters (optional)		
Parameter ID	Value	Description
$FRM\_TX\_SIGNAL_P$	_NORMAL	Transmit Normal Data
	_AIS	Transmit AIS Signal
	_IDLE	Transmit DS3 Idle Signal (DS3 only)

6.3.6.5 Framer RDI Detection (Remote Defect Indication)

Older DS3 standards (esp. ANSI) referred to this signal element as a “Yellow Alarm” or RAI signal. In newer standards, the usage does not correspond to a typical Yellow Alarm or RAI signal, which is only sent after a multi-second soaking period. The more accurate RDI terminology has been adopted in ANSI standards. Note that the defect that is detected upon receipt of this signal is sometimes referred to as a “far-end SEF/AIS defect".

Alarm ID: **ALM_FRM_RDI_DEFECT**

In DS3 mode, an RDI defect (also known as “far-end SEF/AIS defect") is declared when both X-bits in an M-frame are received to zero. It is cleared when both X-bits are received to one.
In E3 mode a dedicated RDI bit exists in the MA byte.
To enable this alarm use message **CMD_SET_NFC_ALM_MODE** (page 96).

Output Parameters		
Parameter ID	Value	Description
$FRM\_RDI\_DEFECT_P$	_DECLARED	RDI defect has been declared.
	_CLEARED	RDI defect has been cleared.
Firmware Actions		
Actions when declared	– Increment RDI counter – Activate RDI LED (if enabled) – Start integration for RDI Failure (DS3 only)	
Actions when cleared	– Deactivate RDI LED (if enabled) – Stop integration for RDI Failure (DS3 only)	

Alarm ID: **ALM_FRM_RDI_FAILURE**

This alarm notifies about both declaring and clearing an Remote Defect Indication (RDI) failure. It is only supported in DS3 mode.
To enable this alarm use message **CMD_SET_NFC_ALM_MODE** (page 96).

Output Parameters		
Parameter ID	Value	Description
$FRM\_RDI\_FAILURE_P$	_DECLARED	RDI failure has been declared since RDI defects persisted for 2.5 sec.
	_CLEARED	RDI failure has been cleared since the last 10.0 sec had no RDI defects.
Firmware Actions		
Actions when declared	–	
Actions when cleared	–	

6.3.6.6 Framer RDI Generation (Remote Defect Indication)

Command ID: **CMD_CFG_RDI_DECLARATION**

This message configures the criteria to declare "Remote Defect Indication" (RDI) towards the far end. By default, RDI is only declared on LOS, OOF and AIS defects. In an E3 configration, also the G.804 "Loss of Cell Delineation" (LCD) event is taken into account.
To be compliant to the 'old' ANSI interpretation of the DS3 "Yellow Alarm" (RAI) set the parameter RDI_ON_LOF_FAIL_ENABLE.

Input Parameters (optional)

Parameter ID	Value	Description
$RDI\_ON\_LOS\_DEFCT_P$	_DISABLE	Do not declare RDI on LOS Defect
	_ENABLE	Declare RDI on LOS Defect
$RDI\_ON\_OOF\_DEFCT_P$	_DISABLE	Do not declare RDI on OOF Defect
	_ENABLE	Declare RDI on OOF Defect
$RDI\_ON\_LOF\_FAIL_P$	_DISABLE	Do not declare RDI on LOF Failure
	_ENABLE	Declare RDI on LOF Failure (DS3 only)
$RDI\_ON\_AIS\_DEFCT_P$	_DISABLE	Do not declare RDI on AIS Defect
	_ENABLE	Declare RDI on AIS Defect
$RDI\_ON\_LCD_P$	_DISABLE	Do not declare RDI on G.804 LCD event
	_ENABLE	Declare RDI on G.804 LCD event (E3 only)
$RDI\_ON\_TIM_P$	_DISABLE	Do not declare RDI on G.832 Trail Trace Identifier Mismatch
	_ENABLE	Declare RDI on G.832 Trail Trace Identifier Mismatch (E3 only)
$RDI\_ON\_UNEQ_P$	_DISABLE	Do not declare RDI on receiving G.832 PTY field 'unequipped'
	_ENABLE	Declare RDI on receiving G.832 PTY field 'unequipped' (E3 only)
$RDI\_ON\_PLM_P$	_DISABLE	Do not declare RDI on G.832 PTY field mismatch
	_ENABLE	Declare RDI on G.832 PTY field mismatch (E3 only)

6.3.6.7 Framer FEAC Detection (Far End Alarm Control)

Alarm ID: **ALM_FEAC_ALARM**

This message indicates to the host, that a FEAC alarm has occured.
To enable this alarm use message **CMD_SET_NFC_ALM_MODE** (page 96).

Output Parameters

Parameter ID	Value	Description
$FEAC\_ALARM_P$	_DS3_SA	DS3 equiment failure (Service Affecting)
	_DS3_LOS	DS3 Loss of Signal LOS
	_DS3_OOF	DS3 Out-of-Frame
	_DS3_AIS	DS3 AIS received
	_DS3_IDLE	DS3 IDLE Signal received
	_DS3_NSA	DS3 equiment failure (Non-Service Affecting)
	_COM_NSA	Common equipment failure (Non-Service Affecting)
	_NONE	No valid FEAC code is being received

6.3.6.8 Framer FEAC Generation (Far End Alarm Control)

Command ID: **CMD_CFG_FEAC_GENERATION**

This message controls the automatic generation of FEAC codes towards the far end. By default all FEAC codes are disabled, i.e. the FEAC channel transmits all ones.

Input Parameters (optional)

Parameter ID	Value	Description
$FEAC\_ON\_LOS\_FAIL_P$	_DISABLE	Do not generate FEAC code on LOS Failure
	_ENABLE	Generate FEAC code on LOS Failure
$FEAC\_ON\_LOF\_FAIL_P$	_DISABLE	Do not generate FEAC code on LOF Failure
	_ENABLE	Generate FEAC code on LOF Failure
$FEAC\_ON\_AIS\_FAIL_P$	_DISABLE	Do not generate FEAC code on AIS Failure
	_ENABLE	Generate FEAC code on AIS Failure
$FEAC\_ON\_IDLE\_RCV_P$	_DISABLE	Do not generate FEAC code on reception of IDLE Pattern
	_ENABLE	Generate FEAC code on reception of IDLE Pattern

6.3.6.9 PLCP OOF Detection (Out-of-Frame)

Alarm ID: **ALM_PLCP_OOF_DEFECT**

This alarm notifies about both declaring and clearing a PLCP Out-of-Frame (OOF) defect. To enable this alarm use message **CMD_SET_NFC_ALM_MODE** (page 96).

Output Parameters		
Parameter ID	Value	Description
$PLCP\_OOF\_DEFECT_P$	_DECLARED _CLEARED	PLCP-OOF defect has been declared. PLCP-OOF defect has been cleared.
Firmware Actions		
Actions when declared	– Declare PLCP-RAI to far end – Increment PLCP-OOF counter	
Actions when cleared	– Clear PLCP-RAI to far end	

6.3.6.10 PLCP RAI Detection (Remote Alarm Indication)

Alarm ID: **ALM_PLCP_RAI_DEFECT**

This alarm notifies about both declaring and clearing a receive PLCP Remote Alarm Indication (RAI) defect.
To enable this alarm use message **CMD_SET_NFC_ALM_MODE** (page 96).

Output Parameters		
Parameter ID	Value	Description
$PLCP\_RAI\_DEFECT_P$	_DECLARED _CLEARED	RDI defect has been declared. RDI defect has been cleared.
Firmware Actions		
Actions when declared	– Increment PLCP-RAI counter	
Actions when cleared	–	

6.3.6.11 G.804 LCD Detection (Loss of Cell Delineation)

Alarm ID: **ALM_G804_LCD**

This message indicates to the host, that the G.804 receiver has lost or gained cell delineation synchronization.
To enable this alarm use message **CMD_SET_NFC_ALM_MODE** (page 96).

Output Parameters		
Parameter ID	Value	Description
$G804\_LCD_P$	_DECLARED	Loss of cell delineation has been declared.
	_CLEARED	Loss of cell delineation has been cleared.
Firmware Actions		
Actions when declared	– Declare RDI to far end (if enabled; E3 only) – Increment LCD counter	
Actions when cleared	– Clear RDI to far end (E3 only)	

6.3.6.12 Buffer XDU/RDO Detection (Tx Underun, Rx Overflow)

Alarm ID: **ALM_TX_UNDERRUN**

This alarm notifies about a transmit data underrun (XDU) event in the PPP/HDLC packet processor. It is not applicable in ATM operation.
To enable this alarm use message **CMD_SET_NFC_ALM_MODE** (page 96).

Output Parameters	*none*

Alarm ID: **ALM_RX_OVERFLOW**

This alarm notifies about a receive data overflow (RDO) event in the receive buffer.
To enable this alarm use message **CMD_SET_NFC_ALM_MODE** (page 96).

Output Parameters	*none*

6.3.7 Performance Measurement

6.3.7.1 Bit Error Ratio Testing (BERT)

Command ID: **CMD_CTRL_BERT**

This message configures the bit error ratio test unit with a programmable bit pattern. Note that the framer gets reset with each start of a BER measurement.

Input Parameters (optional)

Parameter ID	Value	Description
$BERT\_CONTROL_P$	_START	Start bit error ratio measurement with programmed measurement interval. If an interval > 0 is programmed, the BERT result is reported via message **NFC_BERT_RESULT** (page 142).
	_STOP	Stop current bit error ratio measurement. The BERT results can be determined with message **CMD_GET_STATISTICS** (page 149).
$BERT\_PATTERN_P$	_2P15	2^{15} -1 pseudo-random pattern (O.151)
	_2P20	2^{20} -1 pseudo-random pattern (O.153)
	_2P20_QRSS	2^{20} -1 pseudo-random pattern with zero suppression (O.151)
	_2P23	2^{23} -1 pseudo-random pattern (O.151)
	_ALL_ONES	All Ones fixed pattern
	_ALL_ZEROS	All Zeros fixed pattern
	_TOGGLE	Toggling 101010_2... fixed pattern
	_GEN_RAND	Generic pseudo-random test sequence built based on BERT_GEN_LENGTH and BERT_GEN_FBTAP (see **Figure 8**)
	_GEN_FIXED	Generic fixed pattern test sequence built based on BERT_GEN_LENGTH and BERT_GEN_FIXPAT.
$BERT\_INTERVAL_P$	*16-bit field*	Defines a bit error ratio measurement interval from 1 to 1440 minutes (24h). Programming to zero leads to infinite measurement interval (to be stopped manually with BERT_CONTROL_STOP).

Command ID: **CMD_CTRL_BERT** (cont'd)

Note: The parameters listed below are only relevant if a generic pattern shall be built.

$BERT\_GEN\_LENGTH_P$	*16-bit field*	For a *pseudo-random* pattern, the test sequence length is $2^{BERT\_GEN\_LENGTH}$ -1. For a *fixed* pattern, this field defines the length (1..32 bit) of the test sequence. Default is 32.
$BERT\_GEN\_FBTAP_P$	*16-bit field*	Defines the position of the feedback tap (1..32) for a *pseudo-random* pattern (see **Figure 8**). Default is 16.
$BERT\_GEN\_FIXPAT_{32}$	*32-bit field*	For a generic *fixed* pattern, this field, together with BERT_GEN_LENGTH defines the pattern to be generated. Default is 0xAAAAAAAA.
$BERT\_GEN\_INVERT_P$	_DISABLE _ENABLE	No pattern inversion. Pattern generator output gets inverted.

Notification ID: **NFC_BERT_RESULT**

To enable this notification use message **CMD_SET_NFC_ALM_MODE** (page 96).

Output Parameters

Parameter ID	Value	Description
$RPT\_BERT\_TOTAL_{32}$	*2 × 32-bit array*	The first 32-bit word contains the Receive Bit Count. The second 32-bit word contains the Receive Error Count (only incremented in synchronous state).

6.3.7.2 Status Messages

Command ID: **CMD_GET_STATUS**

This message initiates the firmware to send the device status in form of a 32-bit status word.

Input Parameters	*none*

Acknowledgement ID: **ACK_GET_STATUS**

The device status is coded as a 32-bit word with the bit assignment shown below. If multiple failures/indications are active simultaneously, the resulting status word is represented as the sum of the individual status words.

Output Parameters

Parameter ID	Value	Description
$DEVICE\_STATUS_{32}$	$0000\ 0001_H$	No Alarm
	$0000\ 0002_H$	Receiving DS3/E3 RDI Failure
	$0000\ 0004_H$	Transmitting DS3/E3 RDI
	$0000\ 0008_H$	Receiving DS3/E3 AIS Failure
	$0000\ 0010_H$	Transmitting DS3/E3 AIS
	$0000\ 0020_H$	Receiving DS3/E3 LOF Failure
	$0000\ 0040_H$	Receiving DS3/E3 LOS Failure
	$0000\ 0080_H$	Remote Loop active
	$0000\ 0100_H$	Recognizing Test Pattern (BERT)
	$0000\ 0200_H$	Other Failure
	$0000\ 0400_H$	Unavailable State (UAS)
	$0000\ 0800_H$	Out Of Service (OOS)
	$0000\ 4000_H$	Unavailable State Far-End (UAS-FE)
	$0000\ 8000_H$	DS3 Framer in M23 Mode (0: C-bit parity)

Command ID: **CMD_GET_STATUS** (cont'd)

0001 0000$_H$	Receiving DS3/E3 AIS Defect
0002 0000$_H$	Receiving DS3/E3 OOF Defect
0004 0000$_H$	Receiving DS3/E3 RDI Defect
0008 0000$_H$	Receiving DS3/E3 LOS Defect
0010 0000$_H$	Receiving IDLE Pattern
0020 0000$_H$	Transmitting IDLE Pattern
0040 0000$_H$	Local Loop active
0080 0000$_H$	Transmitting LOS (No Output Signal)
0100 0000$_H$	Receiving E3 G.832 Trail Trace Mismatch
0200 0000$_H$	Receiving E3 G.832 PTY "Unequipped"
0400 0000$_H$	Receiving E3 G.832 PTY Mismatch
0800 0000$_H$	Receiving E3 G.832 SSM Mismatch
1000 0000$_H$	Receive G.804 lost cell delineation (LCD)
2000 0000$_H$	Receiving PLCP OOF Defect
4000 0000$_H$	Receiving PLCP Remote Alarm (RAI)
8000 0000$_H$	Transmitting PLCP Remote Alarm (RAI)

6.3.7.3 Statistics Messages

To support performance measurement statistics, several performance counters are realized in TE3-FALC. These counters can be requested anytime with a single message **CMD_GET_STATISTICS** (page 149). It is possible to provide the total count since the last clearing of counters ("TOTAL") and/or the count of the last completed 1-second ("1SEC") interval. **Figure 29** illustrates the accumulation of counts over several seconds and the Read & Clear operation on the total count. The value of the 1-second count is updated periodically every second.

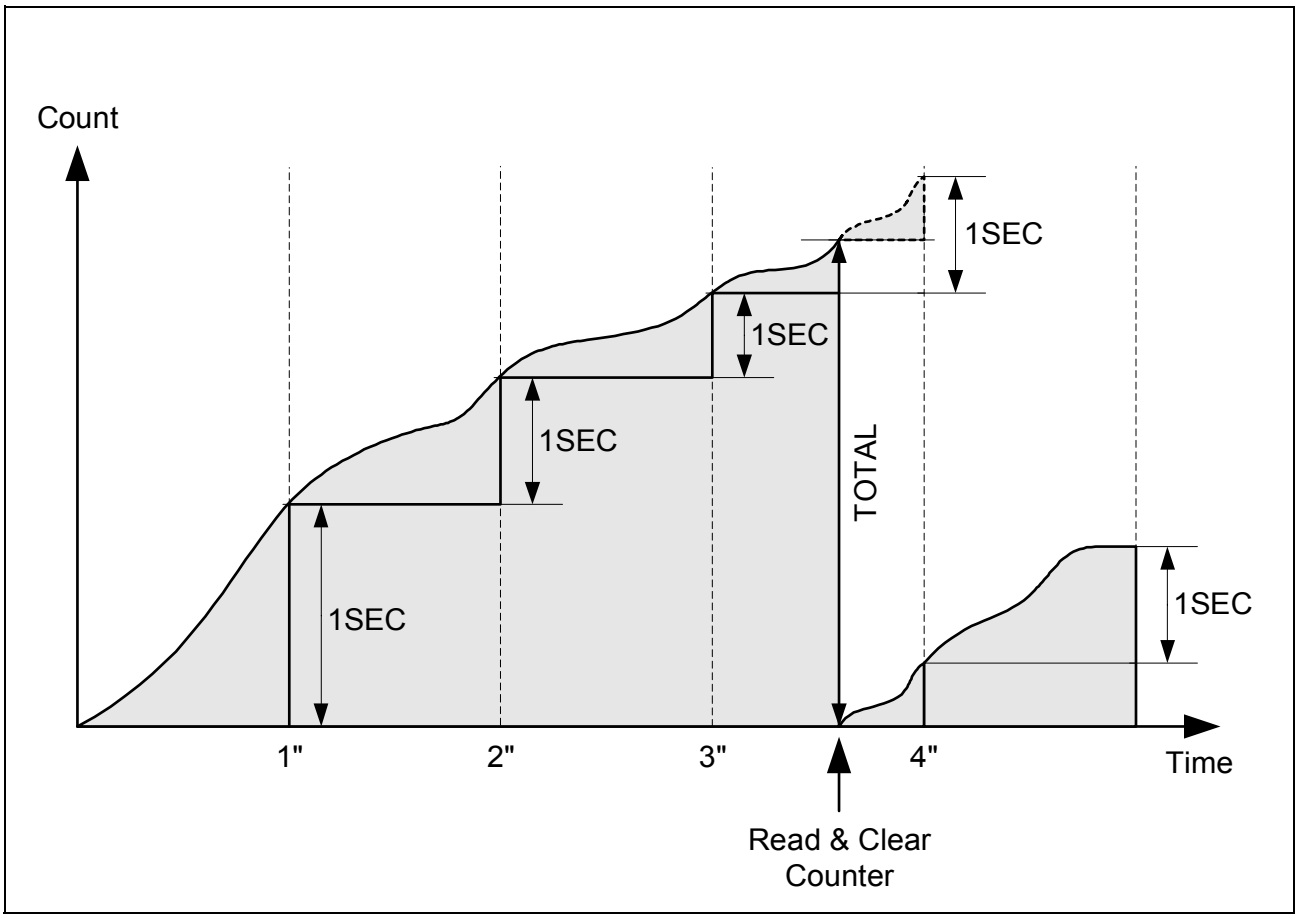


Figure 29 Statistics Counter Operation

The implemented performance counters are listed in Table 43, Table 44, Table 45, Table 46 and Table 47. Reporting of the counter values is performed in the order they are listed.

Table 43 DS3/E3 Framer Performance Counters

Word	Name	Near-/ Far-end	Counter Value	Counter Type
0	PES	NE	DS3/E3: P-bit Errored Seconds	1-sec interval
1	PSES	NE	DS3/E3: P-bit Severely Errored Seconds	1-sec interval
2	SEFS	NE	DS3/E3: Severely Errored Frame Seconds	1-sec interval
3	UAS	NE	DS3/E3: Unavailable Seconds	1-sec interval
4	LCV	NE	DS3/E3: Line Coding Violations	Hardware
5	PCV	NE	DS3: P-bit Coding Violations E3: BIP-8 errors	Hardware
6	LES	NE	DS3/E3: Line Errored Seconds	1-sec interval
7	CCV	NE	DS3: C-bit Coding Violations	Hardware
8	CES	NE	DS3: C-bit Errored Seconds	1-sec interval
9	CSES	NE	DS3: C-bit Severely Errored Seconds	1-sec interval
10	FAE	NE	DS3/E3: Frame Alignment errors	Hardware
11	OOF	NE	DS3/E3: OOF defects	Software
12	LOS	NE	DS3/E3: LOS defects	Software
13	BCV	NE	DS3/E3: Bipolar Coding Violations	Hardware
14	EXZ	NE	DS3/E3: Excessive Zeros	Hardware
15	CCV	FE	DS3: Far end block errors E3: Remote error indications	Hardware
16	CES	FE	DS3: C-bit Errored Seconds	1-sec interval
17	CSES	FE	DS3: C-bit Severely Errored Seconds	1-sec interval
18	UAS	FE	DS3/E3: Unavailable Seconds	1-sec interval
19	RDI	FE	DS3/E3: Received RDI errors	Software

Table 44 PLCP Performance Counters

Word	Name	Near-/ Far-end	Counter Value	Counter Type
0	PLCP_SEFS	- NE	PLCP Severely Errored Frame Seconds	1-sec interval
1	PLCP_UAS	- NE	PLCP Unavailable Seconds	1-sec interval
2	PLCP_FAE	- NE	PLCP Frame Alignment errors	Hardware
3	PLCP_BIPE	- NE	PCLP BIP-8 errors	Hardware
4	PLCP_OOF	- NE	PLCP OOF defects	Software
5	PLCP_FEBE	- FE	PLCP Far end block errors (FEBE)	Hardware
6	PLCP_RAI	- FE	PLCP RAI errors	Software

Table 45 ATM TC-Layer Performance Counters

Word	Counter Value	Counter Type
0	Loss of Cell Delineation (LCD) events	Software
1	Uncorrectable HEC errors	Hardware
2	HEC corrections	Hardware
3	Received user cells	Hardware
4	Received idle cells	Hardware
5	Received bytes	Software
6	Transmitted user cells	Hardware
7	Transmitted idle cells	Hardware
8	Transmitted bytes	Software
9	Buffer Overflow Events	Software

Table 46 HDLC Performance Counters

Word	Counter Value	Counter Type
0	Received errored packets	Hardware
1	CRC errored packets	Hardware
2	Misaligned packets (bitcount of packet not multiple of 8 bits)	Hardware

Table 46 HDLC Performance Counters (cont'd)

Word	Counter Value	Counter Type
3	Too long packets	Hardware
4	Too short packets	Hardware
5	Bad PPP address fields	Hardware
6	Bad PPP control fields	Hardware
7	Overflown packets (rx packets aborted due to buffer overflow)	Software
8	Received valid packets	Hardware
9	Received bytes	Hardware
10	Underflown packets (tx packets aborted due to buffer underrun)	Software
11	Transmitted valid packets	Hardware
12	Transmitted bytes	Hardware

Table 47 BERT Performance Counters

Word	Counter Value	Counter Type
0	Receive Bit Counter	Hardware
1	Receive Error Counter	Hardware

Command ID: **CMD_GET_STATISTICS**

This message causes the firmware to control the reporting of the provided Performance Counters.

Input Parameters (optional)

Parameter ID	Value	Description
STAT_FRAMR_TOTAL$_P$	_RPT	Report Total-Counts for Framer statistics, do NOT clear counters (refer to **Table 43**)
	_RPT_CLEAR	Report Total-Counts for Framer statistics and clear counters
	_NO_RPT	Do not report Total-Counts of Framer statistics
STAT_FRAMR_1SEC$_P$	_RPT	Get counts of Framer statistics for the last completed 1-second interval
	_NO_RPT	Do not get counts of Framer statistics for the last 1-second interval
STAT_FRAMR_T1231$_P$	_RPT	Report 10-second delayed counts for ANSI T1.231 compliant Framer statistics, do NOT clear counters (refer to **Table 43**)
	_RPT_CLEAR	Report 10-second delayed counts for Framer statistics and clear counters
	_NO_RPT	Do not report 10-second delayed counts of Framer statistics
STAT_PLCP_TOTAL$_P$	*as above*	*as above, for PLCP Mapper (refer to **Table 44**)*
STAT_PLCP_1SEC$_P$	*as above*	
STAT_ATM_TOTAL$_P$	*as above*	*as above, for ATM TC-Sublayer (refer to **Table 45**)*
STAT_ATM_1SEC$_P$	*as above*	
STAT_HDLC_TOTAL$_P$	*as above*	*as above, for HDLC Protocol (refer to **Table 46**)*
STAT_HDLC_1SEC$_P$	*as above*	
STAT_BERT_TOTAL$_P$	*as above*	*as above, for Bit Error Rate Tester BERT (refer to **Table 47**)*
STAT_BERT_1SEC$_P$	*as above*	

Command ID: **CMD_GET_STATISTICS** (cont'd)

Acknowledgement ID: **ACK_GET_STATISTICS**

If activated, this acknowledgement is sent out when the command has been processed. This message provides Performance Counters, when requested so by the host via **CMD_GET_STATISTICS** message.

Output Parameters		
$STAT\_TIMESTAMP_P$	*16-bit field*	Continuous running time stamp that increments every second (wrapping from $FFFF_H$ to 0000_H). This allows to align the TE3-FALC's internal 1-second tick with the host's 1-second timer.
$RPT\_FRAMR\_TOTAL_{32}$	*20 × 32-bit array*	The statistics report consists of several 32-bit parameter arrays which are reported if requested so by command message **CMD_GET_STATISTICS**. E.g., parameter array "RPT_FRAMR_TOTAL" contains a report of the total count of all seven 32-bit wide Framer performance counters in the order listed in **Table 43** (analogue for the PLCP, ATM, HDLC and BERT).
$RPT\_FRAMR\_1SEC_{32}$	*20 × 32-bit array*	
$RPT\_FRAMR\_T1231_{32}$	*20 × 32-bit array*	
$RPT\_PLCP\_TOTAL_{32}$	*7 × 32-bit array*	
$RPT\_PLCP\_1SEC_{32}$	*7 × 32-bit array*	
$RPT\_ATM\_TOTAL_{32}$	*10 × 32-bit array*	
$RPT\_ATM\_1SEC_{32}$	*10 × 32-bit array*	
$RPT\_HDLC\_TOTAL_{32}$	*13 × 32-bit array*	
$RPT\_HDLC\_1SEC_{32}$	*13 × 32-bit array*	
$RPT\_BERT\_TOTAL_{32}$	*2 × 32-bit array*	
$RPT\_BERT\_1SEC_{32}$	*2 × 32-bit array*	

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	-40 to +85	°C
Storage temperature	T_{stg}	-65 to +125	°C
Core supply voltage	V_{DD}	-0.4 to 1.89	V
I/O supply voltage Analog PLL supply voltage Analog LIU supply voltage	V_{DDP} V_{DDPLL} V_{DDA}	-0.4 to 3.6	V
Voltage on any pin with respect to ground	V_S	-0.4 to 3.6	V
ESD robustness[1)] HBM: 1.5 kΩ, 100 pF	$V_{ESD,HBM}$	1000	V

1) According to MIL-Std 883D, method 3015.7 and ESD Ass. Standard EOS/ESD-5.1-1993.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Ambient temperature	T_A	-40	85	°C	
Core supply voltage	V_{DD}	1.71	1.89	V	
I/O supply voltage Analog PLL supply voltage Analog LIU supply voltage	V_{DDP} V_{DDPLL} V_{DDA}	3.0	3.6	V	

Note: In the operating range, the functions given in the circuit description are fulfilled.

7.3 Thermal Package Characteristics

Parameter	Symbol	Value	Unit	Test conditions
Thermal package resistance junction to ambient without airflow	$R_{JA(0,25)}$	tbd.	°C/W	T_A = 25 °C

7.4 DC Characteristics

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input low voltage	V_{IL}	-0.4	0.8	V	
Input high voltage	V_{IH}	2.0	3.6	V	
Maximum analog input voltage	$V_{I,ana}$		5.25	V	Applies to analog pins RL1/RL2 and XL1/XL2
Output low voltage	V_{OL}		0.4	V	I_{sink} = 4 mA[1)]
Output high voltage	V_{OH}	2.4		V	I_{source} = 4 mA
Avg. V_{DD} (nom. 1.8 V) power supply current	I_{CC}		550	mA	Mean current flow under worst case conditions.
Avg. V_{DDP} + V_{DDA} + V_{DDPLL} (nom. 3.3 V) power supply current	I_{CCP}		150	mA	
Input leakage current	I_{IL}		1.5	µA	
Output leakage current	I_{OL}		1	µA	
Source current of output pins	$I_{source,B}$	20		mA	V_{OH} = 2.4 V
	$I_{source,C}$	12		mA	
	$I_{source,D}$	8		mA	
	$I_{source,E}$	4		mA	
Sink current of output pins	$I_{sink,B}$	16		mA	V_{OL} = 0.4 V
	$I_{sink,C}$	10		mA	
	$I_{sink,D}$	6		mA	
	$I_{sink,E}$	4		mA	
Pull Up Current	I_{PU}	3.3	9.5	µA	V_{IL} = V_{SS}
Pull Down Current	I_{PD}	3	14	µA	V_{IH} = V_{DDP}

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Analog transmitter leakage current	$I_{OL,XL}$		1	mA	XL1/2 = V_{DDA} or XL1/2 = V_{SS}
Analog transmitter output impedance	R_{XL}	5 (typ.)		Ω	
Transmit differential peak voltage of mark (XL1/XL2)	V_X		2.0	V	
Receive differential peak voltage of mark (RL1/RL2)	V_R		V_{DDA}+0.3	V	
Receiver input impedance (RL1/RL2)	Z_R	tbd.[2]		kΩ	
Receiver sensitivity (RL1/RL2)	S_{RSH}	0	tbd.	dB	
Analog loss of signal threshold E3	$V_{LOS,E3}$	-35	-15	dB	

[1] applies to all digital output pins; not for XL1/XL2

[2] parameter not tested in production

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

7.5 AC Characteristics

T_A = -40 to 85 °C, V_{DDP} = V_{DDA} = V_{DDPLL} = 3.3 V ± 10%, V_{DD} = 1.8 V ± 5%, V_{SS} = 0 V

All outputs are measured at V_{TH} = 2.0 V for a logical “1”and
at V_{TL} = 0.8 V for a logical “0”

All inputs are driven to V_{IH} = 2.4 V for a logical “1” and
to V_{IL} = 0.4 V for a logical “0”

The AC testing input/output waveforms are shown below.

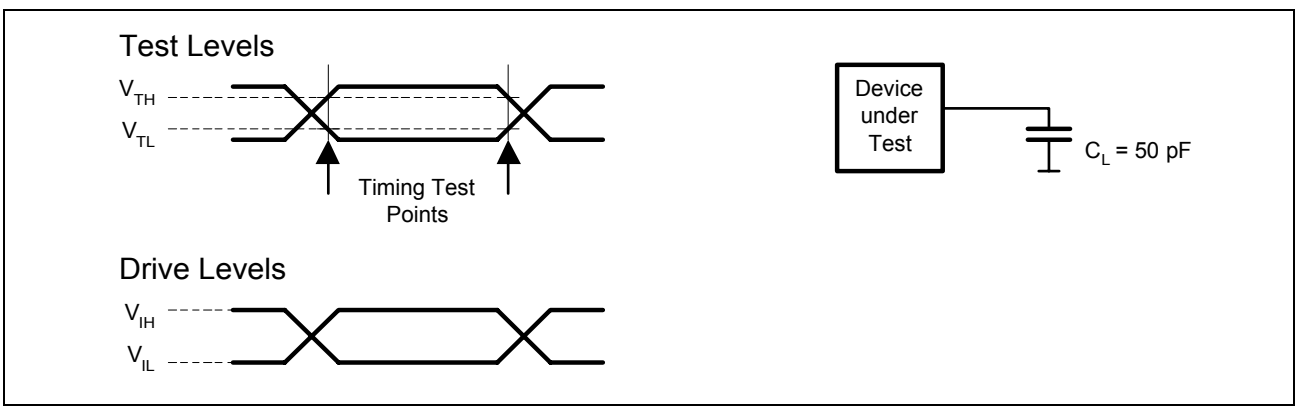


Figure 30 Input/Output Waveforms for AC Measurements

7.5.1 Microprocessor Interface

Some timings of the microprocessor interface refer to T_{SYS}. This is the period of the system clock which is in a range of 16 to 17 ns (58 to 60 MHz) during operation.

As long as the PLL is not programmed properly (during boot-up), the system clock frequency can be between 25 and 50 MHz.

7.5.1.1 Intel Demux Mode

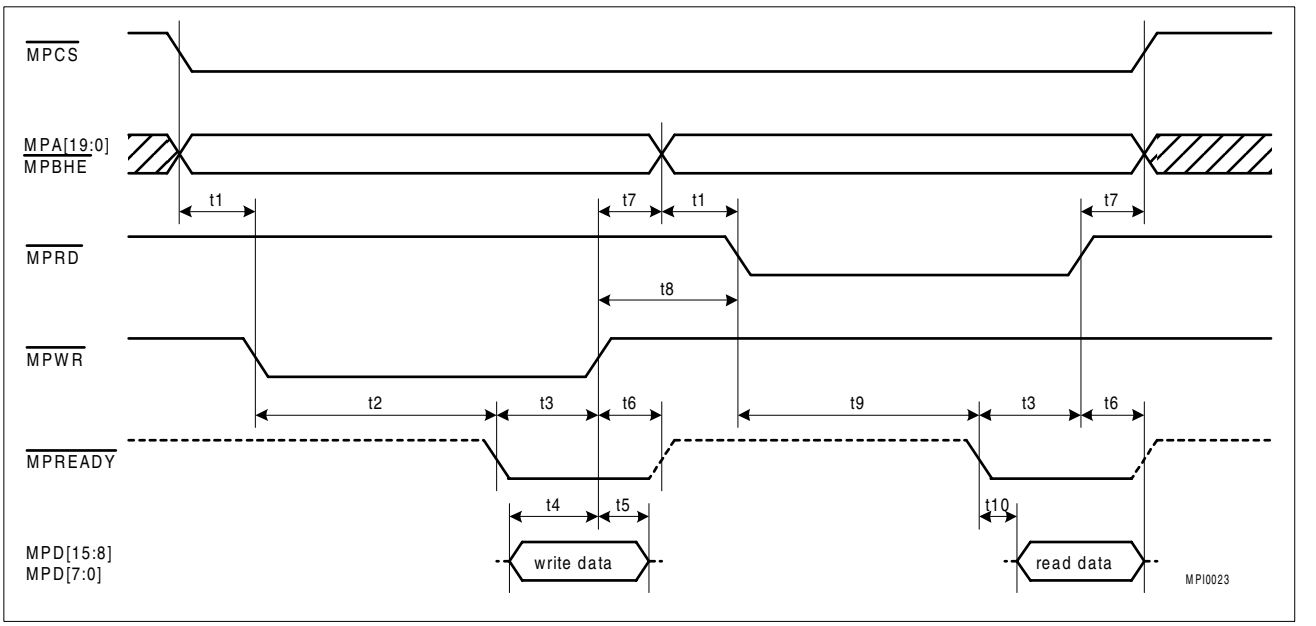


Figure 31 Intel Demux Mode Write/Read Timing

Table 48 Timings for Intel Demux Mode

Timing	Description	Limit Values		Unit
		min.	max.	
t1	$\overline{\text{MPCS}}$, MPA/$\overline{\text{MPBHE}}$ setup to $\overline{\text{MPWR}}$/$\overline{\text{MPRD}}$	0		ns
t2	$\overline{\text{MPWR}}$ to $\overline{\text{MPREADY}}$ delay	1.5 T_{SYS}	10+2.5 T_{SYS} [1)]	ns
t3	$\overline{\text{MPWR}}$/$\overline{\text{MPRD}}$ delay after $\overline{\text{MPREADY}}$	0		ns
t4	MPD setup to $\overline{\text{MPWR}}$	10		ns
t5	MPD hold from $\overline{\text{MPWR}}$	10		ns
t6	$\overline{\text{MPREADY}}$ and read MPD hold/inactive after $\overline{\text{MPWR}}$/$\overline{\text{MPRD}}$	5	15	ns
t7	$\overline{\text{MPCS}}$, MPA/$\overline{\text{MPBHE}}$ hold from $\overline{\text{MPWR}}$/$\overline{\text{MPRD}}$	0		ns
t8 [2)]	$\overline{\text{MPWR}}$ to $\overline{\text{MPWR}}$, $\overline{\text{MPRD}}$ to $\overline{\text{MPRD}}$, $\overline{\text{MPWR}}$ to $\overline{\text{MPRD}}$ and $\overline{\text{MPRD}}$ to $\overline{\text{MPWR}}$ inactive time	5+T_{SYS}		ns
t9	$\overline{\text{MPRD}}$ to $\overline{\text{MPREADY}}$ delay	3.5 T_{SYS} [3)]	10+4.5 T_{SYS} [1)]	ns
t10	delay between $\overline{\text{MPREADY}}$ and read MPD driven and stable	-T_{SYS}	0	ns

1) Only applicable when destination address is located at RAM interface. In case of accessing other internal registers or memories additional clock periods can occur according to the availability of internal ressources.

2) not tested in production

3) Only when destination address is located at RAM interface. In case of other addresses minimum is 4.5 T_{SYS}.

7.5.1.2 Motorola Asynchronous Mode

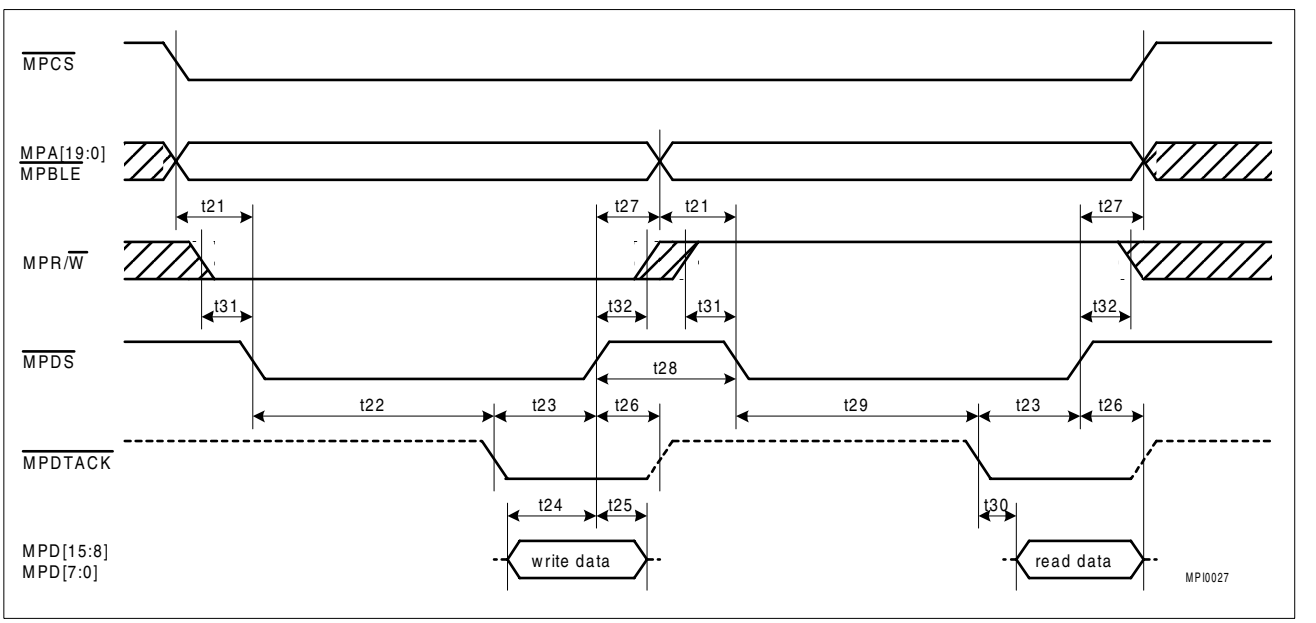


Figure 32 Asynchronous Motorola Mode Write/Read Timing

Table 49 Timings for Asynchronous Motorola Mode

Timing	Description	Limit Values		Unit
		min.	max.	
t21	$\overline{\text{MPCS}}$, MPA/$\overline{\text{MPBLE}}$ setup to $\overline{\text{MPDS}}$	0		ns
t22	$\overline{\text{MPDS}}$ to $\overline{\text{MPDATCK}}$ delay in case of write	1.5 T_{SYS}	10+2.5 T_{SYS} [1)]	ns
t23	$\overline{\text{MPDS}}$ delay after $\overline{\text{MPDTACK}}$	0		ns
t24	write MPD setup to $\overline{\text{MPDS}}$	10		ns
t25	write MPD hold from $\overline{\text{MPDS}}$	10		ns
t26	$\overline{\text{MPDTACK}}$ and read MPD hold/inactive after $\overline{\text{MPDS}}$	5	15	ns
t27	$\overline{\text{MPCS}}$, MPA/$\overline{\text{MPBLE}}$ hold from $\overline{\text{MPDS}}$	0		ns
t28 [2)]	$\overline{\text{MPDS}}$ inactive time	5+T_{SYS}		ns

Table 49 Timings for Asynchronous Motorola Mode (cont'd)

Timing	Description	Limit Values		Unit
		min.	max.	
t29	$\overline{\text{MPDS}}$ to $\overline{\text{MPDTACK}}$ delay in case of read	$3.5T_{SYS}$ 3)	$10+4.5$ T_{SYS} 1)	ns
t30	delay between $\overline{\text{MPDTACK}}$ and read MPD driven and stable	$-T_{SYS}$	0	ns
t31	MPR/$\overline{\text{W}}$ setup to $\overline{\text{MPDS}}$	10		ns
t32	MPR/$\overline{\text{W}}$ hold from $\overline{\text{MPDS}}$	10		ns

1) Only applicable when destination address is located at RAM interface. In case of accessing other internal registers or memories additional clock periods can occur according to the availability of internal ressources.

2) not tested in production

3) Only when destination address is located at RAM interface. In case of other addresses minimum is 4.5 T_{SYS}.

7.5.1.3 Motorola Synchronous Mode

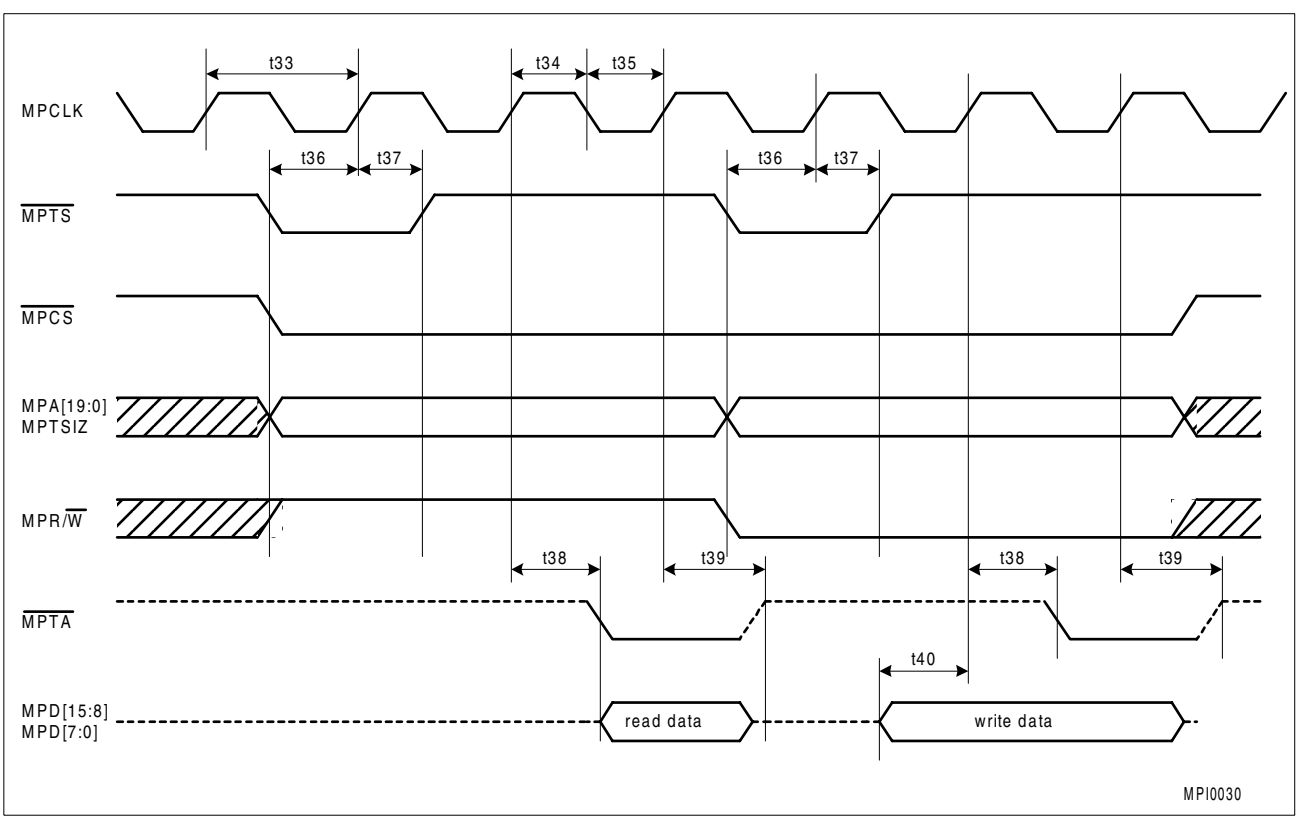


Figure 33 Synchronous Motorola Mode Write/Read Timing

Please refer to the MPC860 specification for the synchronous Motorola mode timing. All given timings fit directly to the MPC860 timing specification.

Table 50 Timings for Synchronous Motorola Mode

Timing	Description	Limit Values		Unit
		min.	max.	
t33	MPCLK period	20		ns
t34	MPCLK high period	8		ns
t35	MPCLK low period	8		ns
t36	$\overline{\text{MPTS}}$, $\overline{\text{MPCS}}$, MPA/MPTSIZ, MPR/$\overline{\text{W}}$ setup to MPCLK rising	8.25		ns
t37	$\overline{\text{MPTS}}$, $\overline{\text{MPCS}}$, MPA/MPTSIZ, MPR/$\overline{\text{W}}$ hold from MPCLK rising	5		ns
t38	$\overline{\text{MPTA}}$, MPD delay after MPCLK high	1	10.25	ns
t39	$\overline{\text{MPTA}}$, MPD deasserted to tristate after MPCLK rising	1	10.25	ns
t40	write MPD setup to MPCLK rising	8.25		ns

7.5.2 UTOPIA Interface

The AC characteristics of the UTOPIA interface fulfills the ATM Forum “UTOPIA level 2 Specification, Version 1.0" as defined for the interface running at 50 MHz.

The setup and the hold times are defined with regard to a positive clock edge, see **Figure 34**. The maximum output delays are chosen such that they fulfill the setup time requirements of the receiveing device, including some margin.

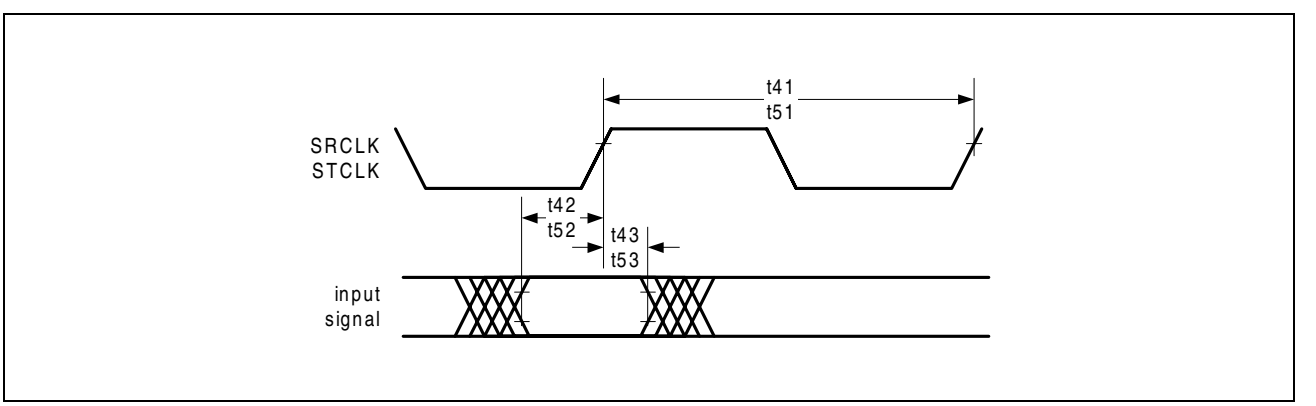


Figure 34 UTOPIA / POS-PHY / UTOPIA-L2X Clock and Input Signal Timing

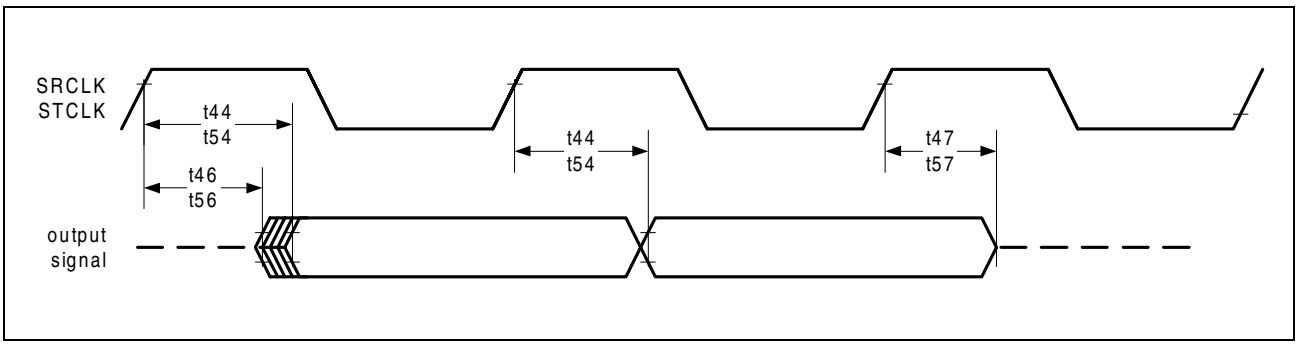


Figure 35 UTOPIA / POS-PHY / UTOPIA-L2X Output Signal Timing

Table 51 Transmit UTOPIA / POS-PHY / UTOPIA-L2X Timing

No.	Signal Name	Description	Limit Values		Unit
			min.	max.	
t41	STCLK	STCLK frequency (nominal)	0	50	MHz
		STCLK duty cycle	40	60	%
		STCLK peak-to-peak jitter		5	%
		STCLK rise/fall time		2	ns
t42	STD(15:0), STPRTY, STSX, STSOP, STEOP, $\overline{\text{STERR}}$, STMOD, $\overline{\text{STENB}}$, STADDR(4:0)	Input setup to STCLK	4		ns
t43		Input hold from STCLK	1		ns
t44	STPA, STRDY	STCLK to output valid delay	1	14	ns
t46		STCLK to output going low impedance	1		ns
t47		STCLK to output going high impedance	1	14	ns

Table 52 Receive UTOPIA / POS-PHY / UTOPIA-L2X Timing

No.	Signal Name	Description	Limit Values		Unit
			min.	max.	
t51	SRCLK	SRCLK frequency (nominal)	0	50	MHz
		SRCLK duty cycle	40	60	%
		SRCLK peak-to-peak jitter		5	%
		SRCLK rise/fall time		2	ns

Table 52 Receive UTOPIA / POS-PHY / UTOPIA-L2X Timing (cont'd)

No.	Signal Name	Description	Limit Values		Unit
			min.	max.	
t52	$\overline{\text{SRENB}}$, SRADDR(4:0)	Input setup to SRCLK	4		ns
t53		Input hold from SRCLK	1		ns
t54	SRPA, SRD(15:0), SRVAL, SRPRTY, SRSX, SRSOP, SREOP, SRERR, SRMOD	SRCLK to output valid delay	1	14	ns
t56		SRCLK to output going low impedance	1		ns
t57		SRCLK to output going high impedance	1	14	ns

7.5.3 Serial Data Interfaces Timing

7.5.3.1 Digital Line Interface Timing

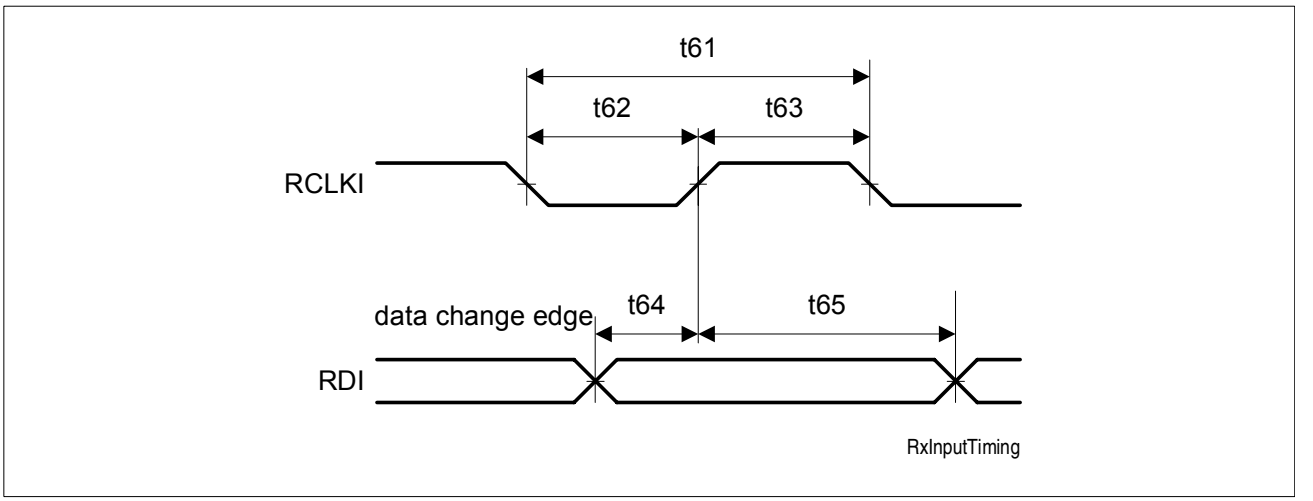


Figure 36 Digital Receive Line Input Timing

Table 53 RCLKI/RDI Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
t61	RCLKI period E3		29.1		ns
	RCLKI period DS3		22.4		ns
t62	RCLKI high		50		%
t63	RCLKI low		50		%
t64	RDI setup time	5			ns
t65	RDI hold time	5			ns

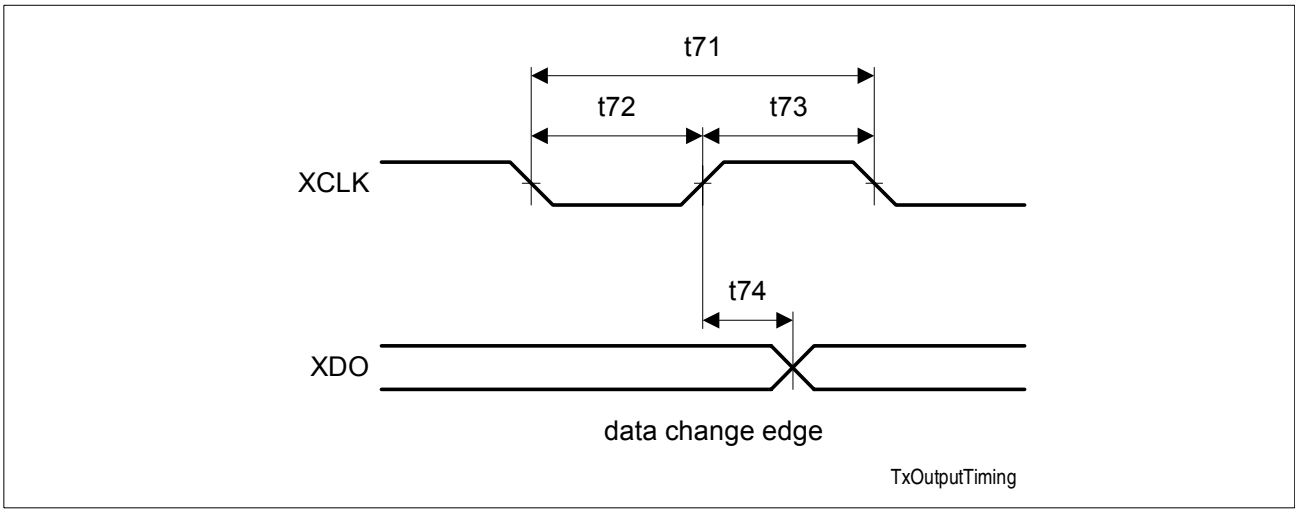


Figure 37 Digital Transmit Line Output Timing

Table 54 XCLK/XDO Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
t71	XCLK period E3		29.1		ns
	XCLK period DS3		22.4		ns
t72	XCLK high	40	50	60	%
t73	XCLK low	40	50	60	%
t74	XDO delay time			14	ns

7.5.3.2 Bitstream Access Interface Timing

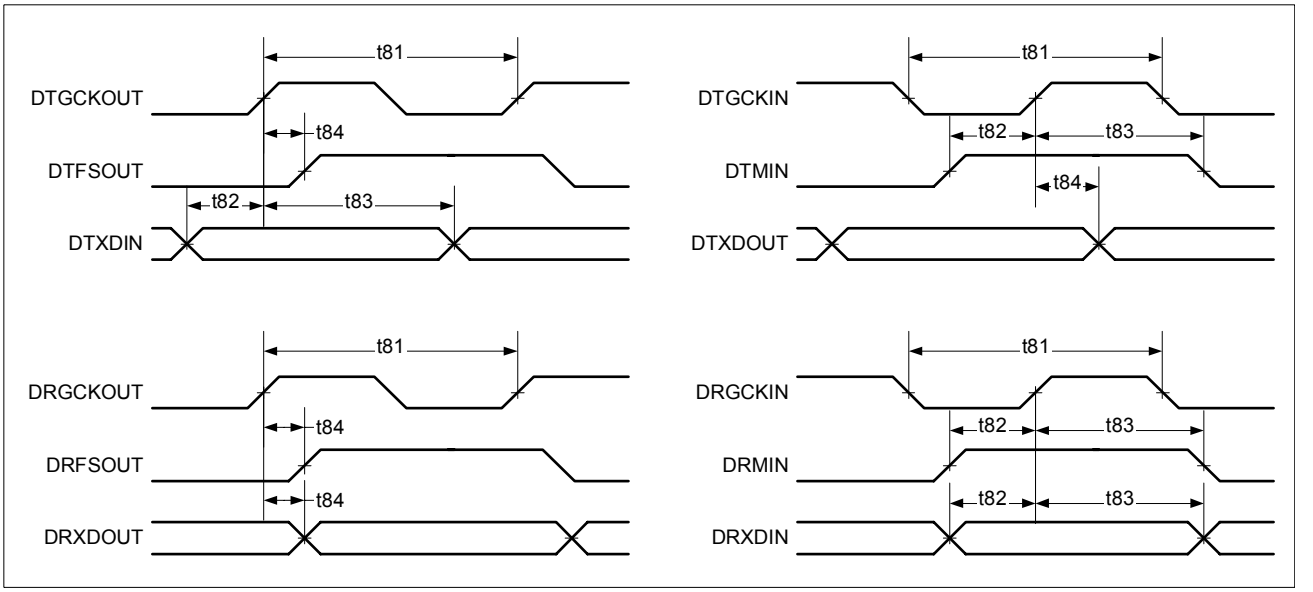


Figure 38 Bitstream Access Interface Timing

Table 55 Bitstream Access Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
t81	DTCGKOUT, DTGCKIN, DRGCKOUT, DRGCKIN clock period (E3)		29.1		ns
	DTCGKOUT, DTGCKIN, DRGCKOUT, DRGCKIN clock period (DS3)		22.4		ns
t82	DTXDIN, DTMIN, DRMIN, DRXDIN setup time	5			ns
t83	DTXDIN, DTMIN, DRMIN, DRXDIN hold time	5			ns
t84	DTFSOUT, DTXDOUT, DRFSOUT, DRXDOUT delay			14	ns

7.5.3.3 DS3/E3 Overhead Access Interface Timing

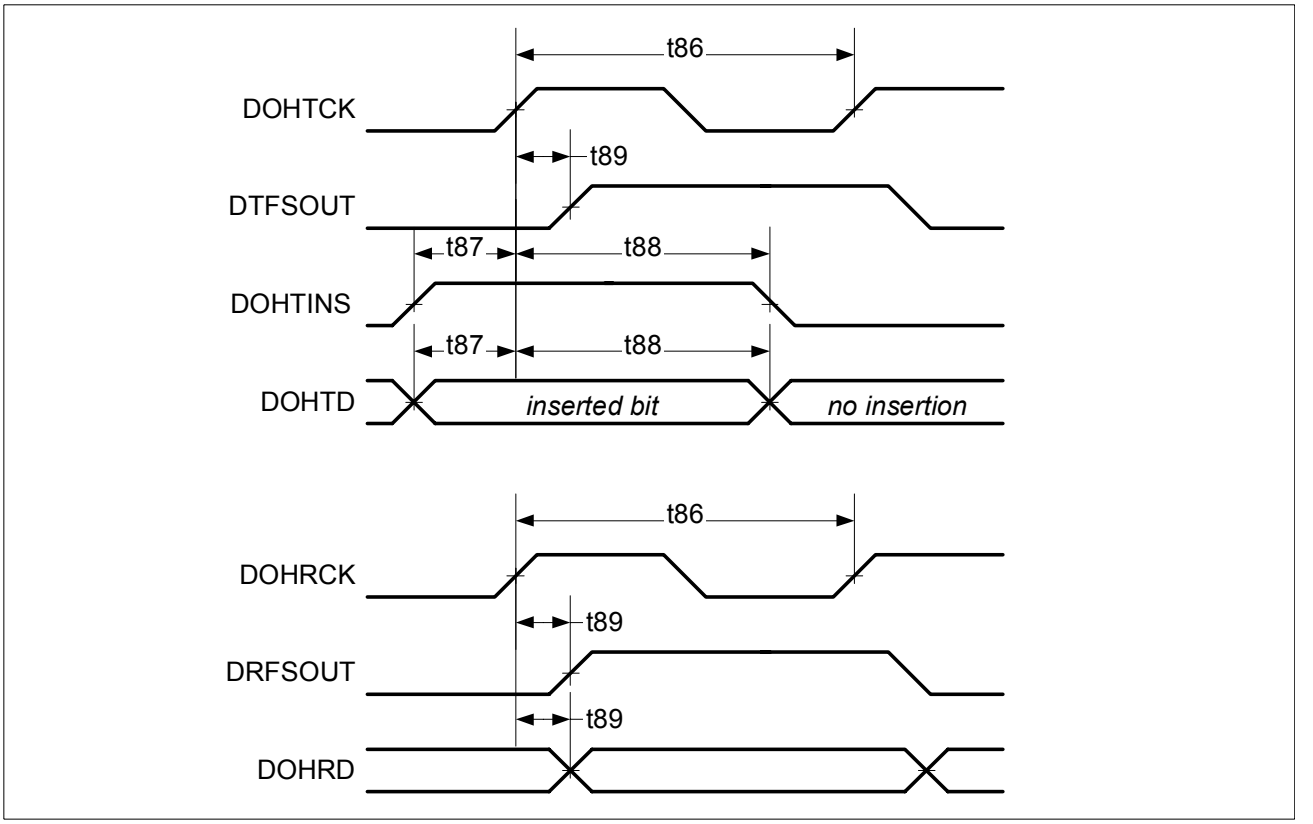


Figure 39 Overhead Access Interface Timing

Table 56 Overhead Access Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
t86	DOHTCK, DOHRCK clock period (DS3, E3)		1.9		µs
t87	DOHTINS, DOHTD setup time	5			ns
t88	DOHTINS, DOHTD hold time	5			ns
t89	DTFSOUT, DRFSOUT, DOHRD delay			20	ns

7.5.4 Reset Timing

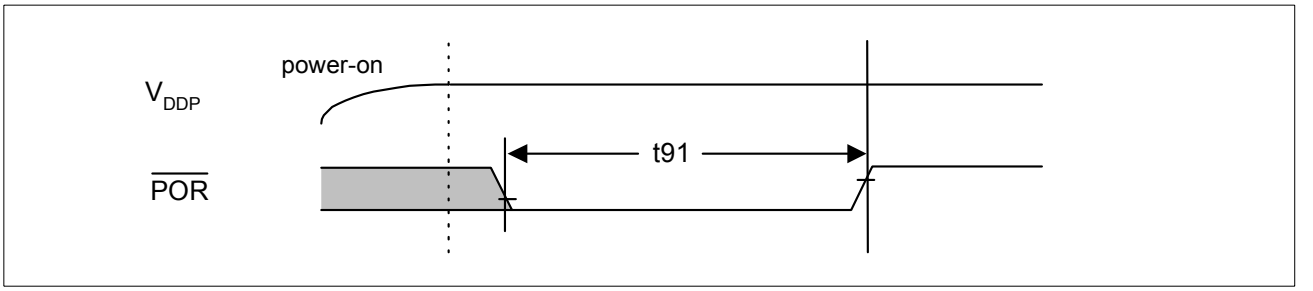


Table 57 Reset Timing

Number	Parameter	Limit Values			Unit
		min.	typ.	max.	
t91	$\overline{\text{POR}}$ pulse width	500			ns

7.5.5 Main Clock (CLKIN) Timing

Table 58 CLKIN Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
t101	CLKIN period	19.2		250	ns
	CLKIN frequency	4		52	MHz
	CLKIN Clock accuracy			20	ppm

7.5.6 JTAG Interface

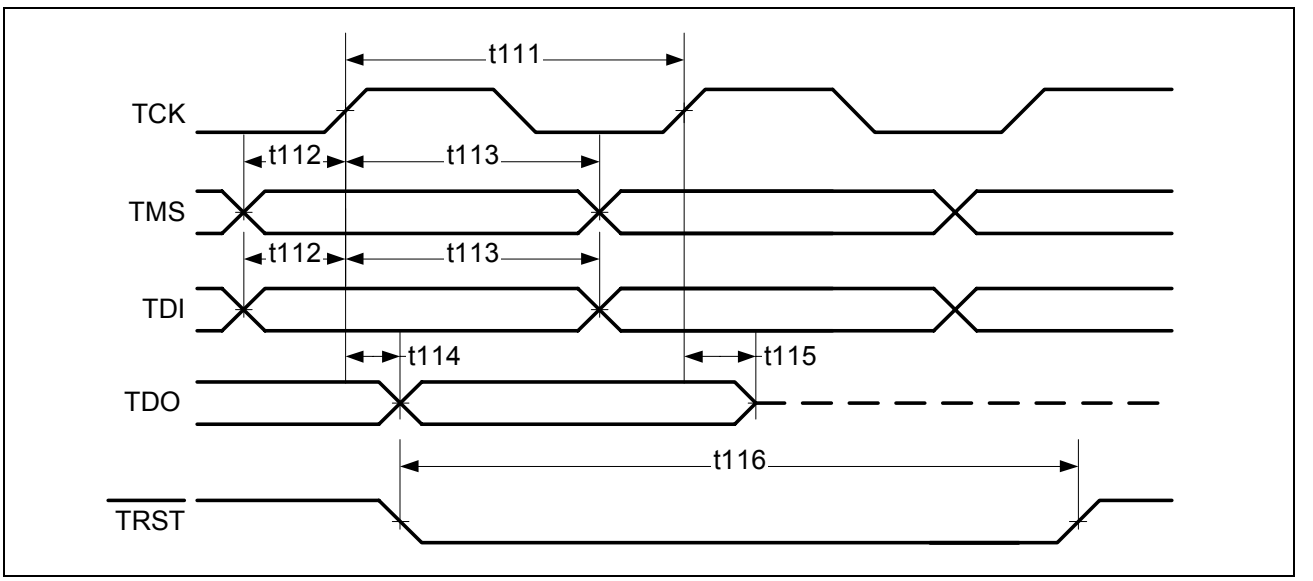


Figure 40 Boundary-Scan Test Interface Timing Diagram

Table 59 Boundary-Scan Test Interface AC Timing Characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
t111	T_{TCK}: Period TCK	160			ns
	F_{TCK}: Frequency TCK			6,25	MHz
t112	Setup time TMS, TDI before TCK rising	10			ns
t113	Hold time TMS, TDI after TCK rising	10			ns
t114	Delay TCK falling to TDO valid	0		30	ns
t115	Delay TCK falling to TDO high impedance	0		30	ns
t116	Pulse width $\overline{\text{TRST}}$ low	$2 \times T_{TCK}$			ns

7.5.7 Analog Line Interface

7.5.7.1 Pulse Template E3

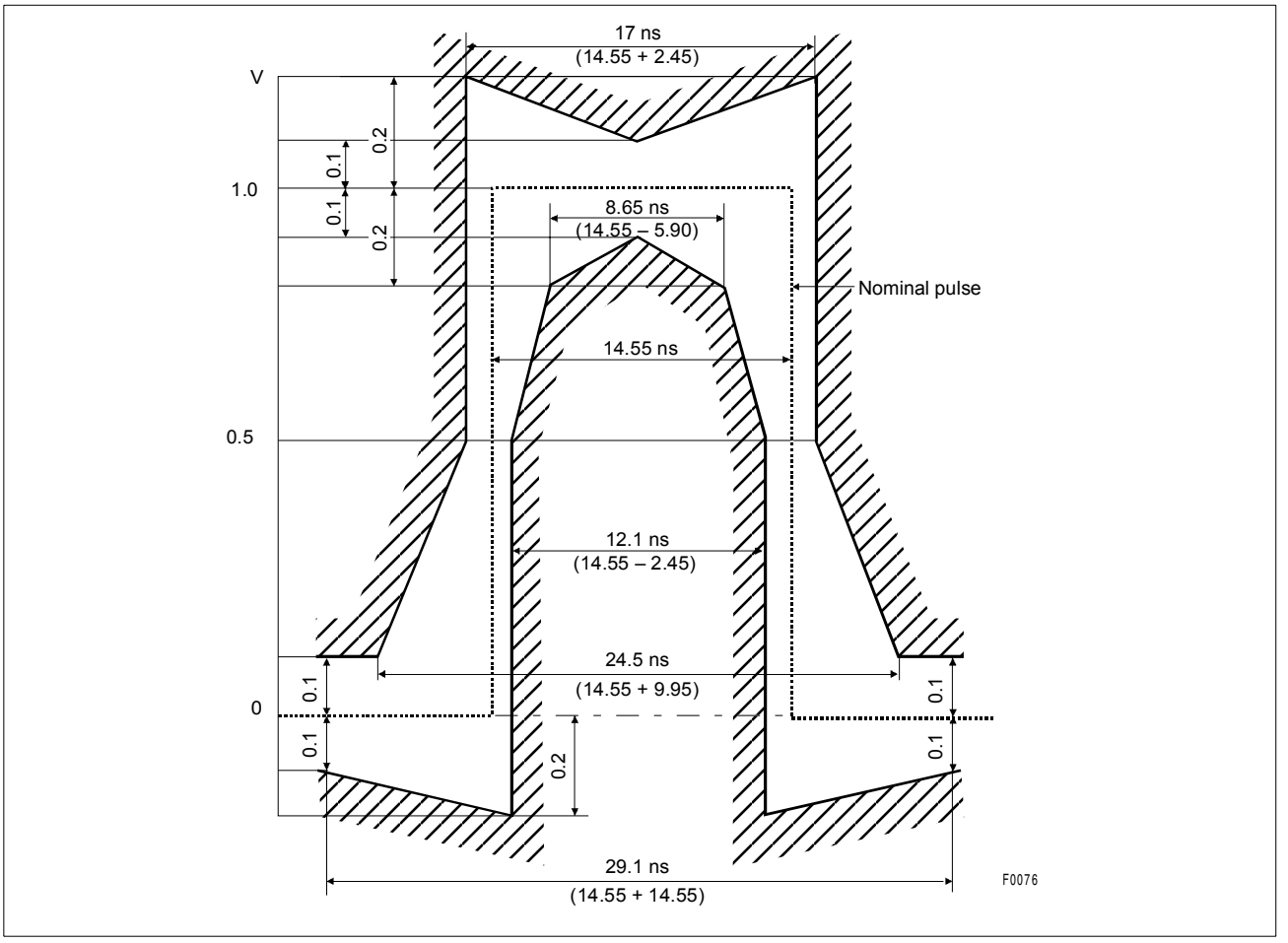


Figure 41 E3 Pulse Shape at Transmitter Output

Table 60 E3 Pulse Mask[1)]

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
	Nominal peak voltage of a mark (pulse)		1.0		V
	Peak voltage of a space (no pulse)	- 0.1		0.1	V
	Nominal pulse width		14.55		ns
	Amplitude ratio of positive to negative pulses[2)]	0.95		1.05	
	Pulse width ratio of positive to negative pulses[3)]	0.95		1.05	

1) measured at the output port without transmission line and 75Ω load;
bit sequence: 0000000(+1)0000000(-1)0000000(+1)0000000(-1)...

2) at the center of a pulse interval

3) at the nominal half amplitude

7.5.7.2 Pulse Template DS3

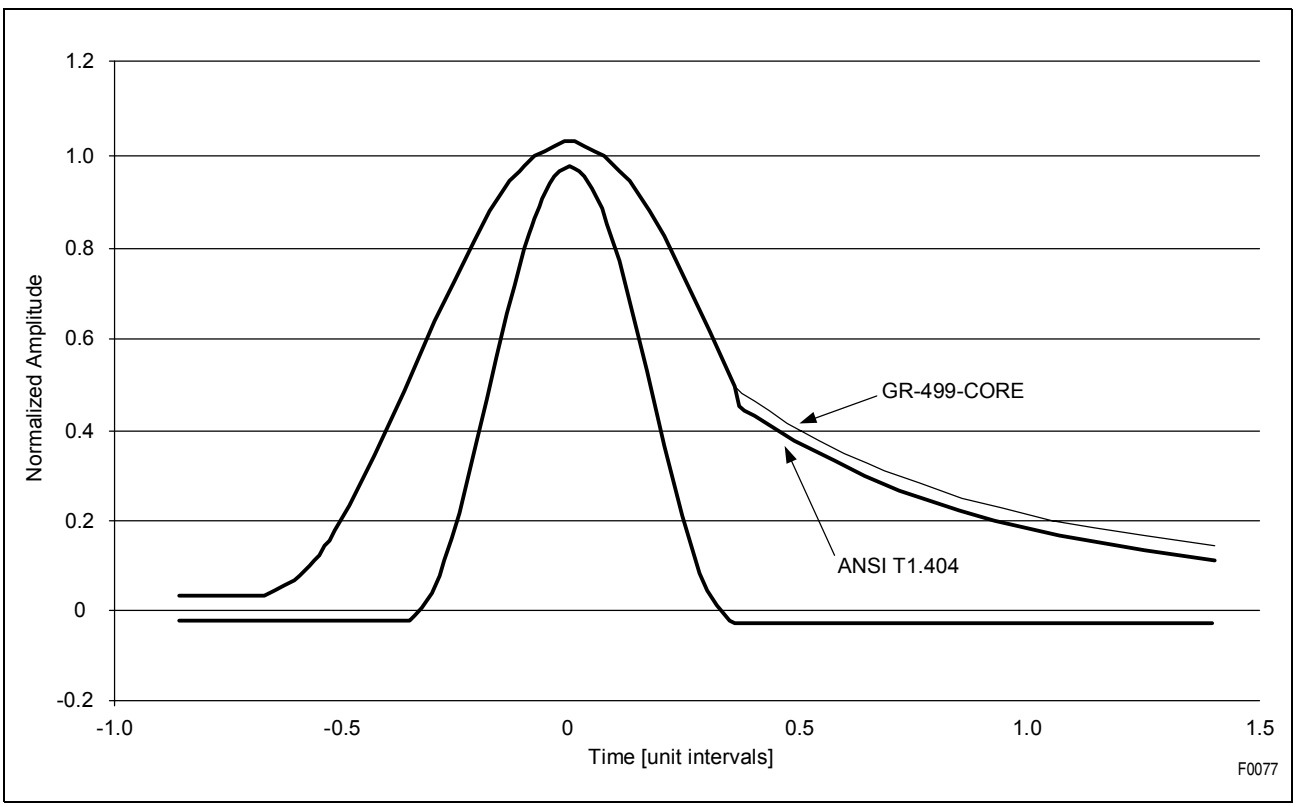


Figure 42 DS3 Pulse Shape at the Cross Connect Point (450 ft.)

Table 61 DS3 Pulse Mask (ANSI T1.404, GR-499-CORE)[1)]

Absolute Voltage Level (100 % Value)	
min.	**max.**
0.36 V	0.85 V

1) bit sequence: 0000000(+1)0000000(-1)0000000(+1)0000000(-1)...

Table 62 DS3 Pulse Mask (ANSI T1.404)

Lower Curve	
Time	**Equation**
T ≤ -0.36	-0.03
-0.36 ≤ T ≤ +0.36	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right] - 0.03$
T ≥ +0.36	-0.03

Upper Curve	
Time	**Equation**
T ≤ -0.68	+0.03
-0.68 ≤ T ≤ +0.36	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right] + 0.03$
T ≥ +0.36	$0.05 + 0.407 \times e^{-1.84[T - 0.36]}$

Table 63 DS3 Pulse Mask (GR-499-CORE)

Lower Curve	
Time	**Equation**
-0.85 ≤ T ≤ -0.36	-0.03
-0.36 ≤ T ≤ +0.36	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right] - 0.03$
+0.36 ≤ T ≤ +1.4	-0.03

Upper Curve	
Time	**Equation**
-0.85 ≤ T ≤ -0.68	+0.03
-0.68 ≤ T ≤ +0.36	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right] + 0.03$
+0.36 ≤ T ≤ +1.4	$0.08 + 0.407 \times e^{-1.84[T - 0.36]}$

7.6 Capacitances

Table 64 Pin Capacitances

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input capacitance[1)]	C_{IN}		10	pF	
Output capacitance[1)]	C_{OUT}		10	pF	all except XL1, XL2
Output capacitance[1)]	C_{OUTX}	8	20	pF	XL1, XL2

1) not tested in production

8 Test Configurations

8.1 JTAG Boundary Scan Mode

A test access port (TAP) is implemented in the TE3-FALC. The essential part of the TAP is a finite state machine (16 states) controlling the different operational modes of the boundary scan. Both, TAP controller and boundary scan, meet the requirements given by the JTAG standard: IEEE 1149.1. **Figure 43** gives an overview about the TAP controller.

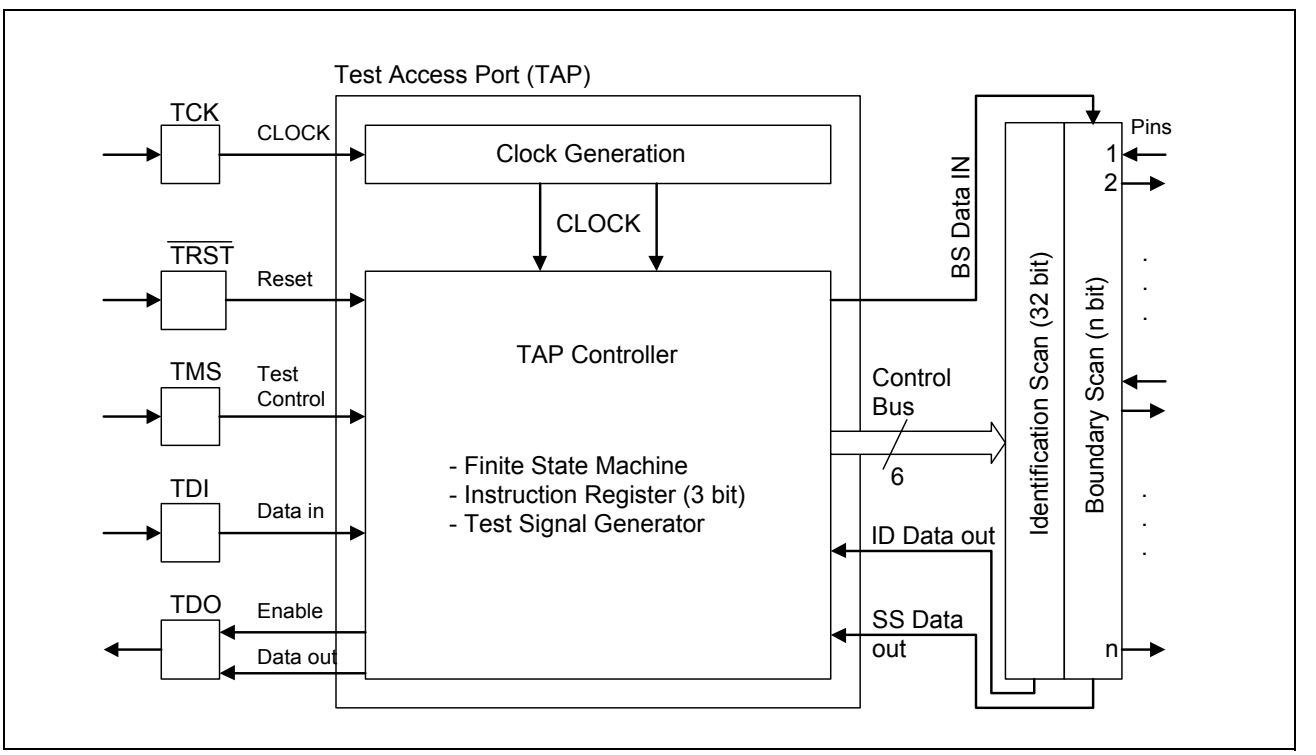


Figure 43 Block Diagram ot Test Access Port and Boundary Scan Unit

If no boundary scan operation is planned, $\overline{\text{TRST}}$ has to be connected with V_{SS} and an external pull-up resistor should be provided to the clock input TCK. The inputs TMS and TDI do not need to be connected since internal pull-up transistors ensure high input levels in this case. Nevertheless it would be a good practice to put the unused inputs to defined levels.

Test handling (boundary scan operation) is performed via the pins TCK (Test Clock), TMS (Test Mode Select), TDI (Test Data Input) and TDO (Test Data Output) when the TAP controller is not in its reset state, i.e. $\overline{\text{TRST}}$ is at V_{DDP} level or it remains unconnected due to its internal pull-up. Test data at TDI is loaded with a clock signal connected to TCK. ‘1’ or ‘0’ on TMS causes a transition from one controller state to another; constant ‘1’ on TMS leads to normal operation of the chip. An input pin (I) uses one boundary scan cell (data in), an output pin (O) uses two cells (data out, enable) and an I/O-pin (I/O) uses three cells (data in, data out, enable). Note that some functional

output and input pins of the TE3-FALC are tested as I/O pins in boundary scan, hence using three cells. The boundary scan unit of the TE3-FALC contains a total of n = 368 scan cells.

The desired test mode is selected by serially loading a 8-bit instruction code into the instruction register via TDI (LSB first); see **Table 65.**

Table 65 Boundary Scan Test Modes

Instruction (Bit 7 ... 0)	Test Mode
0000 0000	EXTEST (external testing)
0000 0010	SAMPLE/PRELOAD (snap-shot testing)
0000 0100	IDCODE (reading ID code)
1111 1111	BYPASS (bypass operation)
others	*Reserved. Do not use.*

EXTEST is used to examine the interconnection of the devices on the board. In this test mode at first all input pins capture the current level on the corresponding external interconnection line, whereas all output pins are held at constant values (‘0’ or ‘1’). Then the contents of the boundary scan is shifted to TDO. At the same time the next scan vector is loaded from TDI. Subsequently all output pins are updated according to the new boundary scan contents and all input pins again capture the current external level afterwards, and so on.

SAMPLE/PRELOAD is a test mode which provides a snapshot of pin levels during normal operation.

IDCODE: A 32-bit identification register is serially read out via TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacturer code (11 bits). The LSB is fixed to ‘1’. The ID code field is set to

- Version : 1_H
- Part Number : $00A0_H$
- Manufacturer : 041_H (including LSB, which is fixed to ’1’)

TDI ->	0001	0000 0000 1010 0000	0000 1000 001	1	-> TDO

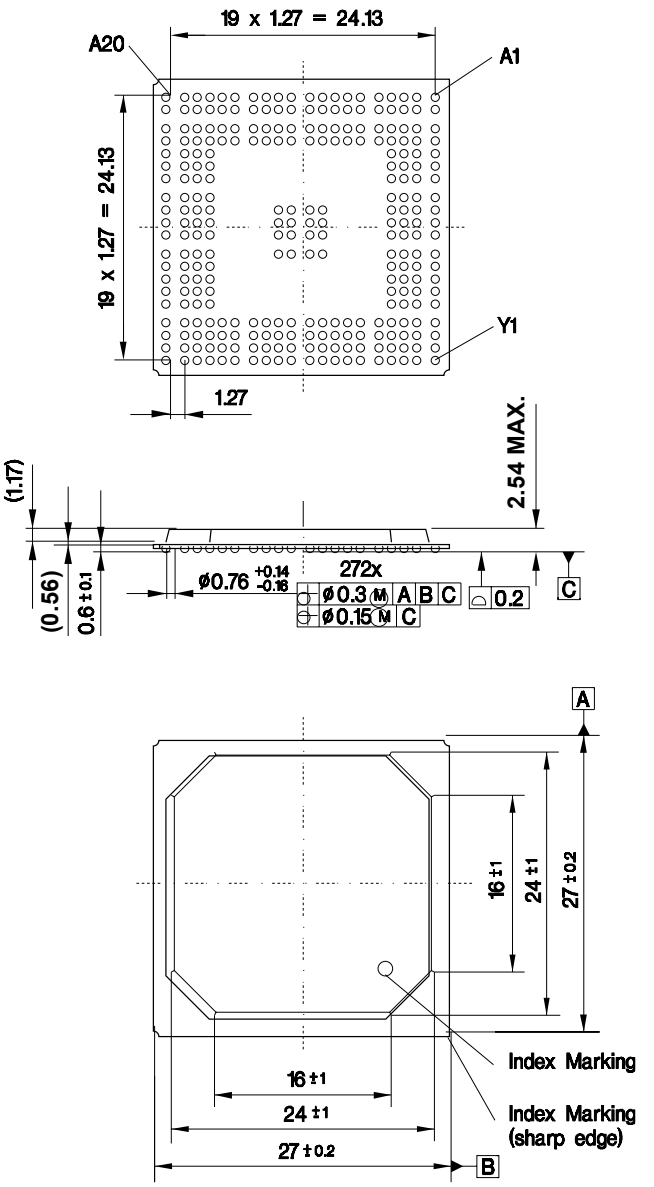
Note: Since in test logic reset state the code ‘0000 0100’ is automatically loaded into the instruction register, the ID code can easily be read out in shift DR state.

BYPASS: A bit entering TDI is shifted to TDO after one TCK clock cycle.

9 Package Outlines

9.1 PBGA-272-4 Package

PBGA-272-4
(Plastic Ball Grid Array)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

Dimensions in mm

10 Appendix

TE3-FALC comes along with a comprehensive support package available on the Infineon Technologies web site at http://www.infineon.com/t3.

10.1 Documentation

Several application notes and technical documentation provide additional information. Online access to supporting information is available on the Internet page:

http://www.infineon.com/t3

On the same page you find as well the

- Boundary Scan file for TE3-FALC Version 1.1 (BSDL File)
- TE3-FALC Firmware Image
- IBIS Model for TE3-FALC Version 1.1

10.2 Tools and Software Support

The following software package is provided together with the TE3-FALC Evaluation Board EASY 3460:

- Schematics, Layout, Gerber Files, Bill of Material of the EASY 3460 Board
- "TE3-FALC Configuration Assistant"
- Reference Source Code Driver for TE3-FALC →API Message Interface with documentation; easy re-use in customer system software

TE3-FALC Configuration Assistant

To make system design easier, the "TE3-FALC Configuration Assistant" is available. This tool runs under Win 9x/ME/NT/2000/XP environment.

The Configuration Assistant is a Windows Application which helps the user to get a quick overview over the chip and to configure it with only a few mouse clicks.

Starting from the archived application, data flow and operational modes of this application translates the setup into configuration messages which need to be given to the device. It therefore simplifies once more the already easy to handle API like interface of the TE3-FALC.

- Configuration of the data flow and main operational modes
- Detailed block configurations (Optional)
- Check for potential misconfiguration
- Online configuration by message transfer to the device
- Online status evaluation, performance and alarm monitoring
- Offline Mode: Output of the minimum configuration message set to ASCII file or printer. This output can be used as base for development of custom software configuration set

Screenshots of the program are shown in **Figure 44** and **Figure 45** below:

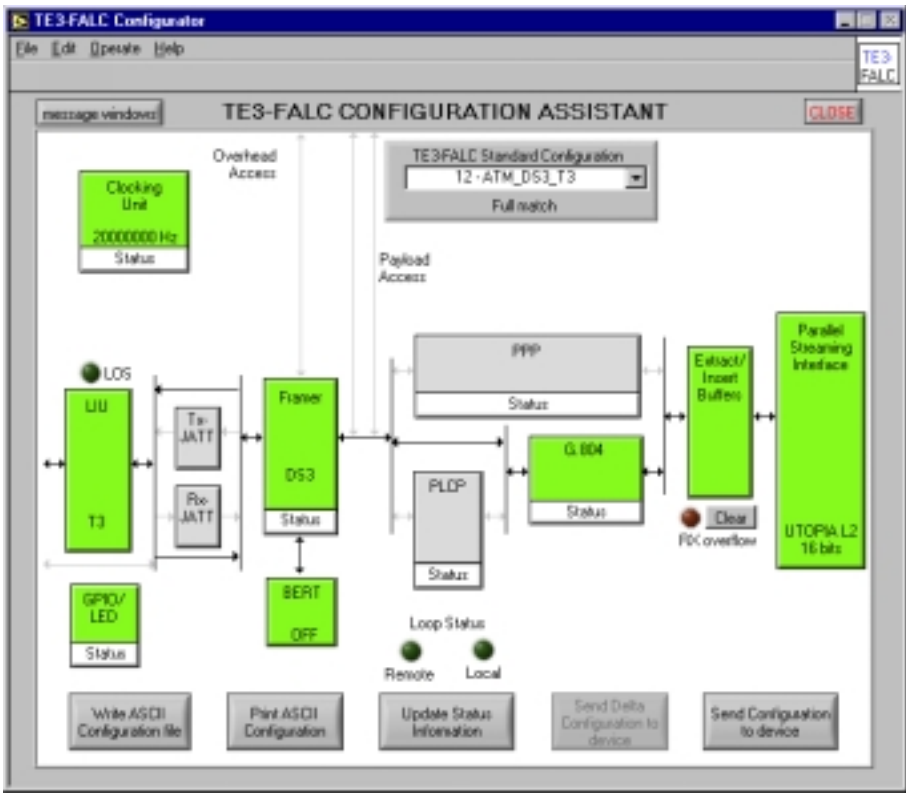


Figure 44 TE3-FALC Configuration Assistant Main Window

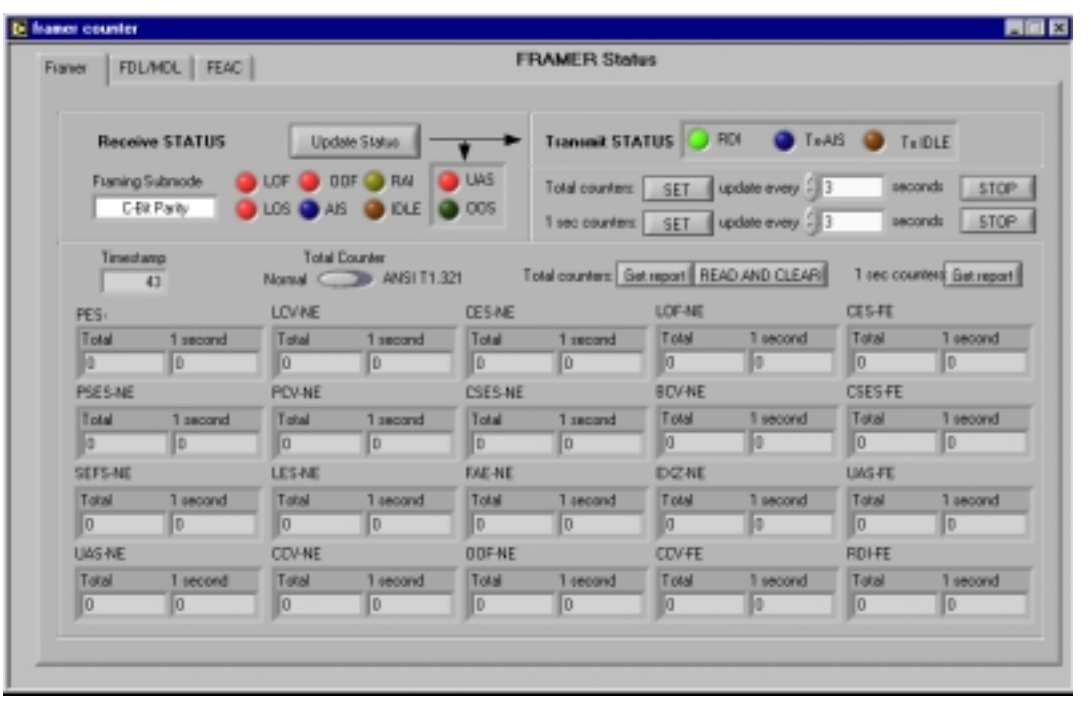


Figure 45 Configuration Assistant Framer Status and Performance Counters

11 Glossary

API	Application Programmer's Interface
ATM	Asynchronous Transfer Mode
BERT	Bit Error Rate Test
BGA	Ball Grid Array (package type)
BOM	Bit Oriented Message
CRC	Cyclic Redundency Check
DS3	Digital Signal Level 3
DWORD	Double Word (32-bit word)
FDL	Facility Data Link
FIFO	First-In First-Out Buffer
GPP	General Purpose Port (Pin)
HCS	Header Check Sequence (form of →CRC)
HDLC	High Level Data Link Control
HEC	Header Error Control (same as →HCS)
JTAG	Joined Test Action Group
LBI	Local Bus Interface
LIU	Line Interface Unit
MPI	Microprocessor Interface
MUX	Multiplexer
NOP	No Operation
OSC	Oscillator
PHY	Physical Layer Device
PLCP	Physical Layer Convergence Protocol
PPP	Point-to-Point Protocol
QoS	Quality of Service
RFIFO	Receive →FIFO
TFIFO	Transmit →FIFO
WAN	Wide Area Network