CX81801-9x SmartV.XX Modem

V.92/V.34/V.32bis Modem in 28-Pin or 38-Pin CTLGA with CX20493 SmartDAA®

Data Sheet

Revision Record

Revision	Date	Comments
D	11/21/2003	Rev. D release.
C	9/5/2003	Rev. C release.
B	7/18/2003	Rev. B release.
A	4/24/2003	Initial release.

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Conexant

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1. Introduction

1.1 Overview

The Conexant® SmartV.XX Modem supports V.92 analog data modem operation with V.44 data compression and supports 14.4 kbps fax modem operation. In addition, the modem supports remote TAM as well as serial and parallel host interface operation. Table 1-1 lists the available models.

The modem operates with PSTN telephone lines worldwide.

Conexant's SmartDAA® technology eliminates the need for a costly analog transformer, relays, and opto-isolators typically used in discrete DAA (Data Access Arrangement) implementations. The SmartDAA architecture also simplifies product implementation by eliminating the need for country-specific board configurations enabling worldwide homologation of a single modem board design and a single bill of materials (BOM).

The SmartDAA system-powered DAA operates reliably without drawing power from the line, unlike line-powered DAAs which operate poorly when line current is insufficient due to long lines or poor line conditions. Enhanced features, such as monitoring of local extension status without going off-hook, are also supported.

Incorporating Conexant's proprietary Digital Isolation Barrier (DIB) design (patent pending) and other innovative DAA features, the SmartDAA architecture simplifies application design, minimizes layout area, and reduces component cost.

The SmartV.XX Modem device set, consisting of a CX81801 Modem in a 28-pin (serial interface) or 38-pin (parallel interface) CTLGA and a CX20493 SmartDAA LSD in a 28-pin QFN, supports data/fax/TAM operation with hardware-based modem controller, digital signal processing, and DAA/telephone line interface functions (Figure 1-1).

The CX81801 Modem integrates modem controller (MCU), modem data pump (MDP), 256 KB ROM, 32 KB RAM, and SmartDAA system side device (SSD) functions onto a single die.

Small, low profile packages, low voltage operation, and low power consumption make this device set an ideal solution for embedded and palmtop applications using serial or parallel DTE interfaces.

Data compression (V.44/V.42 bis/MNP 5) and error correction (V.42/MNP 2-4) modes are supported to maximize data throughput and data transfer integrity. Non-error-correcting mode is also supported.

Fax Group 3 send and receive rates are supported up to 14.4 kbps with T.30 protocol.

V.80 synchronous access mode supports host-controlled communication protocols, e. g., H.324 video conferencing.

In TAM mode, enhanced 2-bit or 4-bit per sample coding schemes at 8 kHz sample rate provide flexible format compatibility and allows efficient digital storage of voice/audio. Also supported are 8-bit linear and IMA 4-bit ADPCM coding. This mode supports applications such as digital telephone answering machine (TAM), voice annotation, and recording from and playback to the telephone line.

This data sheet describes the modem capabilities. Commands and parameters are defined in the Commands Reference Manual (Doc. No. 102184).

Table 1-1. SmartV.XX Modem Models and Functions

Model/Order/Part Numbers				Supported Functions		
Marketing Name	**Device Set Order No.**	**SmartV.XX Modem [28-Pin CTLGA] Part No.**	**Line Side Device (LSD) [28-Pin QFN] Part No.**	**V.92 Data, QC, MOH, PCM**	**V.34 Data**	**V.32bis Data**
SmartV.92	DS56-L147-207	CX81801-94	CX20493-21	Y	Y	Y
SmartV.34	DS28-L147-207	CX81801-92	CX20493-21	-	Y	Y
SmartV.32bis	DS96-L147-207	CX81801-93	CX20493-21	-	-	Y
Lead-Free Device Sets*						
SmartV.92/LF	DS56-L147-208	CX81801-94	CX20493-31	Y	Y	Y
SmartV.34/LF	DS28-L147-208	CX81801-92	CX20493-31	-	Y	Y
SmartV.32bis/LF	DS96-L147-208	CX81801-93	CX20493-31	-	-	Y
Marketing Name	**Device Set Order No.**	**SmartV.XX Modem [38-Pin CTLGA] Part No.**	**Line Side Device (LSD) [28-Pin QFN] Part No.**	**V.92 Data, QC, MOH, PCM**	**V.34 Data**	**V.32bis Data**
SmartV.92	TBA	CX81801-98	CX20493-21	Y	Y	Y
SmartV.34	TBA	CX81801-96	CX20493-21	-	Y	Y
Notes:						
Supported functions (Y=Supported; - = Not supported)						
QC, MOH, PCM Quick connect, Modem-on-Hold, PCM upstream						
TAM Telephone answering machine (Voice playback and record through telephone line)						
* The CX81801-9x devices are all compatible with lead-free & non-lead-free manufacturing process. The only difference between standard and lead-free device sets is the CX20493 device.						

Figure 1-1. SmartV.XX Modem Simplified Interface Diagram
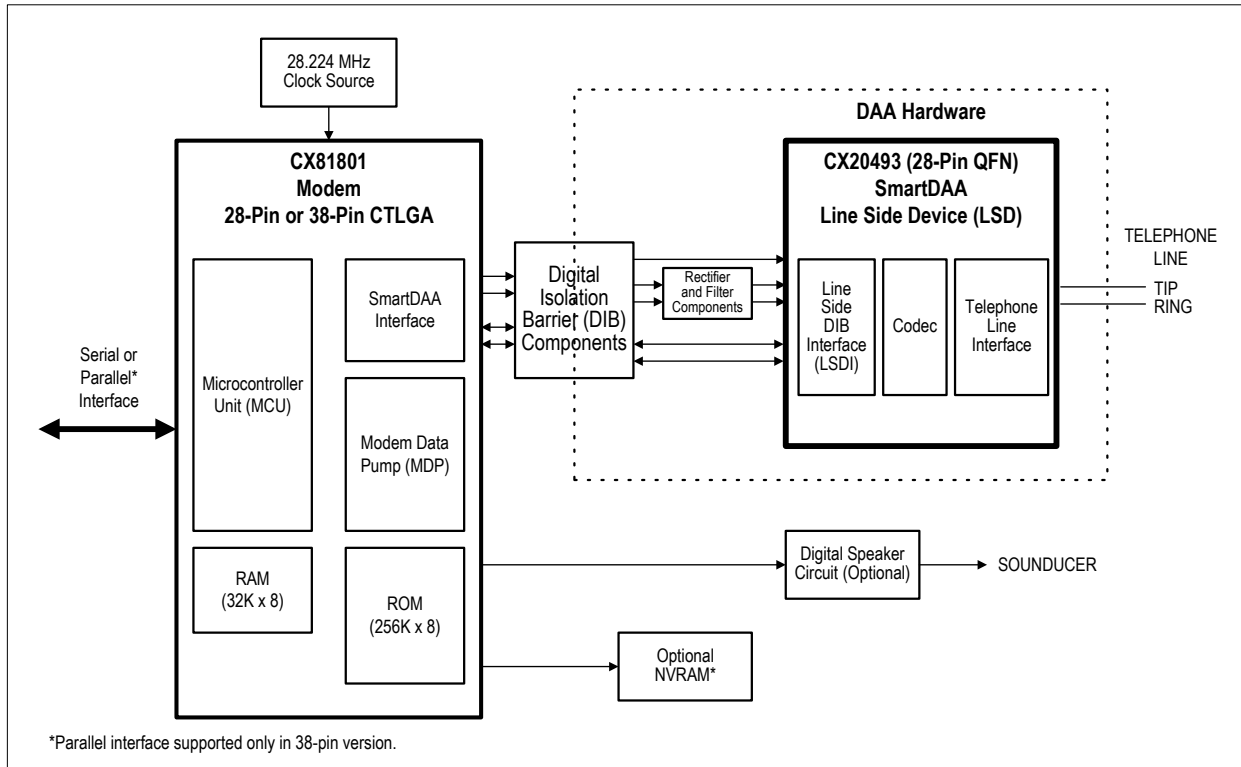
102179_001

1.2   Features

1.2.1   General Modem Features

- Data modem
  - Quick connect, Modem-on-Hold™, and PCM upstream functions (V.92 models)
  - ITU-T V.92 (V.92 models), V.90 (V.92 models), V.34 (V.92 and V.34 models), V.32bis, V.32, V.29, FastPOS (V.29), V.22 bis, V.22, V.22 FastConnect, V.23, and V.21, Bell 212A and Bell 103
  - V.250 and V.251 commands
- Data compression and error correction
  - V.44 data compression
  - V.42 bis and MNP 5 data compression
  - V.42 LAPM and MNP 2-4 error correction
- Fax modem send and receive rates up to 14.4 kbps
  - V.17, V.29, V.27 ter, and V.21 channel 2
  - EIA/TIA 578 Class 1 and T.31 Class 1.0
- V.80 synchronous access mode supports host-controlled communication protocols with H.324 interface support
- Data/Fax/Voice call discrimination
- Hardware-based modem controller
- Hardware-based digital signal processor (DSP)
- Worldwide operation
  - Complies to TBR21 and other country requirements
  - On-hook and/or on-hook Caller ID detection for many countries
  - Call progress, blacklisting
  - Internal ROM includes 29 default country profiles
  - Additional and modified country profile can be stored in internal SRAM, or external NVRAM (38-pin version only)
- Caller ID detect
  - On-hook Caller ID detection
  - Off-hook Call Waiting Caller ID detection during data mode in V.92, V.34, V.32bis, and V.32
- Distinctive ring detect
- Telephony/TAM
  - V.253 commands
  - 2-bit and 4-bit Conexant ADPCM, 8-bit linear PCM, and 4-bit IMA coding
  - 8 kHz sample rate
  - Concurrent DTMF, ring, and Caller ID detection
- Built-in DTE interface
  - Serial ITU-T V.24 (EIA/TIA-232-E) logical interface up to 115.2 kbps (28-pin version only)
  - Parallel 16550 UART-compatible host interface up to 230.4 kbps (38-pin version only)
- Direct mode (serial DTE interface)

- Flow control and speed buffering
- Automatic format/speed sensing
- Serial async data
- Thin packages support low profile designs (1.0 mm max. height)
    - CX81801 Modem in 28-pin or 38-pin CTLGA
    - CX20493 LSD in 28-pin QFN
- Pin-compatible with Conexant CX84100 (SCXV.22bis) modem (28-pin version only)
- Serial NVRAM interface for optional permanent country profile storage (38-pin version only)
- +3.3V operation with +5V tolerant digital inputs
- Typical power use
    - 205 mW (Normal Mode); 59 mW (Sleep Mode)

1.2.2   SmartDAA Features

- System side powered DAA operates under poor line current supply conditions
- Modem Wake-on-Ring
- Ring detection
- Line polarity reversal detection
- Line current loss detection
- Pulse dialing
- Line-in-use detection during on-hook operation
- Remote hang-up detection for efficient call termination
- Extension pickup detection
- Call waiting detection
- Digital PBX line protection
- Meets worldwide DC V-I masks requirements

1.2.3 Applications

- Embedded systems
- Set-top boxes
- Handheld computers
- Gaming devices
- Point of sale terminals
- Remove monitoring and data collection systems
- Modem modules

1.3 Technical Overview

1.3.1 General Description

Modem operation, including dialing, call progress, telephone line interface, telephone handset interface, and host DTE interface functions are supported and controlled through the V.250, V.251, and V.253-compatible command set.

The OEM adds a crystal circuit, DIB components, telephone line interface, telephone handset/telephony extension interface, and other supporting discrete components as supported by the modem model (Table 1-1) and required by the application to complete the system.

1.3.2 Embedded MCU Firmware

Embedded MCU firmware performs processing of general modem control, command sets, data modem, error correction and data compression (ECC), fax class 1, fax class 1.0, TAM, worldwide, V.80, serial DTE interface, and parallel host interface functions according to modem models (Table 1-1).

1.3.3 Operating Modes

1.3.3.1 Data/Fax Modes

In V.92 data modem mode (V.92 models), the modem can receive data from a digital source using a V.92-compatible central site modem at line speeds up to 56 kbps. With PCM upstream enabled, data transmission supports sending data at line speeds up to 48 kbps. When PCM upstream is disabled, data transmission supports sending data at line speeds up to V.34 rates. This mode can fallback to V.34 mode and to lower rates as dictated by line conditions.

The following modes are also supported in V.92 models, when connected to a V.92-compatible server supporting the feature listed.

- Quick connect, which allows quicker subsequent connection to a server using stored line parameters obtained during the initial connection. The server must support quick connect profiles.

- Modem-on-Hold, which allows detection and reporting of incoming phone calls on the PSTN with enabled Call Waiting. If the incoming call is accepted by the user, the user has a pre-defined amount of time of holding the data connection for a brief

conversation. The data connection resumes upon incoming call termination. The server must support Modem-on-Hold functionality.

- PCM upstream, which boosts the upstream data rates between the user and V.92 server. A maximum of 48 kbps upstream rate is supported when connected to a V.92 server that supports PCM upstream.

In V.34 data modem mode (V.92 and V.34 models), the modem can operate in 2-wire, full-duplex, asynchronous modes at line rates up to 33.6 kbps. Data modem modes perform complete handshake and data rate negotiations. Using V.34 modulation to optimize modem configuration for line conditions, the modem can connect at the highest data rate that the channel can support from 33600 bps down to 2400 bps with automatic fallback. Automode operation in V.34 is provided in accordance with PN3320 and in V.32 bis in accordance with PN2330. All tone and pattern detection functions required by the applicable ITU or Bell standards are supported.

In V.32 bis data modem mode, the modem can operate at line speeds up to 14.4 kbps.

In fax modem mode, the modem can operate in 2-wire, half-duplex, synchronous modes and can support Group 3 facsimile send and receive speeds of 14400, 12000, 9600, 7200, 4800, and 2400 bps. Fax data transmission and reception performed by the modem are controlled and monitored through the EIA/TIA-578 Fax Class 1, or T.31 Fax Class 1.0 command interface. Full HDLC formatting, zero insertion/deletion, and CRC generation/checking are provided.

1.3.3.2 V.44 Data Compression

V.44 provides more efficient data compression than V.42 bis that significantly decreases the download time for the types of files associated with Internet use. This significant improvement is most noticeable when browsing and searching the web since HTML text files are highly compressible. (The improved performance amount varies both with the actual format and with the content of individual pages and files.)

1.3.3.3 Synchronous Access Mode (SAM) - Video Conferencing

V.80 Synchronous Access Mode between the modem and the host/DTE is provided for host-controlled communication protocols, e.g., H.324 video conferencing applications.

Voice-call-first (VCF) before switching to a videophone call is also supported.

1.3.3.4 TAM Mode

TAM Mode features include 8-bit linear coding at 8 kHz sample rate. Tone detection/ generation, call discrimination, and concurrent DTMF detection are also supported.

TAM Mode is supported by four submodes:

- Online Voice Command Mode supports connection to the telephone line.
- Voice Receive Mode supports recording voice or audio data input from the telephone line.
- Voice Transmit Mode supports playback of voice or audio data to the telephone line.
- Full-duplex Receive and Transmit Mode.

1.3.3.5   **Worldwide Operation**

The modem operates in TBR21-compliant and other countries. Country-dependent modem parameters for functions such as dialing, carrier transmit level, calling tone, call progress tone detection, answer tone detection, blacklisting, caller ID, and relay control are programmable.

SmartDAA technology allows a single PCB design and single BOM to be homologated worldwide. Advanced features such as extension pickup detection, remote hang-up detection, line-in-use detection, and digital PBX protection are supported.

Country code IDs are defined by ITU-T T.35.

Internal ROM includes default profiles for 29 countries including TBR21-compliant profiles. An additional or modified country profile can be loaded into internal SRAM. A duplicate country profile stored in internal SRAM will override the profile in internal ROM firmware. Additional country profiles can be loaded into external NVRAM for permanent storage (38-pin version only). The default countries supported are listed in Table 1-2. Request additional country profiles from a Conexant Sales Office.

Table 1-2. Default Countries Supported

Country	Country Code	Call Waiting Tone Detection (CW) Supported	On-Hook Type 1 Caller ID (CID) Supported	Off-Hook Type 2 Called ID (CID2) Supported
Australia	09	X	X	
Austria	0A	X	X	
Belgium	0F	X		
Brazil	16	X		
China	26	X	X	
Denmark	31	X	X	
Finland	3C	X	X	
France	3D	X	X	X
Germany	42	X	X	
Hong Kong	50	X	X	X
India	53		X	
Ireland	57		X	
Italy	59	X	X	
Japan	00	X	X	X
Korea	61	X		
Malaysia	6C	X		
Mexico	73			
Netherlands	7B		X	
Norway	82	X	X	
Poland	8A	X		
Portugal	8B	X		
Singapore	9C	X	X	X
South Africa	9F	X		
Spain	A0	X	X	
Sweden	A5	X	X	
Switzerland	A6	X		
Taiwan	FE	X	X	
United Kingdom	B4	X	X	X
United States	B5	X	X	X
Reserved	FD	X	X	X

1.3.4   Reference Designs

A data/fax/TAM reference design is available to minimize modem design time, reduce development cost, and accelerate market entry.

A design package is available in electronic form. This package includes schematics, bill of materials (BOM), vendor part list (VPL), board layout files in Gerber and PADS formats, and complete documentation.

1.4   Hardware Description

SmartDAA technology eliminates the need for a costly analog transformer, relays, and opto-isolators that are typically used in discrete DAA implementations. The programmable SmartDAA architecture simplifies product implementation in worldwide markets by eliminating the need for country-specific components.

1.4.1   CX81801 Modem

The CX81801 modem, packaged in a 28-pin or 38-pin CTLGA, includes a Microcontroller (MCU), a Modem Data Pump (MDP), 256 KB internal ROM, 32 KB internal RAM, and SmartDAA interface functions.

The modem connects to host via a logical V.24 (EIA/TIA-232-E) serial DTE interface or a parallel 16550 UART-compatible host interface (38-pin version only).

The modem performs the command processing, host interface functions, and telephone line signal modulation/demodulation in a hardware digital signal processor (DSP) which reduces computational load on the host processor.

The SmartDAA Interface communicates with, and supplies power and clock to the LSD through the DIB.

1.4.2   Digital Isolation Barrier

The OEM-supplied Digital Isolation Barrier (DIB) electrically DC isolates the CX81801 from the LSD and telephone line. The modem is connected to a fixed digital ground and operates with standard CMOS logic levels. The LSD is connected to a floating ground and can tolerate high voltage input (compatible with telephone line and typical surge requirements).

The DIB transformer couples power and clock from the CX81801 to the LSD.

The DIB data channel supports bidirectional half-duplex serial transfer of data, control, and status information between the CX81801 and the LSD over two lines.

1.4.3   CX20493 SmartDAA Line Side Device

The CX20493 SmartDAA Line Side Device (LSD) includes a Line Side DIB Interface (LSDI), a coder/decoder (codec), and a Telephone Line Interface (TLI).

The LSDI communicates with, and receives power and clock from, the SmartDAA interface in the CX81801 through the DIB.

LSD power is received from the MDP PWRCLKP and PWRCLKN pins via the DIB through a full-wave rectifier bridge and capacitive power filter circuit connected to the DIB transformer secondary winding.

The CLK input is also accepted from the DIB transformer secondary winding through a capacitor and a resistor in series.

Information is transferred between the LSD and the CX81801 through the DIB_P and DIB_N pins. These pins connect to the CX81801 DIB_DATAP and DIB_DATAN pins, respectively, through the DIB.

The TLI integrates DAA and direct telephone line interface functions and connects directly to the line TIP and RING pins, as well as to external line protection components.

Direct LSD connection to TIP and RING allows real-time measurement of telephone line parameters, such as the telephone central office (CO) battery voltage, individual telephone line (copper wire) resistance, and allows dynamic regulation of the off-hook TIP and RING voltage and total current drawn from the central office (CO). This allows the modem to maintain compliance with U.S. and worldwide regulations and to actively control the DAA power dissipation.

1.5 Commands

The modem supports data modem, fax class 1 or 1.0 modem, voice/audio, full-duplex speakerphone (FDSP), and V.80 commands, and S Registers in accordance with modem model options. See Doc. No. 102184 for a description of the commands.

Data Modem Operation. Data modem functions operate in response to the AT commands when +FCLASS=0. Default parameters support U.S./Canada operation.

Fax Modem Operation. Facsimile functions operate in response to fax class 1 commands when +FCLASS=1 or to fax class 1.0 commands when +FCLASS=1.0.

Voice/Audio Operation. Voice/audio mode functions operate in response to voice/audio commands when +FCLASS=8.

2. Technical Specifications

2.1 Serial DTE Interface Operation

2.1.1 Automatic Speed/Format Sensing

Command Mode and Data Modem Mode. The modem can automatically determine the speed and format of the data sent from the DTE. The modem can sense speeds of 300, 600, 1200, 2400, 4800, 7200, 9600, 12000, 14400, 16800, 19200, 21600, 24000, 26400, 28800, 38400, 57600, and 115200 bps and the following data formats:

Parity	Data Length (No. of Bits)	No. of Stop Bits	Character Length (No. of Bits)
None	7	2	10
Odd	7	1	10
Even	7	1	10
None	8	1	10
Odd	8	1	11*
Even	8	1	11*
*11-bit characters are sensed, but the parity bit is stripped off during data transmission in Normal and Error Correction modes.			

The modem can speed sense data with mark or space parity and configures itself as follows:

DTE Configuration	Modem Configuration
7 mark	7 none
7 space	8 none
8 mark	8 none
8 space	8 even

Fax Modem Mode. In V.17 fax mode, the modem can sense speeds up to 115.2 kbps.

2.2 Parallel Host Bus Interface Operation

Command Mode and Data Modem Mode. The modem can operate at rates up to 230.4 kbps by programming the Divisor Latch in the parallel interface registers.

Fax Modem Mode. In V.17 mode, the modem can operate at rates up to 230.4 kbps by programming the Divisor Latch in the parallel interface registers.

2.3 Establishing Data Modem Connections

2.3.1 Dialing

DTMF Dialing. DTMF dialing using DTMF tone pairs is supported in accordance with ITU-T Q.23.

Pulse Dialing. Pulse dialing is supported in accordance with EIA/TIA-496-A.

Blind Dialing. The modem can blind dial in the absence of a dial tone if enabled by the X0, X1, or X3 command.

2.3.2 Modem Handshaking Protocol

If a tone is not detected within the time specified in the S7 register after the last digit is dialed, the modem aborts the call attempt.

2.3.3 Call Progress Tone Detection

Ringback, equipment busy, congested tone, warble tone, and progress tones can be detected in accordance with the applicable standard.

2.3.4 Answer Tone Detection

Answer tone can be detected over the frequency range of 2100 ± 40 Hz in ITU-T modes and 2225 ± 40 Hz in Bell modes.

2.3.5 Ring Detection

A ring signal can be detected from a TTL-compatible 15.3 Hz to 68 Hz square wave input.

2.3.6 Billing Protection

When the modem goes off-hook to answer an incoming call, both transmission and reception of data are prevented for 2 seconds (data modem) or 4 seconds (fax adaptive answer) to allow transmission of the billing tone signal.

2.3.7   Connection Speeds

The modem functions as a data modem when the +FCLASS=0 command is active.

Line connection can be selected using the +MS command. The +MS command selects modulation, enables/disables automode, and selects minimum and maximum line speeds (Table 2-1).

Table 2-1. +MS Command Automode Connectivity

Modulation	<carrier>	Possible (<min_rx_rate>, <min_rx_rate>, (<min_tx_rate>), and <max_tx_rate>) Rates (bps)
Bell 103	B103	300
Bell 212	B212	1200 Rx/75 Tx or 75 Rx/1200 Tx
V.21	V21	300
V.22	V22	1200
V.22 bis	V22B	2400 or 1200
V.23	V23C	1200
V.32	V32	9600 or 4800
V.32 bis	V32B	14400, 12000, 9600, 7200, or 4800
V.34	V34	33600, 31200, 28800, 26400, 24000, 21600, 19200, 16800, 14400, 12000, 9600, 7200, 4800, or 2400
V.90	V90	56000, 54667, 53333, 52000, 50667, 49333, 48000, 46667, 45333, 44000, 42667, 41333, 40000, 38667, 37333, 36000, 34667, 33333, 32000, 30667, 29333, 28000
V.92 downstream	V92	56000, 54667, 53333, 52000, 50667, 49333, 48000, 46667, 45333, 44000, 42667, 41333, 40000, 38667, 37333, 36000, 34667, 33333, 32000, 30667, 29333, 28000
V.92 upstream	V92	48000, 46667, 45333, 44000, 42667, 41333, 40000, 38667, 37333, 36000, 34667, 33333, 32000, 30667, 29333, 28000, 26667, 25333, 24000

2.3.8   Automode

Automode detection can be enabled by the +MS command to allow the modem to connect to a remote modem in accordance with draft PN-3320 for V.34 (Table 2-1).

2.4   Data Mode

Data mode exists when a telephone line connection has been established between modems and all handshaking has been completed.

2.4.1   Speed Buffering (Normal Mode)

Speed buffering allows a DTE to send data to, and receive data from, a modem at a speed different than the line speed. The modem supports speed buffering at all line speeds.

2.4.2   Flow Control

DTE-to-Modem Flow Control. If the modem-to-line speed is less than the DTE-to-modem speed, the modem supports XOFF/XON or RTS/CTS flow control with the DTE to ensure data integrity.

2.4.3 Escape Sequence Detection

The +++ escape sequence can be used to return control to the command mode from the data mode. Escape sequence detection is disabled by an S2 Register value greater than 127.

2.4.4 BREAK Detection

The modem can detect a BREAK signal from either the DTE or the remote modem. The \Kn command determines the modem response to a received BREAK signal.

2.4.5 Telephone Line Monitoring

GSTN Cleardown (V.92, V.90, V.34, V.32 bis, V.32). Upon receiving GSTN Cleardown from the remote modem in a non-error correcting mode, the modem cleanly terminates the call.

Loss of Carrier (V.22 bis and Below). If carrier is lost for a time greater than specified by the S10 register, the modem disconnects.

2.4.6 Fall Forward/Fallback (V.92/V.90/V.34/V.32 bis/V.32)

During initial handshake, the modem will fallback to the optimal line connection within V.92/V.90/V.34/V.32 bis/V.32 mode depending upon signal quality if automode is enabled by the +MS or N1 command.

When connected in V.92/V.90/V.34/V.32 bis/V.32 mode, the modem will fall forward or fallback to the optimal line speed within the current modulation depending upon signal quality if fall forward/fallback is enabled by the %E2 command.

2.4.7 Retrain

The modem may lose synchronization with the received line signal under poor or changing line conditions. If this occurs, retraining may be initiated to attempt recovery depending on the type of connection.

The modem initiates a retrain if line quality becomes unacceptable if enabled by the %E command. The modem continues to retrain until an acceptable connection is achieved, or until 30 seconds elapse resulting in line disconnect.

2.4.8 Programmable Inactivity Timer

The modem disconnects from the line if data is not sent or received for a specified length of time. In normal or error-correction mode, this inactivity timer is reset when data is received from either the DTE or from the line. This timer can be set to a value between 0 and 255 seconds by using register S30. A value of 0 disables the inactivity timer.

2.4.9 DTE Signal Monitoring (Serial DTE Interface Only)

DTR#. When DTR# is asserted, the modem responds in accordance with the &Dn and &Qn commands.

RTS#. RTS# is used for flow control if enabled by the &K command in normal or error-correction mode.

2.5 V.92 Features

Modem-on-Hold, quick connect, and PCM upstream are only available when connecting in V.92 data mode. V.92 features are only available when the server called is a V.92 server that supports that particular feature.

2.5.1 Modem-on-Hold

The Modem-on-Hold (MOH) function (V.92 models only) enables the modem to place an Internet data connection on hold while using the same line to accept an incoming or place an outgoing voice call. This feature is available only with a connection to a server supporting MOH. MOH can be executed through either of two methods:

- One method is to enable MOH through the +PMH command. With Call Waiting Detection (+PCW command) enabled, an incoming call can be detected while on-line. Using a string of commands, the modem negotiates with the server to place the data connection on hold while the line is released so that it can be used to conduct a voice call. Once the voice call is completed, the modem can quickly renegotiate with the server back to the original data call.
- An alternative method is to use communications software that makes use of the Conexant Modem-on-Hold drivers. Using this method, the software can detect an incoming call, place the data connection on hold, and switch back to a data connection.

2.5.2 Quick Connect

The quick connect function (V.92 models only) enables the modem to shorten the connect time of subsequent calls to a server supporting quick connect. The quick connect feature is supported by the +PQC command.

2.5.3 PCM Upstream

PCM upstream boots the upstream data rates between the user and ISP to reduce upload times for large files and email attachments. A maximum of 48 kbps upstream rate is supported with PCM upstream enabled, in contrast to a maximum of 32.2 kbps upstream rate with PCM upstream not enabled. PCM upstream is supported by the +PCM command. PCM upstream is disabled by default.

2.6 Error Correction and Data Compression

2.6.1 V.42 Error Correction

V.42 supports two methods of error correction: LAPM and, as a fallback, MNP 4. The modem provides a detection and negotiation technique for determining and establishing the best method of error correction between two modems.

2.6.2 MNP 2-4 Error Correction

MNP 2-4 is a data link protocol that uses error correction algorithms to ensure data integrity. Supporting stream mode, the modem sends data frames in varying lengths depending on the amount of time between characters coming from the DTE.

2.6.3   V.44 Data Compression

V.44 data compression encodes pages and files associated with Web pages more efficiently than V.42 bis. These files include WEB pages, graphics and image files, and document files. V.44 can provide an effective data throughput rate up to DTE rate for a 56-kbps connection. The improved performance amount varies both with the actual format and with the content of individual pages and files.

2.6.4   V.42 bis Data Compression

V.42 bis data compression mode, enabled by the %Cn command or S46 register, operates when a LAPM connection is established.

The V.42 bis data compression employs a "string learning" algorithm in which a string of characters from the DTE is encoded as a fixed length codeword. Two 2-KB dictionaries are used to store the strings. These dictionaries are dynamically updated during normal operation.

2.6.5   MNP 5 Data Compression

MNP 5 data compression mode, enabled by the %Cn command, operates during an MNP connection.

In MNP 5, the modem increases its throughput by compressing data into tokens before transmitting it to the remote modem, and by decompressing encoded received data before sending it to the DTE.

2.7 Telephony Extensions

The following telephony extension features are supported and are typically implemented in designs for set-top box applications and TAM software applications to enhance end-user experience:

- Line In Use detection

- Extension Pickup detection

- Remote Hang-up detection

The telephony extension features are enabled through the -STE command. The -TTE command can be used to adjust the voltage thresholds for the telephony extension features.

2.7.1 Line In Use Detection

The Line In Use Detection feature can stop the modem from disturbing the phone line when the line is already being used. When an attempt is made to dial using ATDT and the phone line is in use, the modem will not go off hook and will respond with the message "LINE IN USE".

2.7.2 Extension Pickup Detection

The Extension Pickup Detection feature (also commonly referred as PPD or Parallel phone detection) allows the modem to detect when another telephony device (i.e., fax machine, phone, satellite/cable box) is attempting to use the phone line. When an extension pickup has been detected, the modem will go on-hook and respond with the message "OFF-HOOK INTRUSION".

The Remote Hangup Detection feature will cause the modem to go back on-hook and respond with the message "LINE REVERSAL DETECTED" during a data connection when the remote modem is disconnected for abnormal termination reasons (remote phone line unplugged, remote server/modem shutdown). For Voice applications, this method can be used in addition to silence detection to determine when a remote caller has hung up to terminate a voice recording.

This feature can be used to quickly drop a modem connection in the event when a user picks up a extension phone line. For example, this feature allows set top boxes with an integrated SmartV.XX modem to give normal voice users the highest priority over the telephone line.

This feature can also be used in Telephone Answering Machine applications (TAM). Its main use would be to stop the TAM operation when a phone is picked up.

2.7.3 Remote Hangup Detection

The Remote Hangup Detection feature will cause the modem to go back on-hook and respond with the message "LINE REVERSAL DETECTED" during a data connection when the remote modem is disconnected for abnormal termination reasons (remote phone line unplugged, remote server/modem shutdown). For Voice applications, this method can be used in addition to silence detection to determine when a remote caller has hung up to terminate a voice recording.

2.8   Fax Class 1 and Fax Class 1.0 Operation

Facsimile functions operate in response to fax class 1 commands when +FCLASS=1 or to fax class 1.0 commands when +FCLASS=1.0.

In the fax mode, the on-line behavior of the modem is different from the data (non-fax) mode. After dialing, modem operation is controlled by fax commands. Some AT commands are still valid but may operate differently than in data modem mode.

Calling tone is generated in accordance with T.30.

2.9   Point-of-Sales Support

Point-of-Sales (POS) terminals usually need to exchange a small amount of data in the shortest amount of time. Low speed modulations such as Bell212A or V.22 are still mainly used in POS applications. Additionally, new non-standard sequences have been developed to better support POS applications.

Industry standard and shortened answer tone B103 and V.21 are supported, as well as FastPOS (V.29) and V.22 FastConnect. POS terminal modulations are supported by the $F command.

2.10   TAM Mode

Voice and TAM functions are supported by the Voice Mode. Voice Mode includes four submodes: Online Voice Command Mode, Voice Receive Mode, Voice Transmit Mode and Full-Duplex Receive and Transmit Mode.

2.10.1   Online Voice Command Mode

This mode results from the connection to the telephone line or a voice/audio I/O device (e.g., microphone, speaker, or handset) through the use of the +FCLASS=8 and +VLS commands. After mode entry, AT commands can be entered without aborting the connection.

2.10.2   Voice Receive Mode

This mode is entered when the +VRX command is active in order to record voice or audio data input at the RIN pin, typically from a microphone/handset or the telephone line.

Received analog voice samples are converted to digital form and compressed for reading by the host. AT commands control the codec bits-per-sample rate.

Received analog mono audio samples are converted to digital form and formatted into 8-bit unsigned linear PCM format for reading by the host. AT commands control the bit length and sampling rate. Concurrent DTMF/tone detection is available at the 8 kHz sample rate.

2.10.3 Voice Transmit Mode

This mode is entered when the +VTX command is active in order to playback voice or audio data to the TXA output, typically to a speaker/handset or to the telephone line.

Digitized voice data is decompressed and converted to analog form at the original compression quantization sample-per-bits rate then output to the TXA output.

Digitized audio data is converted to analog form then output to the TXA output.

2.10.4 Full-Duplex Receive and Transmit Mode

This mode is entered when the +VTR command is active in order to concurrently receive and transmit voice.

2.10.5 Tone Detectors

The modem is equipped with three tone detectors with signal paths separate from the main received signal path thus enabling tone detection to be independent of the configuration status.

2.10.6 Call Waiting Tone Detection

Call Waiting tones can be detected when in V.92, V.90, V.34, and V.32bis data modes.

2.11 Caller ID

Both Type I Caller ID (On-Hook Caller ID) and Type II Caller ID (Call Waiting Caller ID) are supported for U.S. and many other countries (see Section 2.12). Both types of Caller ID are enabled/disabled using the +VCID command. Call Waiting Tone detection must be enabled using the +PCW command to detect and decode Call Waiting Caller ID. When enabled, caller ID information (date, time, caller code, and name) can be passed to the DTE in formatted or unformatted form. Inquiry support allows the current caller ID mode and mode capabilities of the modem to be retrieved from the modem.

Type II Caller ID (Call Waiting Caller ID) detection operates only during data mode in V.92, V.90, V.34, V.32bis, or V.32.

2.12 Worldwide Country Support

Internal modem firmware supports 29 country profiles (see Section 1.3.3.5). These country profiles include the following country-dependent parameters:

- Dial tone detection levels and frequency ranges.
- DTMF dialing parameters: Transmit output level, DTMF signal duration, and DTMF interdigit interval.
- Pulse dialing parameters: Make/break times, set/clear times, and dial codes are programmable.
- Ring detection frequency range.
- Type I and Type II Caller ID detection are supported for many countries. Contact your local Conexant sales office for additional country support.
- Blind dialing enable/disable.

- Carrier transmit level (through S91 for data and S92 for fax). The maximum, minimum, and default values can be defined to match specific country and DAA requirements.

- Calling tone is generated in accordance with V.25. Calling tone may be toggled (enabled/disabled) by inclusion of a "^" character in a dial string. It may also be disabled.

- Frequency and cadence of tones for busy, ringback, congested, warble, dial tone 1, and dial tone 2.

- Answer tone detection period.

- Blacklist parameters. The modem can operate in accordance with requirements of individual countries to prevent misuse of the network by limiting repeated calls to the same number when previous call attempts have failed. Call failure can be detected for reasons such as no dial tone, number busy, no answer, no ringback detected, voice (rather than modem) detected, and key abort (dial attempt aborted by user). Actions resulting from such failures can include specification of minimum inter-call delay, extended delay between calls, and maximum numbers of retries before the number is permanently forbidden ("blacklisted").

The country profiles may be altered or customized by modifying the country-dependent parameters. Additional profiles may also be included. Additional and modified country profiles are supported by internal SRAM.

Please contact an FAE at the local Conexant sales office for additional and modified country profile support.

2.13 Diagnostics

2.13.1 Commanded Tests

Diagnostics are performed in response to test commands.

Analog Loopback (&T1 Command). Data from the local DTE is sent to the modem, which loops the data back to the local DTE.

DMTF Generation (%TT0 Command). Continuous DTMF tones are generated by the DSP and output through the DAA.

Tone Generation (%TT3 Command). Continuous tones are generated by the DSP and output through the DAA.

2.14 Low Power Sleep Mode

Sleep Mode Entry. The modem enters the low power sleep mode when no line connection exists and no host activity occurs for the period of time specified in the S24 register. All modem circuits are turned off except the internal clock circuitry in order to consume reduced power while being able to immediately wake up and resume normal operation.

Wake-up. Wake-up occurs when a ring is detected on the telephone line, the host writes to the modem (parallel interface), or the DTE sends a character to the modem (serial interface).

3. Hardware Interface

3.1 CX81801 Modem Hardware Pins and Signals

3.1.1 CX81801 Modem 28-Pin CTLGA with Serial Interface Signal Summary

3.1.1.1 LSD Interface (Through DIB)

The DIB interface signals are:

- Clock and Power Positive (PWRCLKP); output
- Clock and Power Negative (PWRCLKN); output
- Data Positive (DIB_DATAP); input/output
- Data Negative (DIB_DATAN); input/output

3.1.1.2 Call Progress Speaker Interface

The call progress speaker interface signal is:

- Digital speaker output (DSPKOUT); output

DSPKOUT is a square wave output in Data/Fax mode used for call progress or carrier monitoring. This output can be optionally connected to a low-cost on-board speaker, e.g., a sounducer, or to an analog speaker circuit.

3.1.1.3 Serial DTE Interface and Indicator Outputs

The supported DTE interface signals are:

- Serial Transmit Data input (TXD#)
- Serial Receive Data output line (RXD#)
- Clear to Send output (CTS#)
- Received Line Signal Detector (RLSD#)
- Ring Indicator (RI#)
- Data Terminal Ready control input (DTR#)
- Request to Send control input (RTS#)

3.1.2 CX81801 Modem 28-Pin CTLGA with Serial Interface Pin Assignments and Signal Definitions

CX81801 Modem 28-pin CTLGA hardware interface signals are shown by major interface in Figure 3-1, are shown by pin number in Figure 3-2, and are listed by pin number in Table 1-1.

CX81801 Modem hardware interface signals are defined in Table 3-2.

Figure 3-1. CX81801 Modem 28-Pin CTLGA with Serial Interface Hardware Signals
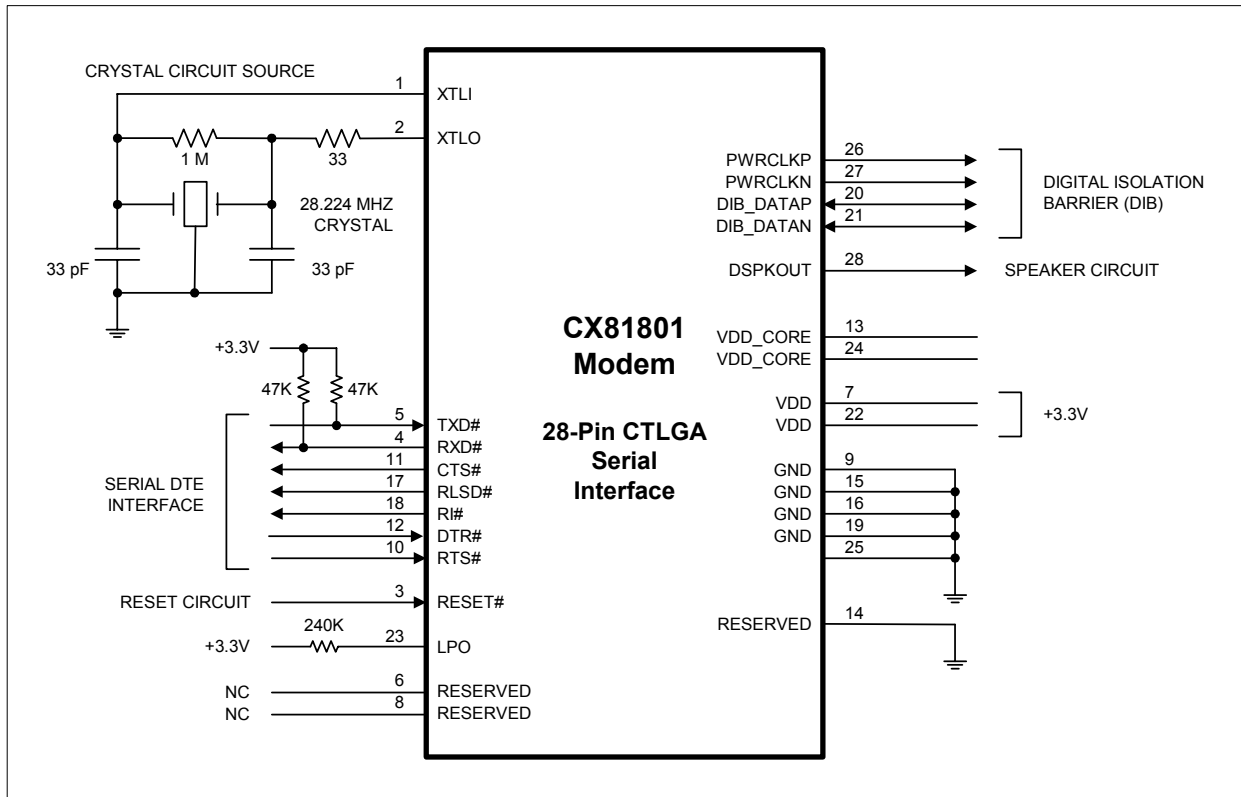
102179_002

Figure 3-2. CX81801 Modem 28-Pin CTLGA with Serial Interface Pin Signals
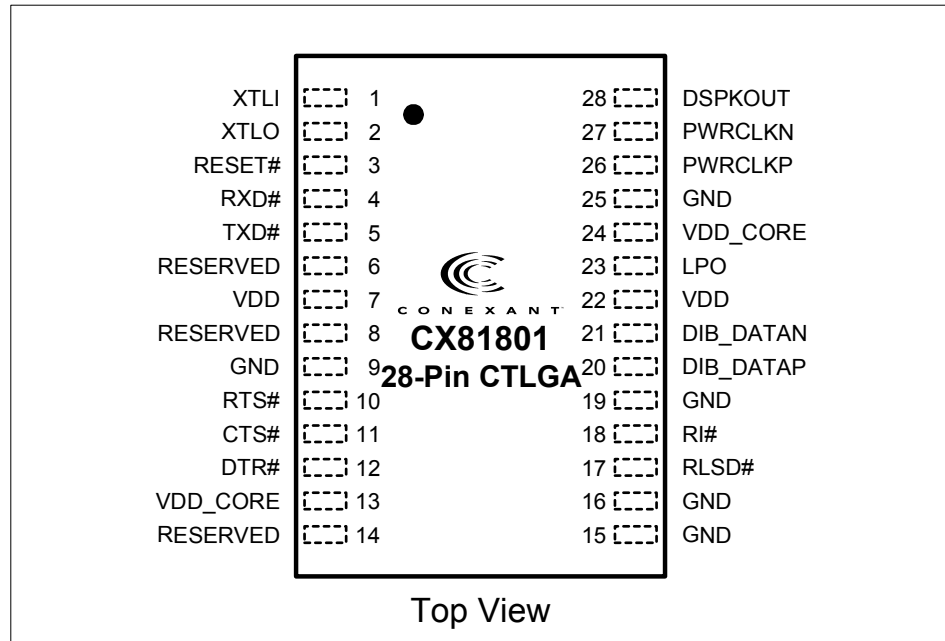
102179_003

Table 3-1. CX81801 Modem 28-Pin CTLGA with Serial Interface Pin Signals

Pin No.	Signal Name	Pin No.	Signal Name
1	XTLI	15	GND
2	XTLO	16	GND
3	RESET#	17	RLSD#
4	RXD#	18	RI#
5	TXD#	19	GND
6	RESERVED	20	DIB_DATAP
7	VDD	21	DIB_DATAN
8	RESERVED	22	VDD
9	GND	23	LPO
10	RTS#	24	VDD_CORE
11	CTS#	25	GND
12	DTR#	26	PWRCLKP
13	VDD_CORE	27	PWRCLKN
14	RESERVED	28	DSPKOUT

Table 3-2. CX81801 Modem 28-Pin CTLGA with Serial Interface Pin Signal Definitions

Label	Pin	I/O	I/O Type	Signal Name/Description
System				
XTLI XTLO	1 2	I O	Ix, Ox	**Crystal In and Crystal Out.** Connect XTLI and XTLO to the external 28.224 MHz ± 50 ppm crystal circuit.
RESET#	3	I	It	**Reset.** The active low RESET# input resets the modem logic and clears the internal SRAM. RESET# low holds the modem in the reset state; RESET# going high releases the modem from the reset state. After application of VDD, RESET# must be held low for at least 15 ms after the VDD power reaches operating range. The modem device set is ready to use 25 ms after the low-to-high transition of RESET#.
VDD	7, 22	P	PWR	**Digital Supply Voltage.** Connect to VCC (+3.3V, filtered).
VDD_CORE	13, 24	P	PWR	**Core Voltage.**
GND	9, 15, 16, 19, 25	G	GND	**Digital Ground.** Connect to digital ground (GND).
LPO	23	I	I/O	**Low Power Oscillator.** Connect to +3.3V through 240 KΩ.
Speaker Interface				
DSPKOUT	28	O	It/Ot2	**Modem Speaker Digital Output.** The DSPKOUT digital output reflects the received analog input signal digitized to TTL high or low level by an internal comparator.
DIB Interface				
PWRCLKP	26	O	Odpc	**Clock and Power Positive.** Provides clock and power to the LSD. Connect to DIB transformer primary winding non-dotted terminal.
PWRCLKN	27	O	Odpc	**Clock and Power Negative.** Provides clock and power to the LSD. Connect to DIB transformer primary winding dotted terminal.
DIB_DATAP	20	I/O	Idd/Odd	**Data Positive.** Transfers data, control, and status information between the CX81801 and the LSD. Connect to LSD through DIB data positive channel components.
DIB_DATAN	21	I/O	Idd/Odd	**Data Negative.** Transfers data, control, and status information between the CX81801 and the LSD. Connect to LSD through DIB data negative channel components.

Table 3-2. CX81801 Modem 28-Pin CTLGA with Serial Interface Pin Signal Definitions (Continued)

Label	Pin	I/O	I/O Type	Signal Name/Description
				V.24 (EIA/TIA-232-E) DTE Serial Interface
TXD#	5	I	It/Ot2	**Transmitted Data (EIA BA/ITU-T CT103).** The DTE uses the TXD# line to send data to the modem for transmission over the telephone line or to transmit commands to the modem.
RXD#	4	O	It/Ot2	**Received Data (EIA BB/ITU-T CT104).** The modem uses the RXD# line to send data received from the telephone line to the DTE and to send modem responses to the DTE. During command mode, RXD# data represents the modem responses to the DTE.
CTS#	11	O	Ith/Ot8	**Clear To Send (EIA CB/ITU-T CT106).** CTS# output ON (low) indicates that the modem is ready to accept data from the DTE. In error correction or normal mode, CTS# is always ON (low) unless RTS/CTS flow control is selected by the &Kn command.
RLSD#	17	O	Ith/Ot8	**Received Line Signal Detector (EIA CF/ITU-T CT109).** When AT&C0 command is not in effect, RLSD# output is ON when a carrier is detected on the telephone line or OFF when carrier is not detected.
RI#	18	O	Ith/Ot8	**Ring Indicator (EIA CE/ITU-T CT125).** RI# output ON (low) indicates the presence of an ON segment of a ring signal on the telephone line.
DTR#	12	I	It	**Data Terminal Ready (EIA CD/ITU-T CT108).** The DTR# input is turned ON (low) by the DTE when the DTE is ready to transmit or receive data. DTR# ON prepares the modem to be connected to the telephone line, and maintains the connection established by the DTE (manual answering) or internally (automatic answering). DTR# OFF places the modem in the disconnect state under control of the &Dn and &Qn commands.
RTS#	10	I	Ithpu	**Request To Send (EIA CA/ITU-T CT105).** RTS# input ON (low) indicates that the DTE is ready to send data to the modem. In the command state, the modem ignores RTS#. The modem ignores RTS# unless RTS/CTS flow control is selected by the &Kn command.
				Reserved
RESERVED	14			**Reserved.** Connect to GND.
RESERVED	6, 8			**Reserved.** Leave open.
Note: I/O Types: See Table 3-5.				

3.1.3   CX81801 Modem 38-Pin CTLGA with Parallel Interface Signal Summary

3.1.3.1   LSD Interface (Through DIB)

The DIB interface signals are:

- Clock and Power Positive (PWRCLKP); output
- Clock and Power Negative (PWRCLKN); output
- Data Positive (DIB_DATAP); input/output
- Data Negative (DIB_DATAN); input/output

3.1.3.2   Call Progress Speaker Interface

The call progress speaker interface signal is:

- Digital speaker output (DSPKOUT); output

3.1.3.3   Serial EEPROM Interface

The 2-line serial interface signals to an optional serial EEPROM are:

- Bidirectional Data input/output (NVMDATA)
- Clock output (NVMCLK)

The EEPROM can hold information such as firmware customization, and country code parameters. Data stored in EEPROM takes precedence over the factory default settings. The serial EEPROM is required only if additional storage is required for country profiles or for firmware customization.

The EEPROM size can range from 2 Kb (256 x 8) to 256 Kb (32K x 8). A 2 Kb EEPROM must support a clock frequency of 100 kHz or 400 kHz; higher capacity EEPROMs must support a clock frequency be 400 kHz.

3.1.3.4   Parallel Host Bus Interface

The parallel host interface signals are:

- Host Reset control input line (RESET#)
- Host Chip Select control input (HCS#)
- Host Read control input (HRD#) and Host Write control input (HWT#)
- Host Interrupt output line (HINT)
- Three Host Address input lines (HA0-HA2)
- Eight Host Data lines (HD0-HD7)

3.1.4 CX81801 Modem 38-Pin CTLGA with Parallel Interface Pin Assignments and Signal Definitions

CX81801 Modem 38-pin CTLGA hardware interface signals are shown by major interface in Figure 3-3 are shown by pin number in Figure 3-4, and are listed by pin number in Table 3-3.

CX81801 Modem hardware interface signals are defined in Table 3-4.

Figure 3-3. CX81801 Modem 38-Pin CTLGA with Parallel Interface Hardware Signals
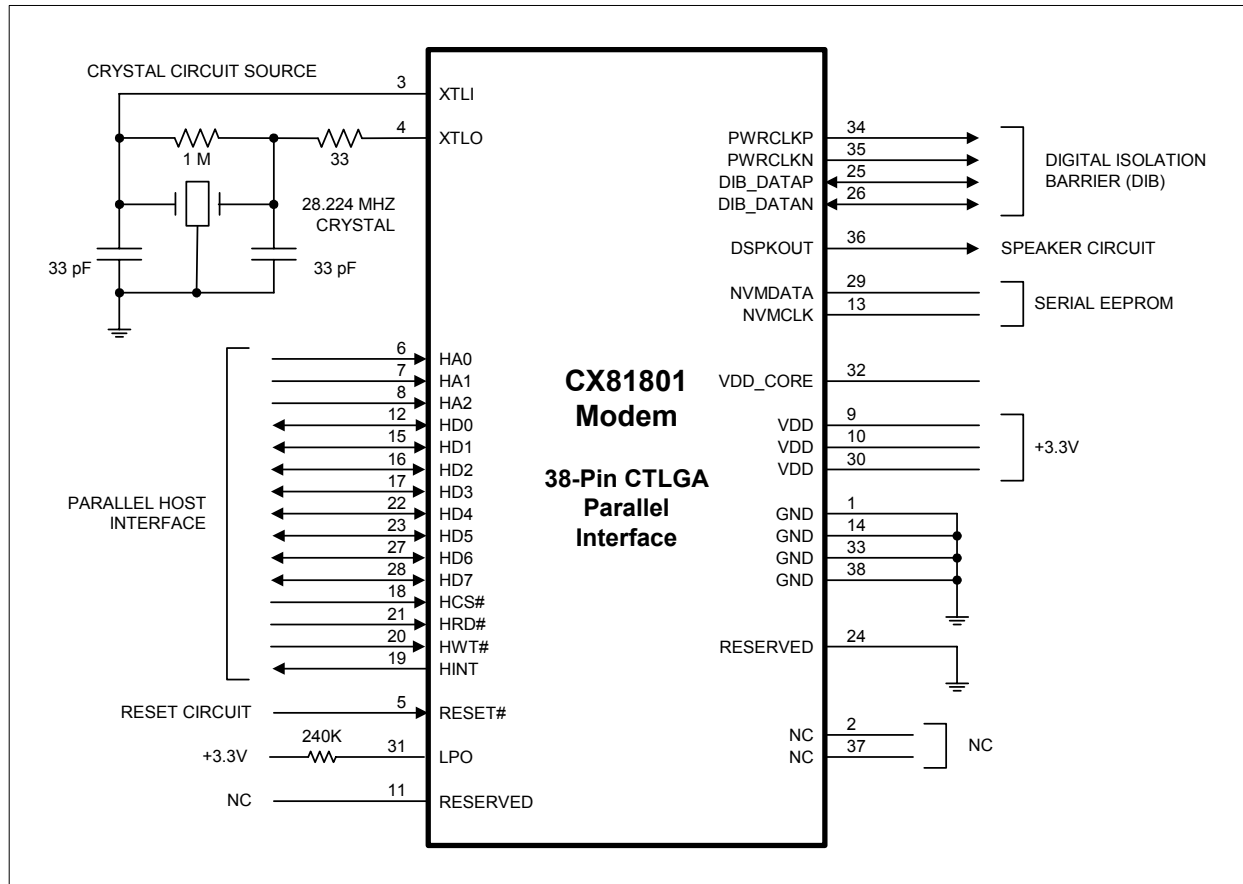
102179_004

Figure 3-4. CX81801 Modem 38-Pin CTLGA with Parallel Interface Pin Signals
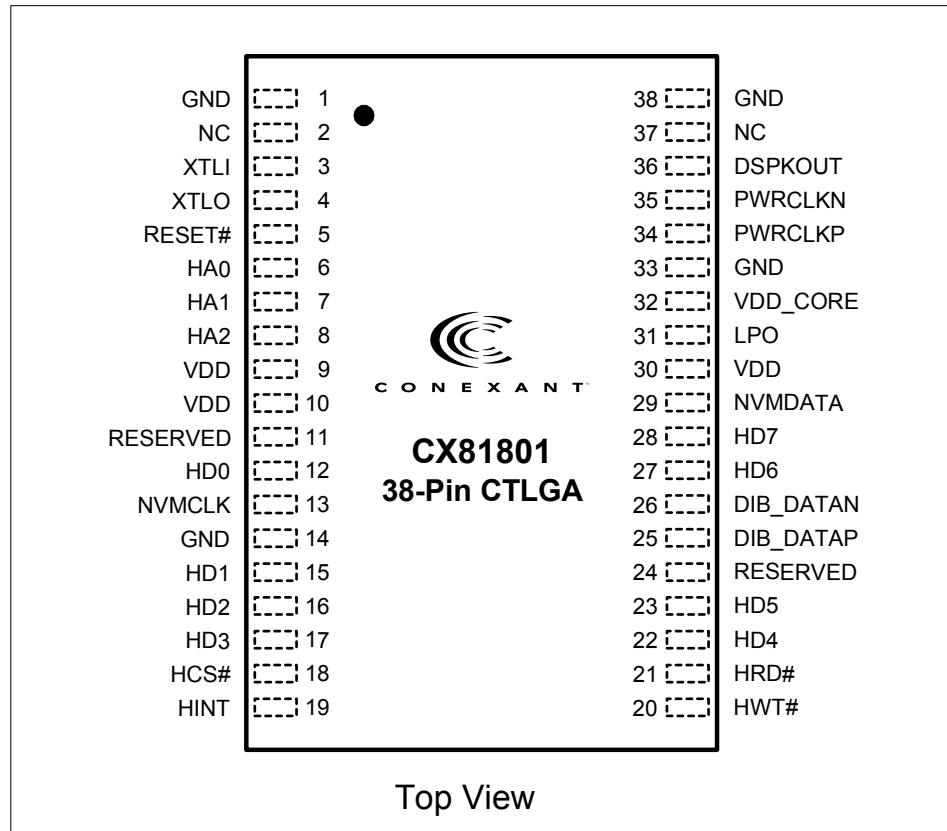
Table 3-3. CX81801 Modem 38-Pin CTLGA with Parallel Interface Pin Signals

Pin No.	Signal Name	Pin No.	Signal Name
1	GND	20	HWT#
2	NC	21	HRD#
3	XTLI	22	HD4
4	XTLO	23	HD5
5	RESET#	24	RESERVED
6	HA0	25	DIB_DATAP
7	HA1	26	DIB_DATAN
8	HA2	27	HD6
9	VDD	28	HD7
10	VDD	29	NVMDATA
11	RESERVED	30	VDD
12	HD0	31	LPO
13	NVMCLK	32	VDD_CORE
14	GND	33	GND
15	HD1	34	PWRCLKP
16	HD2	35	PWRCLKN
17	HD3	36	DSPKOUT
18	HCS#	37	NC
19	HINT	38	GND

Table 3-4. CX81801 Modem 38-Pin CTLGA with Parallel Interface Hardware Signal Definitions

Label	Pin	I/O	I/O Type	Signal Name/Description
System				
XTLI XTLO	3 4	I O	Ix, Ox	**Crystal In and Crystal Out.** Connect XTLI and XTLO to the external 28.224 MHz $\pm$ 50 ppm crystal circuit.
RESET#	5	I	It	**Reset.** The active low RESET# input resets the modem logic and clears the internal SRAM. RESET# low holds the modem in the reset state; RESET# going high releases the modem from the reset state. After application of VDD, RESET# must be held low for at least 15 ms after the VDD power reaches operating range. The modem device set is ready to use 25 ms after the low-to-high transition of RESET#.
VDD_CORE	32	P	PWR	**Core Supply Voltage.** Internal +1.8 V core voltage for decoupling. Do not connect this pin to an external +1.8 V power supply.
VDD	9, 10, 30	P	PWR	**Digital Supply Voltage.** Connect to +3.3V.
GND	1, 14, 33, 38	G	GND	**Digital Ground.** Connect to digital ground (GND).
LPO	31	I	I/O	**Low Power Oscillator.** Connect to +3.3V through 240 KΩ.
Speaker Interface				
DSPKOUT	36	O	It/Ot2	**Modem Speaker Digital Output.** The DSPKOUT digital output reflects the received analog input signal digitized to TTL high or low level by an internal comparator.
DIB Interface				
PWRCLKP	34	O	Odpc	**Clock and Power Positive.** Provides clock and power to the LSD. Connect to DIB transformer primary winding non-dotted terminal.
PWRCLKN	35	O	Odpc	**Clock and Power Negative.** Provides clock and power to the LSD. Connect to DIB transformer primary winding dotted terminal.
DIB_DATAP	25	I/O	Idd/Odd	**Data Positive.** Transfers data, control, and status information between the CX81801 and the LSD. Connect to LSD through DIB data positive channel components.
DIB_DATAN	26	I/O	Idd/Odd	**Data Negative.** Transfers data, control, and status information between the CX81801 and the LSD. Connect to LSD through DIB data negative channel components.
NVRAM Interface				
NVMCLK	13	O	It/Ot2	**NVRAM Clock.** During normal operation, NVMCLK output high enables the EEPROM. Connect to EEPROM SCL pin.
NVMDATA	29	I/O	It/Ot2	**NVRAM Data.** The NVMDATA pin supplies a serial data interface to the EEPROM. Connect to EEPROM SDA pin and to +3.3V through 10 KΩ.

Table 3-4. CX81801 Modem 38-Pin CTLGA with Parallel Interface Hardware Signal Definitions (Continued)

Label	Pin	I/O	I/O Type	Signal Name/Description
Parallel Host Interface				
HCS#	18	I	It	**Host Bus Chip Select.** HCS# input low enables the MCU host bus interface.
HWT#	20	I	Ithpu	**Host Bus Write.** HWT# is an active low, write control input. When HCS# is low, HWT# low allows the host to write data or control words into a selected MCU register.
HRD#	21	I	Ithpu	**Host Bus Read.** HRD# is an active low, read control input. When HCS# is low, HRD# low allows the host to read status information or data from a selected MCU register.
HINT	19	O	It/Ot8	**Host Bus Interrupt.** HINT output is set high when the receiver error flag, received data available, transmitter holding register empty, or modem status interrupt is asserted. HINT is reset low upon the appropriate interrupt service or master reset operation.
HA0-HA2	6-8	I	Ithpd/Ot2	**Host Bus Address Lines 0-2.** During a host read or write operation with HCS# low, HA0-HA2 select an internal MCU 16550A-compatible register.
HD0-HD7	12, 15-17, 22, 23, 27, 28	I/O	Ith/Ot8	**Host Bus Data Lines 0-7**. HD0-HD7 are three-state input/output lines providing bidirectional communication between the host and the MCU. Data, control words, and status information are transferred over HD0-HD7.
Reserved				
RESERVED	24			**Reserved.** Connect to digital ground (GND).
RESERVED	11			**Reserved.** Leave open or connect to digital ground (GND).
No Connect				
NC	2, 37			**No Internal Connection.** Leave open.
Note: I/O Types: See Table 3-5.				

3.1.5 Electrical Characteristics

I/O types are defined in Table 3-5.

DC electrical characteristics are listed in Table 3-6.

Table 3-5. CX81801 Modem I/O Type Definitions

I/O Type	Description
Idd/Odd	Digital input/output, DIB data transceiver
Ix/Ox	I/O, wire
It/Ot2	Digital input / Digital output, 2 mA, Z_{INT} = 120 Ω
Itpu/Ot2	Digital input, 75k Ω pull up/ Digital output, 2 mA, Z_{INT} = 120 Ω
Ith/Ot8	Digital input, hysteresis/Digital output, 8 mA, Z_{INT} = 50 Ω
It	Digital input
Ith	Digital input, hysteresis
Itpu	Digital input, 75k Ω pull up
Ithpu	Digital input, hysteresis, 75k Ω pull up
Odpc	Digital output with adjustable drive, DIB clock and power
PWR	VCC Power
GND	Ground

NOTES:
1. See DC characteristics in Table 3-6.
2. I/O Type corresponds to the device Pad Type. The I/O column in signal interface tables refers to signal I/O direction used in the application.

Table 3-6. CX81801 Modem DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Voltage Low	VIL	0	–	0.3 *VDD	V	
Input Voltage High	VIH	0.7 * VDD	–	5.25	V	
Input Hysteresis	VH	0.3	–		V	
Output Voltage Low	VOL					
Z_{INT} = 150 Ω		0	–	0.4	V	IOL = 1.6 mA
Z_{INT} = 120 Ω		0	–	0.4	V	IOL = 2 mA
Z_{INT} = 50 Ω		0	–	0.4	V	IOL = 8 mA
Output Voltage High	VOH		–		V	
Z_{INT} = 150 Ω		2.4	–	VDD	V	IOL = -1.6 mA
Z_{INT} = 120 Ω		2.4	–	VDD	V	IOL = -2 mA
Z_{INT} = 50 Ω		2.4	–	VDD	V	IOL = -8 mA
Pull-Up Resistance	Rpu	50	–	200	kΩ	
Pull-Down Resistance	Rpd	50	–	200	kΩ	

Test Conditions unless otherwise stated: VDD = +3.3 ± 0.3 VDC; TA = 0°C to 70°C; external load = 50 pF.

3.2　　　CX20493 LSD Hardware Pins and Signals

3.2.1　　　CX20493 LSD Signal Summary

3.2.1.1　　　CX81801 Interface (Through DIB)

The DIB interface, power, and ground signals are:

- Clock (CLK, pin 26); input
- Digital Power (PWR+, pin 7); unregulated input power
- Regulated Digital Voltage Supply (DVdd, pin 24)
- Digital Ground (DGnd, pin 23); digital ground
- Regulated Analog Voltage Supply (AVdd, pin 2)
- Analog Ground (AGnd, pin 6); analog ground
- Data Positive (DIB_P, pin 27); input/output
- Data Negative (DIB_N, pin 28); input/output

3.2.1.2　　　Telephone Line Interface

The telephone line interface signals are:

- RING 1 AC Coupled (RAC1, pin 21); input
- TIP 1 AC Coupled (TAC1, pin 20); input
- RING 2 AC Coupled (RAC2, pin 19); input
- TIP 2 AC Coupled (TAC2, pin 18); input
- TIP and RING DC Measurement (TRDC, pin 12); input
- Electronic Inductor Capacitor (EIC, pin 11)
- Electronic Inductor Output (EIO, pin 17)
- Electronic Inductor Feedback (EIF, pin 16)
- Receive Analog Input (RXI, pin 9); input
- Transmit Output (TXO, pin 14); output
- Transmit Feedback (TXF, pin 13); input
- Virtual Impedance 0 (VZ, pin 10); input
- Electronic Inductor Ground (DC_GND, pin 15)

3.2.1.3　　　Voltage References

There are three reference voltage pins:

- Output Middle (Center) Reference Voltage (Vc, pin 3); output for decoupling
- Output Reference Voltage (VRef, pin 4); output for decoupling
- Bias Resistor (RBias, pin 5); input

3.2.1.4 General Purpose Input/Output

There is one unassigned general purpose input/output pin:

- General Purpose Input/Output 1 (GPIO1, pin 1); input/output

3.2.1.5 No Connects

Three pins are not used:

- No Connect 1 (NC1, pin 8); no internal connection
- No Connect 2 (NC2, pin 22); no internal connection
- No Connect 3 (NC3, pin 25); no internal connection

3.2.2 CX20493 LSD Pin Assignments and Signal Definitions

CX20493 LSD hardware interface signals are shown by major interface in Figure 3-5, are shown by pin number in Figure 3-6, and are listed by pin number in Table 3-7.

CX20493 LSD hardware interface signals are defined in Table 3-8.

CX20493 LSD GPIO DC electrical characteristics are specified in Table 3-9.

CX20493 LSD AVdd DC electrical characteristics are listed in Table 3-10.

Figure 3-5. CX20493 LSD Hardware Interface Signals
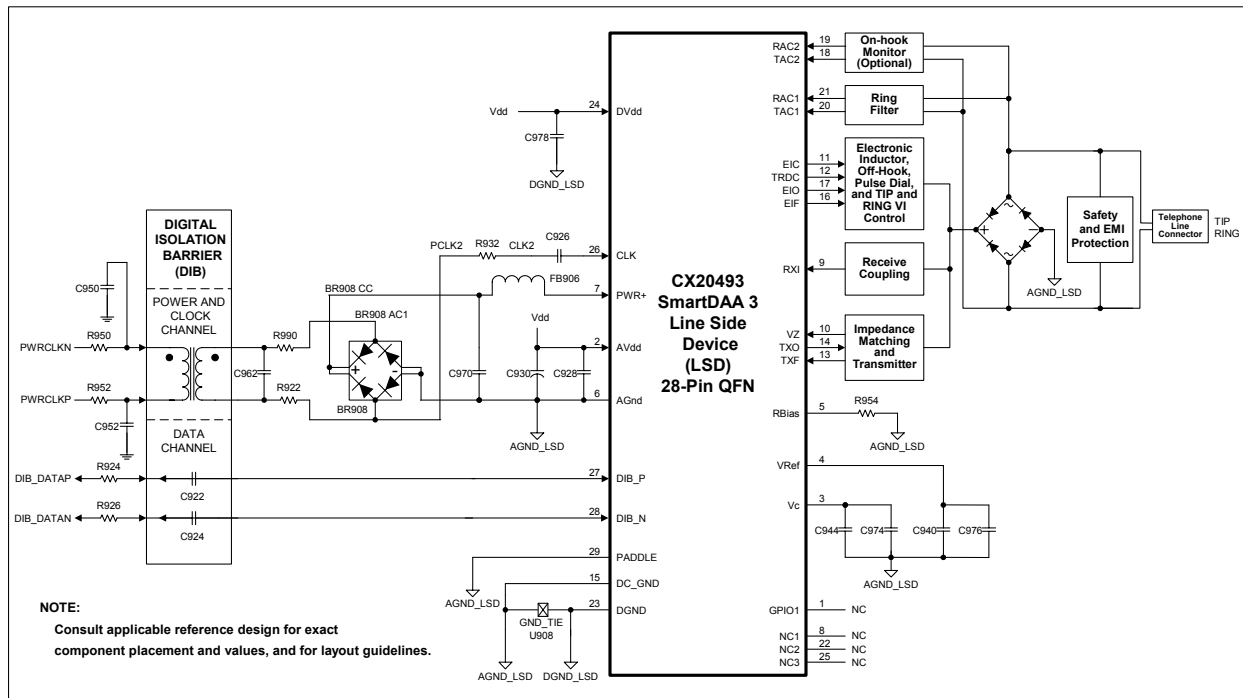
Figure 3-6. CX20493 LSD 28-Pin QFN Pin Signals
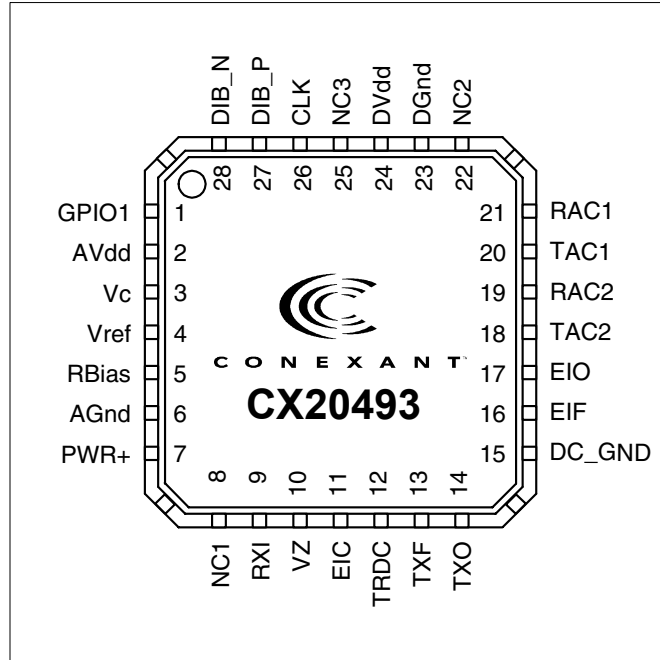
101701A_007

Table 3-7. CX20493 LSD 28-Pin QFN Pin Signals

Pin	Signal Label	Pin	Signal Label
1	GPIO1	15	DC_GND
2	AVdd	16	EIF
3	Vc	17	EIO
4	VRef	18	TAC2
5	RBias	19	RAC2
6	AGnd	20	TAC1
7	PWR+	21	RAC1
8	NC1	22	NC2
9	RXI	23	DGnd
10	VZ	24	DVdd
11	EIC	25	NC3
12	TRDC	26	CLK
13	TXF	27	DIB_P
14	TXO	28	DIB_N

Table 3-8. CX20493 LSD Hardware Signal Definitions

Label	Pin	I/O	I/O Type	Signal Name/Description
System Signals				
AVdd	2	PWR	PWR	**Regulated Power Output.** Provides external power for LSD digital circuits and a connection point for external decoupling. (AVdd is routed internally to LSD analog circuits.) See PWR+ pin description. Connect to LSD DVdd pin and connect to AGND_LSD through C928 and C930 in parallel. C928 and C930 must be placed close to pins 2 and 6. C930 must have ESR < 2 Ω.
AGnd	6	AGND_LSD	AGND_LSD	**Analog Ground.** Connect to minus (-) terminal of full wave rectifier (FWR). Connect FWR BR980 terminal to DIB transformer secondary winding undotted terminal through R922.
VRef	4	REF	REF	**Output Reference Voltage.** Connect to AGND_LSD through C940 and C976, which must be placed close to pin 4. Ensure a very close proximity between C940 and the VRef pin. C940 must have a maximum ESR of 2 Ω.
Vc	3	REF	REF	**Output Middle Reference Voltage.** Connect to AGND_LSD through C944 and C974, which must be placed close to pin 3. Ensure a very close proximity between C944 and the Vc pin. Use a short path and a wide trace to AGND_LSD pin.
PWR+	7	PWR	PWR	**Unregulated Power Input.** Provides unregulated input power to the LSD. PWR+ pin is an input which takes unregulated +3.2V to +4.5V from the DIB power supply made up of the transformer, full-wave rectifier, and filter capacitors. The PWR+ input is regulated by an internal linear regulator to +3.3V ± 5% which is routed to the AVdd pin. If PWR+ is less than +3.4V, then AVdd is equal to the unregulated PWR+ input value minus 150 mV (Table 3-10). Connect to plus (+) terminal of FWR. Connect terminal BR908 AC1 to DIB transformer secondary winding dotted terminal through R990. Connect transformer side of FB906 to AGND_LSD though C970. Place FB906 and C970 close to pin 7 and pin 6 (AGnd).
DVdd	24	PWR	PWR	**Digital Power Input.** Input power for LSD digital circuits. Connect to LSD AVdd pin and connect to DGND_LSD through C978. Place C978 near pin 24.
DGnd	23	DGND_LSD	DGND_LSD	**LSD Digital Ground.** Connect to DGND_LSD, and to AGND_LSD at the DGND_LSD/AGND_LSD tie point (U908).
PADDLE	—	AGND_LSD	AGND_LSD	**Paddle Ground.** Referred to as pin 29 in schematics. Connect to AGND_LSD.
DIB Interface Signals				
CLK	26	I	I	**Clock.** Provides input clock, AC coupled to the LSD. Connect to DIB transformer secondary winding undotted terminal through C926 (closest to the CX20493), R932, then R922 in series. Connect the R932 and R922 node to LSD AGND pin through full-wave rectifier BR908. Place C926 near pin 26 and place R932 near C926.
DIB_P	27	I/O	I/O	**Data and Control Positive.** Connect to DIBDAT_P through R924 in series with C922. DIB_P and DIB_N signals are differential and half-duplex bidirectional.
DIB_N	28	I/O	I/O	**Data and Control Negative.** Connect to DIBDAT_N through R926 in series with C924. DIB_P and DIB_N signals are differential and half-duplex bidirectional.

Table 3-8. CX20493 LSD Hardware Signal Definitions (Continued)

Label	Pin	I/O	I/O Type	Signal Name/Description
				**TIP and RING Interface**
RAC1 TAC1	21 20	I I	Ia Ia	**RING1 AC Coupled and TIP1 AC Coupled.** AC-coupled voltage from telephone line used to detect ring. Connect RAC1 to the diode bridge AC node (RING) through R902 (connects to pin 21) and C902 in series. Connect TAC1 to the diode bridge AC node (TIP) through R904 (connects to pin 20) and C904 in series.
RAC2 TAC2	19 18	I I	Ia Ia	**RING2 AC Coupled and TIP2 AC Coupled.** AC-coupled voltage from telephone line used to optionally detect signal while on-hook. Connect RAC2 to the diode bridge AC node (RING) through R948 (connects to pin 19) and C948. Leave open if not used. Connect TAC2 to the diode bridge AC node (TIP) through R946 (connects to pin 21) and C946. Leave open if not used.
EIC	11	O	Oa	**Electronic Inductor Capacitor Switch.** Internally switched to TRDC when pulse dialing. Connect to AGND_LSD through C958.
TRDC	12	I	Ia	**TIP and RING DC Measurement.** Input on-hook voltage (from a resistive divider). Used internally to extract TIP and RING DC voltage and Line Polarity Reversal (LPR) information. R906 and C918 must be placed very close to pin 12.
EIO	17	O	Oa	**Electronic Inductor Output.** Calculated voltage is applied to this output to control off-hook and DC VI mask operation. Connect to base of Q902.
DC_GND	15	GND	AGND_LSD	**LSD Electronic Inductor Ground.** Connect to AGND_LSD and to the GND_LSD/AGND_LSD tie point (U908).
EIF	16	I	Ia	**Electronic Inductor Feedback.** Connect to emitter of Q904 through R968.
RXI	9	I	Ia	**Receive Analog Input.** Receiver operational amplifier inverting input. AC coupled to the Bridge CC node through R910 (connects to pin 9) and C912 in series. R910 and C912 must be placed very close to pin 9. The length of the PCB trace connecting R910 to the RXI pin must be kept at an absolute minimum.
RBias	5	I	Ia	**Receiver Bias.** Connect to AGND_LSD through R954, which must be placed close to pin 5.
VZ	10	I	Ia	**Virtual Impedance.** Input signal used to provide line complex impedance matching for worldwide countries. AC coupled to Bridge CC node through R908 (connects to pin 10) and C910 in series. R908 and C910 must be placed very close to pin 10. The length of the PCB trace connecting R908 to the VZ pin must be kept at an absolute minimum.
TXO	14	O	Oa	**Transmit Output.** Outputs transmit signal and impedance matching signal; connect to base of transmitter transistor Q906.
TXF	13	I	Ia	**Transmit Feedback.** Connect to emitter of transmitter transistor Q906.
				**Not Used**
GPIO1	1	I/O	It/Ot12	**General Purpose I/O 1.** Leave open if not used.
NC1	8			**No Connect.** No internal connection. Leave open.
NC2	22			**No Connect.** No internal connection. Leave open.
NC3	25			**No Connect.** No internal connection. Leave open.

Notes:

1. I/O types*:

Ia	Analog input
It	Digital input, TTL-compatible
Oa	Analog output
Ot12	Digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω
AGND_LSD	Isolated LSD Analog Ground
GND_LSD	Isolated LSD Digital Ground

*See CX20493 LSD GPIO DC Electrical Characteristics (Table 3-9)

2. Refer to applicable reference design for exact component placement and values.

Table 3-9. CX20493 LSD GPIO DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Voltage	V_{IN}	-0.30	–	3.465	V	DVdd = +3.465V
Input Voltage Low	V_{IL}	–	–	1.0	V	
Input Voltage High	V_{IH}	1.6	–	–	V	
Output Voltage Low	V_{OL}	0	–	0.33	V	
Output Voltage High	V_{OH}	2.97	–	–	V	
Input Leakage Current	–	-10	–	10	µA	
Output Leakage Current (High Impedance)	–	-10	–	10	µA	
GPIO Output Sink Current at 0.33 V maximum	–	2.4	–	-	mA	
GPIO Output Source Current at 2.97 V minimum	–	2.4	–	-	mA	
GPIO Rise Time/Fall Time		20		100	ns	
Test Conditions unless otherwise stated: DVdd = +3.3V +5%; TA = 0°C to 70°C; external load = 50 pF						

Table 3-10. CX20493 AVdd DC Electrical Characteristics

PWR+ Input	AVdd Output
+3.4V < PWR+ < +4.5V	+3.3V ± 5%
+3.2V < PWR+ < +3.39V	3.05V < AVdd < 3.24V
See PWR+, AVdd, and DVdd descriptions in Table 3-8.	

3.3　Electrical and Environmental Specifications

3.3.1　Operating Conditions, Absolute Maximum Ratings, and Power Requirements

The operating conditions are specified in Table 3-11.

The absolute maximum ratings are listed in Table 3-12.

The current and power requirements are listed in Table 3-13.

Table 3-11. Operating Conditions

Parameter	Symbol	Limits	Units
Supply Voltage	VDD	+3.0 to +3.6	VDC
Operating Ambient Temperature	T_A	0 to +70	°C

Table 3-12. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	VDD	-0.5 to +4.0	VDC
Input Voltage	V_{IN}	-0.5 to +5.5	VDC
Storage Temperature Range	T_{STG}	-55 to +125	°C
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.5 to +5.5	VDC
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	V_{ESD}	±2500	VDC
Latch-up Current (25°C)	I_{TRIG}	±400	mA

Handling CMOS Devices

The device contains circuitry to protect the inputs against damage due to high static voltages. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage.

An unterminated input can acquire unpredictable voltages through coupling with stray capacitance and internal cross talk. Both power dissipation and device noise immunity degrades. Therefore, all inputs should be connected to an appropriate supply voltage.

Input signals should never exceed the voltage range from -0.5V to +5.5V. This prevents forward biasing the input protection diodes and possibly entering a latch up mode due to high current transients.

Table 3-13. Current and Power Requirements

Mode	Typical Current (Ityp) (mA)	Maximum Current (Imax) (mA)	Typical Power (Ptyp) (mW)	Maximum Power (Pmax) (mW)	Notes
Normal Mode: Off-hook, normal data connection	62	71	205	256	f = 28.224 MHz
Normal Mode: On-hook, idle, waiting for ring	60	69	198	248	f = 28.224 MHz
Sleep Mode	18	21	59	76	f = 0 MHz

Notes:

1. Operating voltage: VDD = +3.3V ± 0.3V.
2. Test conditions: VDD = +3.3V for typical values; VDD = +3.6V for maximum values.
3. Input Ripple $\leq$ 0.1 Vpeak-peak.
4. f = Internal frequency.
5. Maximum current computed from Ityp: Imax = Ityp * 1.1.
6. Typical power (Ptyp) computed from Ityp: Ptyp = Ityp * 3.3V;
   Maximum power (Pmax) computed from Imax: Pmax = Imax * 3.6V.

3.3.2 Interface and Timing Waveforms

3.3.2.1 Serial DTE Interface

The serial DTE interface waveforms for 4800 and 9600 bps are illustrated in Figure 3-7.

Figure 3-7. Waveforms - Serial DTE Interface
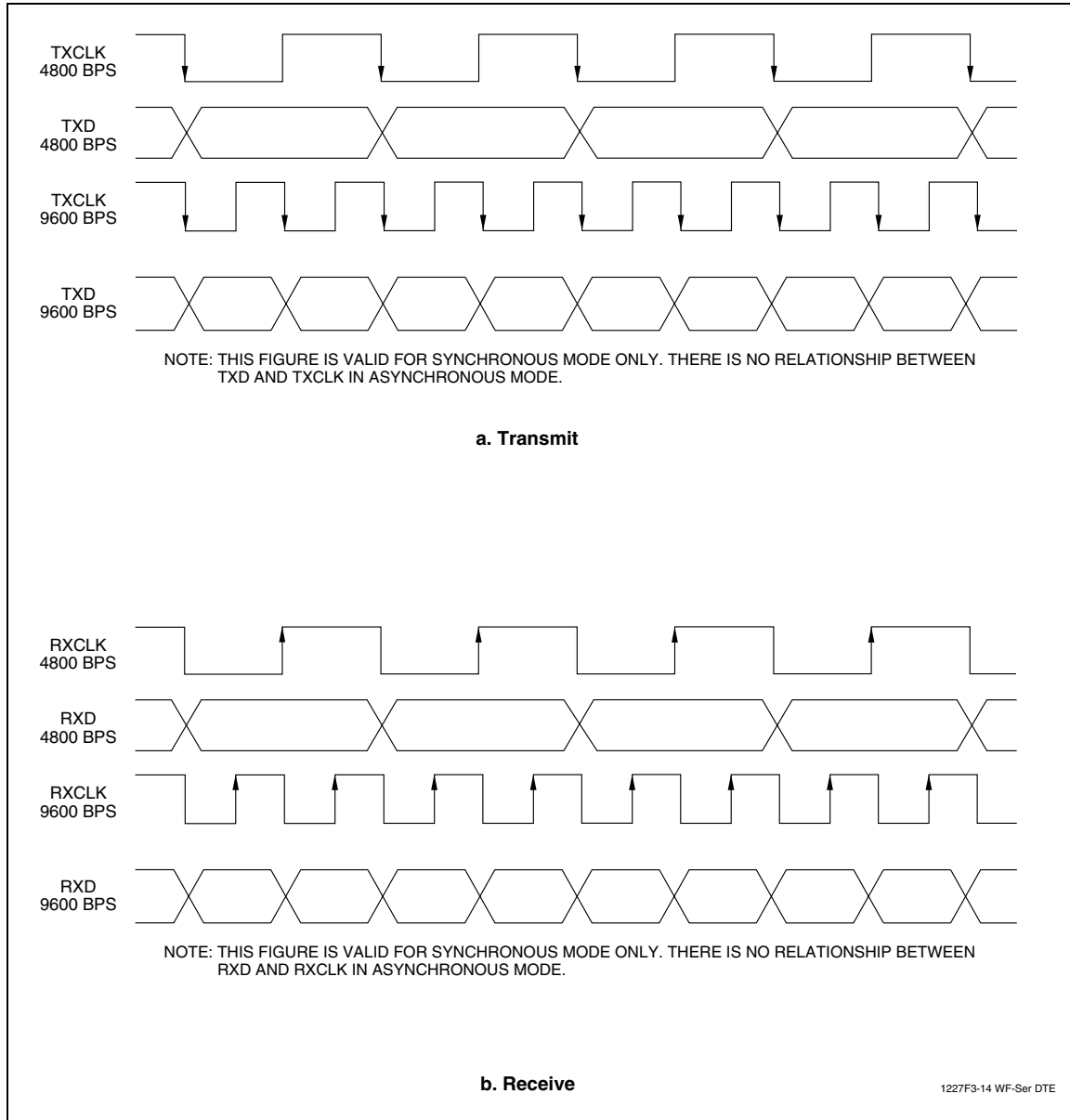
3.3.2.2   Parallel Host Bus Timing

The parallel host bus timing is listed in Table 3-14 and illustrated in Figure 3-8.

Table 3-14. Timing - Parallel Host Bus

Symbol	Parameter	Min	Max	Units
READ (See Notes 1, 2, 3, 4, and 5)				
t_{AS}	Address Setup	5	–	ns
t_{AH}	Address Hold	10	–	ns
t_{CS}	Chip Select Setup	0	–	ns
t_{CH}	Chip Select Hold	10	–	ns
t_{RD}	HRD# Strobe Width	45	–	ns
t_{DD}	Read Data Delay	–	25	ns
t_{DRH}	Read Data Hold	5	–	ns
WRITE (See Notes 1, 2, 3, 4, and 5)				
t_{AS}	Address Setup	5	–	ns
t_{AH}	Address Hold	15	–	ns
t_{CS}	Chip Select Setup	0	–	ns
t_{CH}	Chip Select Hold	10	–	ns
t_{WT}	HWT# Strobe Width	75	–	ns
t_{DS}	Write Data Setup (see Note 4)	–	20	ns
t_{DWH}	Write Data Hold (see Note 5)	5	–	ns

Notes:

1. When the host executes consecutive Rx FIFO reads, a minimum delay of 2 times the internal CPU clock cycle plus 15 ns (85.86 ns at 28.224 MHz) is required from the falling edge of HRD# to the falling edge of the next Host Rx FIFO HRD# clock.

2. When the Host executes consecutive Tx FIFO writes, a minimum delay of 2 times the internal CPU clock cycle plus 15 ns (85.86 ns at 28.224 MHz) is required from the falling edge of HWT# to the falling edge of the next Host Tx FIFO HWT# clock.

3. t_{DS} is measured from the point at which both HCS# and HWT# are active.

4. t_{DWH} is measured from the point at which either HCS# and HWT# become inactive.

5. Clock frequency = 28.224 MHz clock.

Figure 3-8. Waveforms - Parallel Host Bus

a. Host Read

b. Host Write

100491 F3-10 WF-HB
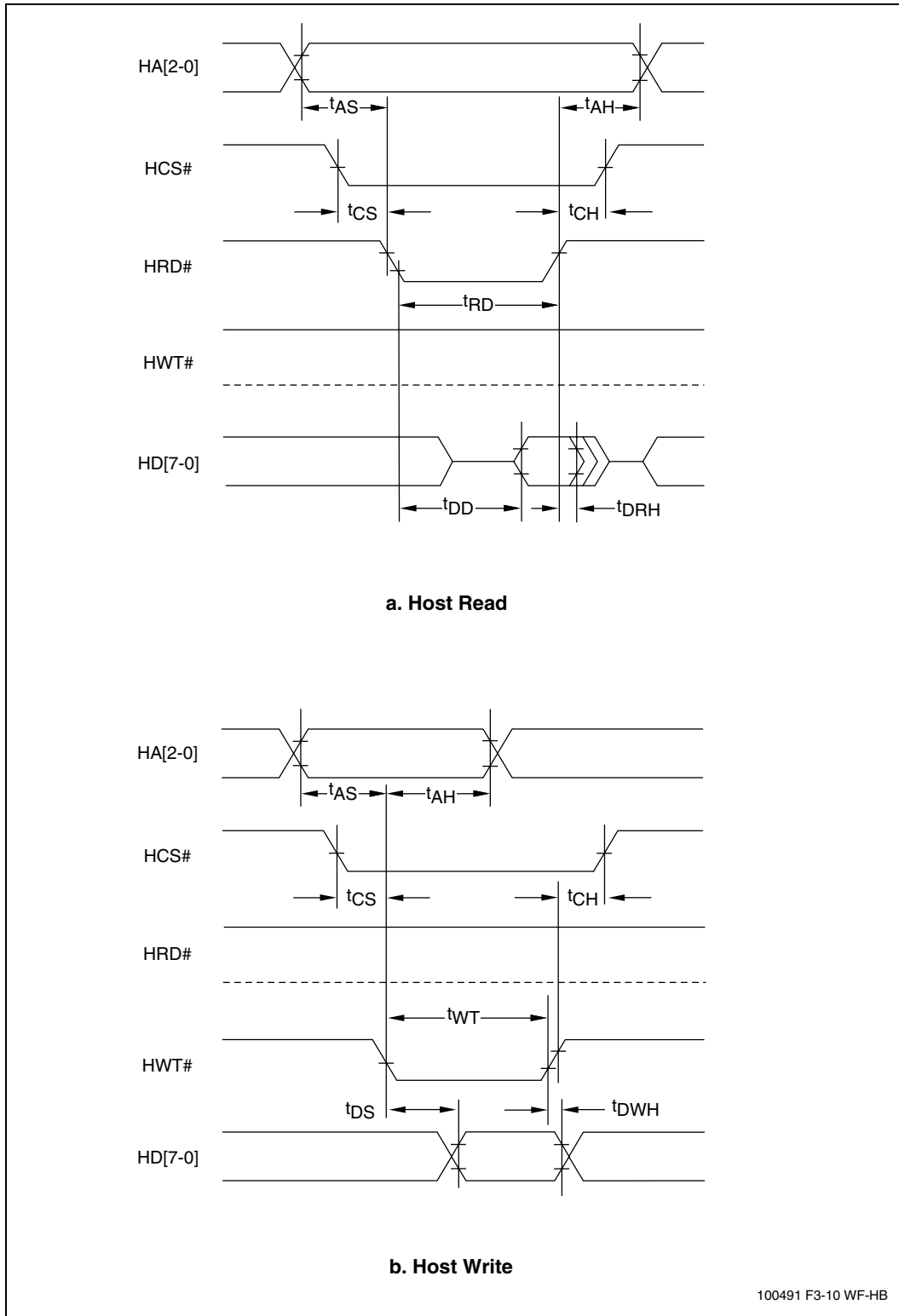
3.4 Crystal Specifications

Crystal specifications are listed in Table 3-15.

Table 3-15. Crystal Specifications

Characteristic	Value
Frequency	28.224 MHz nominal
Calibration Tolerance	±50 ppm at 25°C (C_L = 16.5 and 19.5 pF)
Frequency Stability vs. Temperature	±35 ppm (0°C to 70°C)
Frequency Stability vs. Aging	±20 ppm/5 years
Oscillation Mode	Fundamental
Calibration Mode	Parallel resonant
Load Capacitance, C_L	18 pF nom.
Shunt Capacitance, C_O	7 pF max.
Series Resistance, R_1	35-60 Ω max. @20 nW drive level
Drive Level	100µW correlation; 500µW max.
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to 85°C

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Conexant

4. Package Dimensions

The 28-pin CTLGA package dimensions are shown in Figure 4-1.

The 38-pin CTLGA package dimensions are shown in Figure 4-2.

The 28-pin QFN package dimensions are shown in Figure 4-3.

Figure 4-1. Package Dimensions - 28-Pin CTLGA

Dim.	All Dimensions in Millimeters		
	Min.	**Nom.**	**Max.**
A	0.70	0.80	0.90
A1	----	0.050	----
A2	----	0.028	----
A3	0.55	0.60	0.65
D	6.35	6.40	6.45
E	10.95	11.00	11.05
b	0.35	0.40	0.45
b1	0.65	0.70	0.75
e	0.60	0.65	0.70
L	1.23	1.28	1.33
L1	0.40	0.45	0.50
L2	----	0.95	----
L3	----	0.05	----

FOOTNOTE:
[1] Test Pins are exposed on the bottom of the device. Do not place any exposed traces, vias, test points, or pads in this area.
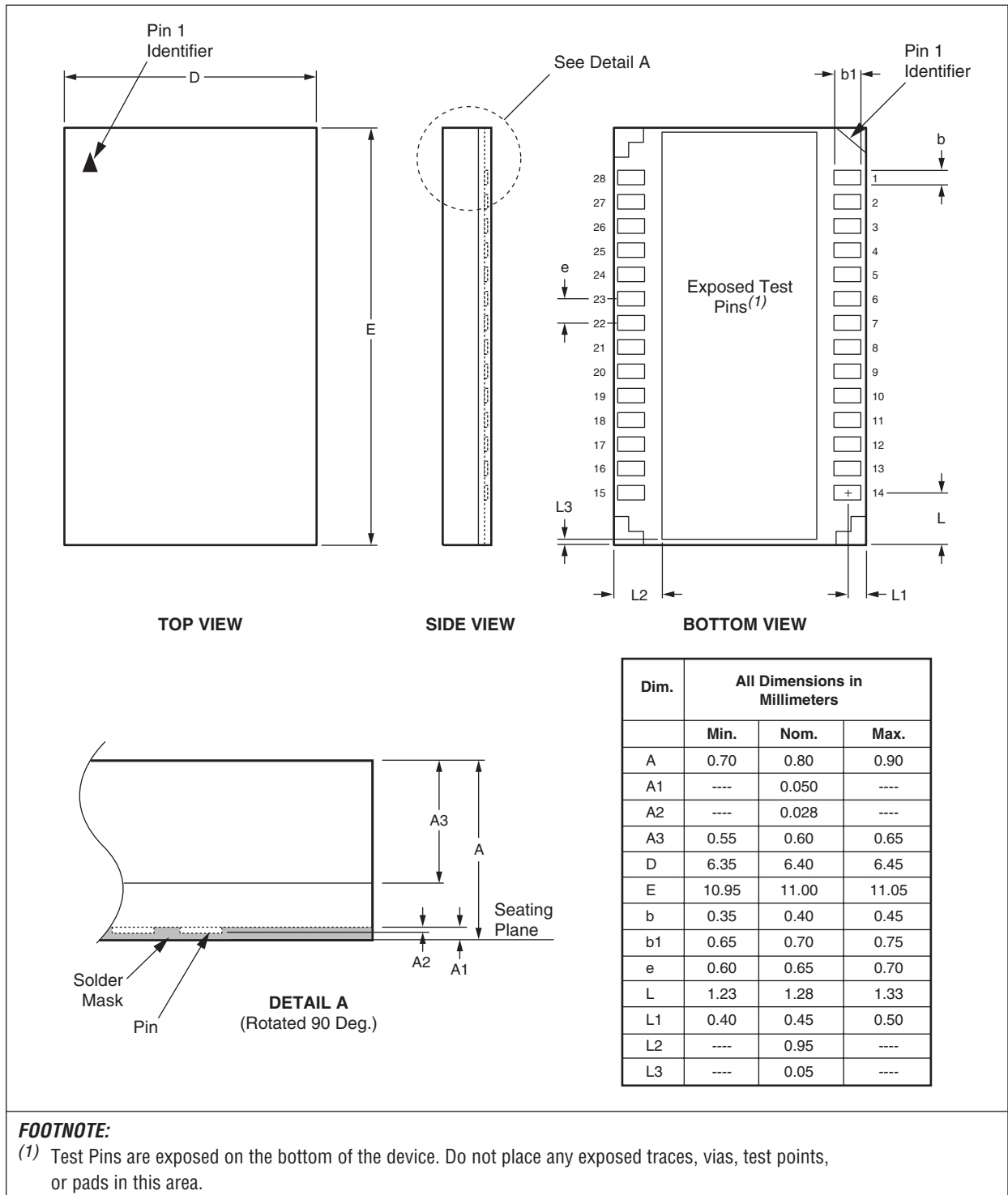
28-Pin CTLGA

Figure 4-2. Package Dimensions - 38-Pin CTLGA

Dim.	All Dimensions in Millimeters		
	Min.	**Nom.**	**Max.**
A	0.70	0.80	0.90
A1	----	0.050	----
A2	----	0.028	----
A3	0.55	0.60	0.65
D	6.35	6.40	6.45
E	10.95	11.00	11.05
b	0.32	0.37	0.42
b1	0.65	0.70	0.75
e	0.45	0.50	0.55
L	0.95	1.00	1.05
L1	0.40	0.45	0.50
L2	----	0.95	----
L3	----	0.05	----

FOOTNOTE:

[1] Test Pins are exposed on the bottom of the device. Do not place any exposed traces, vias, test points, or pads in this area.
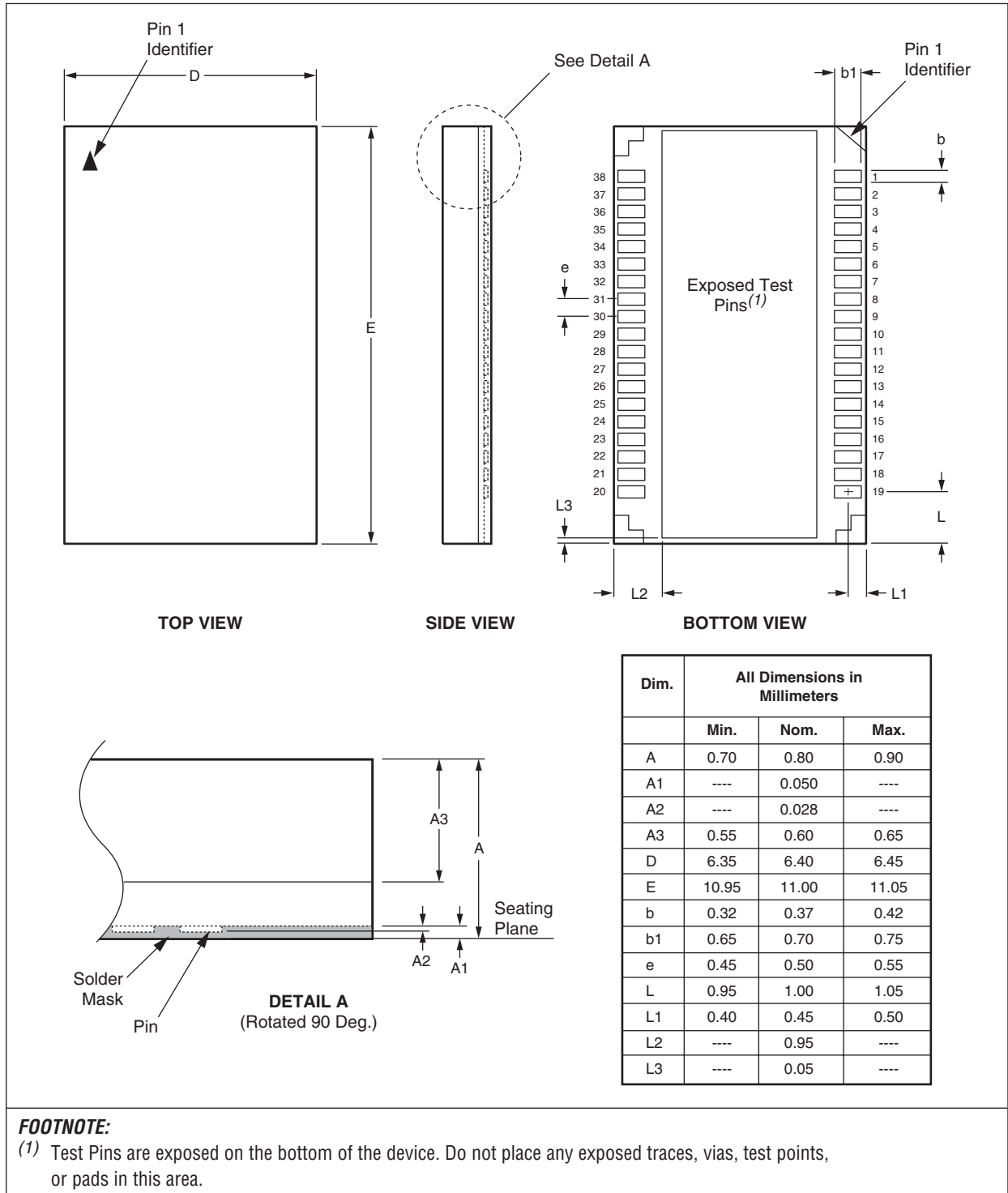
38-Pin CTLGA

Figure 4-3. Package Dimensions - 28-Pin QFN

TOP VIEW

SEATING PLANE

BOTTOM VIEW

SECTION "C-C"
SCALE: NONE

TERMINAL TIP

NOTES:

1. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED
   BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.

2. PACKAGE WARPAGE MAX 0.05mm.

3. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING
   PART OF EXPOSED PAD FROM MEASURING.

Symbol	Dimensions (Millimeters)		
	Min.	Nom.	Max.
e	0.5 BSC		
L	0.50	0.60	0.75
b	0.23	0.28	0.35
D2	2.95	3.10	3.25
E2	2.95	3.10	3.25
A	-	0.85	1.00
A1	0.00	0.01	0.05
A2	-	0.65	0.80
A3	0.15	0.20	0.25
D	4.90	5.00	5.10
D1	4.65	4.75	4.85
E	4.90	5.00	5.10
E1	4.65	4.75	4.85
Ref. GP00-D682-001			

PD_GP00-D682-001

5. Parallel Host Interface

The modem supports a 16550A interface in parallel interface versions. The 16550A interface can operate in FIFO mode or non-FIFO mode. Non-FIFO mode is the same as 16450 interface operation. FIFO mode unique operations are identified.

5.1 Overview

The parallel interface registers and the corresponding bit assignments are shown in Table 5-1.

The modem emulates the 16450/16550A interface and includes both a 16-byte receiver data first-in first-out buffer (RX FIFO) and a 16-byte transmit data first-in first-out buffer (TX FIFO). When FIFO mode is selected in the FIFO Control Register (FCR0 = 1), both FIFOs are operative. Furthermore, when FIFO mode is selected, DMA operation of the FIFO can also be selected (FCR3 = 1). When FIFO mode is not selected, operation is restricted to 16450 interface operation.

The received data is read by the host from the Receiver Buffer (RX Buffer). The RX Buffer corresponds to the Receiver Buffer Register in a 16550A device. In FIFO mode, the RX FIFO operates transparently behind the RX Buffer. Interface operation is described with reference to the RX Buffer in both FIFO and non-FIFO modes.

The transmit data is loaded by the host into the Transmit Buffer (TX Buffer). The TX Buffer corresponds to the Transmit Holding Register in a 16550A device. In FIFO mode, the TX FIFO operates transparently behind the TX Buffer. Interface operation is described with reference to the TX Buffer in both FIFO and non-FIFO modes.

Table 5-1. Parallel Interface Registers

Register	Register	Bit No.							
No.	Name	7	6	5	4	3	2	1	0
7	Scratch Register (SCR)	Scratch Register							
6	Modem Status Register (MSR)	Data Carrier Detect (DCD)	Ring Indicator (RI)	Data Set Ready (DSR)	Clear to Send (CTS)	Delta Data Carrier Detect (DDCD)	Trailing Edge of Ring Indicator (TERI)	Delta Data Set Ready (DDSR)	Delta Clear to Send (DCTS)
5	Line Status Register (LSR)	RX FIFO Error	Transmitter Empty (TEMT)	Transmitter Buffer Register Empty (THRE)	Break Interrupt (BI)	Framing Error (FE)	Parity Error (PE)	Overrun Error (OE)	Receiver Data Ready (DR)
4	Modem Control Register (MCR)	0	0	0	Local Loopback	Out 2	Out 1	Request to Send (RTS)	Data Terminal Ready (DTR)
3	Line Control Register (LCR)	Divisor Latch Access Bit (DLAB)	Set Break	Stick Parity	Even Parity Select (EPS)	Parity Enable (PEN)	Number of Stop Bits (STB)	Word Length Select Bit 1 (WLS1)	Word Length Select Bit 0 (WLS0)
2	Interrupt Identify Register (IIR) (Read Only)	FIFOs Enabled	FIFOs Enabled	0	0	Pending Interrupt ID Bit 2	Pending Interrupt ID Bit 1	Pending Interrupt ID Bit 0	"0" if Interrupt Pending
2	FIFO Control Register (FCR) (Write Only)	Receiver Trigger MSB	Receiver Trigger LSB	Reserved	Reserved	DMA Mode Select	TX FIFO Reset	RX FIFO Reset	FIFO Enable
1 (DLAB = 0)	Interrupt Enable Register (IER)	0	0	0	0	Enable Modem Status Interrupt (EDSSI)	Enable Receiver Line Status Interrupt (ELSI)	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Enable Received Data Available Interrupt (ERBFI)
0 (DLAB = 0)	Transmitter Buffer Register (THR)	Transmitter FIFO Buffer Register (Write Only)							
0 (DLAB = 0)	Receiver Buffer Register (RBR)	Receiver FIFO Buffer Register (Read Only)							
1 (DLAB = 1)	Divisor Latch MSB Register (DLM)	Divisor Latch MSB							
0 (DLAB = 1)	Divisor Latch LSB Register (DLL)	Divisor Latch LSB							

5.2   Register Signal Definitions

5.2.1   IER - Interrupt Enable Register (Addr = 1, DLAB = 0)

The IER enables five types of interrupts that can separately assert the HINT output signal (Table 5-2). A selected interrupt can be enabled by setting the corresponding enable bit to a 1, or disabled by setting the corresponding enable bit to a 0. Disabling an interrupt in the IER prohibits setting the corresponding indication in the IIR and assertion of HINT. Disabling all interrupts (resetting IER0 - IER3 to a 0) inhibits setting of any Interrupt Identifier Register (IIR) bits and inhibits assertion of the HINT output. All other system functions operate normally, including the setting of the Line Status Register (LSR) and the Modem Status Register (MSR).

Bits 7-4   Not used.

Always 0.

Bit 3   Enable Modem Status Interrupt (EDSSI).

This bit, when a 1, enables assertion of the HINT output whenever the Delta CTS (MSR0), Delta DSR (MSR1), Delta TER (MSR2), or Delta DCD (MSR3) bit in the Modem Status Register (MSR) is a 1. This bit, when a 0, disables assertion of HINT due to setting of any of these four MSR bits.

Bit 2   Enable Receiver Line Status Interrupt (ELSI).

This bit, when a 1, enables assertion of the HINT output whenever the Overrun Error (LSR1), Parity Error (LSR2), Framing Error (LSR3), or Break Interrupt (LSR4) receiver status bit in the Line Status Register (LSR) changes state. This bit, when a 0, disables assertion of HINT due to change of the receiver LSR bits 1-4.

Bit 1   Enable Transmitter Holding Register Empty Interrupt (ETBEI).

This bit, when a 1, enables assertion of the HINT output when the Transmitter Empty bit in the Line Status Register (LSR5) is a 1. This bit, when a 0, disables assertion of HINT due to LSR5.

**Bit 0   Enable Receiver Data Available Interrupt (ERBFI) and Character
                Timeout in FIFO Mode.**

This bit, when a 1, enables assertion of the HINT output when the Receiver Data Ready bit in the Line Status Register (LSR0) is a1 or character timeout occurs in the FIFO mode. This bit, when a 0, disables assertion of HINT due to the LSR0 or character timeout.

5.2.2 FCR - FIFO Control Register (Addr = 2, Write Only)

The FCR is a write-only register used to enable FIFO mode, clear the RX FIFO and TX FIFO, enable DMA mode, and set the RX FIFO trigger level.

Bits 7-6   RX FIFO Trigger Level.

FCR7 and FCR6 set the trigger level for the RX FIFO (Receiver Data Available) interrupt.

FCR7	FCR6	RX FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

Bits 5-4   Not used.

Bit 3   DMA Mode Select.

When FIFO mode is selected (FCR0 = 1), FCR3 selects non-DMA operation (FCR3 = 0) or DMA operation (FCR3 = 1). When FIFO mode is not selected (FCR0 = 0), this bit is not used (the modem operates in non-DMA mode in 16450 operation).

> *DMA operation in FIFO mode.*

RXRDY will be asserted when the number of characters in the RX FIFO is equal to or greater than the value in the RX FIFO Trigger Level (IIR0-IIR3 = 4h) or the received character timeout (IIR0-IIR3 = Ch) has occurred. RXRDY will go inactive when there are no more characters in the RX FIFO.

TXRDY will be asserted when there are one or more empty (unfilled) locations in the TX FIFO. TXRDY will go inactive when the TX FIFO is completely full.

> *Non-DMA operation in FIFO mode.*

RXRDY will be asserted when there are one or more characters in the RX FIFO. RXRDY will go inactive when there are no more characters in the RX FIFO.

TXRDY will be asserted when there are no characters in the TX FIFO. TXRDY will go inactive when the first character is loaded into the TX FIFO Buffer.

Bit 2   TX FIFO Reset.

When FCR2 is a 1, all bytes in the TX FIFO are cleared. This bit is cleared automatically by the modem.

Bit 1   RX FIFO Reset.

When FCR1 is a 1, all bytes in the RX FIFO are cleared. This bit is cleared automatically by the modem.

Bit 0   FIFO Enable.

When FCR0 is a 0, 16450 mode is selected and all bits are cleared in both FIFOs. When FCR0 is a 1, FIFO mode (16550A mode) is selected and both FIFOs are enabled. FCR0 must be a 1 when other bits in the FCR are written or they will not be acted upon.

5.2.3 IIR - Interrupt Identifier Register (Addr = 2)

The Interrupt Identifier Register (IIR) identifies the existence and type of up to five prioritized pending interrupts. Four priority levels are set to assist interrupt processing in the host. The four levels, in order of decreasing priority, are: Highest: Receiver Line Status, 2: Receiver Data Available or Receiver Character Timeout, 3: TX Buffer Empty, and 4: Modem Status.

When the IIR is accessed, the modem freezes all interrupts and indicates the highest priority interrupt pending to the host. Any change occurring in interrupt conditions are not indicated until this access is complete.

Bits 7-6   FIFO Mode.

These two bits copy FCR0.

Bits 5-4   Not Used.

Always 0.

Bits 3-1   Highest Priority Pending Interrupt.

These three bits identify the highest priority pending interrupt (Table 5-2). Bit 3 is applicable only when FIFO mode is selected, otherwise bit 3 is a 0.

Bit 0   Interrupt Pending.

When this bit is a 0, an interrupt is pending; IIR bits 1-3 can be used to determine the source of the interrupt. When this bit is a1, an interrupt is not pending.

Table 5-2. Interrupt Sources and Reset Control

Interrupt Identification Register					Interrupt Set and Reset Functions		
Bit 3[1]	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	0	1	—	None	None	—
0	1	1	0	Highest	Receiver Line Status	Overrun Error OE (LSR1), Parity Error (PE) (LSR2), Framing Error (FE) (LSR3), or Break Interrupt (BI) (LSR4)	Reading the LSR
0	1	0	0	2	Received Data Available	Received Data Available (LSR0) or RX FIFO Trigger Level (FCR6-FCR7) Reached[1]	Reading the RX Buffer or the RX FIFO drops below the Trigger Level
1	1	0	0	2	Character Time-out Indication [1]	The RX FIFO contains at least 1 character and no characters have been removed from or input to the RX FIFO during the last 4 character times.	Reading the RX Buffer
0	0	1	0	3	TX Buffer Empty	TX Buffer Empty	Reading the IIR or writing to the TX Buffer
0	0	0	0	4	Modem Status	Delta CTS (DCTS) (MSR0), Delta DSR (DDSR) (MSR1), Trailing Edge Ring Indicator (TERI) (MSR3), or Delta DCD (DCD) (MSR4)	Reading the MSR
Notes: 1. FIFO Mode only.							

5.2.4 LCR - Line Control Register (Addr = 3)

The Line Control Register (LCR) specifies the format of the asynchronous data communications exchange.

Bit 7   Divisor Latch Access Bit (DLAB).

This bit must be set to a 1 to access the Divisor latch registers during a read or write operation. It must be reset to a 0 to access the Receiver Buffer, the Transmitter Buffer, or the Interrupt Enable Register.

Bit 6   Set Break.

When bit 6 is a 1, the transmit data is forced to the break condition, i.e., space (0) is sent. When bit 6 is a 0, break is not sent. The Set Break bit acts only on the transmit data and has no effect on the serial in logic.

Bit 5   Stick Parity.

When parity is enabled (LCR3 = 1) and stick parity is selected (LCR5 = 1), the parity bit is transmitted and checked by the receiver as a 0 if even parity is selected (LCR4 = 1) or as a 1 if odd parity is selected (LCR4 = 0). When stick parity is not selected (LCR3 = 0), parity is transmit and checked as determined by the LCR3 and LCR4 bits.

Bit 4   Even Parity Select (EPS).

When parity is enabled (LCR3 = 1) and stick parity is not selected (LCR5 = 0), the number of 1s transmitted or checked by the receiver in the data word bits and parity bit is either even (LCR4 = 1) or odd (LCR4 = 0).

Bit 3   Enable Parity (PEN).

When bit 3 is a 1, a parity bit is generated in the serial out (transmit) data stream and checked in the serial in (receive) data stream as determined by the LCR 4 and LCR5 bits. The parity bit is located between the last data bit and the first stop bit.

Bit 2   Number of Stop Bits (STB).

This bit specifies the number of stop bits in each serial out character. If bit 2 is a 0, one stop bit is generated regardless of word length. If bit 2 is a 1 and 5-bit word length is selected, one and one-half stop bits are generated. If bit 2 is a 1 and a 6-, 7-, or 8-bit word length is selected, two stop bits are generated. The serial in logic checks the first stop bit only, regardless of the number of stop bits selected.

Bits 1-0   Word Length Select (WLS0 and WLS1).

These two bits specify the number of bits in each serial in or serial out character. The encoding of bits 0 and 1 is:

Bit 1	Bit 0	Word Length
0	0	5 Bits (Not supported)
0	1	6 Bits (Not supported)
1	0	7 Bits
1	1	8 Bits

5.2.5 MCR - Modem Control Register (Addr = 4)

The Modem Control Register (MCR) controls the interface with the modem or data set.

Bit 7-5   Not used.

Always 0.

Bit 4   Local Loopback.

When this bit is set to a 1, the diagnostic mode is selected and the following occurs:

Data written to the Transmit Buffer is looped back to the Receiver Buffer.

The DTS (MCR0), RTS (MCR1), Out1 (MCR2), and Out2 (MCR3) modem control register bits are internally connected to the DSR (MSR5), CTS (MSR4), RI (MSR6), and DCD (MSR7) modem status register bits, respectively.

Bit 3   Output 2.

When this bit is a 1, HINT is enabled. When this bit is a 0, HINT is in the high impedance state.

Bit 2   Output 1.

This bit is used in local loopback (see MCR4).

Bit 1   Request to Send (RTS).

This bit controls the Request to Send (RTS) function. When this bit is a 1, RTS is on. When this bit is a 0, RTS is off.

Bit 0   Data Terminal Ready (DTR).

This bit controls the Data Terminal Ready (DTR) function. When this bit is a 1, DTR is on. When this bit is a 0, DTR is off.

5.2.6 LSR - Line Status Register (Addr = 5)

This 8-bit register provides status information to the host concerning data transfer.

Bit 7   RX FIFO Error.

In the 16450 mode, this bit is not used and is always 0.

In the FIFO mode, this bit is set if there are one or more characters in the RX FIFO with a parity error, framing error, or break indication detected. This bit is reset to a 0 when the host reads the LSR and none of the above conditions exist in the RX FIFO.

Bit 6   Transmitter Empty (TEMT).

This bit is set to a 1 whenever the TX Buffer (THR) and equivalent of the Transmitter Shift Register (TSR) are both empty. It is reset to a 0 whenever either the THR or the equivalent of the TSR contains a character.

In the FIFO mode, this bit is set to a 1 when ever the TX FIFO and the equivalent of the TSR are both empty.

Bit 5   Transmitter Holding Register Empty (THRE) [TX Buffer Empty].

This bit, when set, indicates that the TX Buffer is empty and the modem can accept a new character for transmission. In addition, this bit causes the modem to issue an interrupt to the host when the Transmit Holding Register Empty Interrupt Enable bit (IIR1) is set to 1. The THRE bit is set to a 1 when a character is transferred from the TX Buffer. The bit is reset to 0 when a byte is written into the TX Buffer by the host.

In the FIFO mode, this bit is set when the TX FIFO is empty; it is cleared when at least one byte is in the TX FIFO.

Bit 4   Break Interrupt (BI).

This bit is set to a 1 whenever the received data input is a space (logic 0) for longer than two full word lengths plus 3 bits. The BI bit is reset when the host reads the LSR.

Bit 3   Framing Error (FE).

This bit indicates that the received character did not have a valid stop bit. The FE bit is set to a 1 whenever the stop bit following the last data bit or parity bit is detected as a logic o (space). The FE bit is reset to a 0 when the host reads the LSR.

In the FIFO mode, the error indication is associated with the particular character in the FIFO it applies to; the FE bit is set to a 1 when this character is loaded into the RX Buffer.

Bit 2   Parity Error (PE).

This bit indicates that the received data character in the RX Buffer does not have the correct even or odd parity, as selected by the Even Parity Select bit (LCR4) and the Stick Parity bit (LCR5). The PE bit is reset to a 0 when the host reads the LSR.

In the FIFO mode, the error indication is associated with the particular character in the it applies to; the PE bit is set to a 1 when this character is loaded into the RX Buffer.

Bit 1   Overrun Error (OE).

This bit is set to a 1 whenever received data is loaded into the RX Buffer before the host has read the previous data from the RX Buffer. The OE bit is reset to a 0 when the host reads the LSR.

In the FIFO mode, if data continues to fill beyond the trigger level, an overrun condition will occur only if the RX FIFO is full and the next character has been completely received.

Bit 0   Receiver Data Ready (DR).

This bit is set to a 1 whenever a complete incoming character has been received and has been transferred into the RX Buffer. The DR bit is reset to a 0 when the host reads the RX Buffer.

In the FIFO mode, the DR bit is set when the number of received data bytes in the RX FIFO equals or exceeds the trigger level specified in FCR0-FCR1.

5.2.7 MSR - Modem Status Register (Addr = 6)

The Modem Status Register (MSR) reports current state and change information of the modem. Bits 4-7 supply current state and bits 0-3 supply change information. The change bits are set to a 1 whenever a control input from the modem changes state from the last MSR read by the host. Bits 0-3 are reset to 0 when the host reads the MSR or upon reset.

Whenever bits 0, 1, 2, or 3 are set to a 1, a Modem Status Interrupt (IIR0-IIR3 = 0) is generated.

Bit 7   Data Carrier Detect (DCD).

This bit indicates the logic state of the DCD# (RLSD#) output. If Loopback is selected (MCR4 = 1), this bit reflects the state of the Out2 bit in the MCR (MCR3).

Bit 6   Ring Indicator (RI).

This bit indicates the logic state of the RI# output. If Loopback is selected (MCR4 = 1), this bit reflects the state of the Out1 bit in the MCR (MCR2).

Bit 5   Data Set Ready (DSR).

This bit indicates the logic state of the DSR# output. If Loopback is selected (MCR4 = 1), this bit reflects the state of the DTR bit in the MCR (MCR0).

Bit 4   Clear to Send (CTS).

This bit indicates the logic state of the CTS# output. If Loopback is selected (MCR4 = 1), this bit reflects the state of the RTS bit in the MCR (MCR1).

Bit 3   Delta Data Carrier Detect (DDCD).

This bit is set to a 1 when the DCD bit changes state since the MSR was last read by the host.

Bit 2   Trailing Edge of Ring Indicator (TERI).

This bit is set to a 1 when the RI bit changes from a 1 to a 0 state since the MSR was last read by the host.

Bit 1   Delta Data Set Ready (DDSR).

This bit is set to a 1 when the DSR bit has changed since the MSR was last read by the host.

Bit 0   Delta Clear to Send (DCTS).

This bit is set to a 1 when the CTS bit has changed since the MSR was last read by the host.

5.2.8 RBR - RX Buffer (Receiver Buffer Register) (Addr = 0, DLAB = 0)

The RX Buffer (RBR) is a read-only register at location 0 (with DLAB = 0). Bit 0 is the least significant bit of the data, and is the first bit received.

5.2.9 THR - TX Buffer (Transmitter Holding Register) (Addr = 0, DLAB = 0)

The TX Buffer (THR) is a write-only register at address 0 when DLAB = 0. Bit 0 is the least significant bit and the first bit sent.

5.2.10 Divisor Registers (Addr = 0 and 1, DLAB = 1)

The Divisor Latch LS (least significant byte) and Divisor Latch MS (most significant byte) are two read-write registers at locations 0 and 1 when DLAB = 1, respectively.

The baud rate is selected by loading each divisor latch with the appropriate hex value.

Programmable values corresponding to the desired baud rate are listed in Table 5-3.

5.2.11 SCR - Scratch Register (Addr = 7)

The Scratchpad Register is a read-write register at location 7. This register is not used by the modem and can be used by the host for temporary storage.

Table 5-3. Programmable Baud Rates

Divisor Latch (Hex)			
MS	LS	Divisor (Decimal)	Baud Rate
06	00	1536	75
04	17	1047	110
03	00	768	150
01	80	384	300
00	C0	192	600
00	60	96	1200
00	30	48	2400
00	18	24	4800
00	0C	12	9600
00	06	6	19200
00	04	4	28800
00	03	3	38400
00	02	2	57600
00	01	1	115200
00	00	NA	230400

5.3 Receiver FIFO Interrupt Operation

5.3.1 Receiver Data Available Interrupt

When the FIFO mode is enabled (FCR0 = 1) and receiver interrupt (RX Data Available) is enabled (IER0 = 1), receiver interrupt operation is as follows:

The Receiver Data Available Flag (LSR0) is set as soon as a received data character is available in the RX FIFO. LSR0 is cleared when the RX FIFO is empty.

The Receiver Data Available interrupt code (IIR0-IIR4 = 4h) is set whenever the number of received data bytes in the RX FIFO reaches the trigger level specified by FCR6-FCR7 bits; it is cleared whenever the number of received data bytes in the RX FIFO drops below the trigger level specified by FCR6-FCR7 bits.

The HINT interrupt is asserted whenever the number of received data bytes in the RX FIFO reaches the trigger level specified by FCR6-FCR7 bits. HINT interrupt is de-asserted when the number of received data bytes in the RX FIFO drops below the trigger level specified by FCR6-FCR7 bits.

5.3.2 Receiver Character Timeout Interrupts

When the FIFO mode is enabled (FCR0 = 1) and receiver interrupt (Receiver Data Available) is enabled (IER0 = 1), receiver character timeout interrupt operation is as follows:

1. A Receiver character timeout interrupt code (IIR0-IIR3 = Ch) is set if at least one received character is in the RX FIFO, the most recent received serial character was longer than four continuous character times ago (if 2 stop bits are specified, the second stop bit is included in this time period), and the most recent host read of the RX FIFO was longer than four continuous character times ago.

5.4 Transmitter FIFO Interrupt Operation

5.4.1 Transmitter Empty Interrupt

When the FIFO mode is enabled (FCR0 = 1) and transmitter interrupt (TX Buffer Empty) is enabled (IER0 = 1), transmitter interrupt operation is as follows:

The TX Buffer Empty interrupt code (IIR0-IIR3 = 2h) will occur when the TX Buffer is empty; it is cleared when the TX Buffer is written to (1 to 16 characters) or the IIR is read.

The TX Buffer Empty indications will be delayed 1 character time minus the last stop bit time whenever the following occur: THRE = 1 and there have not been at least two bytes at the same time in the TX FIFO Buffer since the last setting of THRE was set. The first transmitter interrupt after setting FCR0 will be immediate.

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