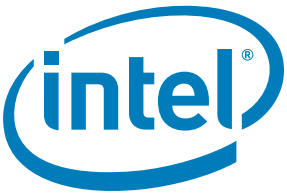

Dual-Core Intel® Xeon® Processor 5000 Series

Datasheet

May 2006

Document Number: 313079-001

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Revision History

Revision	Description	Date
001	Initial release	May 2006

Features

- Dual-Core processor
- Available at 3.73 GHz processor speed
- Includes 16-KB Level 1 data cache per core (2 x 16-KB)
- Includes 12-KB Level 1 trace cache per core (2 x 12-KB)
- 2-MB Advanced Transfer Cache per core (2 x 2-MB, On-die, full speed Level 2 (L2) Cache) with 8-way associativity and Error Correcting Code (ECC)
- 667/1066 MHz front side bus
- 65 nm process technology
- Dual processing (DP) server support
- Intel® NetBurst® microarchitecture
- Hyper-Threading Technology allowing up to 8 threads per platform
- Hardware support for multi-threaded applications
- Intel® Virtualization Technology
- Intel® Extended Memory 64 Technology (Intel® EM64T)
- Execute Disable Bit (XD Bit)
- Enables system support of up to 64 GB of physical memory
- Enhanced branch prediction
- Enhanced floating-point and multimedia unit for enhanced video, audio, encryption, and 3D performance
- Advanced Dynamic Execution
- Very deep out-of-order execution
- System Management mode
- Machine Check Architecture (MCA)
- Interfaces to Memory Controller Hub

The Dual-Core Intel Xeon Processor 5000 series are designed for high-performance dual-processor server and workstation applications. Based on the Intel NetBurst® microarchitecture and Hyper-Threading Technology (HT Technology), it is binary compatible with previous Intel® Architecture (IA-32) processors. The Dual-Core Intel Xeon Processor 5000 series are scalable to two processors in a multiprocessor system, providing exceptional performance for applications running on advanced operating systems such as Windows* XP, Windows Server 2003, Linux*, and UNIX*.

The Dual-Core Intel Xeon Processor 5000 series deliver compute power at unparalleled value and flexibility for powerful servers, internet infrastructure, and departmental server applications. The Intel NetBurst micro-architecture, Intel Virtualization Technology and Hyper-Threading Technology deliver outstanding performance and headroom for peak internet server workloads, resulting in faster response times, support for more users, and improved scalability.

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1 Introduction

The Dual-Core Intel® Xeon® Processor 5000 series are Intel dual core products for dual processor (DP) servers and workstations. The Dual-Core Intel Xeon Processor 5000 series are 64-bit server/workstation processors utilizing two physical Intel NetBurst® microarchitecture cores in one package. The Dual-Core Intel Xeon Processor 5000 series include enhancements to the Intel NetBurst microarchitecture while maintaining the tradition of compatibility with IA-32 software. Some key features include Hyper Pipelined Technology and an Execution Trace Cache. Hyper Pipelined Technology includes a multi-stage pipeline depth, allowing the processor to reach higher core frequencies. The Dual-Core Intel Xeon Processor 5000 series contain a total of 4 MB of L2 Advanced Transfer Cache, 2 MB per core. The 1066 MHz Front Side Bus (FSB) is a quad-pumped bus running off a 266 MHz system clock making 8.5 GBytes per second data transfer rates possible. The 667 MHz Front Side Bus (FSB) is a quad-pumped bus running off a 166 MHz system clock making 5.3 GBytes per second data transfer rates possible.

In addition, enhanced thermal and power management capabilities are implemented including Thermal Monitor (TM1) and Enhanced Intel SpeedStep® technology. These technologies are targeted for dual processor (DP) systems in enterprise environments. TM1 provides efficient and effective cooling in high temperature situations. Enhanced Intel SpeedStep technology provides power management capabilities to servers and workstations.

The Dual-Core Intel Xeon Processor 5000 series also include Hyper-Threading Technology (HT Technology) resulting in four logical processors per package. This feature allows multi-threaded applications to execute more than one thread per physical processor core, increasing the throughput of applications and enabling improved scaling for server and workstation workloads. More information on Hyper-Threading Technology can be found at http://www.intel.com/technology/hyperthread.

Other features within the Intel NetBurst microarchitecture include Advanced Dynamic Execution, Advanced Transfer Cache, enhanced floating point and multi-media units, and Streaming SIMD Extensions 3 (SSE3). Advanced Dynamic Execution improves speculative execution and branch prediction internal to the processor. The Advanced Transfer Cache in each core is a 2 MB level 2 (L2) cache. The floating point and multi-media units include 128-bit wide registers and a separate register for data movement. Streaming SIMD3 (SSE3) instructions provide highly efficient double-precision floating point, SIMD integer, and memory management operations. Other processor enhancements include core frequency improvements and microarchitectural improvements.

The Dual-Core Intel Xeon Processor 5000 series support Intel® Extended Memory 64 Technology (Intel® EM64T) as an enhancement to Intel's IA-32 architecture. This enhancement allows the processor to execute operating systems and applications written to take advantage of the 64-bit extension technology. Further details on Intel Extended Memory 64 Technology and its programming model can be found in the *64-bit Extension Technology Software Developer's Guide* at http://developer.intel.com/technology/64bitextensions/.

In addition, the Dual-Core Intel Xeon Processor 5000 series support the Execute Disable Bit functionality. When used in conjunction with a supporting operating system, Execute Disable allows memory to be marked as executable or non executable. This feature can prevent some classes of viruses that exploit buffer overrun vulnerabilities

and can thus help improve the overall security of the system. For further information on Execute Disable Bit functionality see http://www.intel.com/cd/ids/developer/asmo-na/eng/149308.htm.

The Dual-Core Intel Xeon Processor 5000 series support Intel® Virtualization Technology, virtualization within the processor. Intel Virtualization Technology is a set of hardware enhancements that can improve virtualization solutions. Intel Virtualization Technology is used in conjunction with Virtual Machine Monitor software enabling multiple, independent software environments inside a single platform. More information on Intel Virtualization Technology can be found at http://www.intel.com/technology/computing/vptech/index.htm.

The Dual-Core Intel Xeon Processor 5000 series are intended for high performance workstation and server systems. The Dual-Core Intel Xeon Processor 5063 is a lower power version of the Dual-Core Intel Xeon Processor 5000 series. The Dual-Core Intel Xeon Processor 5000 series support a new Dual Independent Bus (DIB) architecture with one processor socket on each bus, up to two processor sockets in a system. The DIB architecture provides improved performance by allowing increased FSB speeds and bandwidth. The Dual-Core Intel Xeon Processor 5000 series will be packaged in an FC-LGA6 Land Grid Array package with 771 lands for improved power delivery. It utilizes a surface mount LGA771 socket that supports Direct Socket Loading (DSL).

Table 1-1. Dual-Core Intel® Xeon® Processor 5000 Series Features

# Cores Per Package	L2 Advanced Transfer Cache[1]	Hyper-Threading Technology	Front Side Bus Frequency	Package
2	2 MB per core 4 MB total	Yes	667 MHz 1066 MHz	FC-LGA6 771 Lands

Notes:

1. Total accessible size of L2 caches may vary by one cache line pair (128 bytes) per core, depending on usage and operating environment.

The Dual-Core Intel Xeon Processor 5000 series-based platforms implement independent core voltage (V_{CC}) power planes for each processor. FSB termination voltage (V_{TT}) is shared and must connect to all FSB agents. The processor core voltage utilizes power delivery guidelines specified by VRM/EVRD 11.0 and its associated load line. Refer to the appropriate platform design guidelines for implementation details.

The Dual-Core Intel Xeon Processor 5000 series support a 1066/667 MHz Front Side Bus frequency. The FSB utilizes a split-transaction, deferred reply protocol and Source-Synchronous Transfer (SST) of address and data to improve performance. The processor transfers data four times per bus clock (4X data transfer rate, as in AGP 4X). Along with the 4X data bus, the address bus can deliver addresses two times per bus clock and is referred to as a 'double-clocked' or a 2X address bus. In addition, the Request Phase completes in one clock cycle. Working together, the 4X data bus and 2X address bus provide a data bus bandwidth of up to 8.5 GBytes/second. (5.3 GBytes/second for Dual-Core Intel Xeon Processor 5000 series 667) Finally, the FSB is also used to deliver interrupts.

Signals on the FSB use Assisted Gunning Transceiver Logic (AGTL+) level voltages. Section 2.1 contains the electrical specifications of the FSB while implementation details are fully described in the appropriate platform design guidelines (refer to Section 1.3).

1.1 Terminology

A '#' symbol after a signal name refers to an active low signal, indicating a signal is in the asserted state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the '#' symbol implies that the signal is inverted. For example, D[3:0] = 'HLHL' refers to a hex 'A', and D[3:0]# = 'LHLH' also refers to a hex 'A' (H= High logic level, L= Low logic level).

Commonly used terms are explained here for clarification:

- **Dual-Core Intel® Xeon® Processor 5000 Series** – Processor in the FC-LGA6 package with two physical processor cores. Dual-Core Intel Xeon processor 5000 series refers to the "Full Power" Dual-Core Intel Xeon Processor 5000 series with 1066 MHz Front Side Bus. For this document, "processor" is used as the generic term for the "Dual-Core Intel® Xeon® Processor 5000 series".
- **Dual-Core Intel® Xeon® Processor 5063 (MV)** – This is a lower power version of the Dual-Core Intel Xeon Processor 5000 series. Dual-Core Intel Xeon Processor 5063 (MV) refers to the "Mid Power" Dual-Core Intel Xeon Processor 5000 series. Unless otherwise noted, the terms "Dual-Core Intel Xeon 5000 series" and "processor" also refer to the "Dual-Core Intel Xeon Processor 5063".
- **FC-LGA6 (Flip Chip Land Grid Array) Package** – The Dual-Core Intel Xeon Processor 5000 series package is a Land Grid Array, consisting of a processor core mounted on a pinless substrate with 771 lands, and includes an integrated heat spreader (IHS).
- **FSB (Front Side Bus)** – The electrical interface that connects the processor to the chipset. Also referred to as the processor front side bus or the front side bus. All memory and I/O transactions as well as interrupt messages pass between the processor and chipset over the FSB.
- **Functional Operation** – Refers to the normal operating conditions in which all processor specifications, including DC, AC, FSB, signal quality, mechanical and thermal are satisfied.
- **Storage Conditions** – Refers to a non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor lands should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to "free air" (that is, unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
- **Priority Agent** – The priority agent is the host bridge to the processor and is typically known as the chipset.
- **Symmetric Agent** – A symmetric agent is a processor which shares the same I/O subsystem and memory array, and runs the same operating system as another processor in a system. Systems using symmetric agents are known as Symmetric Multiprocessing (SMP) systems.
- **Integrated Heat Spreader (IHS)** – A component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
- **Enhanced Intel SpeedStep Technology** – The next generation implementation of Intel SpeedStep technology which extends power management capabilities of servers and workstations.

- **Thermal Design Power** – Processor thermal solutions should be designed to meet this target. It is the highest expected sustainable power while running known power intensive real applications. TDP is not the maximum power that the processor can dissipate.
- **LGA771 socket** – The Dual-Core Intel Xeon Processor 5000 series interfaces to the baseboard through this surface mount, 771 Land socket. See the *LGA771 Socket Design Guidelines* for details regarding this socket.
- **Processor** – A single package that contains one or more complete execution cores.
- **Processor core** – Processor core die with integrated L2 cache. All AC timing and signal integrity specifications are at the pads of the processor core.
- **Intel® Virtualization Technology** – Processor virtualization which when used in conjunction with Virtual Machine Monitor software enables multiple, robust independent software environments inside a single platform.
- **VRM (Voltage Regulator Module)** – DC-DC converter built onto a module that interfaces with a card edge socket and supplies the correct voltage and current to the processor based on the logic state of the processor VID bits.
- **EVRD (Enterprise Voltage Regulator Down)** – DC-DC converter integrated onto the system board that provides the correct voltage and current to the processor based on the logic state of the processor VID bits.
- **V_{CC}** – The processor core power supply.
- **V_{SS}** – The processor ground.
- **V_{TT}** – FSB termination voltage.

1.2 State of Data

The data contained within this document is subject to change. It is the most accurate information available by the publication date of this document and is based on final silicon characterization. All specifications in this version of the *Dual-Core Intel® Xeon® Processor 5000 Series Datasheet* can be used for platform design purposes (layout studies, characterizing thermal capabilities, and so forth).

1.3 References

Material and concepts available in the following documents may be beneficial when reading this document:

Document	Intel Order Number
AP-485, Intel® Processor Identification and the CPUID Instruction	241618
IA-32 Intel® Architecture Software Developer's Manual • *Volume 1: Basic Architecture* • *Volume 2A: Instruction Set Reference, A-M* • *Volume 2B: Instruction Set Reference, N-Z* • *Volume 3A: System Programming Guide* • *Volume 3B: System Programming Guide*	 253665 253666 253667 253668 253669
64-bit Extension Technology Software Developer's Guide • *Volume 1* • *Volume 2*	 300834 300835
IA-32 Intel® Architecture Optimization Reference Manual	248966

Document	Intel Order Number
Dual-Core Intel® Xeon® Processor 5000 Series Specifications Update	313065
EPS12V Power Supply Design Guide: A Server system Infrastructure (SSI) Specification for Entry Chassis Power Supplies	http:// www.ssiforum.org
Entry-Level Electronics-Bay Specifications: A Server System Infrastructure (SSI) Specification for Entry Pedestal Servers and Workstations	http:// www.ssiforum.org
Dual-Core Intel® Xeon® Processor 5000 Series Thermal/Mechanical Design Guidelines	313062
Dual-Core Intel® Xeon® Processor 5000 Series Boundary Scan Descriptive Language (BSDL) Model	313064

Notes: Contact your Intel representative for the latest revision of those documents.

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2 Electrical Specifications

2.1 Front Side Bus and GTLREF

Most Dual-Core Intel Xeon Processor 5000 series FSB signals use Assisted Gunning Transceiver Logic (AGTL+) signaling technology. This technology provides improved noise margins and reduced ringing through low voltage swings and controlled edge rates. AGTL+ buffers are open-drain and require pull-up resistors to provide the high logic level and termination. AGTL+ output buffers differ from GTL+ buffers with the addition of an active PMOS pull-up transistor to “assist” the pull-up resistors during the first clock of a low-to-high voltage transition. Platforms implement a termination voltage level for AGTL+ signals defined as V_{TT}. Because platforms implement separate power planes for each processor (and chipset), separate V_{CC} and V_{TT} supplies are necessary. This configuration allows for improved noise tolerance as processor frequency increases. Speed enhancements to data and address buses have made signal integrity considerations and platform design methods even more critical than with previous processor families.

The AGTL+ inputs require reference voltages (GTLREF), which are used by the receivers to determine if a signal is a logical 0 or a logical 1. GTLREF must be generated on the baseboard. GTLREF is a generic name for GTLREF_DATA_C[1:0], the reference voltages for the 4X data bus and GTLREF_ADD_C[1:0], the reference voltages for the 2X address bus and common clock signals. Refer to the applicable platform design guidelines for details. Termination resistors (R_{TT}) for AGTL+ signals are provided on the processor silicon and are terminated to V_{TT}. The on-die termination resistors are always enabled on the Dual-Core Intel Xeon Processor 5000 series to control reflections on the transmission line. Intel chipsets also provide on-die termination, thus eliminating the need to terminate the bus on the baseboard for most AGTL+ signals.

Some FSB signals do not include on-die termination (R_{TT}) and must be terminated on the baseboard. See Table 2-7 for details regarding these signals.

The AGTL+ bus depends on incident wave switching. Therefore, timing calculations for AGTL+ signals are based on flight time as opposed to capacitive deratings. Analog signal simulation of the FSB, including trace lengths, is highly recommended when designing a system. Contact your Intel Field Representative to obtain the processor signal integrity models, which includes buffer and package models.

2.2 Power and Ground Lands

For clean on-chip processor core power distribution, the processor has 223 V_{CC} (power) and 271 V_{SS} (ground) inputs. All Vcc lands must be connected to the processor power plane, while all V_{SS} lands must be connected to the system ground plane. The processor V_{CC} lands must be supplied with the voltage determined by the processor **V**oltage **ID**entification (VID) signals. See Table 2-3 for VID definitions.

Twenty two lands are specified as V_{TT}, which provide termination for the FSB and power to the I/O buffers. The platform must implement a separate supply for these lands which meets the V_{TT} specifications outlined in Table 2-10.

2.3 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the Dual-Core Intel Xeon Processor 5000 series are capable of generating large average current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Larger bulk storage (C_{BULK}), such as electrolytic capacitors, supply current during longer lasting changes in current demand by the component, such as coming out of an idle condition. Similarly, they act as a storage well for current when entering an idle condition from a running condition. Care must be taken in the baseboard design to ensure that the voltage provided to the processor remains within the specifications listed in Table 2-10. Failure to do so can result in timing violations or reduced lifetime of the component. For further information and guidelines, refer to the appropriate platform design guidelines.

2.3.1 V_{CC} Decoupling

Vcc regulator solutions need to provide bulk capacitance with a low Effective Series Resistance (ESR), and the baseboard designer must assure a low interconnect resistance from the regulator (EVRD or VRM pins) to the LGA771 socket. Bulk decoupling must be provided on the baseboard to handle large current swings. The power delivery solution must insure the voltage and current specifications are met (as defined in Table 2-10). For further information regarding power delivery, decoupling and layout guidelines, refer to the appropriate platform design guidelines.

2.3.2 V_{TT} Decoupling

Bulk decoupling must be provided on the baseboard. Decoupling solutions must be sized to meet the expected load. To insure optimal performance, various factors associated with the power delivery solution must be considered including regulator type, power plane and trace sizing, and component placement. A conservative decoupling solution consists of a combination of low ESR bulk capacitors and high frequency ceramic capacitors. For further information regarding power delivery, decoupling and layout guidelines, refer to the appropriate platform design guidelines.

2.3.3 Front Side Bus AGTL+ Decoupling

The Dual-Core Intel Xeon Processor 5000 series integrate signal termination on the die, as well as a portion of the required high frequency decoupling capacitance on the processor package. However, additional high frequency capacitance must be added to the baseboard to properly decouple the return currents from the FSB. Bulk decoupling must also be provided by the baseboard for proper AGTL+ bus operation. Decoupling guidelines are described in the appropriate platform design guidelines.

2.4 Front Side Bus Clock (BCLK[1:0]) and Processor Clocking

BCLK[1:0] directly controls the FSB interface speed as well as the core frequency of the processor. As in previous processor generations, the Dual-Core Intel Xeon Processor 5000 series core frequency is a multiple of the BCLK[1:0] frequency. The processor bus ratio multiplier is set during manufacturing. The default setting is for the maximum speed of the processor. It is possible to override this setting using software (see the *IA-32 Intel® Architecture Software Developer's Manual, Volume 3A &3B*). This permits operation at lower frequencies than the processor's tested frequency.

The processor core frequency is configured during reset by using values stored internally during manufacturing. The stored value sets the highest bus fraction at which the particular processor can operate. If lower speeds are desired, the appropriate ratio can be configured via the IA32_FLEX_BRVID_SEL MSR. For details of operation at core frequencies lower than the maximum rated processor speed, refer to the *IA-32 Intel® Architecture Software Developer's Manual, Volume 3A &3B.*

Clock multiplying within the processor is provided by the internal phase locked loop (PLL), which requires a constant frequency BCLK[1:0] input, with exceptions for spread spectrum clocking. The Dual-Core Intel Xeon Processor 5000 series utilize differential clocks. Table 2-1 contains processor core frequency to FSB multipliers and their corresponding core frequencies.

Table 2-1. Core Frequency to FSB Multiplier Configuration

Core Frequency to FSB Multiplier	Core Frequency with 166 MHz FSB Clock	Processor Number	Notes
1/16	2.67 GHz	5030	1, 2, 3, 4
1/18	3 GHz	5050	1, 2, 3, 4
Core Frequency to FSB Multiplier	**Core Frequency with 266 MHz FSB Clock**		**Notes**
1/12	3.20 GHz	5063	1, 2, 3, 4
1/12	3.20 GHz	5060	1, 2, 3, 5
1/14	3.73 GHz	5080	1, 2, 3

Notes:
1. Individual processors operate only at or below the frequency marked on the package.
2. Listed frequencies are not necessarily committed production frequencies.
3. For valid processor core frequencies, refer to the *Dual-Core Intel® Xeon® Processor 5000 series Specification Update*.
4. Mid-voltage (MV) processors only.
5. The lowest bus ratio supported by the Dual-Core Intel Xeon Processor 5000 series is 1/12.

2.4.1 Front Side Bus Frequency Select Signals (BSEL[2:0])

Upon power up, the FSB frequency is set to the maximum supported by the individual processor. BSEL[2:0] are open drain outputs which must be pulled up to VTT, and are used to select the FSB frequency. Please refer to Table 2-12 for DC specifications. Table 2-2 defines the possible combinations of the signals and the frequency associated with each combination. The frequency is determined by the processor(s), chipset, and clock synthesizer. All FSB agents must operate at the same core and FSB frequency. See the appropriate platform design guidelines for further details.

Table 2-2. BSEL[2:0] Frequency Table

BSEL2	BSEL1	BSEL0	Bus Clock Frequency
0	0	0	266.67 MHz
0	0	1	Reserved
0	1	0	Reserved
0	1	1	166.67 MHz
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

2.4.2 Phase Lock Loop (PLL) and Filter

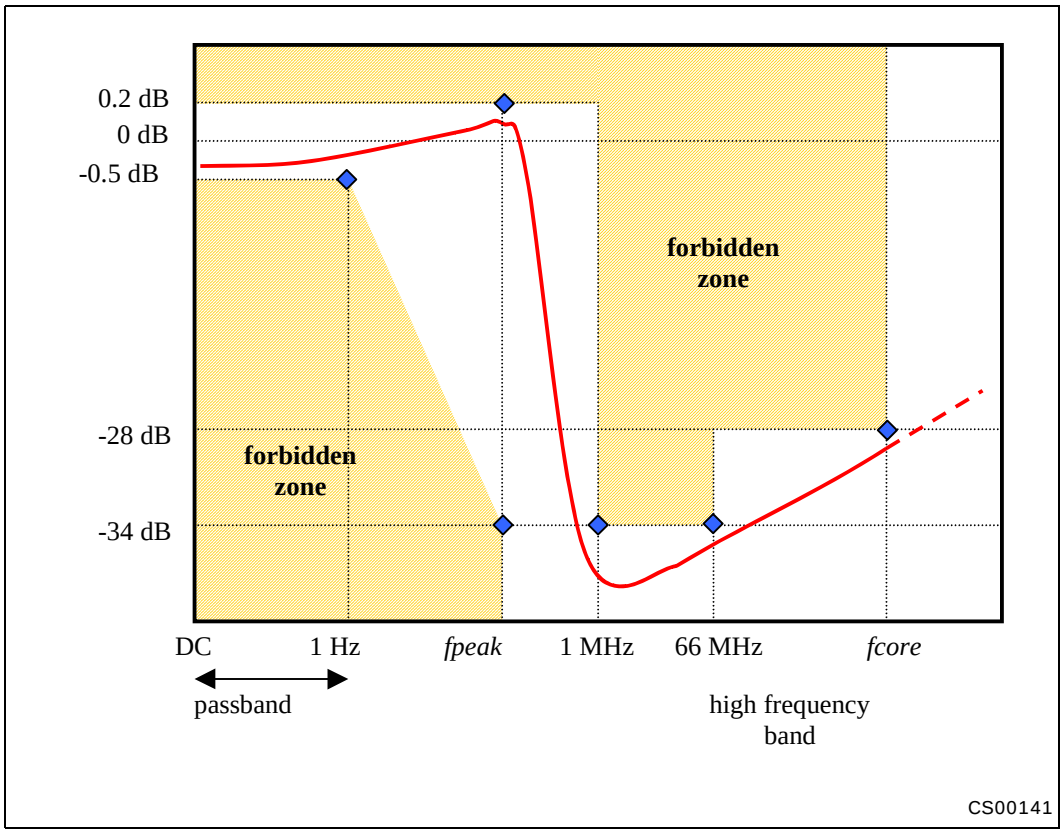
V_{CCA} and $V_{CCIOPLL}$ are power sources required by the PLL clock generators on the Dual-Core Intel Xeon Processor 5000 series. Since these PLLs are analog in nature, they require low noise power supplies for minimum jitter. Jitter is detrimental to the system: it degrades external I/O timings as well as internal core timings (that is, maximum frequency). To prevent this degradation, these supplies must be low pass filtered from V_{TT}.

The AC low-pass requirements are as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

The filter requirements are illustrated in Figure 2-1. For recommendations on implementing the filter, refer to the appropriate platform design guidelines.

Figure 2-1. Phase Lock Loop (PLL) Filter Requirements



Notes:
1. Diagram not to scale.
2. No specifications for frequencies beyond f_{core} (core frequency).
3. f_{peak}, if existent, should be less than 0.05 MHz.
4. f_{core} represents the maximum core frequency supported by the platform.

2.5 Voltage Identification (VID)

The Voltage Identification (VID) specification for the Dual-Core Intel Xeon Processor 5000 series set by the VID signals is the reference VR output voltage to be delivered to the processor Vcc pins. VID signals are open drain outputs, which must be pulled up to V_{TT}. Please refer to Table 2-12 for the DC specifications for these signals. A minimum voltage is provided in Table 2-10 and changes with frequency. This allows processors running at a higher frequency to have a relaxed minimum voltage specification. The specifications have been set such that one voltage regulator can operate with all supported frequencies.

Individual processor VID values may be calibrated during manufacturing such that two devices at the same core frequency may have different default VID settings. This is reflected by the VID range values provided in Table 2-3.

The Dual-Core Intel Xeon Processor 5000 series use six voltage identification signals, VID[5:0], to support automatic selection of power supply voltages. The processor uses the VTTPWRGD input to determine that the supply voltage for VID[5:0] is stable and within specification.Table 2-3 specifies the voltage level corresponding to the state of VID[5:0]. A '1' in this table refers to a high voltage level and a '0' refers to a low voltage level. The definition provided in Table 2-3 is not related in any way to previous Intel® Xeon® processors or voltage regulator designs. If the processor socket is empty (VID[5:0] = x11111), or the voltage regulation circuit cannot supply the voltage that is requested, it must disable itself.

The Dual-Core Intel Xeon Processor 5000 series provide the ability to operate while transitioning to an adjacent VID and its associated processor core voltage (V_{CC}). This will represent a DC shift in the load line. It should be noted that a low-to-high or high-to-low voltage state change may result in as many VID transitions as necessary to reach the target core voltage. Transitions above the specified VID are not permitted. Table 2-10 includes VID step sizes and DC shift ranges. Minimum and maximum voltages must be maintained as shown in Table 2-11 and Figure 2-4.

The VRM or EVRD utilized must be capable of regulating its output to the value defined by the new VID. DC specifications for dynamic VID transitions are included in Table 2-10 and Table 2-11.

Power source characteristics must be guaranteed to be stable whenever the supply to the voltage regulator is stable.

Table 2-3. Voltage Identification Definition (Sheet 1 of 2)

VID4	VID3	VID2	VID1	VID0	VID5	V_{CC_MAX}		VID4	VID3	VID2	VID1	VID0	VID5	V_{CC_MAX}
0	1	0	1	0	0	0.8375		1	1	0	1	0	0	1.2125
0	1	0	0	1	1	0.8500		1	1	0	0	1	1	1.2250
0	1	0	0	1	0	0.8625		1	1	0	0	1	0	1.2375
0	1	0	0	0	1	0.8750		1	1	0	0	0	1	1.2500
0	1	0	0	0	0	0.8875		1	1	0	0	0	0	1.2625
0	0	1	1	1	1	0.9000		1	0	1	1	1	1	1.2750
0	0	1	1	1	0	0.9125		1	0	1	1	1	0	1.2875
0	0	1	1	0	1	0.9250		1	0	1	1	0	1	1.3000
0	0	1	1	0	0	0.9375		1	0	1	1	0	0	1.3125
0	0	1	0	1	1	0.9500		1	0	1	0	1	1	1.3250
0	0	1	0	1	0	0.9625		1	0	1	0	1	0	1.3375

Table 2-3. Voltage Identification Definition (Sheet 2 of 2)

VID4	VID3	VID2	VID1	VID0	VID5	V_{CC_MAX}		VID4	VID3	VID2	VID1	VID0	VID5	V_{CC_MAX}
0	0	1	0	0	1	0.9750		1	0	1	0	0	1	1.3500
0	0	1	0	0	0	0.9875		1	0	1	0	0	0	1.3625
0	0	0	1	1	1	1.0000		1	0	0	1	1	1	1.3750
0	0	0	1	1	0	1.0125		1	0	0	1	1	0	1.3875
0	0	0	1	0	1	1.0250		1	0	0	1	0	1	1.4000
0	0	0	1	0	0	1.0375		1	0	0	1	0	0	1.4125
0	0	0	0	1	1	1.0500		1	0	0	0	1	1	1.4250
0	0	0	0	1	0	1.0625		1	0	0	0	1	0	1.4375
0	0	0	0	0	1	1.0750		1	0	0	0	0	1	1.4500
0	0	0	0	0	0	1.0875		1	0	0	0	0	0	1.4625
1	1	1	1	1	1	OFF[1]		0	1	1	1	1	1	1.4750
1	1	1	1	1	0	OFF[1]		0	1	1	1	1	0	1.4875
1	1	1	1	0	1	1.1000		0	1	1	1	0	1	1.5000
1	1	1	1	0	0	1.1125		0	1	1	1	0	0	1.5125
1	1	1	0	1	1	1.1250		0	1	1	0	1	1	1.5250
1	1	1	0	1	0	1.1375		0	1	1	0	1	0	1.5375
1	1	1	0	0	1	1.1500		0	1	1	0	0	1	1.5500
1	1	1	0	0	0	1.1625		0	1	1	0	0	0	1.5625
1	1	0	1	1	1	1.1750		0	1	0	1	1	1	1.5750
1	1	0	1	1	0	1.1875		0	1	0	1	1	0	1.5875
1	1	0	1	0	1	1.2000		0	1	0	1	0	1	1.6000

Notes:
1. When this VID pattern is observed, the voltage regulator output should be disabled.
2. Shading denotes the expected VID range of the Dual-Core Intel Xeon Processor 5000 series [1.0750 V - 1.3500 V].

Table 2-4. Loadline Selection Truth Table for LL_ID[1:0]

LL_ID1	LL_ID0	Description
0	0	Reserved
0	1	Dual-Core Intel Xeon Processor 5000 Series
1	0	Reserved
1	1	Reserved

Note:
1. The LL_ID[1:0] signals are used to select the correct loadline slope for the processor.
2. These signals are not connected to the processor die.
3. A logic 0 is achieved by pulling the signal to ground on the package.
4. A logic 1 is achieved by leaving the signal as a no connect on the package.

Table 2-5. Market Segment Selection Truth Table for MS_ID[1:0]

MS_ID1	MS_ID0	Description
0	0	Dual-Core Intel Xeon Processor 5000 Series
0	1	Reserved
1	0	Reserved
1	1	Reserved

Note:
1. The MS_ID[1:0] signals are provided to indicate the Market Segment for the processor and may be used for future processor compatibility or for keying. System management software may utilize these signals to identify the processor installed.
2. These signals are not connected to the processor die.
3. A logic 0 is achieved by pulling the signal to ground on the package.
4. A logic 1 is achieved by leaving the signal as a no connect on the package.

2.6 Reserved or Unused Signals

All Reserved signals must remain unconnected. Connection of these signals to V_{CC}, V_{TT}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors. See Chapter 4, “Land Listing” for a land listing of the processor and the location of all Reserved signals.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. Unused active high inputs, should be connected through a resistor to ground (V_{SS}). Unused outputs can be left unconnected; however, this may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bidirectional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. Resistor values should be within ± 20% of the impedance of the baseboard trace for FSB signals. For unused AGTL+ input or I/O signals, use pull-up resistors of the same value as the on-die termination resistors (R_{TT}).

TAP, Asynchronous GTL+ inputs, and Asynchronous GTL+ outputs do not include on-die termination. Inputs and utilized outputs must be terminated on the baseboard. Unused outputs may be terminated on the baseboard or left unconnected. Note that leaving unused outputs unterminated may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. Signal termination for these signal types is discussed in the appropriate platform design guidelines.

The TESTHI signals must be tied to the processor V_{TT} using a matched resistor, where a matched resistor has a resistance value within +/-20% of the impedance of the board transmission line traces. For example, if the trace impedance is 50 Ω, then a value between 40 Ω and 60 Ω is required.

The TESTHI signals may use individual pull-up resistors or be grouped together as detailed below. A matched resistor must be used for each group:

- TESTHI[1:0] - can be grouped together with a single pull-up to V_{TT}
- TESTHI[7:2] - can be grouped together with a single pull-up to V_{TT}
- TESTHI8 – cannot be grouped with other TESTHI signals
- TESTHI9 – cannot be grouped with other TESTHI signals
- TESTHI10 – cannot be grouped with other TESTHI signals
- TESTHI11 – cannot be grouped with other TESTHI signals

2.7 Front Side Bus Signal Groups

The FSB signals have been combined into groups by buffer type. AGTL+ input signals have differential input buffers, which use GTLREF as a reference level. In this document, the term “AGTL+ Input” refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, “AGTL+ Output” refers to the AGTL+ output group as well as the AGTL+ I/O group when driving. AGTL+ asynchronous outputs can become active anytime and include an active PMOS pull-up transistor to assist the during the first clock of a low-to-high voltage transition.

With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals whose timings are specified with respect to rising edge of BCLK0 (ADS#, HIT#, HITM#, and so forth) and the second set is for the source synchronous signals which are relative to their respective strobe lines (data and address) as well as rising edge of BCLK0. Asynchronous signals are still present (A20M#, IGNNE#, and so forth) and can become active at any time during the clock cycle. Table 2-6 identifies which signals are common clock, source synchronous and asynchronous.

Table 2-6. FSB Signal Groups

Signal Group	Type	Signals[1]
AGTL+ Common Clock Input	Synchronous to BCLK[1:0]	BPRI#, DEFER#, RESET#, RS[2:0]#, RSP#, TRDY#
AGTL+ Common Clock I/O	Synchronous to BCLK[1:0]	ADS#, AP[1:0]#, BINIT#[2], BNR#[2], BPM[5:0]#, BR[1:0]#, DBSY#, DP[3:0]#, DRDY#, HIT#[2], HITM#[2], LOCK#, MCERR#[2]
AGTL+ Source Synchronous I/O	Synchronous to assoc. strobe	<table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>REQ[4:0]#,A[16:3]#</td><td>ADSTB0#</td></tr><tr><td>A[35:17]#</td><td>ADSTB1#</td></tr><tr><td>D[15:0]#, DBI0#</td><td>DSTBP0#, DSTBN0#</td></tr><tr><td>D[31:16]#, DBI1#</td><td>DSTBP1#, DSTBN1#</td></tr><tr><td>D[47:32]#, DBI2#</td><td>DSTBP2#, DSTBN2#</td></tr><tr><td>D[63:48]#, DBI3#</td><td>DSTBP3#, DSTBN3#</td></tr></table>
AGTL+ Strobes I/O	Synchronous to BCLK[1:0]	ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#
AGTL+ Asynchronous Output	Asynchronous	FERR#/PBE#, IERR#, PROCHOT#
GTL+ Asynchronous Input	Asynchronous	A20M#, FORCEPR#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, SMI#, STPCLK#
GTL+ Asynchronous Output	Asynchronous	THERMTRIP#
FSB Clock	Clock	BCLK1, BCLK0
TAP Input	Synchronous to TCK	TCK, TDI, TMS TRST#
TAP Output	Synchronous to TCK	TDO
Power/Other	Power/Other	BSEL[2:0], COMP[7:0], GTLREF_ADD_C[1:0], GTLREF_DATA_C[1:0], LL_ID[1:0], MS_ID[1:0], PWRGOOD, Reserved, SKTOCC#, TEST_BUS, TESTHI[11:0], THERMDA, THEMRDA2, THERMDC, THERMDC2, V_{CC}, V_{CCA}, $V_{CCIOPLL}$, VCC_DIE_SENSE, VCC_DIE_SENSE2, VID[5:0], VID_SELECT, VSS_DIE_SENSE, VSS_DIE_SENSE2, V_{SS}, V_{SSA}, V_{TT}, VTTOUT, VTTPWRGD

Notes:
1. Refer to Section 5 for signal descriptions.
2. These signals may be driven simultaneously by multiple agents (Wired-OR).

Table 2-7 outlines the signals which include on-die termination (R_{TT}). Open drain signals are also included. Table 2-8 provides signal reference voltages.

Table 2-7. Signal Description Table

Signals with R_{TT}	Signals with no R_{TT}
A[35:3]#, ADS#, ADSTB[1:0]#, AP[1:0]#, BINIT#, BNR#, BPRI#, COMP[7:4], D[63:0]#, DBI[3:0]#, DBSY#, DEFER#, DP[3:0]#, DRDY#, DSTBN[3:0]#, DSTBP[3:0]#, FORCEPR#, HIT#, HITM#, LOCK#, MCERR#, PROCHOT#, REQ[4:0]#, RS[2:0]#, RSP#, TCK[2], TDI[2], TEST_BUS, TMS[2], TRDY#, TRST#[2]	A20M#, BCLK[1:0], BPM[5:0]#, BR[1:0]#, BSEL[2:0], COMP[3:0], FERR#/PBE#, GTLREF_ADD_C[1:0], GTLREF_DATA_C[1:0], IERR#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, LL_ID[1:0], MS_ID[1:0], PWRGOOD, RESET#, SKTOCC#, SMI#, STPCLK#, TDO, TESTHI[11:0], THERMDA, THERMDA2, THERMDC, THERMDC2, THERMTRIP#, VCC_DIE_SENSE, VCC_DIE_SENSE2, VID[5:0], VID_SELECT, VSS_DIE_SENSE, VSS_DIE_SENSE2, VTTPWRGD
Open Drain Signals[1]	
BPM[5:0]#, BR0#, FERR#/PBE#, IERR#, PROCHOT#, TDO, THERMTRIP#	

Notes:
1. Signals that do not have R_{TT}, nor are actively driven to their high voltage level.
2. The on-die termination for these signals is not R_{TT}. TCK, TDI, and TMS have an approximately 150 KΩ pullup to V_{TT}.

Table 2-8. Signal Reference Voltages

GTLREF	VTT / 2
A[35:3]#, ADS#, ADSTB[1:0]#, AP[1:0]#, BINIT#, BNR#, BPM[5:0]#, BPRI#, BR[1:0]#, D[63:0]#, DBI[3:0]#, DBSY#, DEFER#, DP[3:0]#, DRDY#, DSTBN[3:0]#, DSTBP[3:0]#, FORCEPR#[2], HIT#, HITM#, IERR#, LINT0/INTR, LINT1/NMI, LOCK#, MCERR#, RESET#, REQ[4:0]#, RS[2:0]#, RSP#, TRDY#	A20M#, IGNNE#, INIT#, PWRGOOD[1], SMI#, STPCLK#, TCK[1], TDI[1], TMS[1], TRST#[1], VTTPWRGD

Notes:
1. These signals also have hysteresis added to the reference voltage. See Table 2-14 for more information.
2. Use Table 2-15 for signal FORCEPR# specifications.

2.8 GTL+ Asynchronous and AGTL+ Asynchronous Signals

Input signals such as A20M#, FORCEPR#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, SMI# and STPCLK# utilize GTL+ input buffers. Legacy output FERR#/PBE# and other non-AGTL+ signals IERR#, THERMTRIP# and PROCHOT# utilize GTL+ output buffers. All of these asynchronous GTL+ signals follow the same DC requirements as AGTL+ signals; however, the outputs are not driven high (during the electrical 0-to-1 transition) by the processor. FERR#/PBE#, IERR#, and IGNNE# have now been defined as AGTL+ asynchronous signals as they include an active p-MOS device. Asynchronous GTL+ and asynchronous AGTL+ signals do not have setup or hold time specifications in relation to BCLK[1:0]; however, all of the asynchronous GTL+ and asynchronous AGTL+ signals are required to be asserted/deasserted for at least six BCLKs in order for the processor to recognize them. See Table 2-15 for the DC specifications for the asynchronous GTL+ signal groups.

2.9 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, it is recommended that the processor(s) be first in the TAP chain and followed by any other components within the system. A translation buffer should be used to

connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage. Similar considerations must be made for TCK, TMS, and TRST#. Two copies of each signal may be required with each driving a different voltage level.

2.10 Mixing Processors

Intel supports and validates dual processor configurations only in which both processors operate with the same FSB frequency, core frequency, and have the same internal cache sizes. Mixing components operating at different internal clock frequencies is not supported and will not be validated by Intel [Note: Processors within a system must operate at the same frequency per bits [15:8] of the IA32_FLEX_BRVID_SEL MSR; however this does not apply to frequency transitions initiated due to thermal events, Enhanced HALT, Enhanced Intel SpeedStep® Technology transitions, or assertion of the FORCEPR# signal (See Chapter 6, "Thermal Specifications")]. Low voltage (LV), mid-voltage (MV) and full-power 64-bit Intel Xeon processors should not be mixed within a system. Not all operating systems can support dual processors with mixed frequencies. Intel does not support or validate operation of processors with different cache sizes. Mixing processors of different steppings but the same model (as per CPUID instruction) is supported. Details regarding the CPUID instruction are provided in the *AP-485 Intel® Processor Identification and the CPUID Instruction* application note.

2.11 Absolute Maximum and Minimum Ratings

Table 2-9 specifies absolute maximum and minimum ratings. Within functional operation limits, functionality and long-term reliability can be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function or its reliability will be severely degraded.

Although the processor contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields

Table 2-9. Processor Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes[1, 2]
V_{CC}	Core voltage with respect to V_{SS}	-0.30	1.55	V	
V_{TT}	FSB termination voltage with respect to V_{SS}	-0.30	1.55	V	
T_{CASE}	Processor case temperature	See Section 6	See Section 6	°C	
$T_{STORAGE}$	Storage temperature	-40	85	°C	3, 4, 5

Notes:
1. For functional operation, all processor electrical, signal quality, mechanical and thermal specifications must be satisfied.
2. Overshoot and undershoot voltage guidelines for input, output, and I/O signals are outlined in Section 3. Excessive overshoot or undershoot on any signal will likely result in permanent damage to the processor.
3. Storage temperature is applicable to storage conditions only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, please refer to the processor case temperature specifications.
4. This rating applies to the processor and does not include any tray or packaging.
5. Failure to adhere to this specification can affect the long term reliability of the processor.

2.12 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core (pads) unless noted otherwise. See Section 4.1 for the Dual-Core Intel Xeon Processor 5000 series land listings and Section 5.1 for signal definitions. Voltage and current specifications are detailed in Table 2-10. For platform planning refer to Table 2-11, which provides Voltage-Current projections. This same information is presented graphically in Figure 2-4.

BSEL[2:0] and VID[5:0] signals are specified in Table 2-12. The DC specifications for the AGTL+ signals are listed in Table 2-13. Legacy signals and Test Access Port (TAP) signals follow DC specifications similar to GTL+. The DC specifications for the PWRGOOD input and TAP signal group are listed in Table 2-14 and the Asynchronous GTL+ signal group is listed in Table 2-15. The VTTPWRGD signal is detailed in Table 2-16.

Table 2-10 through Table 2-16 list the DC specifications for the processor and are valid only while meeting specifications for case temperature (T_{CASE} as specified in Table 6-1), clock frequency, and input voltages. **Care should be taken to read all notes associated with each parameter.**

Table 2-10. Voltage and Current Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit	Notes [1,13]
VID	VID range	1.0750		1.3500	V	
V_{CC}	V_{CC} for Dual-Core Intel Xeon Processor 5000 series core. FMB processor.	See Table 2-11 and Figure 2-4			V	2, 3, 4, 6, 11
V_{VID_STEP}	VID step size during a transition			±12.5	mV	
V_{VID_SHIFT}	Total allowable DC load line shift from VID steps			425	mV	12
V_{TT}	FSB termination voltage (DC + AC specification)	1.140	1.20	1.260	V	10, 14
I_{CC}	I_{CC} for Dual-Core Intel Xeon Processor 5000 series with multiple VID **(667 MHz)**			115	A	4, 5, 6, 11
I_{CC}	I_{CC} for Dual-Core Intel Xeon Processor 5000 series with multiple VID **(1066 MHz)**			150	A	4, 5, 6, 11
I_{CC}	I_{CC} for Dual-Core Intel Xeon Processor 5063 (MV) with multiple VID			115	A	4, 5, 6, 11
I_{CC_RESET}	I_{CC_RESET} for Dual-Core Intel Xeon Processor 5000 series with multiple VID **(667 MHz)**			115	A	18

Table 2-10. Voltage and Current Specifications (Sheet 2 of 2)

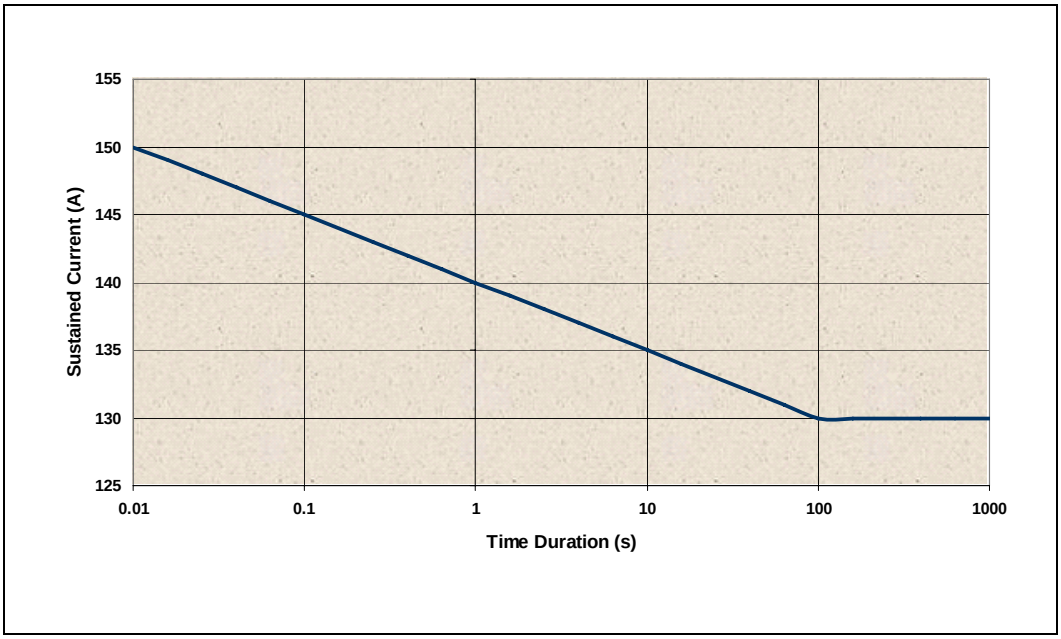
Symbol	Parameter	Min	Typ	Max	Unit	Notes 1,13
I_{CC_RESET}	I_{CC_RESET} for Dual-Core Intel Xeon Processor 5000 series with multiple VID **(1066 MHz)**			150	A	18
I_{CC_RESET}	I_{CC_RESET} for Dual-Core Intel Xeon Processor 5063 (MV) with multiple VID			115	A	18
I_{TT}	Steady-state FSB Termination Current			6.1	A	16
$I_{TT\_POWER-UP}$	Power-up FSB Termination Current			8.0	A	19
I_{CC_TDC}	Thermal Design Current (TDC) for Dual-Core Intel Xeon Processor 5000 series **(667 MHz)**			100	A	6,15
I_{CC_TDC}	Thermal Design Current (TDC) for Dual-Core Intel Xeon Processor 5000 series **(1066 MHz)**			130	A	6,15
I_{CC_TDC}	Thermal Design Current (TDC) for Dual-Core Intel Xeon Processor 5063 (MV)			100	A	6,15
I_{CC_VTTOUT}	DC current that may be drawn from V_{TTOUT} per land			580	mA	17
I_{CC_VCCA}	I_{CC} for PLL power lands			120	mA	8
$I_{CC\_VCCIOPLL}$	I_{CC} for PLL power lands			100	mA	8
I_{CC_GTLREF}	I_{CC} for GTLREF			200	µA	9
I_{TCC}	I_{CC} during active thermal control circuit (TCC) for Dual-Core Intel Xeon Processor 5000 series			150	A	
I_{TCC}	I_{CC} during active thermal control circuit (TCC) for Dual-Core Intel Xeon Processor 5063 (MV)			115	A	
I_{SGNT}	I_{CC} Stop-Grant for Dual-Core Intel Xeon Processor 5000 series **(667 MHz)**			50	A	7
I_{SGNT}	I_{CC} Stop-Grant for Dual-Core Intel Xeon Processor 5000 series **(1066 MHz)**			60	A	7
I_{SGNT}	I_{CC} Stop-Grant for Dual-Core Intel Xeon Processor 5063 (MV)			40	A	7

Notes:

1. Unless otherwise noted, all specifications in this table apply to all processors and are based on final silicon validation/characterization.
2. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required. See Section 2.5 for more information.
3. The voltage specification requirements are measured across the VCC_DIE_SENSE and VSS_DIE_SENSE lands and across the VCC_DIE_SENSE2 and VSS_DIE_SENSE2 lands with a 100 MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
4. The processor must not be subjected to any static V_{CC} level that exceeds the V_{CC_MAX} associated with any particular current. Failure to adhere to this specification can shorten processor lifetime.
5. I_{CC_MAX} is specified at V_{CC_MAX}. The processor is capable of drawing I_{CC_MAX} for up to 10 ms. Refer to Figure 2-2 and Figure 2-3 for further details on the average processor current draw over various time durations.
6. FMB is the flexible motherboard guideline. These guidelines are for estimation purposes only.
7. The current specified is also for HALT and Enhanced HALT State.
8. These specifications apply to the PLL power lands VCCA, VCCIOPLL, and VSSA. See Section 2.4.2 for details. These parameters are based on design characterization and are not tested.
9. This specification represents the total current for GTLREF_DATA and GTLREF_ADD per core.
10. V_{TT} must be provided via a separate voltage source and must not be connected to V_{CC}. This specification is measured at the land.

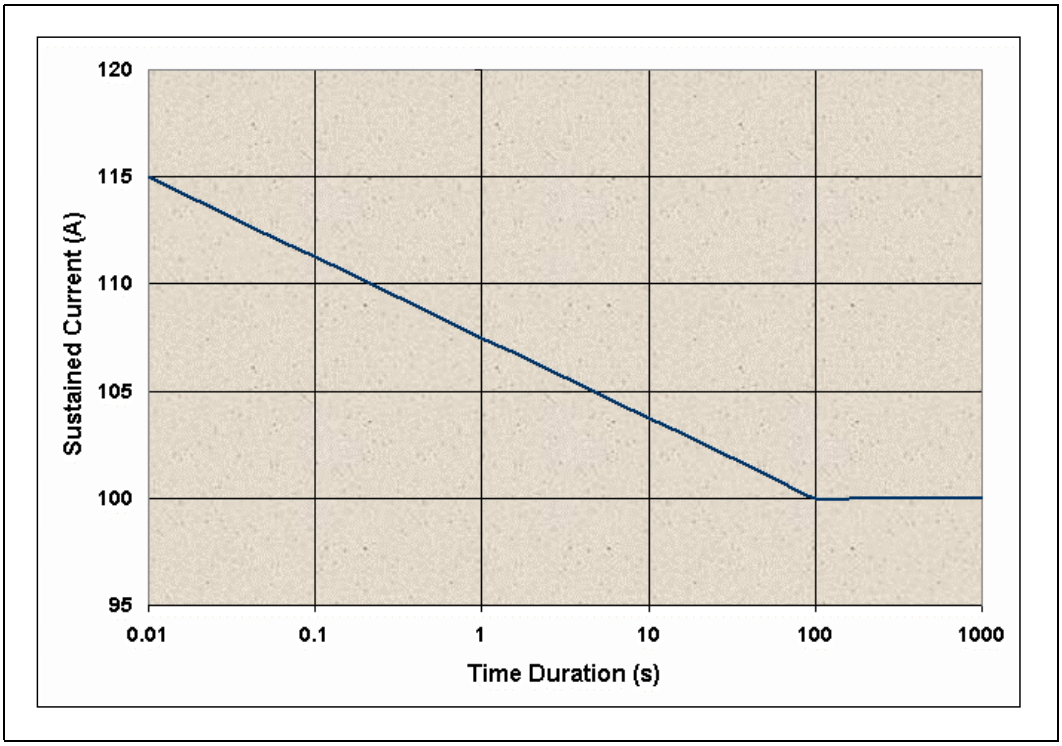
11. Minimum VCC and maximum ICC are specified at the maximum processor case temperature (TCASE) shown in Table 6-1.
12. This specification refers to the total reduction of the load line due to VID transitions below the specified VID.
13. Individual processor VID values may be calibrated during manufacturing such that two devices at the same frequency may have different VID settings.
14. Baseboard bandwidth is limited to 20 MHz.
15. I_{CC_TDC} is the sustained (DC equivalent) current that the processor is capable of drawing indefinitely and should be used for the voltage regulator temperature assessment. The voltage regulator is responsible for monitoring its temperature and asserting the necessary signal to inform the processor of a thermal excursion. Please see the applicable design guidelines for further details. The processor is capable of drawing I_{CC_TDC} indefinitely. Refer to Figure 2-2 and Figure 2-3 for further details on the average processor current draw over various time durations. This parameter is based on design characterization and is not tested.
16. This specification is per-processor. This is a steady-state I_{TT} current specification, which is applicable when both V_{TT} and V_{CC} are high. This parameter is based on design characterization and is not tested. Please refer to the *I_{TT} Analysis of System Bus Components - Bensley Platform Whitepaper* for platform implementation guidance.
17. I_{CC_VTTOUT} is specified at 1.2 V.
18. I_{CC_RESET} is specified while PWRGOOD and RESET# are asserted.
19. This specification is per-processor. This is a power-up peak current specification, which is applicable when V_{TT} is powered up and V_{CC} is not. This parameter is based on design characterization and is not tested.

Figure 2-2. Dual-Core Intel® Xeon® Processor 5000 Series (1066 MHz) Load Current versus Time



Notes:
1. Processor or Voltage Regulator thermal protection circuitry should not trip for load currents greater than I_{CC_TDC}.
2. Not 100% tested. Specified by design characterization.

Figure 2-3. Dual-Core Intel® Xeon® Processor 5000 Series (667 MHz) and Dual-Core Intel® Xeon® Processor 5063 (MV) Load Current versus Time



Notes:
1. Processor or Voltage Regulator thermal protection circuitry should not trip for load currents greater than I_{CC_TDC}.
2. Not 100% tested. Specified by design characterization.

Table 2-11. V_{CC} Static and Transient Tolerance (Sheet 1 of 2)

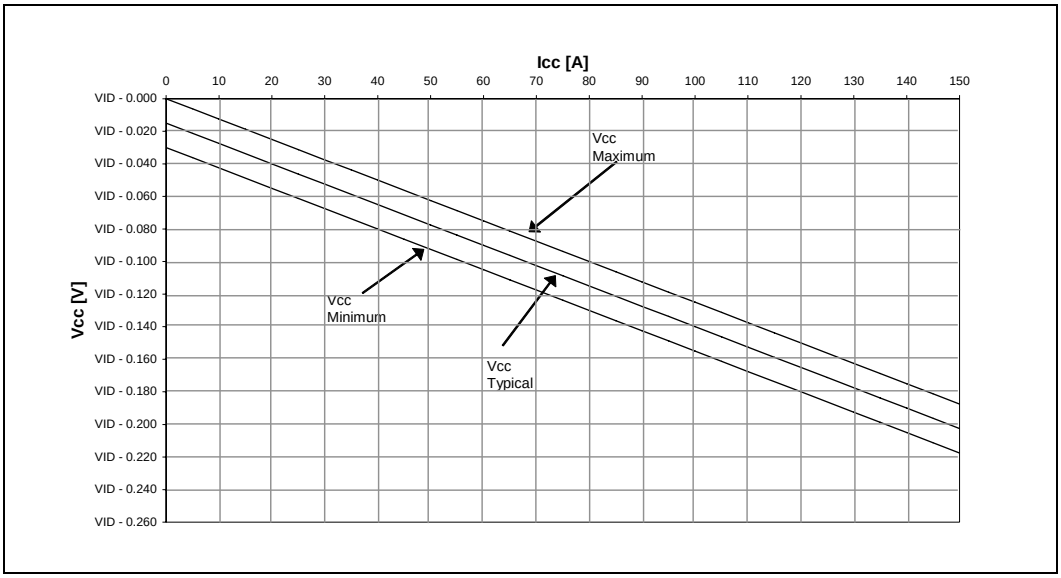
I_{CC} (A)	V_{CC_Max} (V)	V_{CC_Typ} (V)	V_{CC_Min} (V)	Notes
0	VID - 0.000	VID - 0.015	VID - 0.030	1, 2, 3, 4
5	VID - 0.006	VID - 0.021	VID - 0.036	
10	VID - 0.013	VID - 0.028	VID - 0.043	
15	VID - 0.019	VID - 0.034	VID - 0.049	
20	VID - 0.025	VID - 0.040	VID - 0.055	
25	VID - 0.031	VID - 0.046	VID - 0.061	
30	VID - 0.038	VID - 0.053	VID - 0.068	
35	VID - 0.044	VID - 0.059	VID - 0.074	
40	VID - 0.050	VID - 0.065	VID - 0.080	
45	VID - 0.056	VID - 0.071	VID - 0.086	
50	VID - 0.063	VID - 0.078	VID - 0.093	
55	VID - 0.069	VID - 0.084	VID - 0.099	
60	VID - 0.075	VID - 0.090	VID - 0.105	
65	VID - 0.081	VID - 0.096	VID - 0.111	
70	VID - 0.087	VID - 0.103	VID - 0.118	
75	VID - 0.094	VID - 0.109	VID - 0.124	

Table 2-11. V_{CC} Static and Transient Tolerance (Sheet 2 of 2)

I_{CC} (A)	V_{CC_Max} (V)	V_{CC_Typ} (V)	V_{CC_Min} (V)	Notes
80	VID - 0.100	VID - 0.115	VID - 0.130	
85	VID - 0.106	VID - 0.121	VID - 0.136	
90	VID - 0.113	VID - 0.128	VID - 0.143	
95	VID - 0.119	VID - 0.134	VID - 0.149	
100	VID - 0.125	VID - 0.140	VID - 0.155	
105	VID - 0.131	VID - 0.146	VID - 0.161	
110	VID - 0.138	VID - 0.153	VID - 0.168	
115	VID - 0.144	VID - 0.159	VID - 0.174	
120	VID - 0.150	VID - 0.165	VID - 0.180	
125	VID - 0.156	VID - 0.171	VID - 0.186	
130	VID - 0.163	VID - 0.178	VID - 0.193	
135	VID - 0.169	VID - 0.184	VID - 0.199	
140	VID - 0.175	VID - 0.190	VID - 0.205	
145	VID - 0.181	VID - 0.196	VID - 0.211	
150	VID - 0.188	VID - 0.203	VID - 0.218	

Notes:
1. The V_{CC_MIN} and V_{CC_MAX} loadlines represent static and transient limits. Please see Section 2.12.1 for V_{CC} overshoot specifications.
2. This table is intended to aid in reading discrete points on Figure 2-4.
3. The loadlines specify voltage limits at the die measured at the VCC_DIE_SENSE and VSS_DIE_SENSE lands and at the VCC_DIE_SENSE2 and VSS_DIE_SENSE2 lands. Voltage regulation feedback for voltage regulator circuits must also be taken from processor VCC_DIE_SENSE and VSS_DIE_SENSE lands and VCC_DIE_SENSE2 and VSS_DIE_SENSE2 lands. Please refer to the appropriate platform design guide for details on VR implementation.
4. Non-shading denotes the expected I_{CC} range applies to both Dual-Core Intel Xeon Processor 5000 series (1066 MHz & 667 MHz) and Dual-Core Intel Xeon Processor 5063 (MV). Shading denotes the expected I_{CC} range applies to Dual-Core Intel Xeon Processor 5000 series **(1066 MHz)** only. [120 A - 150 A]

Figure 2-4. V_{CC} Static and Transient Tolerance Load Lines



Notes:
1. The V_{CC_MIN} and V_{CC_MAX} loadlines represent static and transient limits. Please see Section 2.12.1 for VCC overshoot specifications.
2. Refer to Table 2-10 for processor VID information.

3. Refer to Table 2-11 for processor VCC information.
4. The load lines specify voltage limits at the die measured at the VCC_DIE_SENSE and VSS_DIE_SENSE lands and at the VCC_DIE_SENSE2 and VSS_DIE_SENSE2 lands. Voltage regulation feedback for voltage regulator circuits must also be taken from processor VCC_DIE_SENSE and VSS_DIE_SENSE lands and VCC_DIE_SENSE2 and VSS_DIE_SENSE2 lands. Please refer to the appropriate platform design guide for details on VR implementation.

Table 2-12. BSEL[2:0], VID[5:0] Signal Group DC Specifications

Symbol	Parameter	Min	Max	Units	Notes[1]
R_{ON}	BSEL[2:0], VID[5:0] Buffer On Resistance	N/A	120	Ω	2
I_{OL}	Output Low Current	N/A	2.4	mA	2, 3
I_{OH}	Output High Current	N/A	460	µA	2, 3
V_{TOL}	Voltage Tolerance	0.95 * V_{TT}	1.05 * V_{TT}	V	4

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. These parameters are based on design characterization and are not tested.
3. I_{OL} is measured at 0.10*V_{TT}, I_{OH} is measured at 0.90*V_{TT}.
4. Please refer to the appropriate platform design guide for implementation details.

Table 2-13. AGTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
V_{IL}	Input Low Voltage	0.0	GTLREF - (0.10 * V_{TT})	V	2
V_{IH}	Input High Voltage	GTLREF + (0.10 * V_{TT})	V_{TT}	V	3, 4
V_{OH}	Output High Voltage	0.90 * V_{TT}	V_{TT}	V	4
I_{OL}	Output Low Current	N/A	V_{TT} / (0.50 * R_{TT_MIN} + R_{ON_MIN})	mA	4
I_{LI}	Input Leakage Current	N/A	± 200	µA	5, 6
I_{LO}	Output Leakage Current	N/A	± 200	µA	5, 6
R_{ON}	Buffer On Resistance	7	11	Ω	7

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the voltage range at a receiving agent that will be interpreted as an electrical low value.
3. V_{IH} is defined as the voltage range at a receiving agent that will be interpreted as an electrical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{TT}. However, input signal drivers must comply with the signal quality specifications in Section 3.
5. Leakage to V_{SS} with land held at V_{TT}.
6. Leakage to V_{TT} with land held at 300 mV.
7. This parameter is based on design characterization and is not tested

Table 2-14. PWRGOOD Input and TAP Signal Group DC Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Unit	Notes [1, 2]
V_{HYS}	Input Hysteresis	120	396	mV	3
V_{t+}	PWRGOOD Input Low to High Threshold Voltage	0.5 * (V_{TT} + V_{HYS_MIN} + 0.24)	0.5 * (V_{TT} + V_{HYS_MAX} + 0.24)	V	
	TAP Input Low to High Threshold Voltage	0.5 * (V_{TT} + V_{HYS_MIN})	0.5 * (V_{TT} + V_{HYS_MAX})	V	
V_{t-}	PWRGOOD Input High to Low Threshold Voltage	0.4 * V_{TT}	0.6 * V_{TT}	V	
	TAP Input High to Low Threshold Voltage	0.5 * (V_{TT} -V_{HYS_MAX})	0.5 * (V_{TT} - V_{HYS_MIN})	V	
V_{OH}	Output High Voltage	N/A	V_{TT}	V	4

Table 2-14. PWRGOOD Input and TAP Signal Group DC Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Unit	Notes [1, 2]
I_{LI}	Input Leakage Current	N/A	± 200	µA	
I_{LO}	Output Leakage Current	N/A	± 200	µA	
R_{ON}	Buffer On Resistance	7	11	Ω	5

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All outputs are open drain.
3. V_{HYS} represents the amount of hysteresis, nominally centered about 0.5 * V_{TT} for all PWRGOOD and TAP inputs.
4. PWRGOOD input and the TAP signal group must meet system signal quality specification in Section 3.
5. The maximum output current is based on maximum current handling capability of the buffer and is not specified into the test load.

Table 2-15. GTL+ Asynchronous and AGTL+ Asynchronous Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
V_{IL}	Input Low Voltage	0.0	(0.5 * V_{TT}) - (0.10 * V_{TT})	V	3, 11
V_{IH}	Input High Voltage	(0.5 * V_{TT}) + (0.10 * V_{TT})	V_{TT}	V	4, 5, 7, 11
V_{OH}	Output High Voltage	0.90*V_{TT}	V_{TT}	V	2, 5, 7
I_{OL}	Output Low Current	-	V_{TT}/ [(0.50*R_{TT_MIN})+(R_{ON_MIN})]	A	8
I_{LI}	Input Leakage Current	N/A	± 200	µA	9
I_{LO}	Output Leakage Current	N/A	± 200	µA	10
R_{ON}	Buffer On Resistance	7	11	Ω	6

Notes:
1.Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2.All outputs are open drain.
3.V_{IL} is defined as the voltage range at a receiving agent that will be interpreted as a logical low value.
4.V_{IH} is defined as the voltage range at a receiving agent that will be interpreted as a logical high value.
5.V_{IH} and V_{OH} may experience excursions above V_{TT}. However, input signal drivers must comply with the signal quality specifications in Section 3.
6.Refer to the processor HSPICE* I/O Buffer Models for I/V characteristics.
7.The V_{TT} referred to in these specifications refers to instantaneous V_{TT}.
8.The maximum output current is based on maximum current handling capability of the buffer and is not specified into the test load.
9.Leakage to V_{SS} with land held at V_{TT}.
10.Leakage to V_{TT} with land held at 300 mV.
11.LINT0/INTR and LINT1/NMI use GTLREF_ADD as a reference voltage. For these two signals V_{IH} = GTLREF_ADD + (0.10 * V_{TT}) and V_{IL}= GTLREF_ADD - (0.10 * V_{TT}).

Table 2-16. VTTPWRGD DC Specifications

Symbol	Parameter	Min	Max	Unit
V_{IL}	Input Low Voltage	0.0	0.30	V
V_{IH}	Input High Voltage	0.90	V_{TT}	V

2.12.1 V_{CC} Overshoot Specification

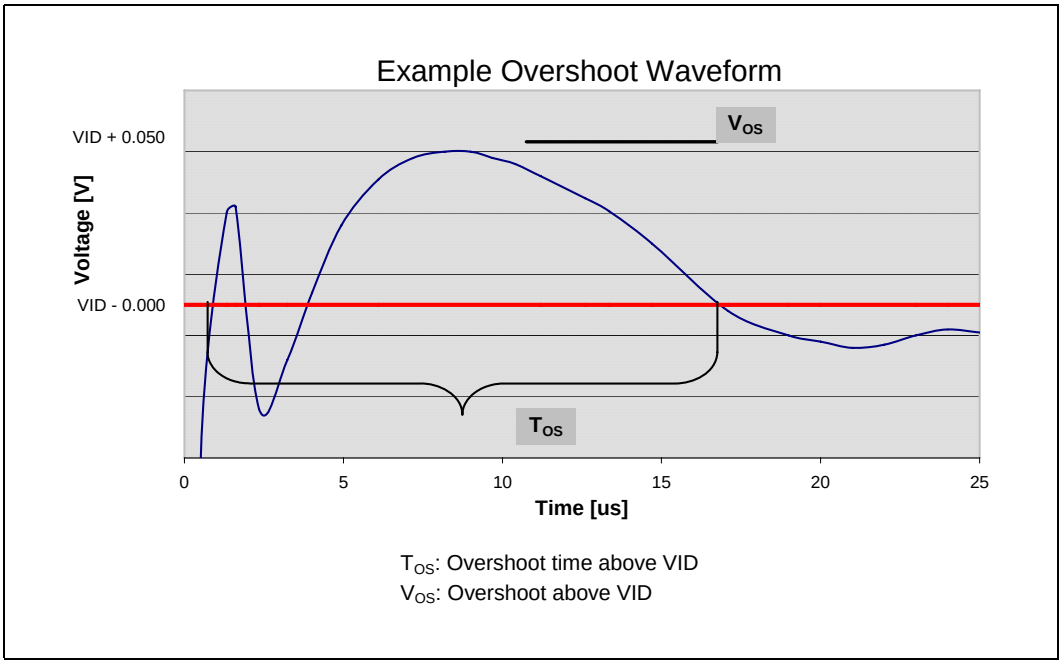
The Dual-Core Intel Xeon Processor 5000 series can tolerate short transient overshoot events where V_{CC} exceeds the VID voltage when transitioning from a high-to-low current load condition. This overshoot cannot exceed VID + V_{OS_MAX} (V_{OS_MAX} is the

maximum allowable overshoot above VID). These specifications apply to the processor die voltage as measured across the VCC_DIE_SENSE and VSS_DIE_SENSE lands and across the VCC_DIE_SENSE2 and VSS_DIE_SENSE2 lands.

Table 2-17. V_{CC} Overshoot Specifications

Symbol	Parameter	Min	Max	Units	Figure	Notes
V_{OS_MAX}	Magnitude of V_{CC} overshoot above VID		50	mV	2-5	
T_{OS_MAX}	Time duration of V_{CC} overshoot above VID		25	µs	2-5	

Figure 2-5. V_{CC} Overshoot Example Waveform



Notes:
1. V_{OS} is the measured overshoot voltage above VID.
2. T_{OS} is the measured time duration above VID.

2.12.2 Die Voltage Validation

Core voltage (VCC) overshoot events at the processor must meet the specifications in Table 2-17 when measured across the VCC_DIE_SENSE and VSS_DIE_SENSE lands and across the VCC_DIE_SENSE2 and VSS_DIE_SENSE2 lands. Overshoot events that are < 10 ns in duration may be ignored. These measurement of processor die level overshoot should be taken with a 100 MHz bandwidth limited oscilloscope.

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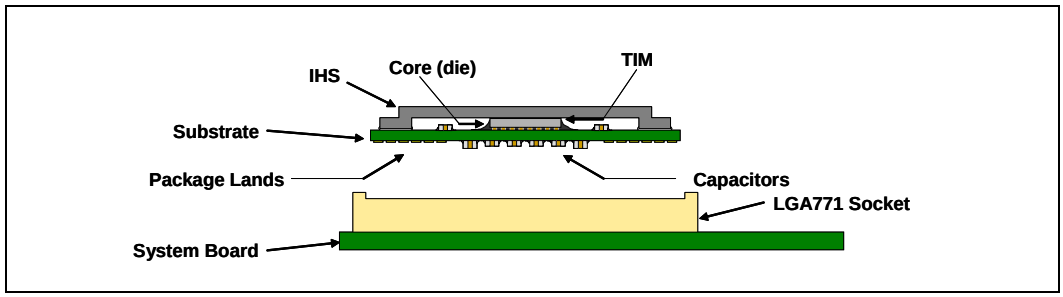
3 Mechanical Specifications

The Dual-Core Intel Xeon Processor 5000 series are packaged in a Flip Chip Land Grid Array (FC-LGA6) package that interfaces to the baseboard via a LGA771 socket. The package consists of a processor core mounted on a pinless substrate with 771 lands. An integrated heat spreader (IHS) is attached to the package substrate and core and serves as the interface for processor component thermal solutions such as a heatsink. Figure 3-1 shows a sketch of the processor package components and how they are assembled together. .

The package components shown in Figure 3-1 include the following:

1. Integrated Heat Spreader (IHS)
2. Thermal Interface Material (TIM)
3. Processor Core (die)
4. Package Substrate
5. Landside capacitors
6. Package Lands

Figure 3-1. Processor Package Assembly Sketch



Note: This drawing is not to scale and is for reference only.

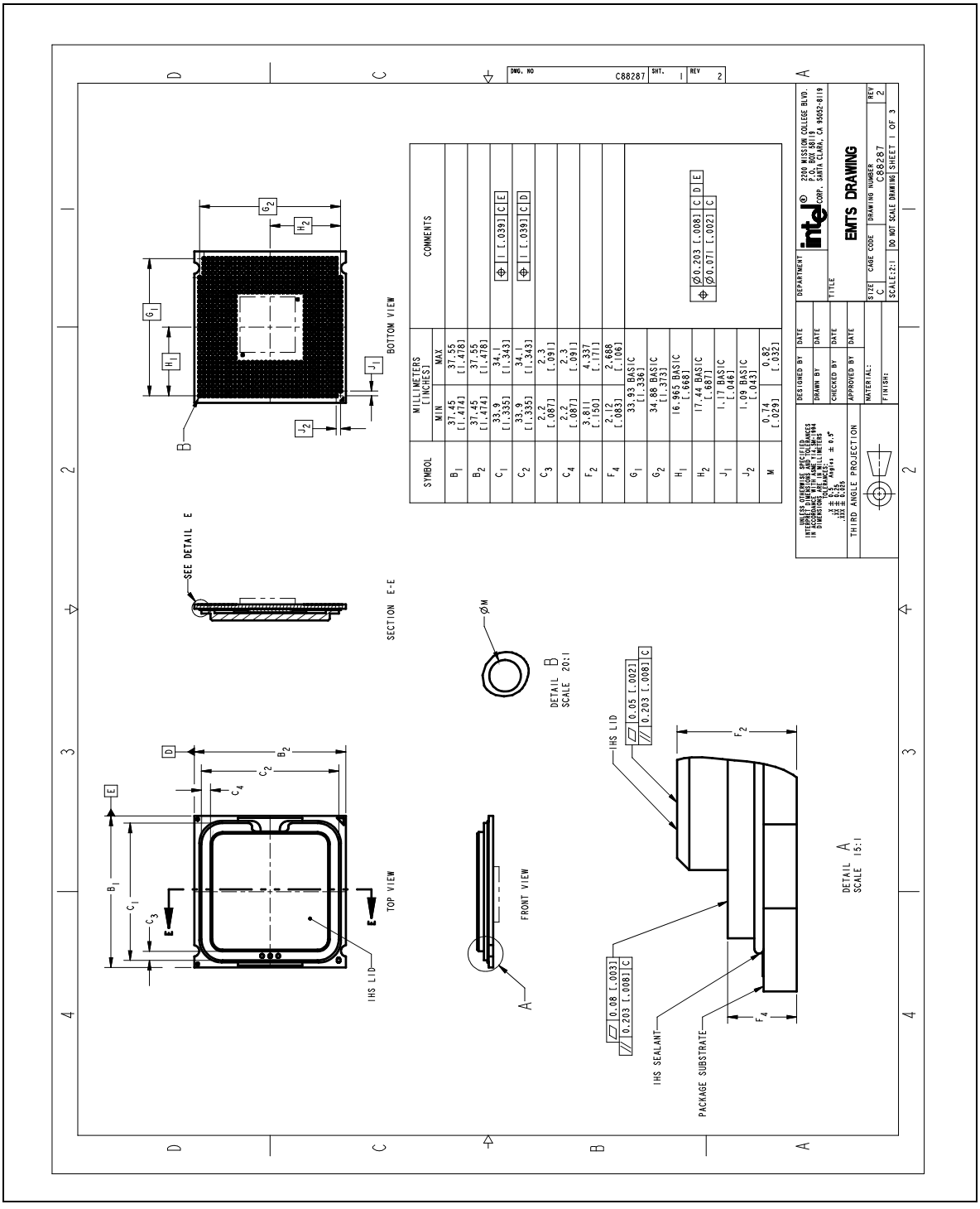
3.1 Package Mechanical Drawings

The package mechanical drawings are shown in Figure 3-2 through Figure 3-4. The drawings include dimensions necessary to design a thermal solution for the processor including:

1. Package reference and tolerance dimensions (total height, length, width, an so forth)
2. IHS parallelism and tilt
3. Land dimensions
4. Top-side and back-side component keepout dimensions
5. Reference datums

Note: All drawing dimensions are in mm [in.].

Figure 3-2. Processor Package Drawing (Sheet 1 of 3)



Note: Guidelines on potential IHS flatness variation with socket load plate actuation and installation of the cooling solution is available in the processor Thermal/Mechanical Design Guidelines.

Figure 3-3. Processor Package Drawing (Sheet 2 of 3)

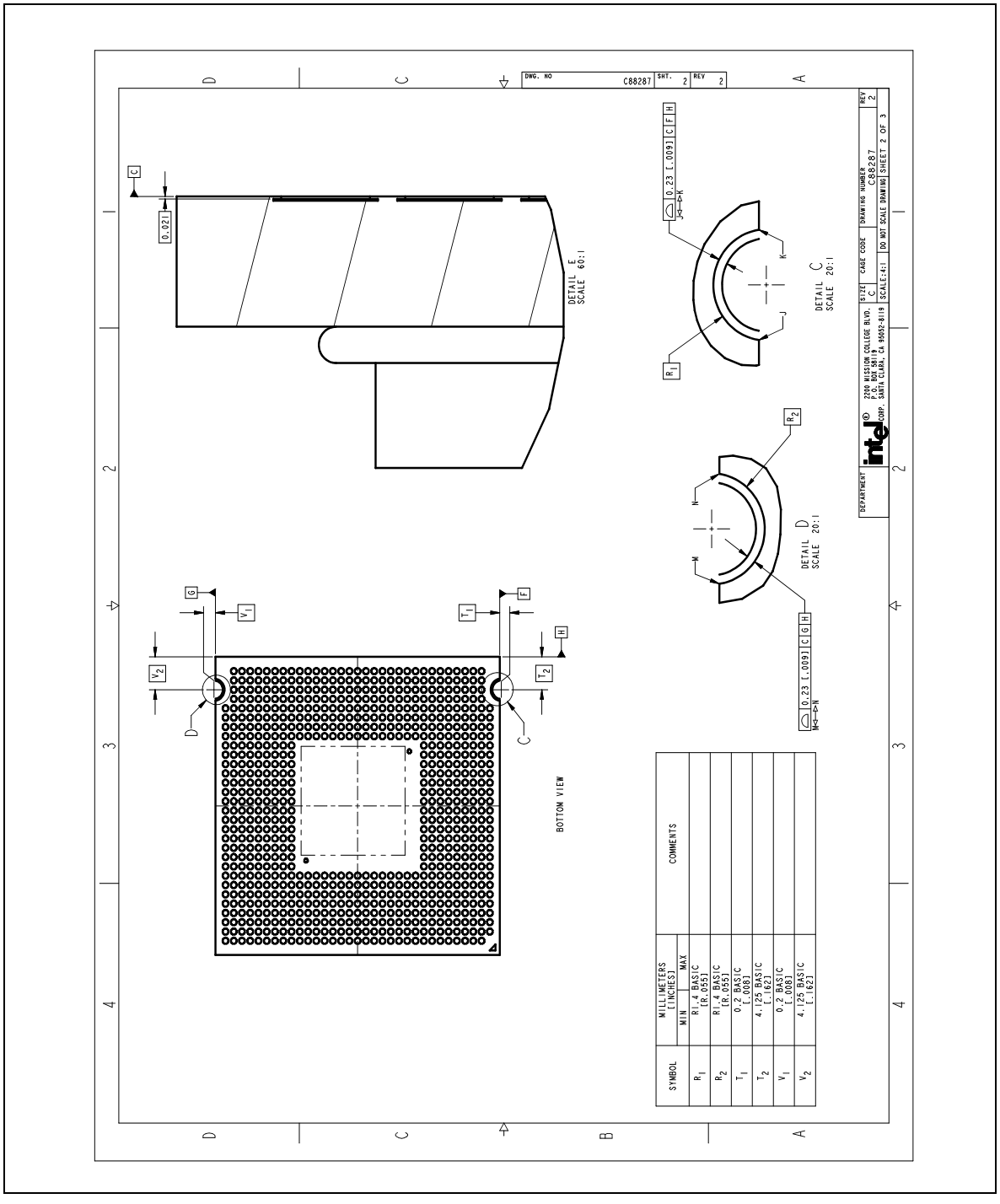
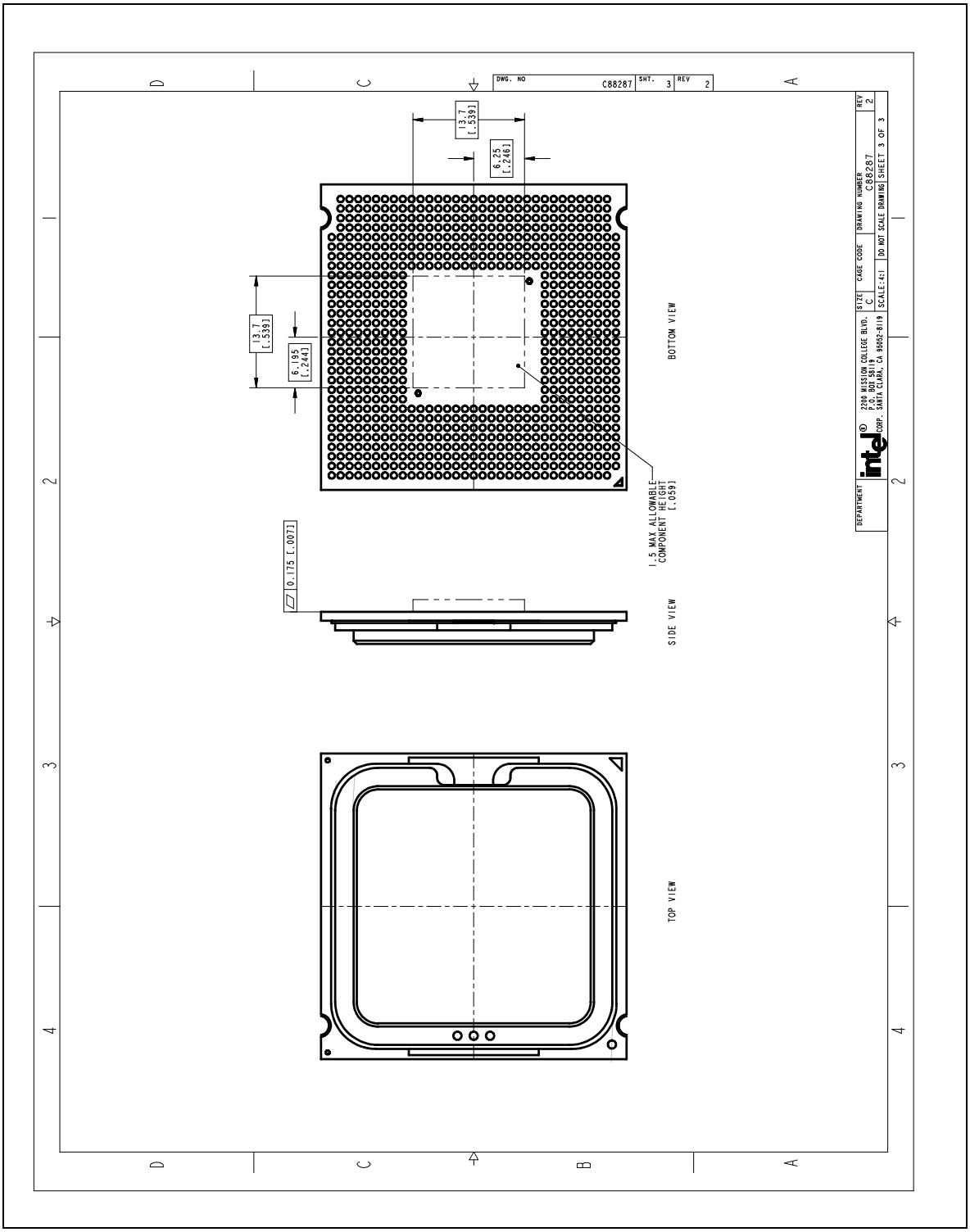


Figure 3-4. Processor Package Drawing (Sheet 3 of 3)



3.2 Processor Component Keepout Zones

The processor may contain components on the substrate that define component keepout zone requirements. A thermal and mechanical solution design must not intrude into the required keepout zones. Decoupling capacitors are typically mounted to either the topside or land-side of the package substrate. See Figure 3-4 for keepout zones.

3.3 Package Loading Specifications

Table 3-1 provides dynamic and static load specifications for the processor package. These mechanical load limits should not be exceeded during heatsink assembly, mechanical stress testing or standard drop and shipping conditions. The heatsink attach solutions must not include continuous stress onto the processor with the exception of a uniform load to maintain the heatsink-to-processor thermal interface. Also, any mechanical system or component testing should not exceed these limits. The processor package substrate should not be used as a mechanical reference or load-bearing surface for thermal or mechanical solutions. Please refer to the *Dual-Core Intel® Xeon® Processor 5000 Series Thermal/Mechanical Design Guidelines* for further details.

Table 3-1. Package Loading Specifications

Parameter	Board Thickness	R	Min	Max	Unit	Notes
Static Compressive Load	Apply for all board thickness from 1.57 mm (0.062”) to 2.54 mm (0.100”)	25mm <R< 45mm	80 18	133 30	N lbf	1, 2, 3, 9, 10, 11, 12, 13
		R>45mm	80 18	311 70	N lbf	
Dynamic Compressive Load	NA	NA	NA	311 N (max static compressive load) + 222 N dynamic loading 70 lbf (max static compressive load) + 50 lbf dynamic loading	N lbf	1, 3, 4, 5, 6
Transient Bend Limits	1.57 mm 0.062”	NA	NA	750	με	1,3,7,8
	2.16 mm 0.085”			700		
	2.54 mm 0.100”			650		

Notes:
1. These specifications apply to uniform compressive loading in a direction perpendicular to the IHS top surface.
2. This is the minimum and maximum static force that can be applied by the heatsink and retention solution to maintain the heatsink and processor interface.
3. Loading limits are for the LGA771 socket.
4. Dynamic compressive load applies to all board thickness.
5. Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement.
6. Test condition used a heatsink mass of 1 lbm with 50 g acceleration measured at heatsink mass. The dynamic portion of this specification in the product application can have flexibility in specific values, but the ultimate product of mass times acceleration should not exceed this dynamic load.
7. Transient bend is defined as the transient board deflection during manufacturing such as board assembly and system integration. It is a relatively slow bending event compared to shock and vibration tests.
8. For more information on the transient bend limits, please refer to the MAS document entitled *Manufacturing with Intel® Components using 771-land LGA Package that Interfaces with the Motherboard via a LGA771 Socket*.
9. Refer to the *Dual-Core Intel® Xeon® Processor 5000 Series Thermal/Mechanical Design Guidelines* for information on heatsink clip load metrology.

10. R is defined as the radial distance from the center of the LGA771 socket ball array to the center of heatsink load reaction point closest to the socket.
11. Applies to populated sockets in fully populated and partially populated socket configurations.
12. Through life or product. Condition must be satisfied at the beginning of life and at the end of life.
13. Rigid back is not allowed. The board should flex in the enabled configuration.

3.4 Package Handling Guidelines

Table 3-2 includes a list of guidelines on a package handling in terms of recommended maximum loading on the processor IHS relative to a fixed substrate. These package handling loads may be experienced during heatsink removal.

Table 3-2. Package Handling Guidelines

Parameter	Maximum Recommended	Units	Notes
Shear	311 70	N lbf	1,4,5
Tensile	111 25	N lbf	2,4,5
Torque	3.95 35	N-m LBF-in	3,4,5

Notes:
1. A shear load is defined as a load applied to the IHS in a direction parallel to the IHS top surface.
2. A tensile load is defined as a pulling load applied to the IHS in a direction normal to the IHS surface.
3. A torque load is defined as a twisting load applied to the IHS in an axis of rotation normal to the IHS top surface.
4. These guidelines are based on limited testing for design characterization and incidental applications (one time only).
5. Handling guidelines are for the package only and do not include the limits of the processor socket.

3.5 Package Insertion Specifications

The Dual-Core Intel Xeon Processor 5000 Series can be inserted and removed 15 times from an LGA771 socket.

3.6 Processor Mass Specifications

The typical mass of the Dual-Core Intel Xeon Processor 5000 series is 21.5 grams [0.76 oz.]. This includes all components which make up the entire processor product.

3.7 Processor Materials

The Dual-Core Intel Xeon Processor 5000 series are assembled from several components. The basic material properties are described in Table 3-3.

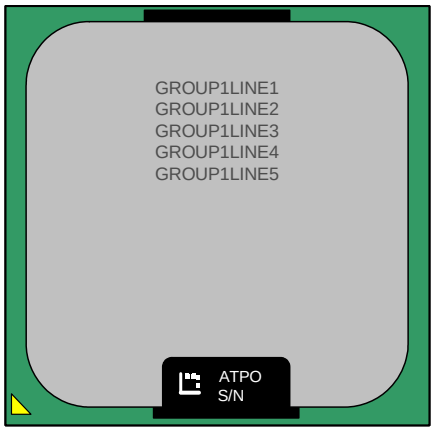
Table 3-3. Processor Materials

Component	Material
Integrated Heat Spreader (IHS)	Nickel over copper
Substrate	Fiber-reinforced resin
Substrate Lands	Gold over nickel

3.8 Processor Markings

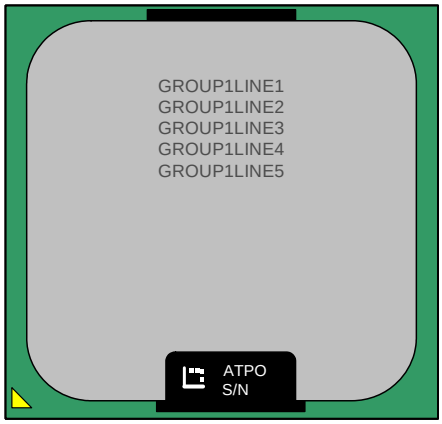
Figure 3-5 and Figure 3-6 shows the topside markings on the processor. This diagram aids in the identification of the Dual-Core Intel Xeon Processor 5000 series.

Figure 3-5. Dual-Core Intel Xeon Processor 5000 Series Top-side Markings



Legend:	Mark Text (Production Mark):
GROUP1LINE1	3733DP/4M/1066
GROUP1LINE2	Intel ® Xeon ®
GROUP1LINE3	5080 SXXX COO
GROUP1LINE4	i (M) © ‘05
GROUP1LINE5	FPO

Figure 3-6. Dual-Core Intel Xeon Processor 5063 (MV) Top-side Markings



Legend:	Mark Text (Production Mark):
GROUP1LINE1	3200DP/4M/1066/MV
GROUP1LINE2	Intel ® Xeon ®
GROUP1LINE3	5063 SXXX COO
GROUP1LINE4	i (M) © ‘05
GROUP1LINE5	FPO

3.9 Processor Land Coordinates

Figure 3-7 and Figure 3-8 show the top and bottom view of the processor land coordinates, respectively. The coordinates are referred to throughout the document to identify processor lands.

Figure 3-7. Processor Land Coordinates, Top View

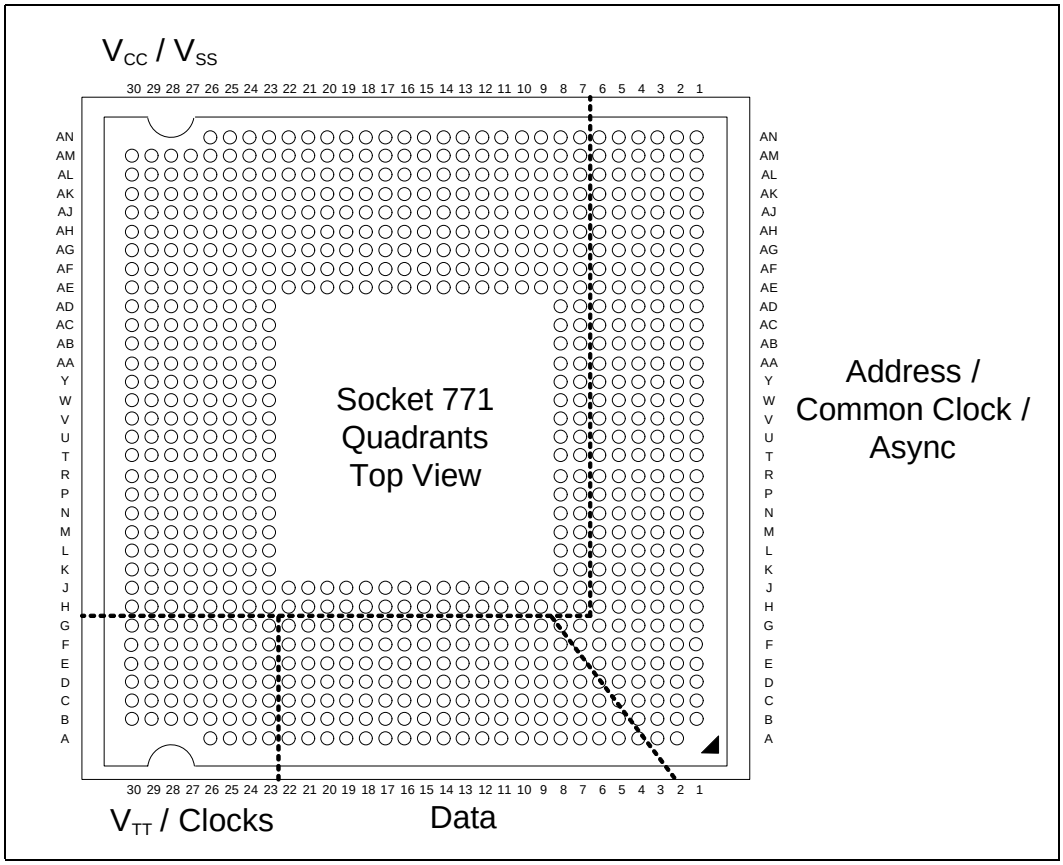
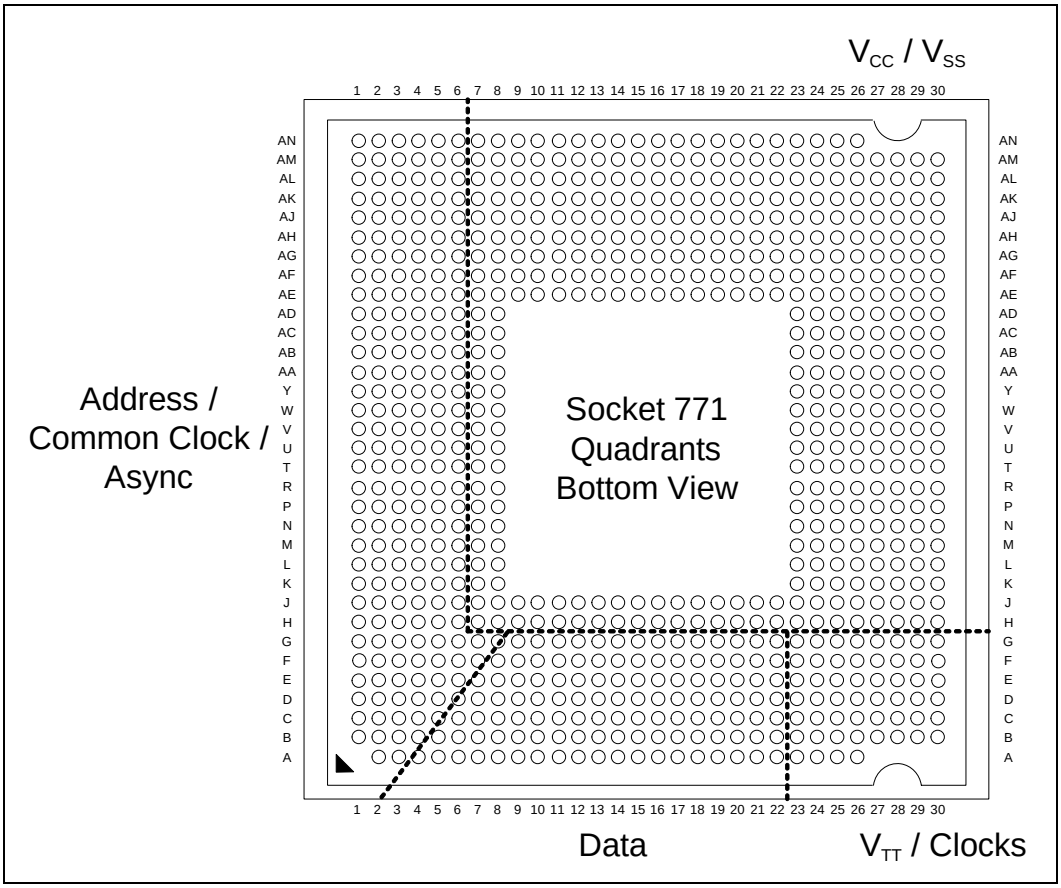


Figure 3-8. Processor Land Coordinates, Bottom View



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4 Land Listing

4.1 Dual-Core Intel Xeon Processor 5000 Series Land Assignments

This section provides sorted land list in Table 4-1 and Table 4-2. Table 4-1 is a listing of all processor lands ordered alphabetically by land name. Table 4-2 is a listing of all processor lands ordered by land number.

4.1.1 Land Listing by Land Name

Table 4-1. Land Listing by Land Name (Sheet 1 of 9)

Land Name	Land No.	Signal Buffer Type	Direction
A03#	M5	Source Sync	Input/Output
A04#	P6	Source Sync	Input/Output
A05#	L5	Source Sync	Input/Output
A06#	L4	Source Sync	Input/Output
A07#	M4	Source Sync	Input/Output
A08#	R4	Source Sync	Input/Output
A09#	T5	Source Sync	Input/Output
A10#	U6	Source Sync	Input/Output
A11#	T4	Source Sync	Input/Output
A12#	U5	Source Sync	Input/Output
A13#	U4	Source Sync	Input/Output
A14#	V5	Source Sync	Input/Output
A15#	V4	Source Sync	Input/Output
A16#	W5	Source Sync	Input/Output
A17#	AB6	Source Sync	Input/Output
A18#	W6	Source Sync	Input/Output
A19#	Y6	Source Sync	Input/Output
A20#	Y4	Source Sync	Input/Output
A21#	AA4	Source Sync	Input/Output
A22#	AD6	Source Sync	Input/Output
A23#	AA5	Source Sync	Input/Output
A24#	AB5	Source Sync	Input/Output
A25#	AC5	Source Sync	Input/Output
A26#	AB4	Source Sync	Input/Output
A27#	AF5	Source Sync	Input/Output
A28#	AF4	Source Sync	Input/Output
A29#	AG6	Source Sync	Input/Output
A30#	AG4	Source Sync	Input/Output
A31#	AG5	Source Sync	Input/Output
A32#	AH4	Source Sync	Input/Output
COMP5	T2	Power/Other	Input
COMP6	Y3	Power/Other	Input
COMP7	AE3	Power/Other	Input
D00#	B4	Source Sync	Input/Output
D01#	C5	Source Sync	Input/Output

Land Name	Land No.	Signal Buffer Type	Direction
A33#	AH5	Source Sync	Input/Output
A34#	AJ5	Source Sync	Input/Output
A35#	AJ6	Source Sync	Input/Output
A20M#	K3	ASync GTL+	Input
ADS#	D2	Common Clk	Input/Output
ADSTB0#	R6	Source Sync	Input/Output
ADSTB1#	AD5	Source Sync	Input/Output
AP0#	U2	Common Clk	Input/Output
AP1#	U3	Common Clk	Input/Output
BCLK0	F28	Clk	Input
BCLK1	G28	Clk	Input
BINIT#	AD3	Common Clk	Input/Output
BNR#	C2	Common Clk	Input/Output
BPM0#	AJ2	Common Clk	Input/Output
BPM1#	AJ1	Common Clk	Input/Output
BPM2#	AD2	Common Clk	Input/Output
BPM3#	AG2	Common Clk	Input/Output
BPM4#	AF2	Common Clk	Input/Output
BPM5#	AG3	Common Clk	Input/Output
BPRI#	G8	Common Clk	Input
BR0#	F3	Common Clk	Input/Output
BR1#	H5	Common Clk	Input
BSEL0	G29	Power/Other	Output
BSEL1	H30	Power/Other	Output
BSEL2	G30	Power/Other	Output
COMP0	A13	Power/Other	Input
COMP1	T1	Power/Other	Input
COMP2	G2	Power/Other	Input
COMP3	R1	Power/Other	Input
COMP4	J2	Power/Other	Input
D40#	E19	Source Sync	Input/Output
D41#	F20	Source Sync	Input/Output
D42#	E21	Source Sync	Input/Output
D43#	F21	Source Sync	Input/Output
D44#	G21	Source Sync	Input/Output

Table 4-1. Land Listing by Land Name (Sheet 2 of 9)

Land Name	Land No.	Signal Buffer Type	Direction
D02#	A4	Source Sync	Input/Output
D03#	C6	Source Sync	Input/Output
D04#	A5	Source Sync	Input/Output
D05#	B6	Source Sync	Input/Output
D06#	B7	Source Sync	Input/Output
D07#	A7	Source Sync	Input/Output
D08#	A10	Source Sync	Input/Output
D09#	A11	Source Sync	Input/Output
D10#	B10	Source Sync	Input/Output
D11#	C11	Source Sync	Input/Output
D12#	D8	Source Sync	Input/Output
D13#	B12	Source Sync	Input/Output
D14#	C12	Source Sync	Input/Output
D15#	D11	Source Sync	Input/Output
D16#	G9	Source Sync	Input/Output
D17#	F8	Source Sync	Input/Output
D18#	F9	Source Sync	Input/Output
D19#	E9	Source Sync	Input/Output
D20#	D7	Source Sync	Input/Output
D21#	E10	Source Sync	Input/Output
D22#	D10	Source Sync	Input/Output
D23#	F11	Source Sync	Input/Output
D24#	F12	Source Sync	Input/Output
D25#	D13	Source Sync	Input/Output
D26#	E13	Source Sync	Input/Output
D27#	G13	Source Sync	Input/Output
D28#	F14	Source Sync	Input/Output
D29#	G14	Source Sync	Input/Output
D30#	F15	Source Sync	Input/Output
D31#	G15	Source Sync	Input/Output
D32#	G16	Source Sync	Input/Output
D33#	E15	Source Sync	Input/Output
D34#	E16	Source Sync	Input/Output
D35#	G18	Source Sync	Input/Output
D36#	G17	Source Sync	Input/Output
D37#	F17	Source Sync	Input/Output
D38#	F18	Source Sync	Input/Output
D39#	E18	Source Sync	Input/Output
DSTBP3#	C17	Source Sync	Input/Output
FERR#/PBE#	R3	ASync GTL+	Output
FORCEPR#	AK6	ASync GTL+	Input
GTLREF_ADD_C0	H1	Power/Other	Input
GTLREF_ADD_C1	H2	Power/Other	Input
GTLREF_DATA_C0	G10	Power/Other	Input
GTLREF_DATA_C1	F2	Power/Other	Input
HIT#	D4	Common Clk	Input/Output
HITM#	E4	Common Clk	Input/Output
IERR#	AB2	ASync GTL+	Output

Land Name	Land No.	Signal Buffer Type	Direction
D45#	E22	Source Sync	Input/Output
D46#	D22	Source Sync	Input/Output
D47#	G22	Source Sync	Input/Output
D48#	D20	Source Sync	Input/Output
D49#	D17	Source Sync	Input/Output
D50#	A14	Source Sync	Input/Output
D51#	C15	Source Sync	Input/Output
D52#	C14	Source Sync	Input/Output
D53#	B15	Source Sync	Input/Output
D54#	C18	Source Sync	Input/Output
D55#	B16	Source Sync	Input/Output
D56#	A17	Source Sync	Input/Output
D57#	B18	Source Sync	Input/Output
D58#	C21	Source Sync	Input/Output
D59#	B21	Source Sync	Input/Output
D60#	B19	Source Sync	Input/Output
D61#	A19	Source Sync	Input/Output
D62#	A22	Source Sync	Input/Output
D63#	B22	Source Sync	Input/Output
DBI0#	A8	Source Sync	Input/Output
DBI1#	G11	Source Sync	Input/Output
DBI2#	D19	Source Sync	Input/Output
DBI3#	C20	Source Sync	Input/Output
DBR#	AC2	Power/Other	Output
DBSY#	B2	Common Clk	Input/Output
DEFER#	G7	Common Clk	Input
DP0#	J16	Common Clk	Input/Output
DP1#	H15	Common Clk	Input/Output
DP2#	H16	Common Clk	Input/Output
DP3#	J17	Common Clk	Input/Output
DRDY#	C1	Common Clk	Input/Output
DSTBN0#	C8	Source Sync	Input/Output
DSTBN1#	G12	Source Sync	Input/Output
DSTBN2#	G20	Source Sync	Input/Output
DSTBN3#	A16	Source Sync	Input/Output
DSTBP0#	B9	Source Sync	Input/Output
DSTBP1#	E12	Source Sync	Input/Output
DSTBP2#	G19	Source Sync	Input/Output
RESERVED	E23		
RESERVED	E24		
RESERVED	E5		
RESERVED	E6		
RESERVED	E7		
RESERVED	F23		
RESERVED	F29		
RESERVED	F6		
RESERVED	G5		
RESERVED	G6		

Table 4-1. Land Listing by Land Name (Sheet 3 of 9)

Land Name	Land No.	Signal Buffer Type	Direction
IGNNE#	N2	ASync GTL+	Input
INIT#	P3	ASync GTL+	Input
LINT0	K1	ASync GTL+	Input
LINT1	L1	ASync GTL+	Input
LL_ID0	V2	Power/Other	Output
LL_ID1	AA2	Power/Other	Output
LOCK#	C3	Common Clk	Input/Output
MCERR#	AB3	Common Clk	Input/Output
MS_ID0	W1	Power/Other	Output
MS_ID1	V1	Power/Other	Output
PROCHOT#	AL2	ASync GTL+	Output
PWRGOOD	N1	Power/Other	Input
REQ0#	K4	Source Sync	Input/Output
REQ1#	J5	Source Sync	Input/Output
REQ2#	M6	Source Sync	Input/Output
REQ3#	K6	Source Sync	Input/Output
REQ4#	J6	Source Sync	Input/Output
RESERVED	A20		
RESERVED	AC4		
RESERVED	AE4		
RESERVED	AE6		
RESERVED	AK3		
RESERVED	AJ3		
RESERVED	AM5		
RESERVED	AN5		
RESERVED	AN6		
RESERVED	B13		
RESERVED	C9		
RESERVED	D1		
RESERVED	D14		
RESERVED	D16		
RESERVED	D23		
RESERVED	E1		
THERMDC2	AH7	Power/Other	Output
THERMTRIP#	M2	ASync GTL+	Output
TMS	AC1	TAP	Input
TRDY#	E3	Common Clk	Input
TRST#	AG1	TAP	Input
VCC	AA8	Power/Other	
VCC	AB8	Power/Other	
VCC	AC23	Power/Other	
VCC	AC24	Power/Other	
VCC	AC25	Power/Other	
VCC	AC26	Power/Other	
VCC	AC27	Power/Other	
VCC	AC28	Power/Other	
VCC	AC29	Power/Other	
VCC	AC30	Power/Other	

Land Name	Land No.	Signal Buffer Type	Direction
RESERVED	J3		
RESERVED	N4		
RESERVED	N5		
RESERVED	P5		
RESERVED	W2		
RESERVED	Y1		
RESET#	G23	Common Clk	Input
RS0#	B3	Common Clk	Input
RS1#	F5	Common Clk	Input
RS2#	A3	Common Clk	Input
RSP#	H4	Common Clk	Input
SKTOCC#	AE8	Power/Other	Output
SMI#	P2	ASync GTL+	Input
STPCLK#	M3	ASync GTL+	Input
TCK	AE1	TAP	Input
TDI	AD1	TAP	Input
TDO	AF1	TAP	Output
TEST_BUS	AH2	Power/Other	
TESTHI00	F26	Power/Other	Input
TESTHI01	W3	Power/Other	Input
TESTHI02	F25	Power/Other	Input
TESTHI03	G25	Power/Other	Input
TESTHI04	G27	Power/Other	Input
TESTHI05	G26	Power/Other	Input
TESTHI06	G24	Power/Other	Input
TESTHI07	F24	Power/Other	Input
TESTHI08	G3	Power/Other	Input
TESTHI09	G4	Power/Other	Input
TESTHI10	P1	Power/Other	Input
TESTHI11	L2	Power/Other	Input
THERMDA	AL1	Power/Other	Output
THERMDA2	AJ7	Power/Other	Output
THERMDC	AK1	Power/Other	Output
VCC	AF8	Power/Other	
VCC	AF9	Power/Other	
VCC	AG11	Power/Other	
VCC	AG12	Power/Other	
VCC	AG14	Power/Other	
VCC	AG15	Power/Other	
VCC	AG18	Power/Other	
VCC	AG19	Power/Other	
VCC	AG21	Power/Other	
VCC	AG22	Power/Other	
VCC	AG25	Power/Other	
VCC	AG26	Power/Other	
VCC	AG27	Power/Other	
VCC	AG28	Power/Other	
VCC	AG29	Power/Other	

Table 4-1. Land Listing by Land Name (Sheet 4 of 9)

Land Name	Land No.	Signal Buffer Type	Direction
VCC	AC8	Power/Other	
VCC	AD23	Power/Other	
VCC	AD24	Power/Other	
VCC	AD25	Power/Other	
VCC	AD26	Power/Other	
VCC	AD27	Power/Other	
VCC	AD28	Power/Other	
VCC	AD29	Power/Other	
VCC	AD30	Power/Other	
VCC	AD8	Power/Other	
VCC	AE11	Power/Other	
VCC	AE12	Power/Other	
VCC	AE14	Power/Other	
VCC	AE15	Power/Other	
VCC	AE18	Power/Other	
VCC	AE19	Power/Other	
VCC	AE21	Power/Other	
VCC	AE22	Power/Other	
VCC	AE23	Power/Other	
VCC	AE9	Power/Other	
VCC	AF11	Power/Other	
VCC	AF12	Power/Other	
VCC	AF14	Power/Other	
VCC	AF15	Power/Other	
VCC	AF18	Power/Other	
VCC	AF19	Power/Other	
VCC	AF21	Power/Other	
VCC	AF22	Power/Other	
VCC	AJ26	Power/Other	
VCC	AJ8	Power/Other	
VCC	AJ9	Power/Other	
VCC	AK11	Power/Other	
VCC	AK12	Power/Other	
VCC	AK14	Power/Other	
VCC	AK15	Power/Other	
VCC	AK18	Power/Other	
VCC	AK19	Power/Other	
VCC	AK21	Power/Other	
VCC	AK22	Power/Other	
VCC	AK25	Power/Other	
VCC	AK26	Power/Other	
VCC	AK8	Power/Other	
VCC	AK9	Power/Other	
VCC	AL11	Power/Other	
VCC	AL12	Power/Other	
VCC	AL14	Power/Other	
VCC	AL15	Power/Other	
VCC	AL18	Power/Other	

Land Name	Land No.	Signal Buffer Type	Direction
VCC	AG30	Power/Other	
VCC	AG8	Power/Other	
VCC	AG9	Power/Other	
VCC	AH11	Power/Other	
VCC	AH12	Power/Other	
VCC	AH14	Power/Other	
VCC	AH15	Power/Other	
VCC	AH18	Power/Other	
VCC	AH19	Power/Other	
VCC	AH21	Power/Other	
VCC	AH22	Power/Other	
VCC	AH25	Power/Other	
VCC	AH26	Power/Other	
VCC	AH27	Power/Other	
VCC	AH28	Power/Other	
VCC	AH29	Power/Other	
VCC	AH30	Power/Other	
VCC	AH8	Power/Other	
VCC	AH9	Power/Other	
VCC	AJ11	Power/Other	
VCC	AJ12	Power/Other	
VCC	AJ14	Power/Other	
VCC	AJ15	Power/Other	
VCC	AJ18	Power/Other	
VCC	AJ19	Power/Other	
VCC	AJ21	Power/Other	
VCC	AJ22	Power/Other	
VCC	AJ25	Power/Other	
VCC	AN12	Power/Other	
VCC	AN14	Power/Other	
VCC	AN15	Power/Other	
VCC	AN18	Power/Other	
VCC	AN19	Power/Other	
VCC	AN21	Power/Other	
VCC	AN22	Power/Other	
VCC	AN25	Power/Other	
VCC	AN26	Power/Other	
VCC	AN8	Power/Other	
VCC	AN9	Power/Other	
VCC	J10	Power/Other	
VCC	J11	Power/Other	
VCC	J12	Power/Other	
VCC	J13	Power/Other	
VCC	J14	Power/Other	
VCC	J15	Power/Other	
VCC	J18	Power/Other	
VCC	J19	Power/Other	
VCC	J20	Power/Other	

Table 4-1. Land Listing by Land Name (Sheet 5 of 9)

Land Name	Land No.	Signal Buffer Type	Direction
VCC	AL19	Power/Other	
VCC	AL21	Power/Other	
VCC	AL22	Power/Other	
VCC	AL25	Power/Other	
VCC	AL26	Power/Other	
VCC	AL29	Power/Other	
VCC	AL30	Power/Other	
VCC	AL9	Power/Other	
VCC	AM11	Power/Other	
VCC	AM12	Power/Other	
VCC	AM14	Power/Other	
VCC	AM15	Power/Other	
VCC	AM18	Power/Other	
VCC	AM19	Power/Other	
VCC	AM21	Power/Other	
VCC	AM22	Power/Other	
VCC	AM25	Power/Other	
VCC	AM26	Power/Other	
VCC	AM29	Power/Other	
VCC	AM30	Power/Other	
VCC	AM8	Power/Other	
VCC	AM9	Power/Other	
VCC	AN11	Power/Other	
VCC	M24	Power/Other	
VCC	M25	Power/Other	
VCC	M26	Power/Other	
VCC	M27	Power/Other	
VCC	M28	Power/Other	
VCC	M29	Power/Other	
VCC	M30	Power/Other	
VCC	M8	Power/Other	
VCC	N23	Power/Other	
VCC	N24	Power/Other	
VCC	N25	Power/Other	
VCC	N26	Power/Other	
VCC	N27	Power/Other	
VCC	N28	Power/Other	
VCC	N29	Power/Other	
VCC	N30	Power/Other	
VCC	N8	Power/Other	
VCC	P8	Power/Other	
VCC	R8	Power/Other	
VCC	T23	Power/Other	
VCC	T24	Power/Other	
VCC	T25	Power/Other	
VCC	T26	Power/Other	
VCC	T27	Power/Other	
VCC	T28	Power/Other	

Land Name	Land No.	Signal Buffer Type	Direction
VCC	J21	Power/Other	
VCC	J22	Power/Other	
VCC	J23	Power/Other	
VCC	J24	Power/Other	
VCC	J25	Power/Other	
VCC	J26	Power/Other	
VCC	J27	Power/Other	
VCC	J28	Power/Other	
VCC	J29	Power/Other	
VCC	J30	Power/Other	
VCC	J8	Power/Other	
VCC	J9	Power/Other	
VCC	K23	Power/Other	
VCC	K24	Power/Other	
VCC	K25	Power/Other	
VCC	K26	Power/Other	
VCC	K27	Power/Other	
VCC	K28	Power/Other	
VCC	K29	Power/Other	
VCC	K30	Power/Other	
VCC	K8	Power/Other	
VCC	L8	Power/Other	
VCC	M23	Power/Other	
VCC	W28	Power/Other	
VCC	W29	Power/Other	
VCC	W30	Power/Other	
VCC	W8	Power/Other	
VCC	Y23	Power/Other	
VCC	Y24	Power/Other	
VCC	Y25	Power/Other	
VCC	Y26	Power/Other	
VCC	Y27	Power/Other	
VCC	Y28	Power/Other	
VCC	Y29	Power/Other	
VCC	Y30	Power/Other	
VCC	Y8	Power/Other	
VCC_DIE_SENSE	AN3	Power/Other	Output
VCC_DIE_SENSE2	AL8	Power/Other	Output
VCCA	A23	Power/Other	Input
VCCIOPLL	C23	Power/Other	Input
VID0	AM2	Power/Other	Output
VID1	AL5	Power/Other	Output
VID2	AM3	Power/Other	Output
VID3	AL6	Power/Other	Output
VID4	AK4	Power/Other	Output
VID5	AL4	Power/Other	Output
VID_SELECT	AN7	Power/Other	Output
VSS	A12	Power/Other	

Table 4-1. Land Listing by Land Name (Sheet 6 of 9)

Land Name	Land No.	Signal Buffer Type	Direction
VCC	T29	Power/Other	
VCC	T30	Power/Other	
VCC	T8	Power/Other	
VCC	U23	Power/Other	
VCC	U24	Power/Other	
VCC	U25	Power/Other	
VCC	U26	Power/Other	
VCC	U27	Power/Other	
VCC	U28	Power/Other	
VCC	U29	Power/Other	
VCC	U30	Power/Other	
VCC	U8	Power/Other	
VCC	V8	Power/Other	
VCC	W23	Power/Other	
VCC	W24	Power/Other	
VCC	W25	Power/Other	
VCC	W26	Power/Other	
VCC	W27	Power/Other	
VSS	AB1	Power/Other	
VSS	AB23	Power/Other	
VSS	AB24	Power/Other	
VSS	AB25	Power/Other	
VSS	AB26	Power/Other	
VSS	AB27	Power/Other	
VSS	AB28	Power/Other	
VSS	AB29	Power/Other	
VSS	AB30	Power/Other	
VSS	AB7	Power/Other	
VSS	AC3	Power/Other	
VSS	AC6	Power/Other	
VSS	AC7	Power/Other	
VSS	AD4	Power/Other	
VSS	AD7	Power/Other	
VSS	AE10	Power/Other	
VSS	AE13	Power/Other	
VSS	AE16	Power/Other	
VSS	AE17	Power/Other	
VSS	AE2	Power/Other	
VSS	AE20	Power/Other	
VSS	AE24	Power/Other	
VSS	AE25	Power/Other	
VSS	AE26	Power/Other	
VSS	AE27	Power/Other	
VSS	AE28	Power/Other	
VSS	AE29	Power/Other	
VSS	AE30	Power/Other	
VSS	AE5	Power/Other	
VSS	AE7	Power/Other	

Land Name	Land No.	Signal Buffer Type	Direction
VSS	A15	Power/Other	
VSS	A18	Power/Other	
VSS	A2	Power/Other	
VSS	A21	Power/Other	
VSS	A24	Power/Other	
VSS	A6	Power/Other	
VSS	A9	Power/Other	
VSS	AA23	Power/Other	
VSS	AA24	Power/Other	
VSS	AA25	Power/Other	
VSS	AA26	Power/Other	
VSS	AA27	Power/Other	
VSS	AA28	Power/Other	
VSS	AA29	Power/Other	
VSS	AA3	Power/Other	
VSS	AA30	Power/Other	
VSS	AA6	Power/Other	
VSS	AA7	Power/Other	
VSS	AF30	Power/Other	
VSS	AF6	Power/Other	
VSS	AF7	Power/Other	
VSS	AG10	Power/Other	
VSS	AG13	Power/Other	
VSS	AG16	Power/Other	
VSS	AG17	Power/Other	
VSS	AG20	Power/Other	
VSS	AG23	Power/Other	
VSS	AG24	Power/Other	
VSS	AG7	Power/Other	
VSS	AH1	Power/Other	
VSS	AH10	Power/Other	
VSS	AH13	Power/Other	
VSS	AH16	Power/Other	
VSS	AH17	Power/Other	
VSS	AH20	Power/Other	
VSS	AH23	Power/Other	
VSS	AH24	Power/Other	
VSS	AH3	Power/Other	
VSS	AH6	Power/Other	
VSS	AJ10	Power/Other	
VSS	AJ13	Power/Other	
VSS	AJ16	Power/Other	
VSS	AJ17	Power/Other	
VSS	AJ20	Power/Other	
VSS	AJ23	Power/Other	
VSS	AJ24	Power/Other	
VSS	AJ27	Power/Other	
VSS	AJ28	Power/Other	

Table 4-1. Land Listing by Land Name (Sheet 7 of 9)

Land Name	Land No.	Signal Buffer Type	Direction
VSS	AF10	Power/Other	
VSS	AF13	Power/Other	
VSS	AF16	Power/Other	
VSS	AF17	Power/Other	
VSS	AF20	Power/Other	
VSS	AF23	Power/Other	
VSS	AF24	Power/Other	
VSS	AF25	Power/Other	
VSS	AF26	Power/Other	
VSS	AF27	Power/Other	
VSS	AF28	Power/Other	
VSS	AF29	Power/Other	
VSS	AF3	Power/Other	
VSS	AK29	Power/Other	
VSS	AK30	Power/Other	
VSS	AK5	Power/Other	
VSS	AK7	Power/Other	
VSS	AL10	Power/Other	
VSS	AL13	Power/Other	
VSS	AL16	Power/Other	
VSS	AL17	Power/Other	
VSS	AL20	Power/Other	
VSS	AL23	Power/Other	
VSS	AL24	Power/Other	
VSS	AL27	Power/Other	
VSS	AL28	Power/Other	
VSS	AL3	Power/Other	
VSS	AM1	Power/Other	
VSS	AM10	Power/Other	
VSS	AM13	Power/Other	
VSS	AM16	Power/Other	
VSS	AM17	Power/Other	
VSS	AM20	Power/Other	
VSS	AM23	Power/Other	
VSS	AM24	Power/Other	
VSS	AM27	Power/Other	
VSS	AM28	Power/Other	
VSS	AM4	Power/Other	
VSS	AM7	Power/Other	
VSS	AN1	Power/Other	
VSS	AN10	Power/Other	
VSS	AN13	Power/Other	
VSS	AN16	Power/Other	
VSS	AN17	Power/Other	
VSS	AN2	Power/Other	
VSS	AN20	Power/Other	
VSS	AN23	Power/Other	
VSS	AN24	Power/Other	

Land Name	Land No.	Signal Buffer Type	Direction
VSS	AJ29	Power/Other	
VSS	AJ30	Power/Other	
VSS	AJ4	Power/Other	
VSS	AK10	Power/Other	
VSS	AK13	Power/Other	
VSS	AK16	Power/Other	
VSS	AK17	Power/Other	
VSS	AK2	Power/Other	
VSS	AK20	Power/Other	
VSS	AK23	Power/Other	
VSS	AK24	Power/Other	
VSS	AK27	Power/Other	
VSS	AK28	Power/Other	
VSS	C10	Power/Other	
VSS	C13	Power/Other	
VSS	C16	Power/Other	
VSS	C19	Power/Other	
VSS	C22	Power/Other	
VSS	C24	Power/Other	
VSS	C4	Power/Other	
VSS	C7	Power/Other	
VSS	D12	Power/Other	
VSS	D15	Power/Other	
VSS	D18	Power/Other	
VSS	D21	Power/Other	
VSS	D24	Power/Other	
VSS	D3	Power/Other	
VSS	D5	Power/Other	
VSS	D6	Power/Other	
VSS	D9	Power/Other	
VSS	E11	Power/Other	
VSS	E14	Power/Other	
VSS	E17	Power/Other	
VSS	E2	Power/Other	
VSS	E20	Power/Other	
VSS	E25	Power/Other	
VSS	E26	Power/Other	
VSS	E27	Power/Other	
VSS	E28	Power/Other	
VSS	E29	Power/Other	
VSS	E8	Power/Other	
VSS	F1	Power/Other	
VSS	F10	Power/Other	
VSS	F13	Power/Other	
VSS	F16	Power/Other	
VSS	F19	Power/Other	
VSS	F22	Power/Other	
VSS	F4	Power/Other	

Table 4-1. Land Listing by Land Name (Sheet 8 of 9)

Land Name	Land No.	Signal Buffer Type	Direction
VSS	B1	Power/Other	
VSS	B11	Power/Other	
VSS	B14	Power/Other	
VSS	B17	Power/Other	
VSS	B20	Power/Other	
VSS	B24	Power/Other	
VSS	B5	Power/Other	
VSS	B8	Power/Other	
VSS	H18	Power/Other	
VSS	H19	Power/Other	
VSS	H20	Power/Other	
VSS	H21	Power/Other	
VSS	H22	Power/Other	
VSS	H23	Power/Other	
VSS	H24	Power/Other	
VSS	H25	Power/Other	
VSS	H26	Power/Other	
VSS	H27	Power/Other	
VSS	H28	Power/Other	
VSS	H29	Power/Other	
VSS	H3	Power/Other	
VSS	H6	Power/Other	
VSS	H7	Power/Other	
VSS	H8	Power/Other	
VSS	H9	Power/Other	
VSS	J4	Power/Other	
VSS	J7	Power/Other	
VSS	K2	Power/Other	
VSS	K5	Power/Other	
VSS	K7	Power/Other	
VSS	L23	Power/Other	
VSS	L24	Power/Other	
VSS	L25	Power/Other	
VSS	L26	Power/Other	
VSS	L27	Power/Other	
VSS	L28	Power/Other	
VSS	L29	Power/Other	
VSS	L3	Power/Other	
VSS	L30	Power/Other	
VSS	L6	Power/Other	
VSS	L7	Power/Other	
VSS	M1	Power/Other	
VSS	M7	Power/Other	
VSS	N3	Power/Other	
VSS	N6	Power/Other	
VSS	N7	Power/Other	
VSS	P23	Power/Other	
VSS	P24	Power/Other	

Land Name	Land No.	Signal Buffer Type	Direction
VSS	F7	Power/Other	
VSS	G1	Power/Other	
VSS	H10	Power/Other	
VSS	H11	Power/Other	
VSS	H12	Power/Other	
VSS	H13	Power/Other	
VSS	H14	Power/Other	
VSS	H17	Power/Other	
VSS	P28	Power/Other	
VSS	P29	Power/Other	
VSS	P30	Power/Other	
VSS	P4	Power/Other	
VSS	P7	Power/Other	
VSS	R2	Power/Other	
VSS	R23	Power/Other	
VSS	R24	Power/Other	
VSS	R25	Power/Other	
VSS	R26	Power/Other	
VSS	R27	Power/Other	
VSS	R28	Power/Other	
VSS	R29	Power/Other	
VSS	R30	Power/Other	
VSS	R5	Power/Other	
VSS	R7	Power/Other	
VSS	T3	Power/Other	
VSS	T6	Power/Other	
VSS	T7	Power/Other	
VSS	U1	Power/Other	
VSS	U7	Power/Other	
VSS	V23	Power/Other	
VSS	V24	Power/Other	
VSS	V25	Power/Other	
VSS	V26	Power/Other	
VSS	V27	Power/Other	
VSS	V28	Power/Other	
VSS	V29	Power/Other	
VSS	V3	Power/Other	
VSS	V30	Power/Other	
VSS	V6	Power/Other	
VSS	V7	Power/Other	
VSS	W4	Power/Other	
VSS	W7	Power/Other	
VSS	Y2	Power/Other	
VSS	Y5	Power/Other	
VSS	Y7	Power/Other	
VSS_DIE_SENSE	AN4	Power/Other	Output
VSS_DIE_SENSE2	AL7	Power/Other	Output
VSSA	B23	Power/Other	Input

Table 4-1. Land Listing by Land Name (Sheet 9 of 9)

Land Name	Land No.	Signal Buffer Type	Direction
VSS	P25	Power/Other	
VSS	P26	Power/Other	
VSS	P27	Power/Other	
VTT	B26	Power/Other	
VTT	B27	Power/Other	
VTT	B28	Power/Other	
VTT	B29	Power/Other	
VTT	B30	Power/Other	
VTT	C25	Power/Other	
VTT	C26	Power/Other	
VTT	C27	Power/Other	
VTT	C28	Power/Other	
VTT	C29	Power/Other	
VTT	C30	Power/Other	
VTT	D25	Power/Other	

Land Name	Land No.	Signal Buffer Type	Direction
VTT	A25	Power/Other	
VTT	A26	Power/Other	
VTT	B25	Power/Other	
VTT	D26	Power/Other	
VTT	D27	Power/Other	
VTT	D28	Power/Other	
VTT	D29	Power/Other	
VTT	D30	Power/Other	
VTT	E30	Power/Other	
VTT	F30	Power/Other	
VTT_OUT	AA1	Power/Other	Output
VTT_OUT	J1	Power/Other	Output
RESERVED	F27		
VTTPWRGD	AM6	Power/Other	Input

4.1.2 Land Listing by Land Number

Table 4-2. Land Listing by Land Number (Sheet 1 of 9)

Land No.	Land Name	Signal Buffer Type	Direction
A10	D08#	Source Sync	Input/Output
A11	D09#	Source Sync	Input/Output
A12	VSS	Power/Other	
A13	COMP0	Power/Other	Input
A14	D50#	Source Sync	Input/Output
A15	VSS	Power/Other	
A16	DSTBN3#	Source Sync	Input/Output
A17	D56#	Source Sync	Input/Output
A18	VSS	Power/Other	
A19	D61#	Source Sync	Input/Output
A2	VSS	Power/Other	
A20	RESERVED		
A21	VSS	Power/Other	
A22	D62#	Source Sync	Input/Output
A23	VCCA	Power/Other	Input
A24	VSS	Power/Other	
A25	VTT	Power/Other	
A26	VTT	Power/Other	
A3	RS2#	Common Clk	Input
A4	D02#	Source Sync	Input/Output
A5	D04#	Source Sync	Input/Output
A6	VSS	Power/Other	
A7	D07#	Source Sync	Input/Output
A8	DBI0#	Source Sync	Input/Output
A9	VSS	Power/Other	
AA1	VTT_OUT	Power/Other	Output
AA2	LL_ID1	Power/Other	Output
AA23	VSS	Power/Other	
AA24	VSS	Power/Other	
AA25	VSS	Power/Other	
AA26	VSS	Power/Other	
AA27	VSS	Power/Other	
AA28	VSS	Power/Other	
AA29	VSS	Power/Other	
AA3	VSS	Power/Other	
AA30	VSS	Power/Other	
AA4	A21#	Source Sync	Input/Output
AA5	A23#	Source Sync	Input/Output
AA6	VSS	Power/Other	
AA7	VSS	Power/Other	
AA8	VCC	Power/Other	
AD3	BINIT#	Common Clk	Input/Output
AD30	VCC	Power/Other	
AD4	VSS	Power/Other	
AD5	ADSTB1#	Source Sync	Input/Output
AD6	A22#	Source Sync	Input/Output

Land No.	Land Name	Signal Buffer Type	Direction
AB1	VSS	Power/Other	
AB2	IERR#	ASync GTL+	Output
AB23	VSS	Power/Other	
AB24	VSS	Power/Other	
AB25	VSS	Power/Other	
AB26	VSS	Power/Other	
AB27	VSS	Power/Other	
AB28	VSS	Power/Other	
AB29	VSS	Power/Other	
AB3	MCERR#	Common Clk	Input/Output
AB30	VSS	Power/Other	
AB4	A26#	Source Sync	Input/Output
AB5	A24#	Source Sync	Input/Output
AB6	A17#	Source Sync	Input/Output
AB7	VSS	Power/Other	
AB8	VCC	Power/Other	
AC1	TMS	TAP	Input
AC2	DBR#	Power/Other	Output
AC23	VCC	Power/Other	
AC24	VCC	Power/Other	
AC25	VCC	Power/Other	
AC26	VCC	Power/Other	
AC27	VCC	Power/Other	
AC28	VCC	Power/Other	
AC29	VCC	Power/Other	
AC3	VSS	Power/Other	
AC30	VCC	Power/Other	
AC4	RESERVED		
AC5	A25#	Source Sync	Input/Output
AC6	VSS	Power/Other	
AC7	VSS	Power/Other	
AC8	VCC	Power/Other	
AD1	TDI	TAP	Input
AD2	BPM2#	Common Clk	Input/Output
AD23	VCC	Power/Other	
AD24	VCC	Power/Other	
AD25	VCC	Power/Other	
AD26	VCC	Power/Other	
AD27	VCC	Power/Other	
AD28	VCC	Power/Other	
AD29	VCC	Power/Other	
AF15	VCC	Power/Other	
AF16	VSS	Power/Other	
AF17	VSS	Power/Other	
AF18	VCC	Power/Other	
AF19	VCC	Power/Other	

Table 4-2. Land Listing by Land Number (Sheet 2 of 9)

Land No.	Land Name	Signal Buffer Type	Direction
AD7	VSS	Power/Other	
AD8	VCC	Power/Other	
AE1	TCK	TAP	Input
AE10	VSS	Power/Other	
AE11	VCC	Power/Other	
AE12	VCC	Power/Other	
AE13	VSS	Power/Other	
AE14	VCC	Power/Other	
AE15	VCC	Power/Other	
AE16	VSS	Power/Other	
AE17	VSS	Power/Other	
AE18	VCC	Power/Other	
AE19	VCC	Power/Other	
AE2	VSS	Power/Other	
AE20	VSS	Power/Other	
AE21	VCC	Power/Other	
AE22	VCC	Power/Other	
AE23	VCC	Power/Other	
AE24	VSS	Power/Other	
AE25	VSS	Power/Other	
AE26	VSS	Power/Other	
AE27	VSS	Power/Other	
AE28	VSS	Power/Other	
AE29	VSS	Power/Other	
AE3	COMP7	Power/Other	Input
AE30	VSS	Power/Other	
AE4	RESERVED		
AE5	VSS	Power/Other	
AE6	RESERVED		
AE7	VSS	Power/Other	
AE8	SKTOCC#	Power/Other	Output
AE9	VCC	Power/Other	
AF1	TDO	TAP	Output
AF10	VSS	Power/Other	
AF11	VCC	Power/Other	
AF12	VCC	Power/Other	
AF13	VSS	Power/Other	
AF14	VCC	Power/Other	
AG27	VCC	Power/Other	
AG28	VCC	Power/Other	
AG29	VCC	Power/Other	
AG3	BPM5#	Common Clk	Input/Output
AG30	VCC	Power/Other	
AG4	A30#	Source Sync	Input/Output
AG5	A31#	Source Sync	Input/Output
AG6	A29#	Source Sync	Input/Output
AG7	VSS	Power/Other	
AG8	VCC	Power/Other	

Land No.	Land Name	Signal Buffer Type	Direction
AF2	BPM4#	Common Clk	Input/Output
AF20	VSS	Power/Other	
AF21	VCC	Power/Other	
AF22	VCC	Power/Other	
AF23	VSS	Power/Other	
AF24	VSS	Power/Other	
AF25	VSS	Power/Other	
AF26	VSS	Power/Other	
AF27	VSS	Power/Other	
AF28	VSS	Power/Other	
AF29	VSS	Power/Other	
AF3	VSS	Power/Other	
AF30	VSS	Power/Other	
AF4	A28#	Source Sync	Input/Output
AF5	A27#	Source Sync	Input/Output
AF6	VSS	Power/Other	
AF7	VSS	Power/Other	
AF8	VCC	Power/Other	
AF9	VCC	Power/Other	
AG1	TRST#	TAP	Input
AG10	VSS	Power/Other	
AG11	VCC	Power/Other	
AG12	VCC	Power/Other	
AG13	VSS	Power/Other	
AG14	VCC	Power/Other	
AG15	VCC	Power/Other	
AG16	VSS	Power/Other	
AG17	VSS	Power/Other	
AG18	VCC	Power/Other	
AG19	VCC	Power/Other	
AG2	BPM3#	Common Clk	Input/Output
AG20	VSS	Power/Other	
AG21	VCC	Power/Other	
AG22	VCC	Power/Other	
AG23	VSS	Power/Other	
AG24	VSS	Power/Other	
AG25	VCC	Power/Other	
AG26	VCC	Power/Other	
AJ11	VCC	Power/Other	
AJ12	VCC	Power/Other	
AJ13	VSS	Power/Other	
AJ14	VCC	Power/Other	
AJ15	VCC	Power/Other	
AJ16	VSS	Power/Other	
AJ17	VSS	Power/Other	
AJ18	VCC	Power/Other	
AJ19	VCC	Power/Other	
AJ2	BPM0#	Common Clk	Input/Output

Table 4-2. Land Listing by Land Number (Sheet 3 of 9)

Land No.	Land Name	Signal Buffer Type	Direction
AG9	VCC	Power/Other	
AH1	VSS	Power/Other	
AH10	VSS	Power/Other	
AH11	VCC	Power/Other	
AH12	VCC	Power/Other	
AH13	VSS	Power/Other	
AH14	VCC	Power/Other	
AH15	VCC	Power/Other	
AH16	VSS	Power/Other	
AH17	VSS	Power/Other	
AH18	VCC	Power/Other	
AH19	VCC	Power/Other	
AH2	TEST_BUS	Power/Other	
AH20	VSS	Power/Other	
AH21	VCC	Power/Other	
AH22	VCC	Power/Other	
AH23	VSS	Power/Other	
AH24	VSS	Power/Other	
AH25	VCC	Power/Other	
AH26	VCC	Power/Other	
AH27	VCC	Power/Other	
AH28	VCC	Power/Other	
AH29	VCC	Power/Other	
AH3	VSS	Power/Other	
AH30	VCC	Power/Other	
AH4	A32#	Source Sync	Input/Output
AH5	A33#	Source Sync	Input/Output
AH6	VSS	Power/Other	
AH7	THERMDC2	Power/Other	Output
AH8	VCC	Power/Other	
AH9	VCC	Power/Other	
AJ1	BPM1#	Common Clk	Input/Output
AJ10	VSS	Power/Other	
AK23	VSS	Power/Other	
AK24	VSS	Power/Other	
AK25	VCC	Power/Other	
AK26	VCC	Power/Other	
AK27	VSS	Power/Other	
AK28	VSS	Power/Other	
AK29	VSS	Power/Other	
AK3	RESERVED		
AK30	VSS	Power/Other	
AK4	VID4	Power/Other	Output
AK5	VSS	Power/Other	
AK6	FORCEPR#	ASync GTL+	Input
AK7	VSS	Power/Other	
AK8	VCC	Power/Other	
AK9	VCC	Power/Other	

Land No.	Land Name	Signal Buffer Type	Direction
AJ20	VSS	Power/Other	
AJ21	VCC	Power/Other	
AJ22	VCC	Power/Other	
AJ23	VSS	Power/Other	
AJ24	VSS	Power/Other	
AJ25	VCC	Power/Other	
AJ26	VCC	Power/Other	
AJ27	VSS	Power/Other	
AJ28	VSS	Power/Other	
AJ29	VSS	Power/Other	
AJ3	RESERVED		
AJ30	VSS	Power/Other	
AJ4	VSS	Power/Other	
AJ5	A34#	Source Sync	Input/Output
AJ6	A35#	Source Sync	Input/Output
AJ7	THERMDA2	Power/Other	Output
AJ8	VCC	Power/Other	
AJ9	VCC	Power/Other	
AK1	THERMDC	Power/Other	Output
AK10	VSS	Power/Other	
AK11	VCC	Power/Other	
AK12	VCC	Power/Other	
AK13	VSS	Power/Other	
AK14	VCC	Power/Other	
AK15	VCC	Power/Other	
AK16	VSS	Power/Other	
AK17	VSS	Power/Other	
AK18	VCC	Power/Other	
AK19	VCC	Power/Other	
AK2	VSS	Power/Other	
AK20	VSS	Power/Other	
AK21	VCC	Power/Other	
AK22	VCC	Power/Other	
AL8	VCC_DIE_SENSE2	Power/Other	Output
AL9	VCC	Power/Other	
AM1	VSS	Power/Other	
AM10	VSS	Power/Other	
AM11	VCC	Power/Other	
AM12	VCC	Power/Other	
AM13	VSS	Power/Other	
AM14	VCC	Power/Other	
AM15	VCC	Power/Other	
AM16	VSS	Power/Other	
AM17	VSS	Power/Other	
AM18	VCC	Power/Other	
AM19	VCC	Power/Other	
AM2	VID0	Power/Other	Output
AM20	VSS	Power/Other	

Table 4-2. Land Listing by Land Number (Sheet 4 of 9)

Land No.	Land Name	Signal Buffer Type	Direction
AL1	THERMDA	Power/Other	Output
AL10	VSS	Power/Other	
AL11	VCC	Power/Other	
AL12	VCC	Power/Other	
AL13	VSS	Power/Other	
AL14	VCC	Power/Other	
AL15	VCC	Power/Other	
AL16	VSS	Power/Other	
AL17	VSS	Power/Other	
AL18	VCC	Power/Other	
AL19	VCC	Power/Other	
AL2	PROCHOT#	ASync GTL+	Output
AL20	VSS	Power/Other	
AL21	VCC	Power/Other	
AL22	VCC	Power/Other	
AL23	VSS	Power/Other	
AL24	VSS	Power/Other	
AL25	VCC	Power/Other	
AL26	VCC	Power/Other	
AL27	VSS	Power/Other	
AL28	VSS	Power/Other	
AL29	VCC	Power/Other	
AL3	VSS	Power/Other	
AL30	VCC	Power/Other	
AL4	VID5	Power/Other	Output
AL5	VID1	Power/Other	Output
AL6	VID3	Power/Other	Output
AL7	VSS_DIE_SENSE2	Power/Other	Output
AN2	VSS	Power/Other	
AN20	VSS	Power/Other	
AN21	VCC	Power/Other	
AN22	VCC	Power/Other	
AN23	VSS	Power/Other	
AN24	VSS	Power/Other	
AN25	VCC	Power/Other	
AN26	VCC	Power/Other	
AN3	VCC_DIE_SENSE	Power/Other	Output
AN4	VSS_DIE_SENSE	Power/Other	Output
AN5	RESERVED		
AN6	RESERVED		
AN7	VID_SELECT	Power/Other	Output
AN8	VCC	Power/Other	
AN9	VCC	Power/Other	
B1	VSS	Power/Other	
B10	D10#	Source Sync	Input/Output
B11	VSS	Power/Other	
B12	D13#	Source Sync	Input/Output
B13	RESERVED		

Land No.	Land Name	Signal Buffer Type	Direction
AM21	VCC	Power/Other	
AM22	VCC	Power/Other	
AM23	VSS	Power/Other	
AM24	VSS	Power/Other	
AM25	VCC	Power/Other	
AM26	VCC	Power/Other	
AM27	VSS	Power/Other	
AM28	VSS	Power/Other	
AM29	VCC	Power/Other	
AM3	VID2	Power/Other	Output
AM30	VCC	Power/Other	
AM4	VSS	Power/Other	
AM5	RESERVED		
AM6	VTTPWRGD	Power/Other	Input
AM7	VSS	Power/Other	
AM8	VCC	Power/Other	
AM9	VCC	Power/Other	
AN1	VSS	Power/Other	
AN10	VSS	Power/Other	
AN11	VCC	Power/Other	
AN12	VCC	Power/Other	
AN13	VSS	Power/Other	
AN14	VCC	Power/Other	
AN15	VCC	Power/Other	
AN16	VSS	Power/Other	
AN17	VSS	Power/Other	
AN18	VCC	Power/Other	
AN19	VCC	Power/Other	
B8	VSS	Power/Other	
B9	DSTBP0#	Source Sync	Input/Output
C1	DRDY#	Common Clk	Input/Output
C10	VSS	Power/Other	
C11	D11#	Source Sync	Input/Output
C12	D14#	Source Sync	Input/Output
C13	VSS	Power/Other	
C14	D52#	Source Sync	Input/Output
C15	D51#	Source Sync	Input/Output
C16	VSS	Power/Other	
C17	DSTBP3#	Source Sync	Input/Output
C18	D54#	Source Sync	Input/Output
C19	VSS	Power/Other	
C2	BNR#	Common Clk	Input/Output
C20	DBI3#	Source Sync	Input/Output
C21	D58#	Source Sync	Input/Output
C22	VSS	Power/Other	
C23	VCCIOPLL	Power/Other	Input
C24	VSS	Power/Other	
C25	VTT	Power/Other	

Table 4-2. Land Listing by Land Number (Sheet 5 of 9)

Land No.	Land Name	Signal Buffer Type	Direction
B14	VSS	Power/Other	
B15	D53#	Source Sync	Input/Output
B16	D55#	Source Sync	Input/Output
B17	VSS	Power/Other	
B18	D57#	Source Sync	Input/Output
B19	D60#	Source Sync	Input/Output
B2	DBSY#	Common Clk	Input/Output
B20	VSS	Power/Other	
B21	D59#	Source Sync	Input/Output
B22	D63#	Source Sync	Input/Output
B23	VSSA	Power/Other	Input
B24	VSS	Power/Other	
B25	VTT	Power/Other	
B26	VTT	Power/Other	
B27	VTT	Power/Other	
B28	VTT	Power/Other	
B29	VTT	Power/Other	
B3	RS0#	Common Clk	Input
B30	VTT	Power/Other	
B4	D00#	Source Sync	Input/Output
B5	VSS	Power/Other	
B6	D05#	Source Sync	Input/Output
B7	D06#	Source Sync	Input/Output
D2	ADS#	Common Clk	Input/Output
D20	D48#	Source Sync	Input/Output
D21	VSS	Power/Other	
D22	D46#	Source Sync	Input/Output
D23	RESERVED		
D24	VSS	Power/Other	
D25	VTT	Power/Other	
D26	VTT	Power/Other	
D27	VTT	Power/Other	
D28	VTT	Power/Other	
D29	VTT	Power/Other	
D3	VSS	Power/Other	
D30	VTT	Power/Other	
D4	HIT#	Common Clk	Input/Output
D5	VSS	Power/Other	
D6	VSS	Power/Other	
D7	D20#	Source Sync	Input/Output
D8	D12#	Source Sync	Input/Output
D9	VSS	Power/Other	
E1	RESERVED		
E10	D21#	Source Sync	Input/Output
E11	VSS	Power/Other	
E12	DSTBP1#	Source Sync	Input/Output
E13	D26#	Source Sync	Input/Output
E14	VSS	Power/Other	

Land No.	Land Name	Signal Buffer Type	Direction
C26	VTT	Power/Other	
C27	VTT	Power/Other	
C28	VTT	Power/Other	
C29	VTT	Power/Other	
C3	LOCK#	Common Clk	Input/Output
C30	VTT	Power/Other	
C4	VSS	Power/Other	
C5	D01#	Source Sync	Input/Output
C6	D03#	Source Sync	Input/Output
C7	VSS	Power/Other	
C8	DSTBN0#	Source Sync	Input/Output
C9	RESERVED		
D1	RESERVED		
D10	D22#	Source Sync	Input/Output
D11	D15#	Source Sync	Input/Output
D12	VSS	Power/Other	
D13	D25#	Source Sync	Input/Output
D14	RESERVED		
D15	VSS	Power/Other	
D16	RESERVED		
D17	D49#	Source Sync	Input/Output
D18	VSS	Power/Other	
D19	DBI2#	Source Sync	Input/Output
E4	HITM#	Common Clk	Input/Output
E5	RESERVED		
E6	RESERVED		
E7	RESERVED		
E8	VSS	Power/Other	
E9	D19#	Source Sync	Input/Output
F1	VSS	Power/Other	
F10	VSS	Power/Other	
F11	D23#	Source Sync	Input/Output
F12	D24#	Source Sync	Input/Output
F13	VSS	Power/Other	
F14	D28#	Source Sync	Input/Output
F15	D30#	Source Sync	Input/Output
F16	VSS	Power/Other	
F17	D37#	Source Sync	Input/Output
F18	D38#	Source Sync	Input/Output
F19	VSS	Power/Other	
F2	GTLREF_DATA_C1	Power/Other	Input
F20	D41#	Source Sync	Input/Output
F21	D43#	Source Sync	Input/Output
F22	VSS	Power/Other	
F23	RESERVED		
F24	TESTHI07	Power/Other	Input
F25	TESTHI02	Power/Other	Input
F26	TESTHI00	Power/Other	Input

Table 4-2. Land Listing by Land Number (Sheet 6 of 9)

Land No.	Land Name	Signal Buffer Type	Direction
E15	D33#	Source Sync	Input/Output
E16	D34#	Source Sync	Input/Output
E17	VSS	Power/Other	
E18	D39#	Source Sync	Input/Output
E19	D40#	Source Sync	Input/Output
E2	VSS	Power/Other	
E20	VSS	Power/Other	
E21	D42#	Source Sync	Input/Output
E22	D45#	Source Sync	Input/Output
E23	RESERVED		
E24	RESERVED		
E25	VSS	Power/Other	
E26	VSS	Power/Other	
E27	VSS	Power/Other	
E28	VSS	Power/Other	
E29	VSS	Power/Other	
E3	TRDY#	Common Clk	Input
E30	VTT	Power/Other	
G16	D32#	Source Sync	Input/Output
G17	D36#	Source Sync	Input/Output
G18	D35#	Source Sync	Input/Output
G19	DSTBP2#	Source Sync	Input/Output
G2	COMP2	Power/Other	Input
G20	DSTBN2#	Source Sync	Input/Output
G21	D44#	Source Sync	Input/Output
G22	D47#	Source Sync	Input/Output
G23	RESET#	Common Clk	Input
G24	TESTHI06	Power/Other	Input
G25	TESTHI03	Power/Other	Input
G26	TESTHI05	Power/Other	Input
G27	TESTHI04	Power/Other	Input
G28	BCLK1	Clk	Input
G29	BSEL0	Power/Other	Output
G3	TESTHI08	Power/Other	Input
G30	BSEL2	Power/Other	Output
G4	TESTHI09	Power/Other	Input
G5	RESERVED		
G6	RESERVED		
G7	DEFER#	Common Clk	Input
G8	BPRI#	Common Clk	Input
G9	D16#	Source Sync	Input/Output
H1	GTLREF_ADD_C0	Power/Other	Input
H10	VSS	Power/Other	
H11	VSS	Power/Other	
H12	VSS	Power/Other	
H13	VSS	Power/Other	
H14	VSS	Power/Other	
H15	DP1#	Common Clk	Input/Output

Land No.	Land Name	Signal Buffer Type	Direction
F27	RESERVED		
F28	BCLK0	Clk	Input
F29	RESERVED		
F3	BR0#	Common Clk	Input/Output
F30	VTT	Power/Other	
F4	VSS	Power/Other	
F5	RS1#	Common Clk	Input
F6	RESERVED		
F7	VSS	Power/Other	
F8	D17#	Source Sync	Input/Output
F9	D18#	Source Sync	Input/Output
G1	VSS	Power/Other	
G10	GTLREF_DATA_C0	Power/Other	Input
G11	DBI1#	Source Sync	Input/Output
G12	DSTBN1#	Source Sync	Input/Output
G13	D27#	Source Sync	Input/Output
G14	D29#	Source Sync	Input/Output
G15	D31#	Source Sync	Input/Output
H28	VSS	Power/Other	
H29	VSS	Power/Other	
H3	VSS	Power/Other	
H30	BSEL1	Power/Other	Output
H4	RSP#	Common Clk	Input
H5	BR1#	Common Clk	Input
H6	VSS	Power/Other	
H7	VSS	Power/Other	
H8	VSS	Power/Other	
H9	VSS	Power/Other	
J1	VTT_OUT	Power/Other	Output
J10	VCC	Power/Other	
J11	VCC	Power/Other	
J12	VCC	Power/Other	
J13	VCC	Power/Other	
J14	VCC	Power/Other	
J15	VCC	Power/Other	
J16	DP0#	Common Clk	Input/Output
J17	DP3#	Common Clk	Input/Output
J18	VCC	Power/Other	
J19	VCC	Power/Other	
J2	COMP4	Power/Other	Input
J20	VCC	Power/Other	
J21	VCC	Power/Other	
J22	VCC	Power/Other	
J23	VCC	Power/Other	
J24	VCC	Power/Other	
J25	VCC	Power/Other	
J26	VCC	Power/Other	
J27	VCC	Power/Other	

Table 4-2. Land Listing by Land Number (Sheet 7 of 9)

Land No.	Land Name	Signal Buffer Type	Direction
H16	DP2#	Common Clk	Input/Output
H17	VSS	Power/Other	
H18	VSS	Power/Other	
H19	VSS	Power/Other	
H2	GTLREF_ADD_C1	Power/Other	Input
H20	VSS	Power/Other	
H21	VSS	Power/Other	
H22	VSS	Power/Other	
H23	VSS	Power/Other	
H24	VSS	Power/Other	
H25	VSS	Power/Other	
H26	VSS	Power/Other	
H27	VSS	Power/Other	
K24	VCC	Power/Other	
K25	VCC	Power/Other	
K26	VCC	Power/Other	
K27	VCC	Power/Other	
K28	VCC	Power/Other	
K29	VCC	Power/Other	
K3	A20M#	ASync GTL+	Input
K30	VCC	Power/Other	
K4	REQ0#	Source Sync	Input/Output
K5	VSS	Power/Other	
K6	REQ3#	Source Sync	Input/Output
K7	VSS	Power/Other	
K8	VCC	Power/Other	
L1	LINT1	ASync GTL+	Input
L2	TESTHI11	ASync GTL+	Input
L23	VSS	Power/Other	
L24	VSS	Power/Other	
L25	VSS	Power/Other	
L26	VSS	Power/Other	
L27	VSS	Power/Other	
L28	VSS	Power/Other	
L29	VSS	Power/Other	
L3	VSS	Power/Other	
L30	VSS	Power/Other	
L4	A06#	Source Sync	Input/Output
L5	A05#	Source Sync	Input/Output
L6	VSS	Power/Other	
L7	VSS	Power/Other	
L8	VCC	Power/Other	
M1	VSS	Power/Other	
M2	THERMTRIP#	ASync GTL+	Output
M23	VCC	Power/Other	
M24	VCC	Power/Other	
M25	VCC	Power/Other	
M26	VCC	Power/Other	

Land No.	Land Name	Signal Buffer Type	Direction
J28	VCC	Power/Other	
J29	VCC	Power/Other	
J3	RESERVED		
J30	VCC	Power/Other	
J4	VSS	Power/Other	
J5	REQ1#	Source Sync	Input/Output
J6	REQ4#	Source Sync	Input/Output
J7	VSS	Power/Other	
J8	VCC	Power/Other	
J9	VCC	Power/Other	
K1	LINT0	ASync GTL+	Input
K2	VSS	Power/Other	
K23	VCC	Power/Other	
M7	VSS	Power/Other	
M8	VCC	Power/Other	
N1	PWRGOOD	Power/Other	Input
N2	IGNNE#	ASync GTL+	Input
N23	VCC	Power/Other	
N24	VCC	Power/Other	
N25	VCC	Power/Other	
N26	VCC	Power/Other	
N27	VCC	Power/Other	
N28	VCC	Power/Other	
N29	VCC	Power/Other	
N3	VSS	Power/Other	
N30	VCC	Power/Other	
N4	RESERVED		
N5	RESERVED		
N6	VSS	Power/Other	
N7	VSS	Power/Other	
N8	VCC	Power/Other	
P1	TESTHI10	Power/Other	Input
P2	SMI#	ASync GTL+	Input
P23	VSS	Power/Other	
P24	VSS	Power/Other	
P25	VSS	Power/Other	
P26	VSS	Power/Other	
P27	VSS	Power/Other	
P28	VSS	Power/Other	
P29	VSS	Power/Other	
P3	INIT#	ASync GTL+	Input
P30	VSS	Power/Other	
P4	VSS	Power/Other	
P5	RESERVED		
P6	A04#	Source Sync	Input/Output
P7	VSS	Power/Other	
P8	VCC	Power/Other	
R1	COMP3	Power/Other	Input

Table 4-2. Land Listing by Land Number (Sheet 8 of 9)

Land No.	Land Name	Signal Buffer Type	Direction
M27	VCC	Power/Other	
M28	VCC	Power/Other	
M29	VCC	Power/Other	
M3	STPCLK#	ASync GTL+	Input
M30	VCC	Power/Other	
M4	A07#	Source Sync	Input/Output
M5	A03#	Source Sync	Input/Output
M6	REQ2#	Source Sync	Input/Output
R3	FERR#/PBE#	ASync GTL+	Output
R30	VSS	Power/Other	
R4	A08#	Source Sync	Input/Output
R5	VSS	Power/Other	
R6	ADSTB0#	Source Sync	Input/Output
R7	VSS	Power/Other	
R8	VCC	Power/Other	
T1	COMP1	Power/Other	Input
T2	COMP5	Power/Other	Input
T23	VCC	Power/Other	
T24	VCC	Power/Other	
T25	VCC	Power/Other	
T26	VCC	Power/Other	
T27	VCC	Power/Other	
T28	VCC	Power/Other	
T29	VCC	Power/Other	
T3	VSS	Power/Other	
T30	VCC	Power/Other	
T4	A11#	Source Sync	Input/Output
T5	A09#	Source Sync	Input/Output
T6	VSS	Power/Other	
T7	VSS	Power/Other	
T8	VCC	Power/Other	
U1	VSS	Power/Other	
U2	AP0#	Common Clk	Input/Output
U23	VCC	Power/Other	
U24	VCC	Power/Other	
U25	VCC	Power/Other	
U26	VCC	Power/Other	
U27	VCC	Power/Other	
U28	VCC	Power/Other	
U29	VCC	Power/Other	
U3	AP1#	Common Clk	Input/Output
U30	VCC	Power/Other	
U4	A13#	Source Sync	Input/Output
U5	A12#	Source Sync	Input/Output
U6	A10#	Source Sync	Input/Output
U7	VSS	Power/Other	
U8	VCC	Power/Other	
V1	MS_ID1	Power/Other	Output

Land No.	Land Name	Signal Buffer Type	Direction
R2	VSS	Power/Other	
R23	VSS	Power/Other	
R24	VSS	Power/Other	
R25	VSS	Power/Other	
R26	VSS	Power/Other	
R27	VSS	Power/Other	
R28	VSS	Power/Other	
R29	VSS	Power/Other	
V24	VSS	Power/Other	
V25	VSS	Power/Other	
V26	VSS	Power/Other	
V27	VSS	Power/Other	
V28	VSS	Power/Other	
V29	VSS	Power/Other	
V3	VSS	Power/Other	
V30	VSS	Power/Other	
V4	A15#	Source Sync	Input/Output
V5	A14#	Source Sync	Input/Output
V6	VSS	Power/Other	
V7	VSS	Power/Other	
V8	VCC	Power/Other	
W1	MS_ID0	Power/Other	Output
W2	RESERVED		
W23	VCC	Power/Other	
W24	VCC	Power/Other	
W25	VCC	Power/Other	
W26	VCC	Power/Other	
W27	VCC	Power/Other	
W28	VCC	Power/Other	
W29	VCC	Power/Other	
W3	TESTHI01	Power/Other	Input
W30	VCC	Power/Other	
W4	VSS	Power/Other	
W5	A16#	Source Sync	Input/Output
W6	A18#	Source Sync	Input/Output
W7	VSS	Power/Other	
W8	VCC	Power/Other	
Y1	RESERVED		
Y2	VSS	Power/Other	
Y23	VCC	Power/Other	
Y24	VCC	Power/Other	
Y25	VCC	Power/Other	
Y26	VCC	Power/Other	
Y27	VCC	Power/Other	
Y28	VCC	Power/Other	
Y29	VCC	Power/Other	
Y3	COMP6	Power/Other	Input
Y30	VCC	Power/Other	

Table 4-2. Land Listing by Land Number (Sheet 9 of 9)

Land No.	Land Name	Signal Buffer Type	Direction
V2	LL_ID0	Power/Other	Output
V23	VSS	Power/Other	
Y6	A19#	Source Sync	Input/Output
Y7	VSS	Power/Other	
Y8	VCC	Power/Other	

Land No.	Land Name	Signal Buffer Type	Direction
Y4	A20#	Source Sync	Input/Output
Y5	VSS	Power/Other	

§

5 Signal Definitions

5.1 Signal Definitions

Table 5-1. Signal Definitions (Sheet 1 of 8)

Name	Type	Description	Notes
A[35:3]#	I/O	A[35:3]# (Address) define a 2^{36}-byte physical memory address space. In sub-phase 1 of the address phase, these signals transmit the address of a transaction. In sub-phase 2, these signals transmit transaction type information. These signals must connect the appropriate pins of all agents on the FSB. A[35:3]# are protected by parity signals AP[1:0]#. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. On the active-to-inactive transition of RESET#, the processors sample a subset of the A[35:3]# lands to determine their power-on configuration. See Section 7.1.	3
A20M#	I	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1 MB boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O write bus transaction.	2
ADS#	I/O	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# lands. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. This signal must connect the appropriate pins on all Dual-Core Intel Xeon Processor 5000 series FSB agents.	3
ADSTB[1:0]#	I/O	Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edge. Strobes are associated with signals as shown below. **Signals** / **Associated Strobes** REQ[4:0], A[16:3]# — ADSTB0# A[35:17]# — ADSTB1#	3
AP[1:0]#	I/O	AP[1:0]# (Address Parity) are driven by the request initiator along with ADS#, A[35:3]#, and the transaction type on the REQ[4:0]# signals. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are high. AP[1:0]# should connect the appropriate pins of all Dual-Core Intel Xeon Processor 5000 series FSB agents. The following table defines the coverage model of these signals. **Request Signals** / **Subphase 1** / **Subphase 2** A[35:24]# — AP0# — AP1# A[23:3]# — AP1# — AP0# REQ[4:0]# — AP1# — AP0#	3
BCLK[1:0]	I	The differential bus clock pair BCLK[1:0] (Bus Clock) determines the FSB frequency. All processor FSB agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V_{CROSS}.	3

Table 5-1. Signal Definitions (Sheet 2 of 8)

Name	Type	Description	Notes
BINIT#	I/O	BINIT# (Bus Initialization) may be observed and driven by all processor FSB agents and if used, must connect the appropriate pins of all such agents. If the BINIT# driver is enabled during power on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future operation. If BINIT# observation is enabled during power-on configuration (see Figure 7.1) and BINIT# is sampled asserted, symmetric agents reset their bus LOCK# activity and bus request arbitration state machines. The bus agents do not reset their I/O Queue (IOQ) and transaction tracking state machines upon observation of BINIT# assertion. Once the BINIT# assertion has been observed, the bus agents will re-arbitrate for the FSB and attempt completion of their bus queue and IOQ entries. If BINIT# observation is disabled during power-on configuration, a priority agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.	3
BNR#	I/O	BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions. Since multiple agents might need to request a bus stall at the same time, BNR# is a wired-OR signal which must connect the appropriate pins of all processor FSB agents. In order to avoid wired-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.	3
BPM[5:0]#	I/O	BPM[5:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[5:0]# should connect the appropriate pins of all FSB agents. BPM4# provides PRDY# (Probe Ready) functionality for the TAP port. PRDY# is a processor output used by debug tools to determine processor debug readiness. BPM5# provides PREQ# (Probe Request) functionality for the TAP port. PREQ# is used by debug tools to request debug operation of the processors. BPM[5:4]# must be bussed to all bus agents. Please refer to the appropriate platform design guidelines for more detailed information.	2
BPRI#	I	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor FSB. It must connect the appropriate pins of all processor FSB agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.	3
BR[1:0]#	I/O	The BR[1:0]# signals are sampled on the active-to-inactive transition of RESET#. The signal which the agent samples asserted determines its agent ID. BR0# drives the BREQ0# signal in the system and is used by the processor to request the bus. These signals do not have on-die termination and must be terminated.	3
BSEL[2:0]	O	The BCLK[1:0] frequency select signals BSEL[2:0] are used to select the processor input clock frequency. Table 2-2 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processors, chipset, and clock synthesizer. All FSB agents must operate at the same frequency. The Dual-Core Intel Xeon Processor 5000 series currently operate at either 667 or 1066 MHz FSB frequency. For more information about these signals, including termination recommendations, refer to the appropriate platform design guideline.	
COMP[3:0]	I	COMP[3:0] must be terminated to V_{SS} on the baseboard using precision resistors. These inputs configure the AGTL+ drivers of the processor. Refer to the appropriate platform design guidelines for implementation details.	
COMP[7:4]	I	COMP[7:4] must be terminated to V_{TT} on the baseboard using precision resistors. These inputs configure the AGTL+ drivers of the processor. Refer to the appropriate platform design guidelines for implementation details.	

Table 5-1. Signal Definitions (Sheet 3 of 8)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th><th>Notes</th></tr>
<tr><td>D[63:0]#</td><td>I/O</td><td>D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor FSB agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer.
D[63:0]# are quad-pumped signals, and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to strobes and DBI#.
<table><tr><th>Data Group</th><th>DSTBN# / DSTBP#</th><th>DBI#</th></tr><tr><td>D[15:0]#</td><td>0</td><td>0</td></tr><tr><td>D[31:16]#</td><td>1</td><td>1</td></tr><tr><td>D[47:32]#</td><td>2</td><td>2</td></tr><tr><td>D[63:48]#</td><td>3</td><td>3</td></tr></table>
Furthermore, the DBI# signals determine the polarity of the data signals. Each group of 16 data signals corresponds to one DBI# signal. When the DBI# signal is active, the corresponding data group is inverted and therefore sampled active high.</td><td>3</td></tr>
<tr><td>DBI[3:0]#</td><td>I/O</td><td>DBI[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DBI[3:0]# signals are activated when the data on the data bus is inverted. If more than half the data bits, within, within a 16-bit group, would have been asserted electronically low, the bus agent may invert the data bus signals for that particular sub-phase for that 16-bit group.
DBI[3:0]# Assignment to Data Bus
<table><tr><th>Bus Signal</th><th>Data Bus Signals</th></tr><tr><td>DBI0#</td><td>D[15:0]#</td></tr><tr><td>DBI1#</td><td>D[31:16]#</td></tr><tr><td>DBI2#</td><td>D[47:32]#</td></tr><tr><td>DBI3#</td><td>D[63:48]#</td></tr></table></td><td>3</td></tr>
<tr><td>DBR#</td><td>O</td><td>DBR# is used only in systems where no debug port connector is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port connector is implemented in the system, DBR# is treated as a no connect for the processor socket. DBR# is not a processor signal.</td><td></td></tr>
<tr><td>DBSY#</td><td>I/O</td><td>DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor FSB to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on all processor FSB agents.</td><td>3</td></tr>
<tr><td>DEFER#</td><td>I</td><td>DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or I/O agent. This signal must connect the appropriate pins of all processor FSB agents.</td><td>3</td></tr>
<tr><td>DP[3:0]#</td><td>I/O</td><td>DP[3:0]# (Data Parity) provide parity protection for the D[63:0]# signals. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins of all processor FSB agents.</td><td>3</td></tr>
<tr><td>DRDY#</td><td>I/O</td><td>DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of all processor FSB agents.</td><td>3</td></tr>
</table>

Table 5-1. Signal Definitions (Sheet 4 of 8)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th><th>Notes</th></tr>
<tr><td>DSTBN[3:0]#</td><td>I/O</td><td>Data strobe used to latch in D[63:0]#.
<table>
<tr><th>Signals</th><th>Associated Strobes</th></tr>
<tr><td>D[15:0]#, DBI0#</td><td>DSTBN0#</td></tr>
<tr><td>D[31:16]#, DBI1#</td><td>DSTBN1#</td></tr>
<tr><td>D[47:32]#, DBI2#</td><td>DSTBN2#</td></tr>
<tr><td>D[63:48]#, DBI3#</td><td>DSTBN3#</td></tr>
</table></td><td>3</td></tr>
<tr><td>DSTBP[3:0]#</td><td>I/O</td><td>Data strobe used to latch in D[63:0]#.
<table>
<tr><th>Signals</th><th>Associated Strobes</th></tr>
<tr><td>D[15:0]#, DBI0#</td><td>DSTBP0#</td></tr>
<tr><td>D[31:16]#, DBI1#</td><td>DSTBP1#</td></tr>
<tr><td>D[47:32]#, DBI2#</td><td>DSTBP2#</td></tr>
<tr><td>D[63:48]#, DBI3#</td><td>DSTBP3#</td></tr>
</table></td><td>3</td></tr>
<tr><td>FERR#/PBE#</td><td>O</td><td>FERR#/PBE# (floating-point error/pending break event) is a multiplexed signal and its meaning is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating-point error and will be asserted when the processor detects an unmasked floating-point error. When STPCLK# is not asserted, FERR#/PBE# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. For additional information on the pending break event functionality, including the identification of support of the feature and enable/disable information, refer to Vol. 3 of the Intel Architecture Software Developer's Manual and the Intel Processor Identification and the CPUID Instruction application note.</td><td>2</td></tr>
<tr><td>FORCEPR#</td><td>I</td><td>The FORCEPR# (force power reduction) input can be used by the platform to cause the Dual-Core Intel Xeon Processor 5000 series to activate the Thermal Control Circuit (TCC).</td><td></td></tr>
<tr><td>GTLREF_ADD_C0
GTLREF_ADD_C1</td><td>I</td><td>GTLREF_ADD_C0 and GTLREF_ADD_C1 determine the signal reference level for AGTL+ address and common clock input lands on processor core 0 and processor core 1 respectively. GTLREF_ADD is used by the AGTL+ receivers to determine if a signal is a logical 0 or a logical 1. Please refer to the appropriate platform design guidelines for additional details.</td><td></td></tr>
<tr><td>GTLREF_DATA_C0
GTLREF_DATA_C1</td><td>I</td><td>GTLREF_DATA_C0 AND GTLREF_DATA_C1 determine the signal reference level for AGTL+ data input lands on processor core 0 and processor core 1 respectively. GTLREF_DATA is used by the AGTL+ receivers to determine if a signal is a logical 0 or a logical 1. Please refer to the appropriate platform design guidelines for additional details.</td><td></td></tr>
<tr><td>HIT#
HITM#</td><td>I/O
I/O</td><td>HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Any FSB agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.</td><td>3</td></tr>
<tr><td>IERR#</td><td>O</td><td>IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor FSB. This transaction may optionally be converted to an external error signal (for example, NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#.
This signal does not have on-die termination.</td><td>2</td></tr>
</table>

Table 5-1. Signal Definitions (Sheet 5 of 8)

Name	Type	Description	Notes
IGNNE#	I	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O write bus transaction.	2
INIT#	I	INIT# (Initialization), when asserted, resets integer registers inside all processors without affecting their internal caches or floating-point registers. Each processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all processor FSB agents.	2
LINT[1:0]	I	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all FSB agents. When the APIC functionality is disabled, the LINT0/INTR signal becomes INTR, a maskable interrupt request signal, and LINT1/NMI becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium® processor. Both signals are asynchronous. These signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.	2
LL_ID[1:0]	O	The LL_ID[1:0] signals are used to select the correct loadline slope for the processor. The Dual-Core Intel Xeon Processor 5000 series pull these signals to ground on the package for a logic 0 as these signals are not connected to the processor die. A logic 1 is a no-connect on the Dual-Core Intel Xeon Processor 5000 series package.	
LOCK#	I/O	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all processor FSB agents. For a locked series of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor FSB, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor FSB throughout the bus locked operation and ensure the atomicity of lock.	3
MCERR#	I/O	MCERR# (Machine Check Error) is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor FSB agents. MCERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options: • Enabled or disabled. • Asserted, if configured, for internal errors along with IERR#. • Asserted, if configured, by the request initiator of a bus transaction after it observes an error. • Asserted by any bus agent when it observes an error in a bus transaction. For more details regarding machine check architecture, refer to the *IA-32 Software Developer's Manual, Volume 3: System Programming Guide*.	
MS_ID[1:0]	O	These signals are provided to indicate the Market Segment for the processor and may be used for future processor compatibility or for keying. The Dual-Core Intel Xeon Processor 5000 series pull these signals to ground on the package for a logic 0 as these signals are not connected to the processor die. A logic 1 is a no-connect on the Dual-Core Intel Xeon Processor 5000 series package.	
PROCHOT#	O	PROCHOT# (Processor Hot) will go active when the processor's temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the Thermal Control Circuit (TCC) has been activated, if enabled. The TCC will remain active until shortly after the processor deasserts PROCHOT#. See Section 6.2.3 for more details. PROCHOT# from each processor socket should be kept separated and not tied together on platform designs.	

Table 5-1. Signal Definitions (Sheet 6 of 8)

Name	Type	Description	Notes
PWRGOOD	I	PWRGOOD (Power Good) is an input. The processor requires this signal to be a clean indication that all processor clocks and power supplies are stable and within their specifications. “Clean” implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state.PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification in Table 2-15, and be followed by a 1-10 ms RESET# pulse. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.	2
REQ[4:0]#	I/O	REQ[4:0]# (Request Command) must connect the appropriate pins of all processor FSB agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[1:0]#. Refer to the AP[1:0]# signal description for details on parity checking of these signals.	3
RESET#	I	Asserting the RESET# signal resets all processors to known states and invalidates their internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least 1 ms after VCC and BCLK have reached their proper specifications. On observing active RESET#, all FSB agents will deassert their outputs within two clocks. RESET# must not be kept asserted for more than 10 ms while PWRGOOD is asserted. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the Section 7.1. This signal does not have on-die termination and must be terminated on the system board.	3
RS[2:0]#	I	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor FSB agents.	3
RSP#	I	RSP# (Response Parity) is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect to the appropriate pins of all processor FSB agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.	3
SKTOCC#	O	SKTOCC# (Socket occupied) will be pulled to ground by the processor to indicate that the processor is present. There is no connection to the processor silicon for this signal.	
SMI#	I	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, processors save the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tri-state its outputs.	2
STPCLK#	I	STPCLK# (Stop Clock), when asserted, causes processors to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the FSB and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.	2
TCK	I	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).	
TDI	I	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.	
TDO	O	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.	
TEST_BUS	Other	Must be connected to all other processor TEST_BUS signals in the system. See the appropriate platform design guideline for termination details.	

Table 5-1. Signal Definitions (Sheet 7 of 8)

Name	Type	Description	Notes
TESTHI[11:0]	I	TESTHI[11:0] must be connected to a V_{TT} power source through a resistor for proper processor operation. Refer to Section 2.6 for TESTHI grouping restrictions.	
THERMDA THERMDA2	Other	Thermal Diode Anode. THERMDA connects to processor core 0, THERMDA2 connects to processor core 1. Refer to the appropriate platform design guidelines for implementation details.	
THERMDC THERMDC2	Other	Thermal Diode Cathode. THERMDC connects to processor core 0. THERMDC2 connects to processor core 1. Refer to the appropriate platform design guidelines for implementation details.	
THERMTRIP#	O	Assertion of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a temperature beyond which permanent silicon damage may occur. Measurement of the temperature is accomplished through an internal thermal sensor. Upon assertion of THERMTRIP#, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature. To protect the processor its core voltage (V_{CC}) must be removed following the assertion of THERMTRIP#. Intel is currently evaluating whether V_{TT} must also be removed. Driving of the THERMTRIP# signals is enabled within 10 ms of the assertion of PWRGOOD and is disabled on de-assertion of PWRGOOD. Once activated, THERMTRIP# remains latched until PWRGOOD is de-asserted. While the de-assertion of the PWRGOOD signal will de-assert THERMTRIP#, if the processor's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted within 10 ms of the assertion of PWRGOOD.	1
TMS	I	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools. See the *eXtended Debug Port: Debug Port Design Guide for UP and DP Platforms* for further information.	
TRDY#	I	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all FSB agents.	
TRST#	I	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.	
V_{CCA}	I	V_{CCA} provides isolated power for the analog portion of the internal processor core PLL's. Refer to the appropriate platform design guidelines for complete implementation details.	
$V_{CCIOPLL}$	I	$V_{CCIOPLL}$ provides isolated power for digital portion of the internal processor core PLL's. Follow the guidelines for V_{CCA}, and refer to the appropriate platform design guidelines for complete implementation details.	
VCC_DIE_SENSE VCC_DIE_SENSE2	O	VCC_DIE_SENSE and VCC_DIE_SENSE2 provide an isolated, low impedance connection to each processor core power and ground. These signals should be connected to the voltage regulator feedback signal, which insures the output voltage (that is, processor voltage) remains within specification. Please see the applicable platform design guide for implementation details.	
VID[5:0]	O	VID[5:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (V_{CC}). These are CMOS signals that are driven by the processor and must be pulled up through a resistor. Conversely, the voltage regulator output must be disabled prior to the voltage supply for these pins becomes invalid. The VID pins are needed to support processor voltage specification variations. See Table 2-3 for definitions of these pins. The VR must supply the voltage that is requested by these pins, or disable itself.	
VID_SELECT	O	VID_SELECT is an output from the processor which selects the appropriate VID table for the Voltage Regulator. Dual-Core Intel Xeon Processor 5000 series pull this signal to ground on the package as this signal is not connected to the processor die.	
VSS_DIE_SENSE VSS_DIE_SENSE2	O	VSS_DIE_SENSE and VSS_DIE_SENSE2 provide an isolated, low impedance connection to each processor core power and ground. These signals should be connected to the voltage regulator feedback signal, which insures the output voltage (that is, processor voltage) remains within specification. Please see the applicable platform design guide for implementation details.	
V_{SSA}	I	V_{SSA} provides an isolated, internal ground for internal PLL's. Do not connect directly to ground. This pin is to be connected to V_{CCA} and $V_{CCIOPLL}$ through a discrete filter circuit.	

Table 5-1. Signal Definitions (Sheet 8 of 8)

Name	Type	Description	Notes
V_{TT}	P	The FSB termination voltage input pins. Refer to Table 2-10 for further details.	
VTT_OUT	O	The VTT_OUT signals are included in order to provide a local V_{TT} for some signals that require termination to V_{TT} on the motherboard.	
VTTPWRGD	I	The processor requires this input to determine that the supply voltage for BSEL[2:0] and VID[5:0] is stable and within specification.	

Notes:
1. For this pin on Dual-Core Intel Xeon Processor 5000 series, the maximum number of symmetric agents is one. Maximum number of priority agents is zero.
2. For this pin on Dual-Core Intel Xeon Processor 5000 series, the maximum number of symmetric agents is two. Maximum number of priority agents is zero.
3. For this pin on Dual-Core Intel Xeon Processor 5000 series, the maximum number of symmetric agents is two. Maximum number of priority agents is one.

§

6 Thermal Specifications

6.1 Package Thermal Specifications

The Dual-Core Intel Xeon Processor 5000 series require a thermal solution to maintain temperatures within its operating limits. Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components within the system. As processor technology changes, thermal management becomes increasingly crucial when building computer systems. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete solution includes both component and system level thermal management features. Component level thermal solutions can include active or passive heatsinks attached to the processor integrated heat spreader (IHS). Typical system level thermal solutions may consist of system fans combined with ducting and venting.

This section provides data necessary for developing a complete thermal solution. For more information on designing a component level thermal solution, refer to the *Dual-Core Intel® Xeon® Processor 5000 Series Thermal/Mechanical Design Guidelines*.

Note: The boxed processor will ship with a component thermal solution. Refer to Chapter 8, "Boxed Processor Specifications"for details on the boxed processor.

6.1.1 Thermal Specifications

To allow the optimal operation and long-term reliability of Intel processor-based systems, the processor must remain within the minimum and maximum case temperature (T_{CASE}) specifications as defined by the applicable thermal profile (refer to Table 6-1, Table 6-4 and Table 6-7; Figure 6-1, Figure 6-2 and Figure 6-3). Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system. For more details on thermal solution design, please refer to the processor thermal/mechanical design guidelines.

The Dual-Core Intel Xeon Processor 5000 series implement a methodology for managing processor temperatures, which is intended to support acoustic noise reduction through fan speed control and to ensure processor reliability. Selection of the appropriate fan speed is based on the temperature reported by the processor's Thermal Diode. If the diode temperature is greater than or equal to Tcontrol (refer to Section 6.2.6), then the processor case temperature must remain at or below the temperature specified by the thermal profile (refer to Figure 6-1, Figure 6-2 and Figure 6-3). If the diode temperature is less than Tcontrol, then the case temperature is permitted to exceed the thermal profile, but the diode temperature must remain at or below Tcontrol. Systems that implement fan speed control must be designed to take these conditions into account. Systems that do not alter the fan speed only need to guarantee the case temperature meets the thermal profile specifications.

Intel has developed two thermal profiles, either of which can be implemented with the Dual-Core Intel Xeon Processor 5000 series. Both ensure adherence to Intel reliability requirements. Thermal Profile A (refer to Figure 6-1, Figure 6-2; Table 6-2 and Table 6-5) is representative of a volumetrically unconstrained thermal solution (that is, industry enabled 2U heatsink). In this scenario, it is expected that the Thermal Control Circuit (TCC) would only be activated for very brief periods of time when running the most power intensive applications. Thermal Profile B (refer to Figure 6-1 and

Figure 6-2; Table 6-3 and Table 6-6) is indicative of a constrained thermal environment (that is, 1U form factor). Because of the reduced cooling capability represented by this thermal solution, the probability of TCC activation and performance loss is increased. Additionally, utilization of a thermal solution that does not meet Thermal Profile B will violate the thermal specifications and may result in permanent damage to the processor. Intel has developed these thermal profiles to allow OEMs to choose the thermal solution and environmental parameters that best suit their platform implementation. Refer to the *Dual-Core Intel® Xeon® Processor 5000 Series Thermal/ Mechanical Design Guidelines* for details on system thermal solution design, thermal profiles and environmental considerations.

The Dual-Core Intel Xeon Processor 5063 (MV) supports a single Thermal Profile targeted at volumetrically constrained thermal environments (for example, blades, 1U form factors.) With this Thermal Profile, it's expected that the Thermal Control Circuit (TCC) would only be activated for very brief periods of time when running the most power-intensive applications. Refer to the *Dual-Core Intel® Xeon® Processor 5000 Series Thermal/Mechanical Design Guidelines* for further details.

The upper point of the thermal profile consists of the Thermal Design Power (TDP) defined in Table 6-1, Table 6-4, Table 6-7 and the associated T_{CASE} value. It should be noted that the upper point associated with Thermal Profile B (x = TDP and y = $T_{CASE\_MAX\_B}$ @ TDP) represents a thermal solution design point. In actuality the processor case temperature will not reach this value due to TCC activation (refer to Figure 6-1 and Figure 6-2). The lower point of the thermal profile consists of x = P_profile_min and y = T_{CASE_MAX} @ P_profile_min. P_profile_min is defined as the processor power at which T_{CASE} , calculated from the thermal profile, is equal to 50 °C.

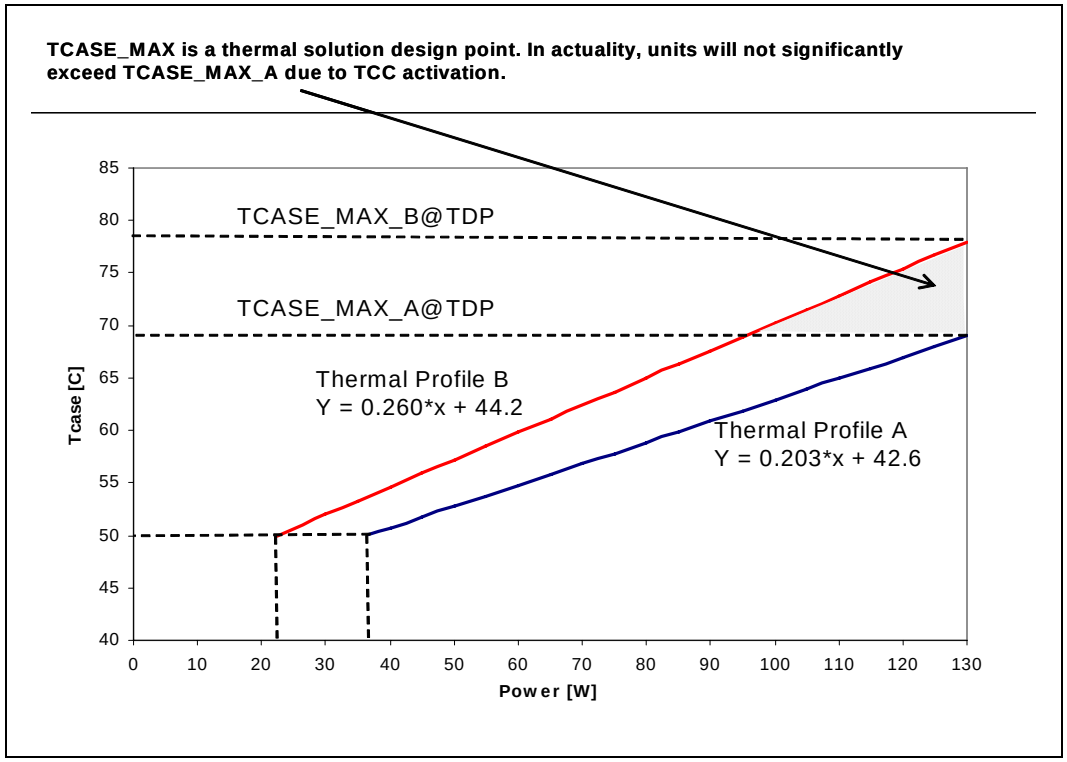
The case temperature is defined at the geometric top center of the processor IHS. Analysis indicates that real applications are unlikely to cause the processor to consume maximum power dissipation for sustained time periods. Intel recommends that complete thermal solution designs target the Thermal Design Power (TDP) indicated in Table 6-1, Table 6-4 and Table 6-7, instead of the maximum processor power consumption. The Thermal Monitor feature is intended to help protect the processor in the event that an application exceeds the TDP recommendation for a sustained time period. For more details on this feature, refer to Section 6.2. To ensure maximum flexibility for future requirements, systems should be designed to the Flexible Motherboard (FMB) guidelines, even if a processor with lower power dissipation is currently planned. **The Thermal Monitor feature must be enabled for the processor to remain within its specifications.**

Table 6-1. Dual-Core Intel Xeon Processor 5000 Series (1066 MHz) Thermal Specifications

Core Frequency	Thermal Design Power (W)	Minimum TCASE (°C)	Maximum TCASE (°C)	Notes
Launch to FMB	130	5	Refer to Figure 6-1; Table 6-2; Table 6-3	1, 2, 3, 4, 5

Notes:
1. These values are specified at V_{CC_MAX} for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} at specified I_{CC}. Please refer to the loadline specifications in Chapter 2, "Electrical Specifications".
2. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum T_{CASE}.
3. These specifications are based on final silicon validation/characterization.
4. Power specifications are defined at all VIDs found in Table 2-10. The Dual-Core Intel Xeon Processor 5000 series may be shipped under multiple VIDs for each frequency.
5. FMB, or Flexible Motherboard, guidelines provide a design target for meeting all planned processor frequency requirements.

Figure 6-1. Dual-Core Intel Xeon Processor 5000 Series (1066 MHz) Thermal Profiles A and B



Notes:

1. Thermal Profile A is representative of a volumetrically unconstrained platform. Please refer to Table 6-2 for discrete points that constitute the thermal profile.
2. Implementation of Thermal Profile A should result in virtually no TCC activation. Furthermore, utilization of thermal solutions that do not meet processor Thermal Profile A will result in increased probability of TCC activation and may incur measurable performance loss. (Refer to Section 6.2 for details on TCC activation.)
3. Thermal Profile B is representative of a volumetrically constrained platform. Please refer to Table 6-3 for discrete points that constitute the thermal profile.
4. Implementation of Thermal Profile B will result in increased probability of TCC activation and measurable performance loss. Furthermore, utilization of thermal solutions that do not meet Thermal Profile B do not meet the processor's thermal specifications and may result in permanent damage to the processor.
5. Refer to the *Dual-Core Intel® Xeon® processor 5000 Series Thermal/Mechanical Design Guidelines* for system and environmental implementation details.

Table 6-2. Dual-Core Intel Xeon Processor 5000 Series (1066 MHz) Thermal Profile A Table

Power (W)	T_{CASE_MAX} (°C)
P_profile_min $_A$=36.5	50.0
40	50.7
45	51.7
50	52.8
55	53.8
60	54.8
65	55.8
70	56.8
75	57.8
80	58.8

Power (W)	T_{CASE_MAX} (°C)
85	59.9
90	60.9
95	61.9
100	62.9
105	63.9
110	64.9
115	65.9
120	67.0
125	68.0
130	69.0

Table 6-3. Dual-Core Intel Xeon Processor 5000 Series (1066 MHz) Thermal Profile B Table

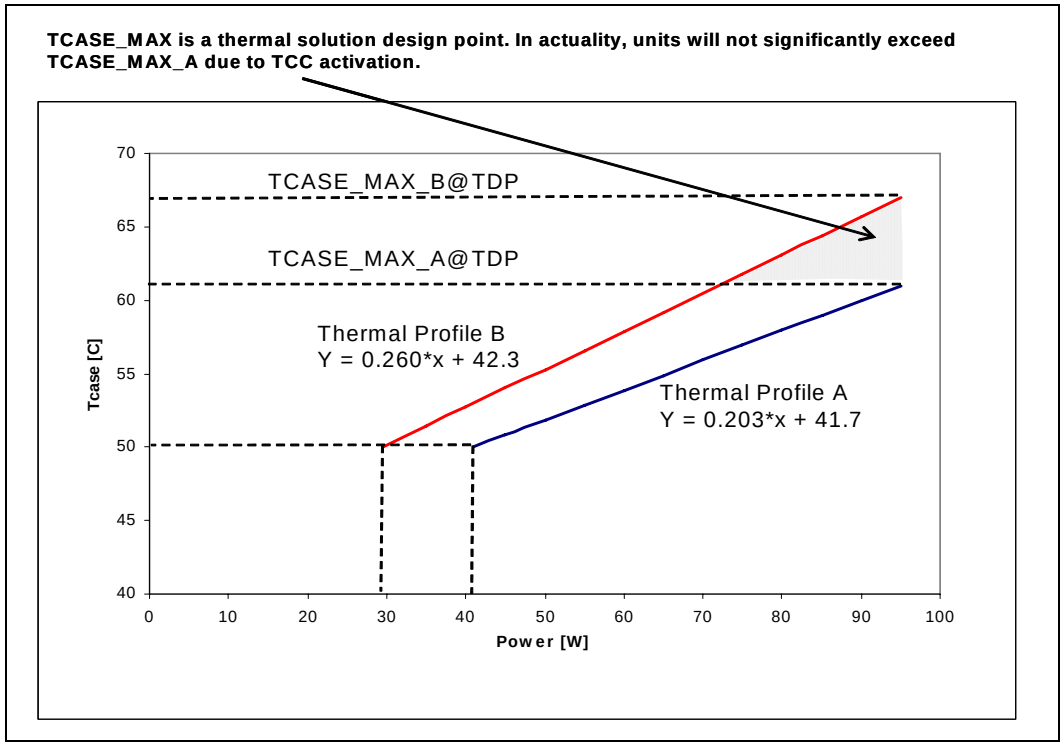
Power (W)	T_{CASE_MAX} (°C)	Power (W)	T_{CASE_MAX} (°C)
$P\_profile\_min_B$=22.3	50.0	80	65.0
30	52.0	85	66.3
35	53.3	90	67.6
40	54.6	95	68.9
45	55.9	100	70.2
50	57.2	105	71.5
55	58.5	110	72.8
60	59.8	115	74.1
65	61.1	120	75.4
70	62.4	125	76.7
75	63.7	130	78.0

Table 6-4. Dual-Core Intel Xeon Processor 5000 Series (667 MHz) Thermal Specifications

Core Frequency	Thermal Design Power (W)	Minimum TCASE (°C)	Maximum TCASE (°C)	Notes
Launch to FMB	95	5	Refer to Figure 6-2; Table 6-5; Table 6-6	1, 2, 3, 4, 5

Notes:
1. These values are specified at V_{CC_MAX} for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} at specified I_{CC}. Please refer to the loadline specifications in Chapter 2, "Electrical Specifications."
2. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum T_{CASE}.
3. These specifications are based on final silicon validation/characterization.
4. Power specifications are defined at all VIDs found in Table 2-10. The Dual-Core Intel Xeon Processor 5000 series may be shipped under multiple VIDs for each frequency.
5. FMB, or Flexible Motherboard, guidelines provide a design target for meeting all planned processor frequency requirements.

Figure 6-2. Dual-Core Intel Xeon Processor 5000 Series (667 MHz) Thermal Profiles



Notes:

1. Thermal Profile A is representative of a volumetrically unconstrained platform. Please refer to Table 6-5 for discrete points that constitute the thermal profile.
2. Implementation of Thermal Profile A should result in virtually no TCC activation. Furthermore, utilization of thermal solutions that do not meet processor Thermal Profile A will result in increased probability of TCC activation and may incur measurable performance loss. (Refer to Section 6.2 for details on TCC activation).
3. Thermal Profile B is representative of a volumetrically constrained platform. Please refer to Table 6-6 for discrete points that constitute the thermal profile.
4. Implementation of Thermal Profile B will result in increased probability of TCC activation and measurable performance loss. Furthermore, utilization of thermal solutions that do not meet Thermal Profile B do not meet the processor's thermal specifications and may result in permanent damage to the processor.
5. Refer to the *Dual-Core Intel® Xeon® Processor 5000 Series Thermal/Mechanical Design Guidelines* for system and environmental implementation details.

Table 6-5. Dual-Core Intel Xeon Processor 5000 Series (667 MHz) Thermal Profile A Table

Power (W)	T_{CASE_MAX} (°C)
$P\_profile\_min_A$=40.9	50.0
45	50.8
50	51.9
55	52.9
60	53.9
65	54.9
70	55.9
75	56.9

Power (W)	T_{CASE_MAX} (°C)
80	57.9
85	59.0
90	60.0
95	61.0

Table 6-6. Dual-Core Intel Xeon 5000 Series (667 MHz) Thermal Profile B Table

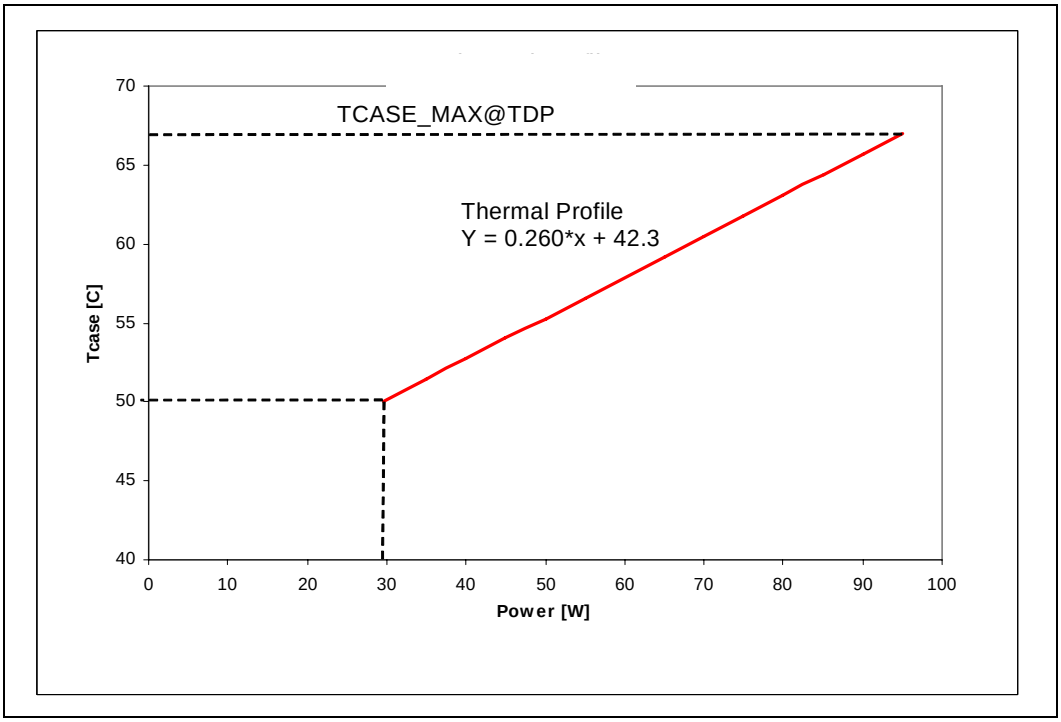
Power (W)	T_{CASE_MAX} (°C)	Power (W)	T_{CASE_MAX} (°C)
P_profile_min $_B$=29.6	50.0	75	61.8
35	51.4	80	63.1
40	52.7	85	64.4
45	54.0	90	65.7
50	55.3	95	67.0
55	56.6		
60	57.9		
65	59.2		
70	60.5		

Table 6-7. Dual-Core Intel Xeon Processor 5063 (MV) Thermal Specifications

Core Frequency	Thermal Design Power (W)	Minimum TCASE (°C)	Maximum TCASE (°C)	Notes
Launch to FMB	95	5	Refer to Figure 6-3; Table 6-8	1, 2, 3, 4, 5

Notes:
1. These values are specified at V_{CC_MAX} for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} at specified I_{CC}. Please refer to the loadline specifications in Chapter 2, "Electrical Specifications."
2. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum T_{CASE}.
3. These specifications are based on final silicon validation/characterization.
4. Power specifications are defined at all VIDs found in Table 2-10. The Dual-Core Intel Xeon Processor 5000 series may be shipped under multiple VIDs for each frequency.
5. FMB, or Flexible Motherboard, guideline provide a design target for meeting all planned processor frequency requirements.

Figure 6-3. Dual-Core Intel Xeon Processor 5063 (MV) Thermal Profile



Notes:
1. Thermal Profile is representative of a volumetrically constrained platform. Please refer to Table 6-8 for discrete points that constitute the thermal profile.
2. Implementation of Thermal Profile should result in virtually no TCC activation. Furthermore, utilization of thermal solutions that do not meet Thermal Profile will not meet the processor's thermal specifications and may result in permanent damage to the processor.
3. Refer to the *Dual-Core Intel® Xeon® Processor 5000 Series Thermal/Mechanical Design Guidelines* for system and environment implementation details.

Table 6-8. Dual-Core Intel Xeon Processor 5063 (MV) Thermal Profile Table

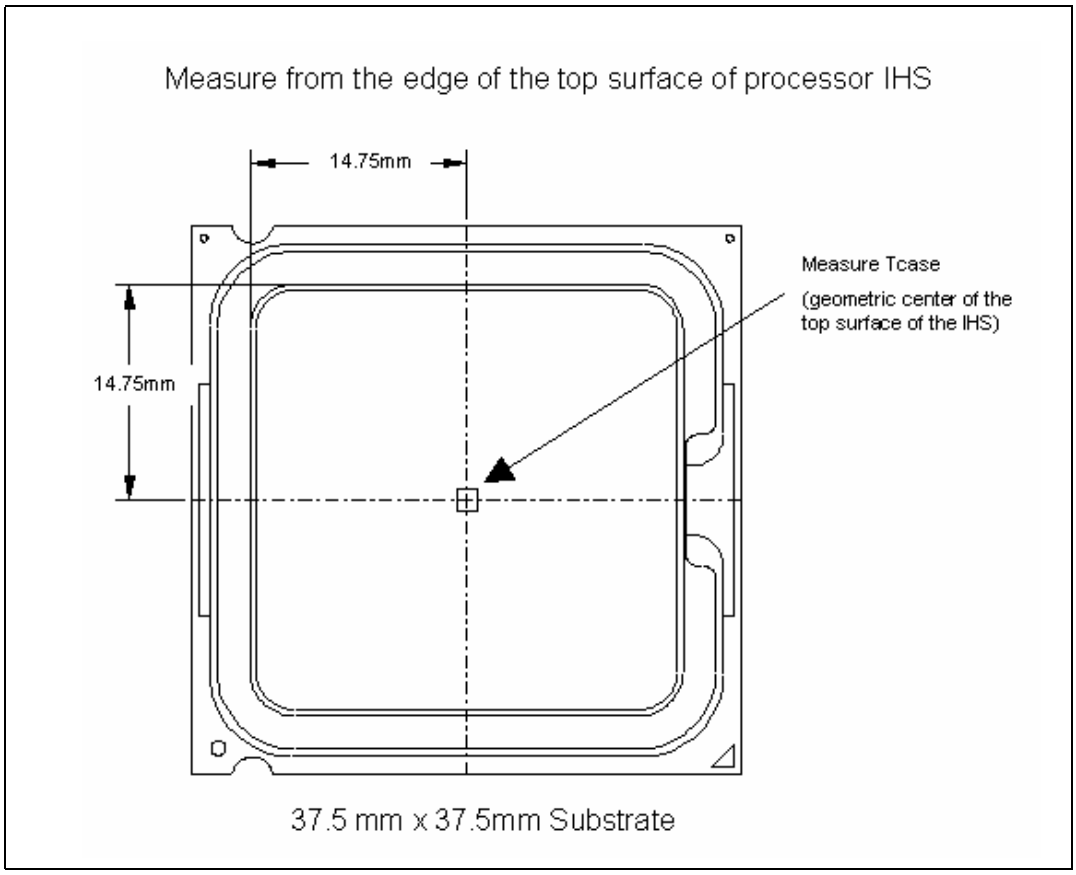
Power (W)	T_{CASE_MAX} (°C)	Power (W)	T_{CASE_MAX} (°C)
$P\_profile\_min_B$=29.6	50.0	75	61.8
35	51.4	80	63.1
40	52.7	85	64.4
45	54.0	90	65.7
50	55.3	95	67.0
55	56.6		
60	57.9		
65	59.2		
70	60.5		

6.1.2 Thermal Metrology

The minimum and maximum case temperatures (T_{CASE}) specified in Table 6-2, Table 6-3, Table 6-5, and Table 6-6 are measured at the geometric top center of the processor integrated heat spreader (IHS). Figure 6-4 illustrates the location where

T_{CASE} temperature measurements should be made. For detailed guidelines on temperature measurement methodology, refer to the *Dual-Core Intel® Xeon® Processor 5000 Series Thermal/Mechanical Design Guidelines*.

Figure 6-4. Case Temperature (T_{CASE}) Measurement Location



Note: Figure is not to scale and is for reference only.

6.2 Processor Thermal Features

6.2.1 Thermal Monitor

The Thermal Monitor (TM1) feature helps control the processor temperature by activating the Thermal Control Circuit (TCC) when the processor silicon reaches its maximum operating temperature. The TCC reduces processor power consumption as needed by modulating (starting and stopping) the internal processor core clocks. The Thermal Monitor (TM1) must be enabled for the processor to be operating within specifications. The temperature at which Thermal Monitor activates the thermal control circuit is not user configurable and is not software visible. Bus traffic is snooped in the normal manner, and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

When the Thermal Monitor is enabled and a high temperature situation exists (that is, TCC is active), the clocks will be modulated by alternately turning the clocks off and on at a duty cycle specific to the processor (typically 30 -50%). Cycle times are processor speed dependent and will decrease as processor core frequencies increase. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the TCC goes inactive and clock modulation ceases.

With a thermal solution designed to meet Thermal Profile A, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. A thermal solution that is designed to Thermal Profile B may cause a noticeable performance loss due to increased TCC activation. Thermal Solutions that exceed Thermal Profile B will exceed the maximum temperature specification and affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under designed may not be capable of cooling the processor even when the TCC is active continuously. Refer to the *Dual-Core Intel® Xeon® Processor 5000 Series Thermal/Mechanical Design Guidelines* for information on designing a thermal solution.

The duty cycle for the TCC, when activated by the TM1, is factory configured and cannot be modified. The TM1 does not require any additional hardware, software drivers, or interrupt handling routines.

6.2.2 On-Demand Mode

The processor provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption. This mechanism is referred to as “On-Demand” mode and is distinct from the Thermal Monitor feature. On-Demand mode is intended as a means to reduce system level power consumption. Systems utilizing the Dual-Core Intel Xeon Processor 5000 series must not rely on software usage of this mechanism to limit the processor temperature. If bit 4 of the IA32_CLOCK_MODULATION MSR is set to a ‘1’, the processor will immediately reduce its power consumption via modulation (starting and stopping) of the internal core clock, independent of the processor temperature. When using On-Demand mode, the duty cycle of the clock modulation is programmable via bits 3:1 of the same IA32_CLOCK_MODULATION MSR. In On-Demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off to 87.5% on/12.5% off in 12.5% increments. On-Demand mode may be used in conjunction with the Thermal Monitor; however, if

the system tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode.

6.2.3 PROCHOT# Signal

An external signal, PROCHOT# (processor hot) is asserted when the processor die temperature has reached its factory configured trip point. If Thermal Monitor is enabled (note that Thermal Monitor must be enabled for the processor to be operating within specification), the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT#. Refer to the *Intel Architecture Software Developer's Manual* for specific register and programming details.

PROCHOT# is designed to assert at or a few degrees higher than maximum T_{CASE} (as specified by Thermal Profile A) when dissipating TDP power and cannot be interpreted as an indication of processor case temperature. This temperature delta accounts for processor package, lifetime and manufacturing variations and attempts to ensure the Thermal Control Circuit is not activated below maximum T_{CASE} when dissipating TDP power. There is no defined or fixed correlation between the PROCHOT# trip temperature, the case temperature or the thermal diode temperature. Thermal solutions must be designed to the processor specifications and cannot be adjusted based on experimental measurements of T_{CASE}, PROCHOT#, or Tdiode on random processor samples.

6.2.4 FORCEPR# Signal

The FORCEPR# (force power reduction) input can be used by the platform to cause the Dual-Core Intel Xeon Processor 5000 series to activate the TCC. If the Thermal Monitor is enabled, the TCC will be activated upon the assertion of the FORCEPR# signal. Assertion of the FORCEPR# signal will activate TCC for both processor cores. The TCC will remain active until the system deasserts FORCEPR#. FORCEPR# is an asynchronous input. FORCEPR# can be used to thermally protect other system components. To use the VR as an example, when FORCEPR# is asserted, the TCC circuit in the processor will activate, reducing the current consumption of the processor and the corresponding temperature of the VR.

It should be noted that assertion of FORCEPR# does not automatically assert PROCHOT#. As mentioned previously, the PROCHOT# signal is asserted when a high temperature situation is detected. A minimum pulse width of 500 µs is recommended when FORCEPR# is asserted by the system. Sustained activation of the FORCEPR# signal may cause noticeable platform performance degradation. Refer to the appropriate platform design guidelines for details on implementing the FORCEPR# signal feature.

6.2.5 THERMTRIP# Signal

Regardless of whether or not Thermal Monitor is enabled, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached an elevated temperature (refer to the THERMTRIP# definition in Table 5-1). At this point, the FSB signal THERMTRIP# will go active and stay active as described in Table 5-1. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. Intel also recommends the removal of V_{TT}.

6.2.6 Tcontrol and Fan Speed Reduction

Tcontrol is a temperature specification based on a temperature reading from the thermal diode. The value for Tcontrol will be calibrated in manufacturing and configured for each processor. The Tcontrol value is set identically for both processor cores. The Tcontrol temperature for a given processor can be obtained by reading the IA32_TEMPERATURE_TARGET MSR in the processor. The Tcontrol value that is read from the IA32_TEMPERATURE_TARGET MSR must be converted from Hexadecimal to Decimal and added to a base value of 60° C. The value of Tcontrol may vary from 0x00h to 0x1Eh.

When Tdiode is above Tcontrol, then T_{CASE} must be at or below T_{CASE_MAX} as defined by the thermal profile. (Refer to Figure 6-1, Figure 6-2 and Figure 6-3 ; Table 6-2, Table 6-3, Table 6-5, Table 6-6 and Table 6-8). Otherwise, the processor temperature can be maintained at or below Tcontrol.

6.2.7 Thermal Diode

The Dual-Core Intel Xeon Processor 5000 series incorporates an on-die PNP transistor whose base emitter junction is used as a thermal “diode”, one per core, with its collector shorted to Ground. A thermal sensor located on the system board may monitor the die temperature of the processor for thermal management and fan speed control. Table 6-9, Table 6-11 and Table 6-12 provide the “diode” parameters and interface specifications. Two different sets of “diode” parameters are listed in Table 6-9 and Table 6-11. The Diode Model parameters (Table 6-9) apply to traditional thermal sensors that use the Diode Equation to determine the processor temperature. Transistor Model parameters (Table 6-11) have been added to support thermal sensors that use the transistor equation method. The Transistor Model may provide more accurate temperature measurements when the diode ideality factor is closer to the maximum or minimum limits. This thermal “diode” is separate from the Thermal Monitor’s thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

When calculating a temperature based on thermal diode measurements, a number of parameters must be either measured or assumed. Most devices measure the diode ideality and assume a series resistance and ideality trim value, although some are capable of also measuring the series resistance. Calculating the temperature is then accomplished by using the equations listed under Table 6-9. In most temperature sensing devices, an expected value for the diode ideality is designed-in to the temperature calculation equation. If the designer of the temperature sensing device assumes a perfect diode, the ideality value (also called n_{trim}) will be 1.000. Given that most diodes are not perfect, the designers usually select an n_{trim} value that more closely matches the behavior of the diodes in the processor. If the processors diode ideality deviates from that of n_{trim}, each calculated temperature will be offset by a fixed amount. The temperature offset can be calculated with the equation:

$$T_{error(nf)} = T_{measured} \times (1 - n_{actual}/n_{trim})$$

where $T_{error(nf)}$ is the offset in degrees C, $T_{measured}$ is in Kelvin, n_{actual} is the measured ideality of the diode, and n_{trim} is the diode ideality assumed by the temperature sensing device.

In order to improve the accuracy of diode based temperature measurements, a new register (Tdiode_Offset) has been added to Dual-Core Intel Xeon Processor 5000 series which will contain thermal diode characterization data. During manufacturing each processor’s thermal diode will be evaluated for its behavior relative to a theoretical diode. Using the equation above, the temperature error created by the difference

between n_{trim} and the actual ideality of the particular processor will be calculated. This value (Tdiode_Offset) will be programmed into the new diode correction MSR and then added to the Tdiode_Base value can be used to correct temperatures read by diode based temperature sensing devices.

If the n_{trim} value used to calculating Tdiode_Offset differs from the n_{trim} value used in a temperature sensing device, the $T_{error(nf)}$ may not be accurate. If desired, the Tdiode_Offset can be adjusted by calculating n_{actual} and then recalculating the offset using the actual n_{trim} as defined in the temperature sensor manufacturers' datasheet.

The parameters used to calculate the Thermal Diode (Tdiode) Correction Factor are listed in Table 6-12. For Dual-Core Intel Xeon Processor 5000 series, the range of Tdiode Correction Factor is ±14°C.

Table 6-9. Thermal Diode Parameters using Diode Model

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{FW}	Forward Bias Current	5	-	200	µA	1
n	Diode Ideality Factor	1.000	1.009	1.050	-	2, 3, 4
R_T	Series Resistance	2.79	4.52	6.24	Ω	2, 3, 5

Notes:
1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Characterized across a temperature range of 50-80°C.
3. Not 100% tested. Specified by design characterization.
4. The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode equation: $I_{FW} = I_S * (e^{qVD/nkT} - 1)$
   Where I_S = saturation current, q = electronic charge, V_D = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).
5. The series resistance, R_T, is provided to allow for a more accurate measurement of the junction temperature. R_T, as defined, includes the lands of the processor but does not include any socket resistance or board trace resistance between the socket and external remote diode thermal sensor. R_T can be used by remote diode thermal sensors with automatic series resistance cancellation to calibrate out this error term. Another application is that a temperature offset can be manually calculated and programmed into an offset register in the remote diode thermal sensors as exemplified by the equation:
   Terror = $[R_T * (N-1) * I_{FW}min] / [nk/q * \ln N]$
   Where Terror=sensor temperature error, N=sensor current ratio, k=Boltzmann Constant, q=electronic charge.

Table 6-10. Thermal Diode Interface

Land Name	Land Number	Description
THERMDA	AL1	diode anode
THERMDC	AK1	diode cathode
THERMDA2	AJ7	diode anode
THERMDC2	AH7	diode cathode

Table 6-11. Thermal Diode Parameters using Transistor Model

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{FW}	Forward Bias Current	5	-	200	µA	1, 2
I_E	Emitter Current	5	-	200	µA	
n_Q	Transistor Ideality	0.997	1.001	1.005	-	3, 4, 5
Beta	-	0.391	-	0.760	-	3, 4
R_T	Series Resistance	2.79	4.52	6.24	Ω	3, 6

Notes:
1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Same as I_{FW} in the diode model in Table 6-9.
3. Characterized across a temperature range of 50-80°C.
4. Not 100% tested. Specified by design characterization.
5. The ideality factor, n_Q, represents the deviation from ideal transistor model behavior as exemplified by the equation for the collector current: $I_C = I_S * (e^{qVBE/n_Q kT} - 1)$
   Where I_S = saturation current, q = electronic charge, V_{BE} = voltage across the transistor based emitter junction (same nodes as V_D), k = Boltzmann Constant, and T = absolute temperature (Kelvin).
6. The series resistance, R_T provided in Table 6-9 can be used for more accurate readings as needed.

Table 6-12. Parameters for Tdiode Correction Factor

Symbol	Parameter	Typ	Unit	Notes
n_{trim}	Diode Ideality used to calculate Tdiode_Offset	1.008		1
Tdiode_Base		0	°C	1

Notes:
1. See the *Dual-Core Intel® Xeon® Processor 5000 Series Thermal/Mechanical Design Guidelines* for more information on how to use the Tdiode_Offset, Tdiode_Base and n_{trim} parameters for fan speed control.

§

7 Features

7.1 Power-On Configuration Options

Several configuration options can be configured by hardware. The Dual-Core Intel Xeon Processor 5000 series samples its hardware configuration at reset, on the active-to-inactive transition of RESET#. For specifics on these options, please refer to Table 7-1.

The sampled information configures the processor for subsequent operation. These configuration options cannot be changed except by another reset. All resets reconfigure the processor, for reset configuration purposes, the processor does not distinguish between a “warm” reset (PWRGOOD signal remains asserted during reset) and a “power-on” reset.

Table 7-1. Power-On Configuration Option Lands

Configuration Option	Land Name	Notes
Output tri state	SMI#	1,2
Execute BIST (Built-In Self Test)	A3#	1,2
In Order Queue de-pipelining (set IOQ depth to 1)	A7#	1,2
Disable MCERR# observation	A9#	1,2
Disable BINIT# observation	A10#	1,2
Disable bus parking	A15#	1,2
Symmetric agent arbitration ID	BR[1:0]#	1,2
Force single logical processor	A31#	1,2,3

Notes:

1. Asserting this signal during RESET# will select the corresponding option.
2. Address pins not identified in this table as configuration options should not be asserted during RESET#.
3. This mode is not tested.

7.2 Clock Control and Low Power States

The Dual-Core Intel Xeon Processor 5000 series support the Enhanced HALT Powerdown state in addition to the HALT Powerdown state and Stop-Grant states to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See Figure 7-1 for a visual representation of the processor low power states.

The Enhanced HALT state is enabled by default in the Dual-Core Intel Xeon Processor 5000 series. The Enhanced HALT state must remain enabled via the BIOS for the processor to remain within its specifications. For processors that are already running at the lowest core to bus ratio for its nominal operating point, the processor will transition to the HALT Powerdown state instead of the Enhanced HALT state.

The Stop Grant state requires chipset and BIOS support on multiprocessor systems. In a multiprocessor system, all the STPCLK# signals are bussed together, thus all processors are affected in unison. The Hyper-Threading Technology feature adds the conditions that all logical processors share the same STPCLK# signal internally. When the STPCLK# signal is asserted, the processor enters the Stop Grant state, issuing a Stop Grant Special Bus Cycle (SBC) for each processor or logical processor. The chipset

needs to account for a variable number of processors asserting the Stop Grant SBC on the bus before allowing the processor to be transitioned into one of the lower processor power states. Refer to the applicable chipset specification for more information.

7.2.1 Normal State

This is the normal operating state for the processor.

7.2.2 HALT or Enhanced Powerdown States

The Enhanced HALT power down state is enabled by default in the Dual-Core Intel Xeon Processor 5000 series. The Enhanced HALT power down state must remain enabled via the BIOS. The Enhanced HALT state requires support for dynamic VID transitions in the platform.

7.2.2.1 HALT Powerdown State

HALT is a low power state entered when all logical processors have executed the HALT or MWAIT instruction. When one of the logical processors executes the HALT or MWAIT instruction, that logical processor is halted; however, the other processor continues normal operation. The processor will transition to the Normal state upon the occurrence of SMI#, BINIT#, INIT#, LINT[1:0] (NMI, INTR), or an interrupt delivered over the front side bus. RESET# will cause the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the HALT Power Down state. Refer to the *IA-32 Intel® Architecture Software Developer's Manual, Volume III: System Programming Guide* for more information.

The system can generate a STPCLK# while the processor is in the HALT Power Down state. When the system deasserts the STPCLK#, the processor will return execution to the HALT state.

While in HALT Power Down state, the processor will process front side bus snoops and interrupts.

7.2.2.2 Enhanced HALT Powerdown State

Enhanced HALT state is a low power state entered when all logical processors have executed the HALT or MWAIT instructions. When one of the logical processors executes the HALT instruction, that logical processor is halted; however, the other processor continues normal operation. The Enhanced HALT state is generally a lower power state than the Stop Grant state.

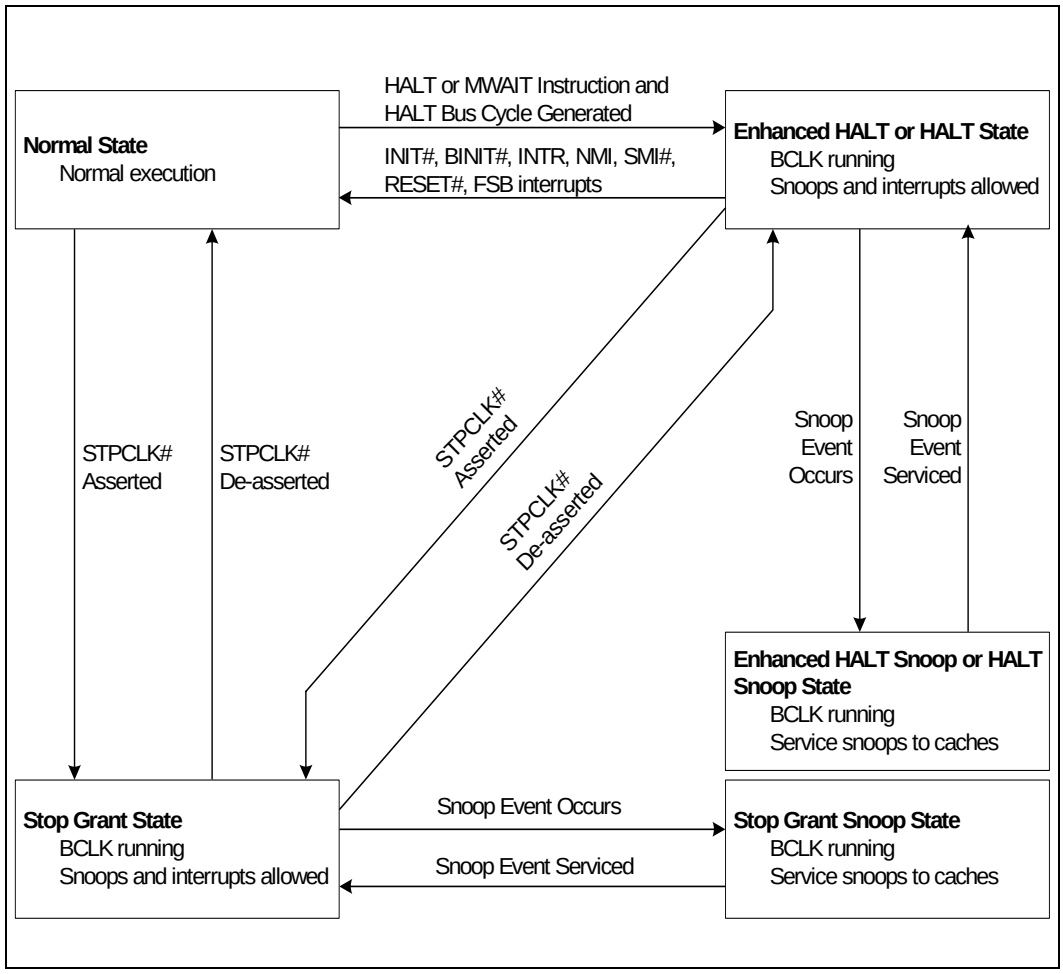
The processor will automatically transition to a lower core frequency and voltage operating point before entering the Enhanced HALT state. Note that the processor FSB frequency is not altered; only the internal core frequency is changed. When entering the low power state, the processor will first switch to the lower bus ratio and then transition to the lower VID.

While in the Enhanced HALT state, the processor will process bus snoops.

The processor exits the Enhanced HALT state when a break event occurs. When the processor exits the Enhanced HALT state, it will first transition the VID to the original value and then change the bus ratio back to the original value.

The Enhanced HALT state must be enabled by way of the BIOS for the processor to remain within its specifications. The Enhanced HALT state requires support for dynamic VID transitions in the platform.

Figure 7-1. Stop Clock State Machine



7.2.3 Stop-Grant State

When the STPCLK# pin is asserted, the Stop-Grant state of the processor is entered 20 bus clocks after the response phase of the processor-issued Stop Grant Acknowledge special bus cycle. Once the STPCLK# pin has been asserted, it may only be deasserted once the processor is in the Stop Grant state. For the Dual-Core Intel Xeon Processor 5000 series, all logical processor cores will enter the Stop-Grant state once the STPCLK# pin is asserted. Additionally, all logical cores must be in the Stop Grant state before the deassertion of STPCLK#.

Since the AGTL+ signal pins receive power from the front side bus, these pins should not be driven (allowing the level to return to V_{TT}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the front side bus should be driven to the inactive state.

BINIT# will not be serviced while the processor is in Stop-Grant state. The event will be latched and can be serviced by software upon exit from the Stop Grant state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state will occur with the de-assertion of the STPCLK# signal.

A transition to the Grant Snoop state will occur when the processor detects a snoop on the front side bus (see Section 7.2.4.1).

While in the Stop-Grant state, SMI#, INIT#, BINIT# and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the Normal state. Only one occurrence of each event will be recognized upon return to the Normal state.

While in Stop-Grant state, the processor will process snoops on the front side bus and it will latch interrupts delivered on the front side bus.

The PBE# signal can be driven when the processor is in Stop-Grant state. PBE# will be asserted if there is any pending interrupt latched within the processor. Pending interrupts that are blocked by the EFLAGS.IF bit being clear will still cause assertion of PBE#. Assertion of PBE# indicates to system logic that it should return the processor to the Normal state.

7.2.4 Enhanced HALT Snoop or HALT Snoop State, Stop Grant Snoop State

The Enhanced HALT Snoop state is used in conjunction with the Enhanced HALT state. If the Enhanced HALT state is not enabled in the BIOS, the default Snoop state entered will be the HALT Snoop state. Refer to the sections below for details on HALT Snoop state, Stop Grant Snoop state and Enhanced HALT Snoop state.

7.2.4.1 HALT Snoop State, Stop Grant Snoop State

The processor will respond to snoop or interrupt transactions on the front side bus while in Stop-Grant state or in HALT Power Down state. During a snoop or interrupt transaction, the processor enters the HALT/Grant Snoop state. The processor will stay in this state until the snoop on the front side bus has been serviced (whether by the processor or another agent on the front side bus) or the interrupt has been latched. After the snoop is serviced or the interrupt is latched, the processor will return to the Stop-Grant state or HALT Power Down state, as appropriate.

7.2.4.2 Enhanced HALT Snoop State

The Enhanced HALT Snoop state is the default Snoop state when the Enhanced HALT state is enabled via the BIOS. The processor will remain in the lower bus ratio and VID operating point of the Enhanced HALT state.

While in the Enhanced HALT Snoop state, snoops and interrupt transactions are handled the same way as in the HALT Snoop state. After the snoop is serviced or the interrupt is latched, the processor will return to the Enhanced HALT state.

7.3 Enhanced Intel SpeedStep® Technology

The Dual-Core Intel Xeon Processor 5000 series support Enhanced Intel SpeedStep Technology. This technology enables the processor to switch between multiple frequency and voltage points, which results in platform power savings. Enhanced Intel SpeedStep Technology requires support for dynamic VID transitions in the platform. Switching between voltage/frequency states is software controlled.

Note: Not all Dual-Core Intel Xeon Processor 5000 series are capable of supporting Enhanced Intel SpeedStep Technology. More details on which processor frequencies will support this feature will be provided in future releases of the *Dual-Core Intel® Xeon® Processor 5000 Series Specification Update* when available.

Enhanced Intel SpeedStep Technology creates processor performance states (P-states) or voltage/frequency operating points. P-states are lower power capability states within the Normal state as shown in Figure 7-1. Enhanced Intel SpeedStep Technology enables real-time dynamic switching between frequency and voltage points. It alters the performance of the processor by changing the bus to core frequency ratio and voltage. This allows the processor to run at different core frequencies and voltages to best serve the performance and power requirements of the processor and system. The Dual-Core Intel Xeon Processor 5000 series have hardware logic that coordinates the requested processor voltage between the processor cores. The highest voltage that is requested for either of the processor cores is selected for that processor. Note that the front side bus is not altered; only the internal core frequency is changed. In order to run at reduced power consumption, the voltage is altered in step with the bus ratio.

The following are key features of Enhanced Intel SpeedStep Technology:

- Multiple voltage/frequency operating points provide optimal performance at reduced power consumption.
- Voltage/frequency selection is software controlled by writing to processor MSR's (Model Specific Registers), thus eliminating chipset dependency.
  - If the target frequency is higher than the current frequency, V_{CC} is incremented in steps (+12.5 mV) by placing a new value on the VID signals and the processor shifts to the new frequency. Note that the top frequency for the processor can not be exceeded.
  - If the target frequency is lower than the current frequency, the processor shifts to the new frequency and V_{CC} is then decremented in steps (-12.5 mV) by changing the target VID through the VID signals.

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8 Boxed Processor Specifications

8.1 Introduction

Intel boxed processors are intended for system integrators who build systems from components available through distribution channels. The Dual-Core Intel® Xeon® Processor 5000 series will be offered as an Intel boxed processor.

Intel will offer the Dual-Core Intel Xeon Processor 5000 series boxed processor with two heat sink configurations available for each processor frequency: 1U passive/2U active combination solution and a 2U passive only solution. The 1U passive/2U active combination solution is based on a 1U passive heat sink with a removable fan that will be pre-attached at shipping. This heat sink solution is intended to be used as either a 1U passive heat sink or a 2U+ active heat sink. Although the active combination solution with removable fan mechanically fits into a 2U keepout, additional design considerations may need to be addressed to provide sufficient airflow to the fan inlet.

The 1U passive/2U active combination solution in the active fan configuration is primarily designed to be used in a pedestal chassis where sufficient air inlet space is present and strong side directional airflow is not an issue. The 1U passive/active combination solution with the fan removed and the 2U passive thermal solution require the use of chassis ducting and are targeted for use in rack mount servers. The retention solution used for these products is called the Common Enabling Kit, or CEK. The CEK base is compatible with both thermal solutions and uses the same hole locations as the Intel® Xeon® processor with 800 MHz FSB.

The 1U passive/active combination solution will utilize a removable fan with a 4-pin pulse width modulated (PWM) T-diode control. Use of a 4-pin PWM T-diode controlled active thermal solution helps customers meet acoustic targets in pedestal platforms through the motherboards's ability to directly control the RPM of the processor heat sink fan. Please see Section 8.3 for more details. Figure 8-1 through Figure 8-3 are representations of the two heat sink solutions.

Figure 8-1. Boxed Dual-Core Intel Xeon Processor 5000 Series 1U Passive/2U Active Combination Heat Sink (With Removable Fan)

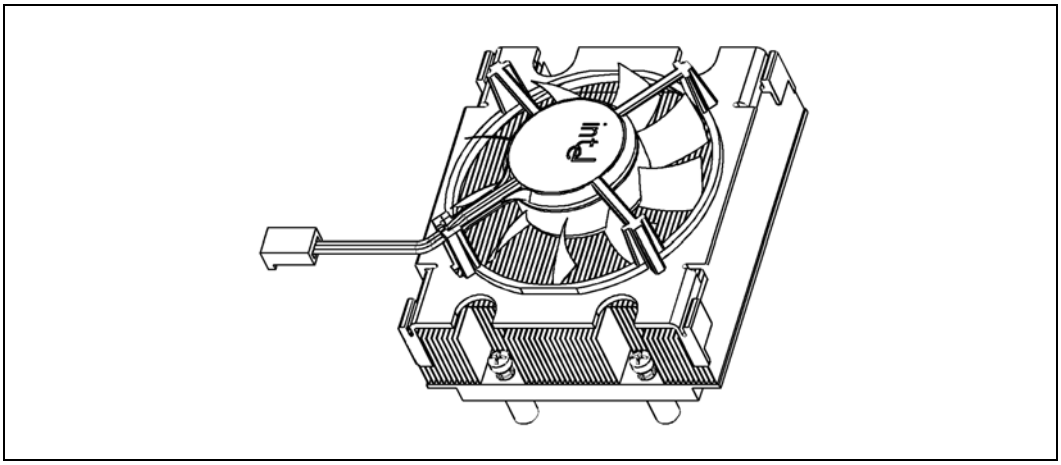


Figure 8-2. Boxed Dual-Core Intel Xeon Processor 5000 Series 2U Passive Heat Sink

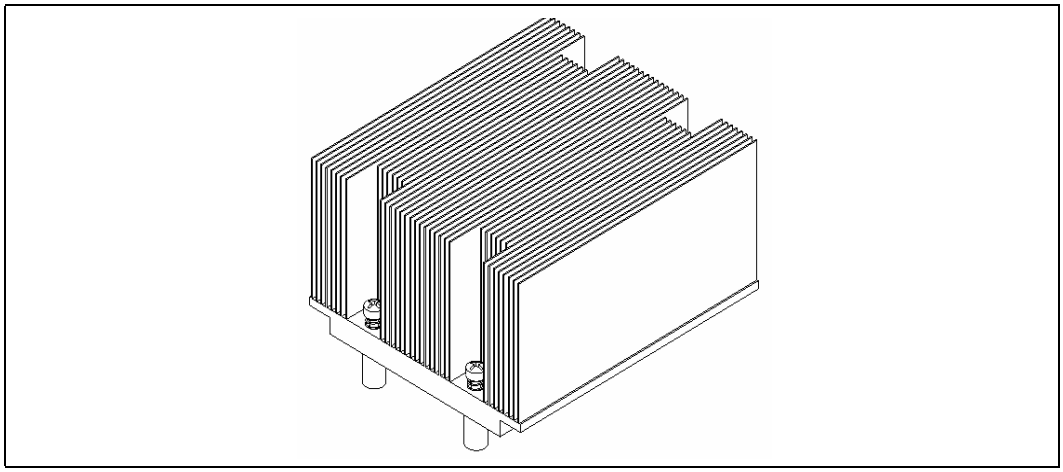
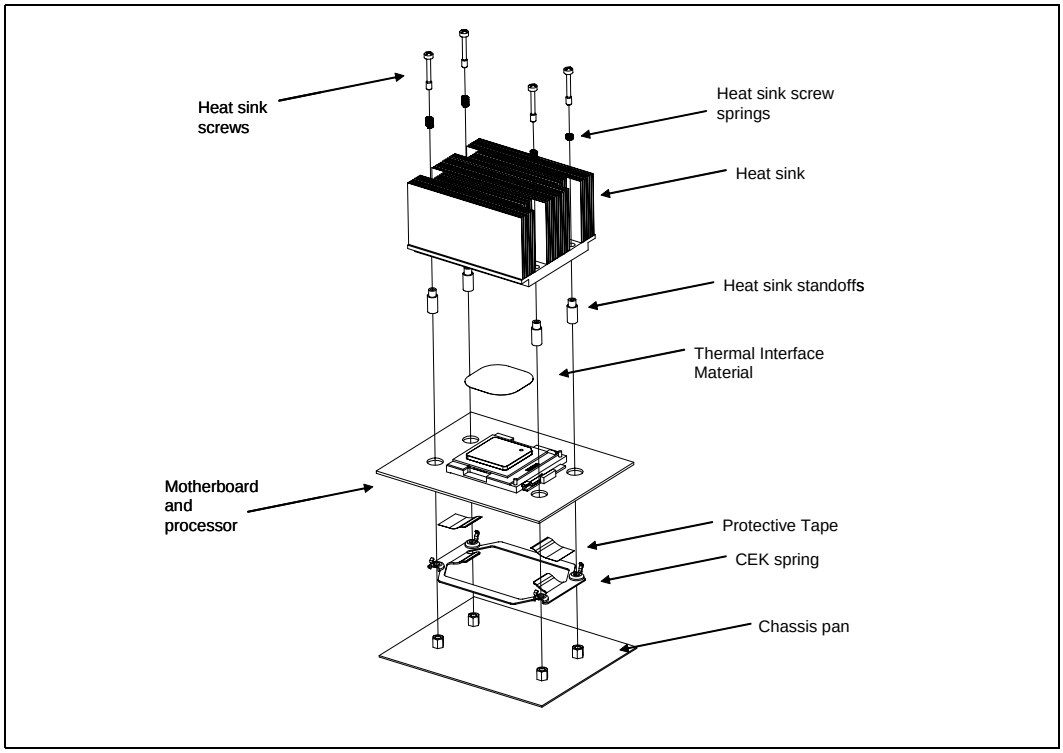


Figure 8-3. 2U Passive Dual-Core Intel Xeon Processor 5000 Series Thermal Solution (Exploded View)



Notes:
1. The heat sinks represented in these images are for reference only, and may not represent the final boxed processor heat sinks.
2. The screws, springs, and standoffs will be captive to the heat sink. This image shows all of the components in an exploded view.
3. It is intended that the CEK spring will ship with the base board and be pre-attached prior to shipping.

8.2 Mechanical Specifications

This section documents the mechanical specifications of the boxed processor.

8.2.1 Boxed Processor Heat Sink Dimensions (CEK)

The boxed processor will be shipped with an unattached thermal solution. Clearance is required around the thermal solution to ensure unimpeded airflow for proper cooling. The physical space requirements and dimensions for the boxed processor and assembled heat sink are shown in Figure 8-4 through Figure 8-8. Figure 8-9 through Figure 8-10 are the mechanical drawings for the 4-pin board fan header and 4-pin connector used for the active CEK fan heat sink solution.

Figure 8-4. Top Side Board Keep-Out Zones (Part 1)

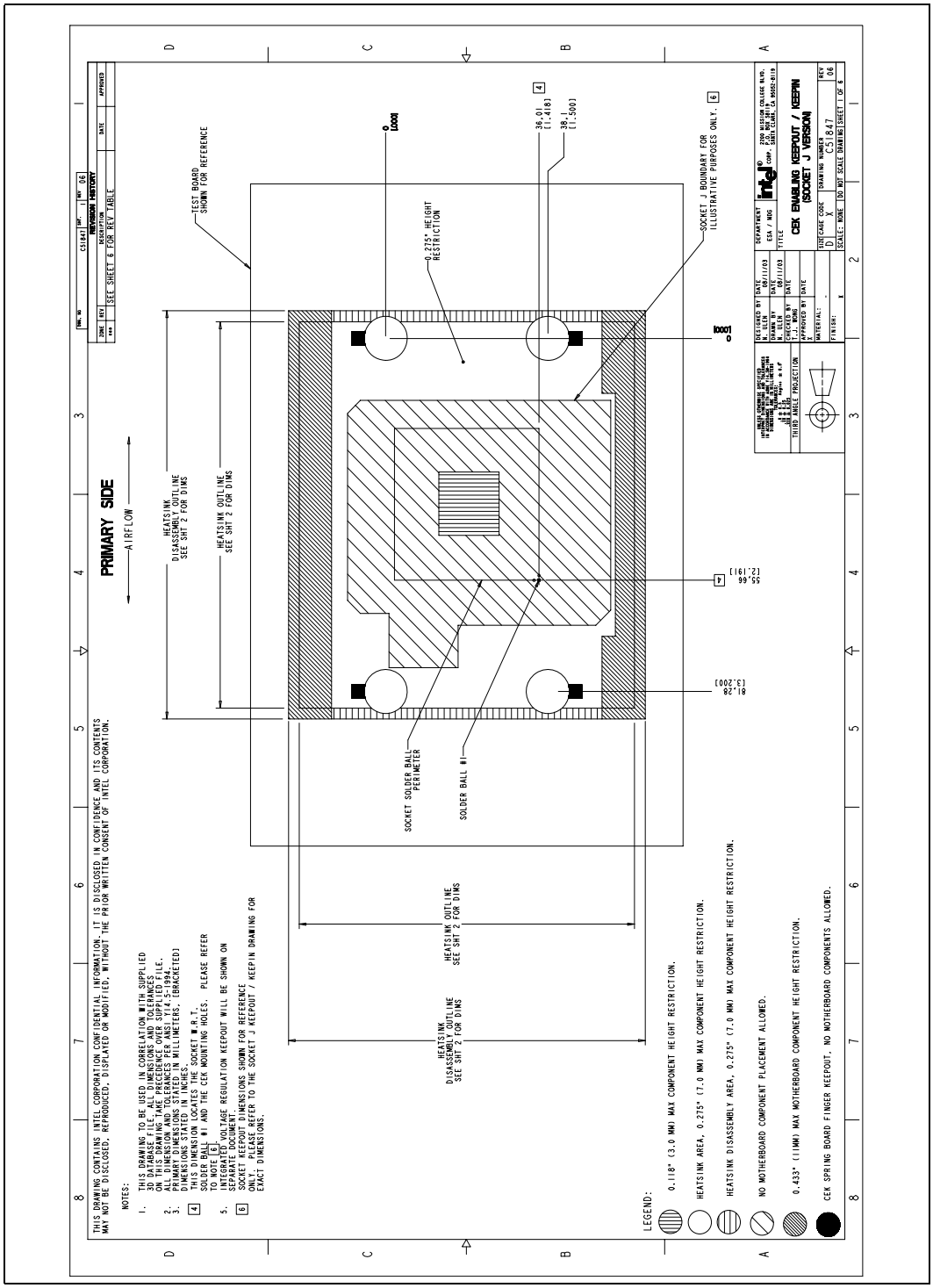


Figure 8-5. Top Side Board Keep-Out Zones (Part 2)

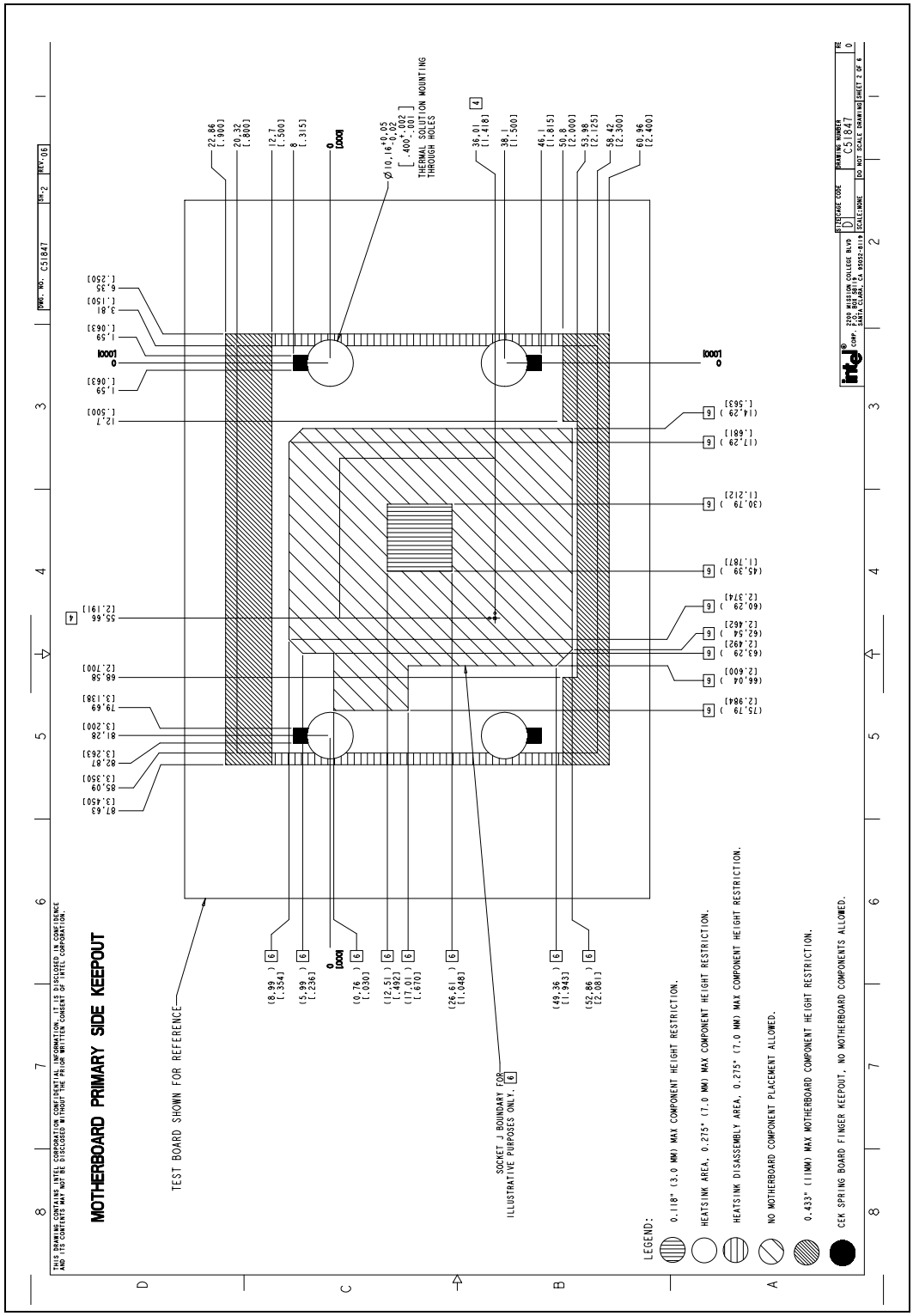


Figure 8-6. Bottom Side Board Keep-Out Zones

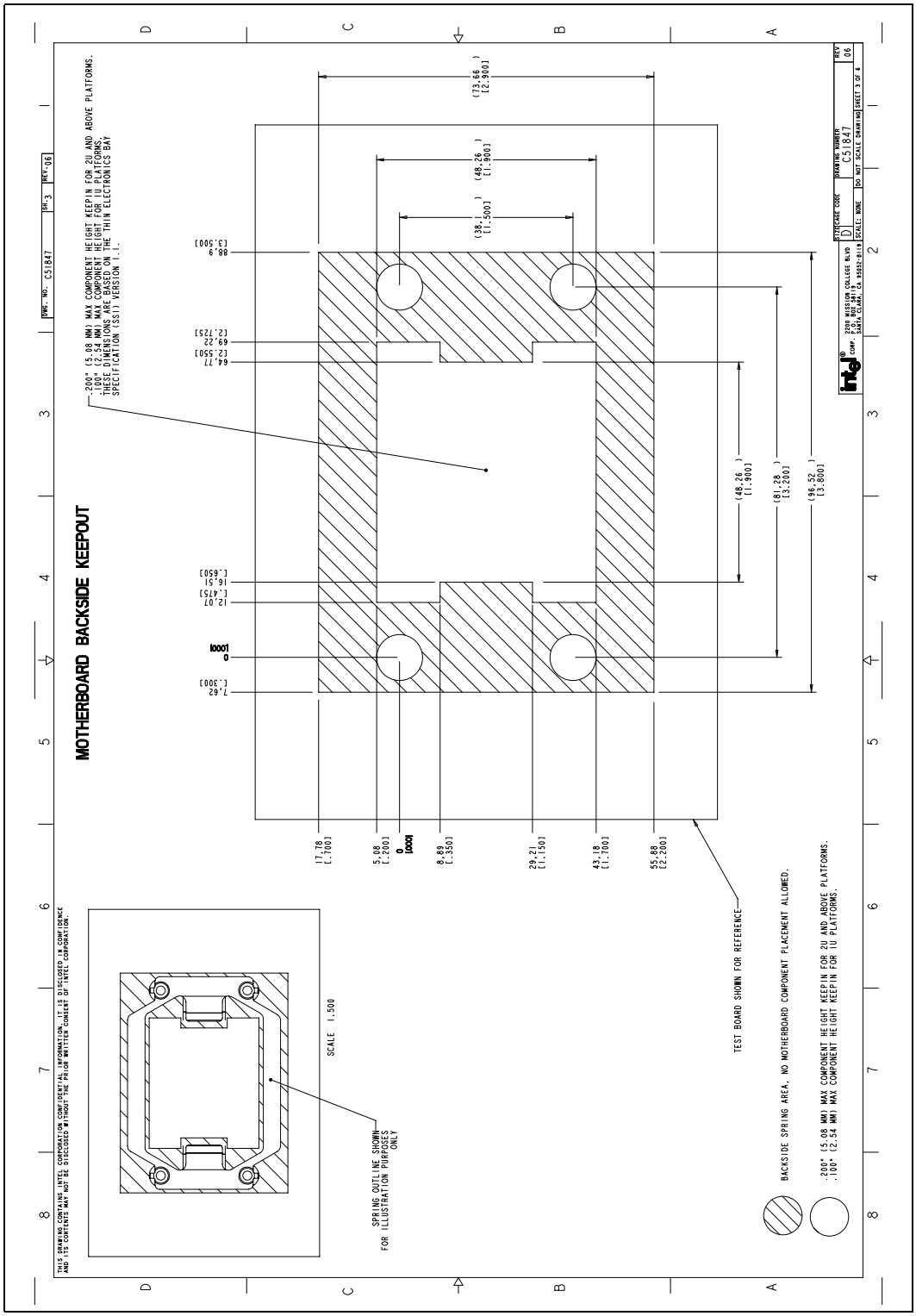


Figure 8-7. Board Mounting Hole Keep-Out Zones

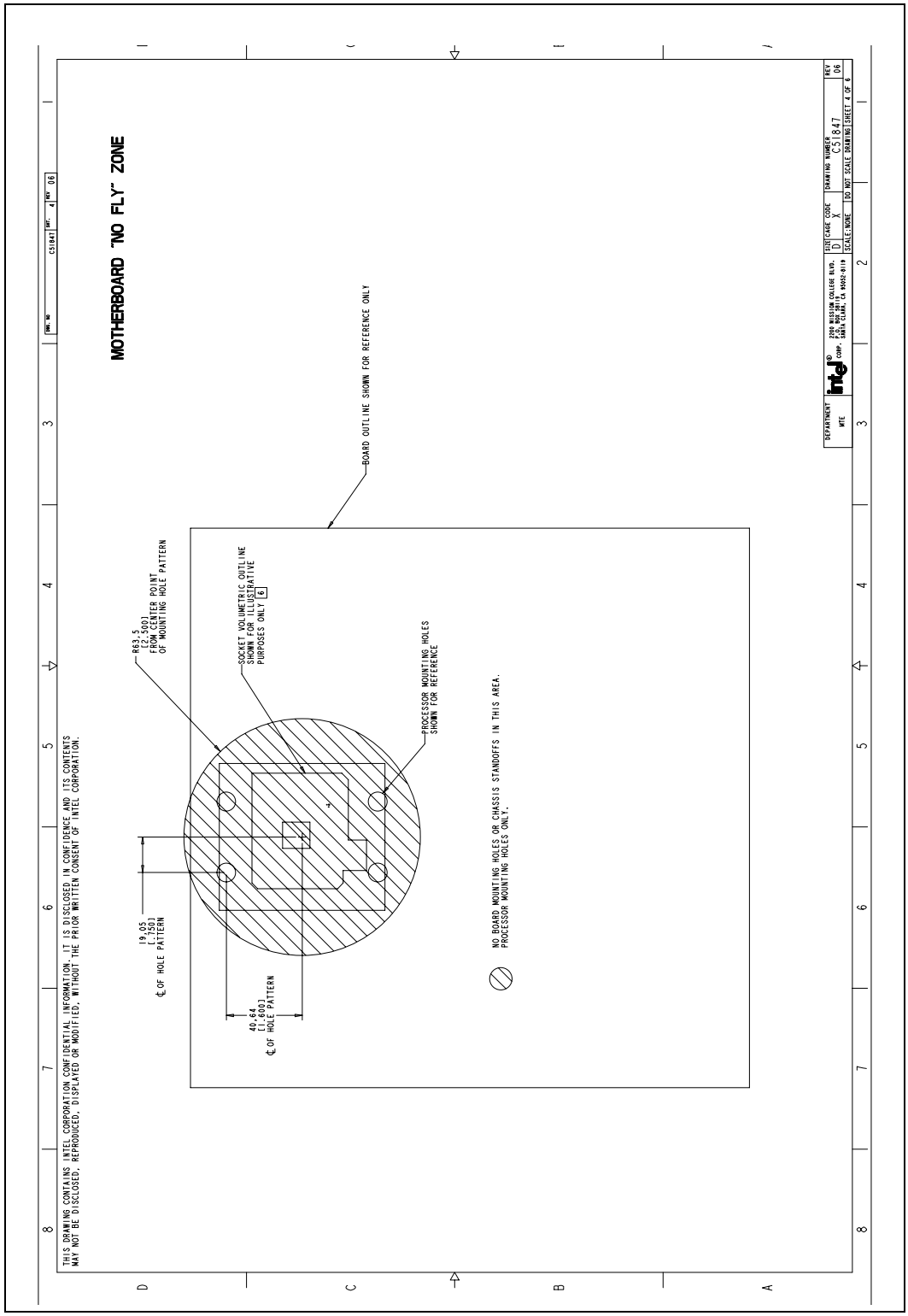


Figure 8-8. Volumetric Height Keep-Ins

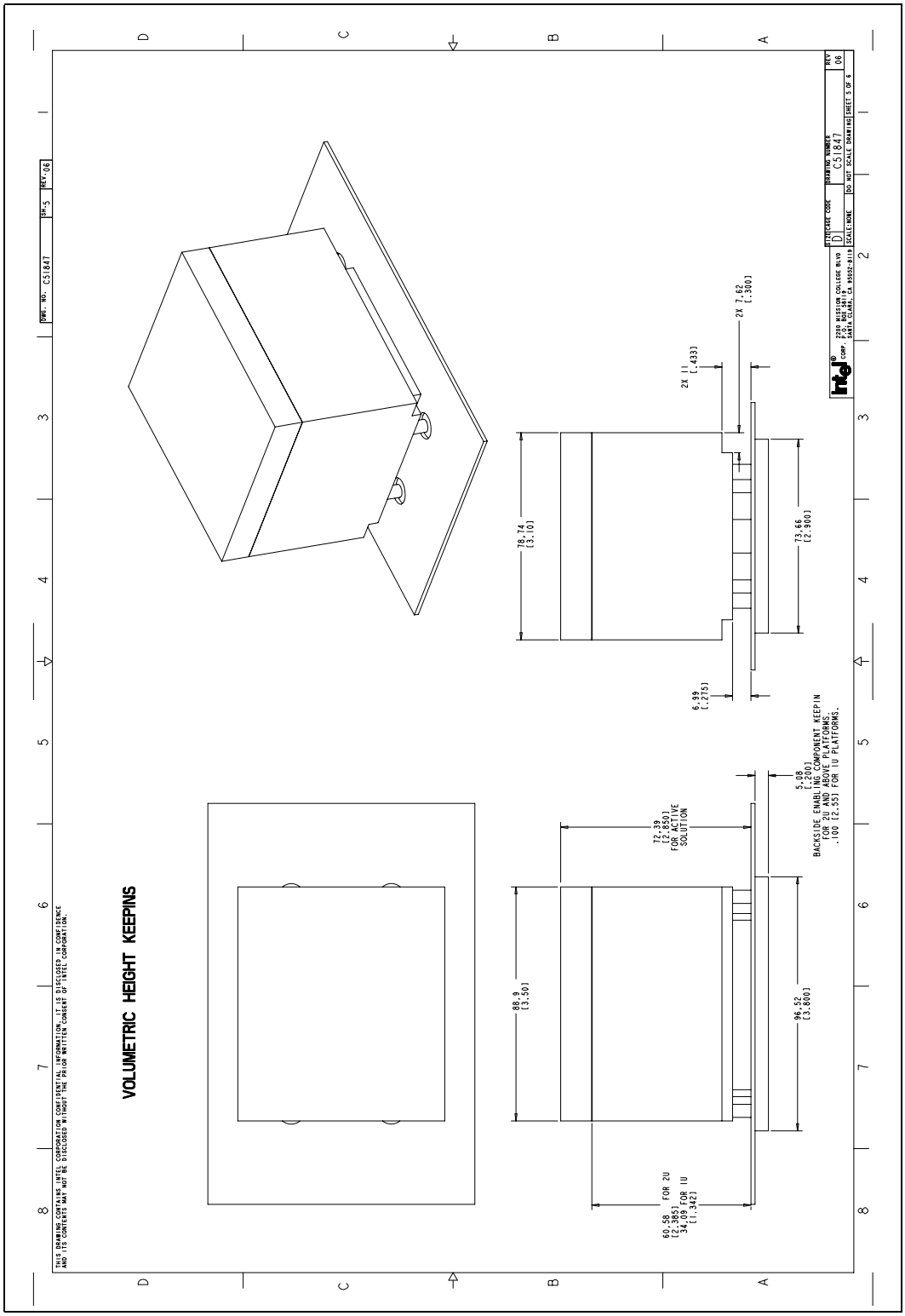


Figure 8-9. 4-Pin Fan Cable Connector (For Active CEK Heat Sink)

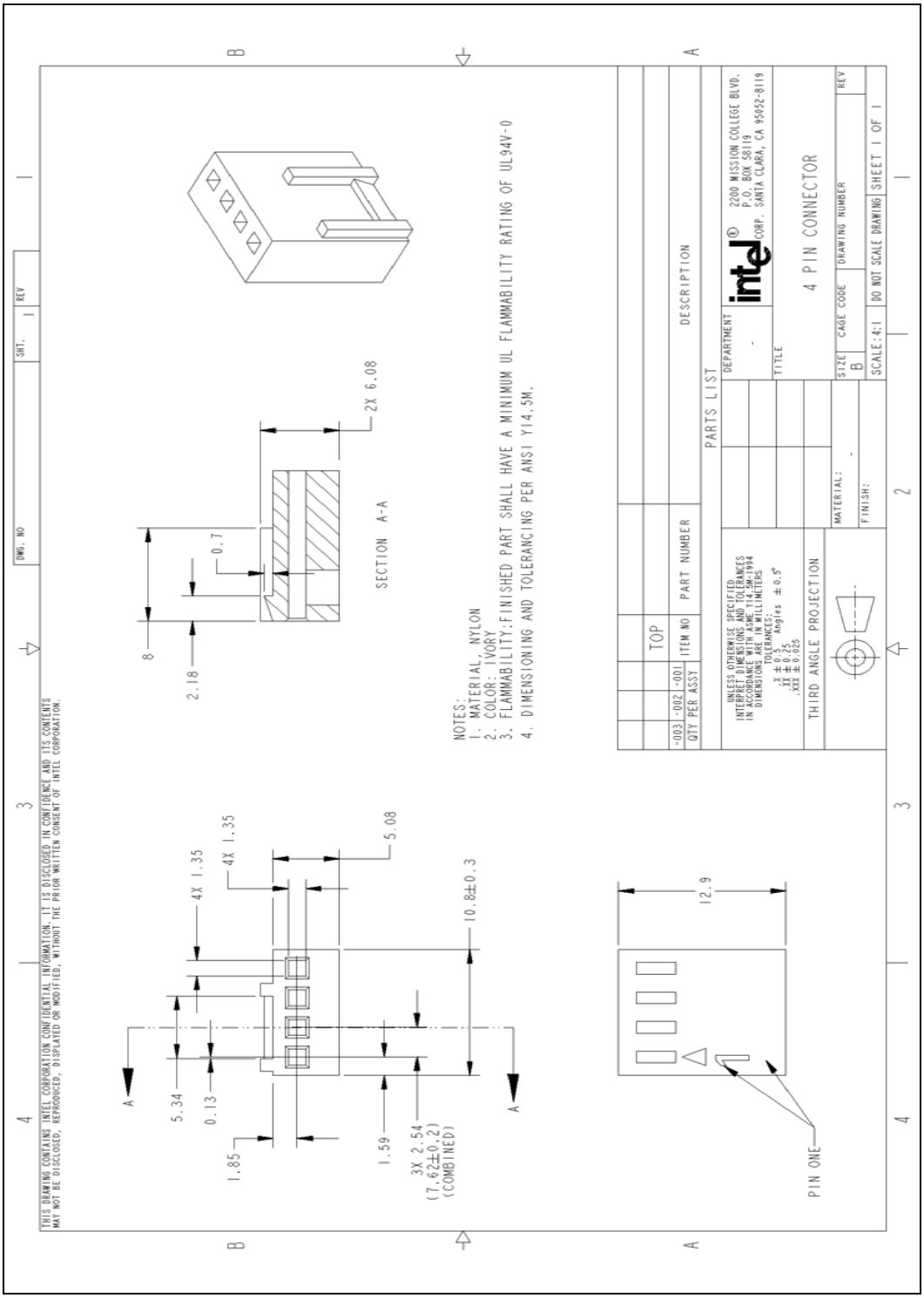
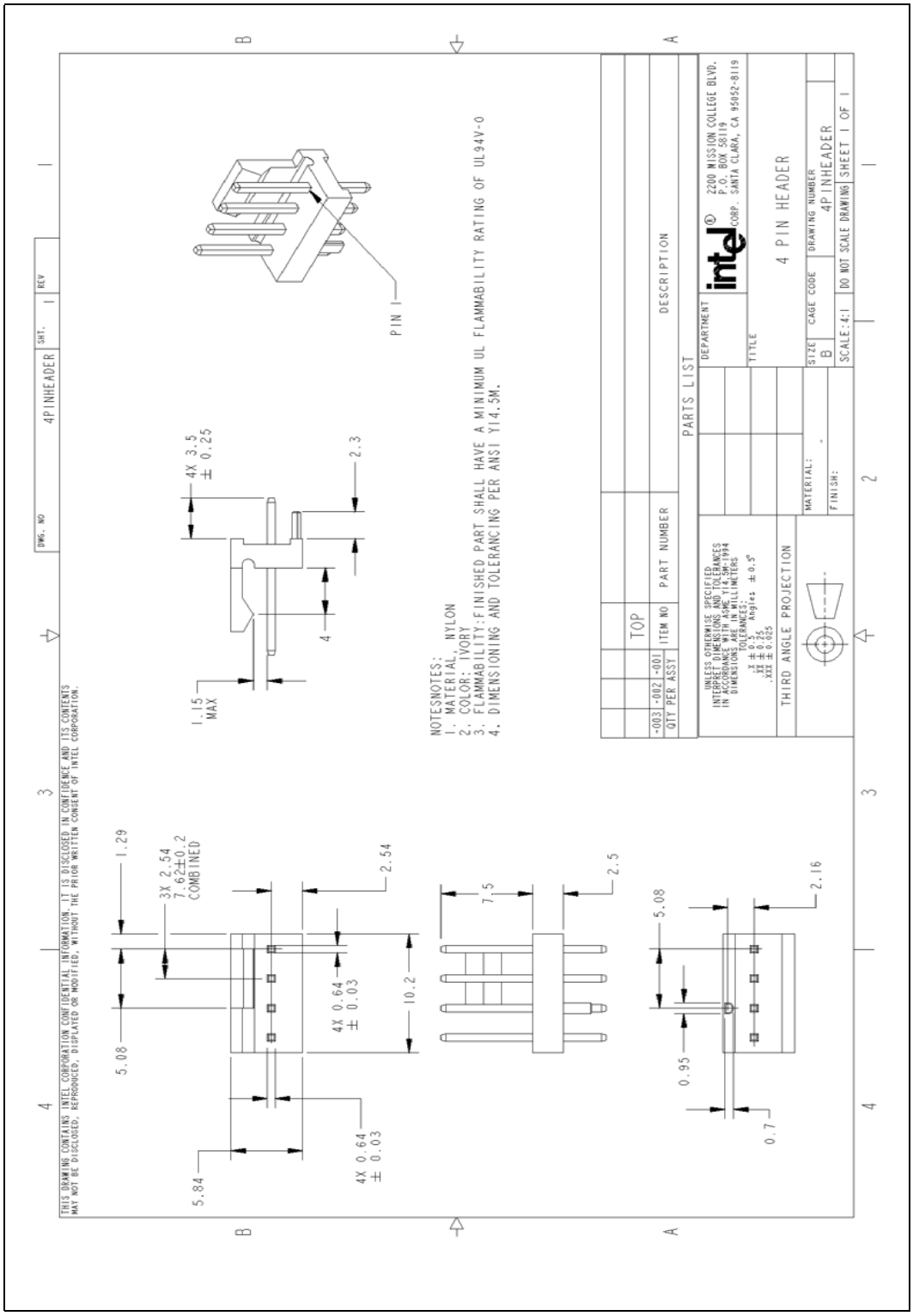


Figure 8-10. 4-Pin Base Board Fan Header (For Active CEK Heat Sink)



8.2.2 Boxed Processor Heat Sink Weight

8.2.2.1 Thermal Solution Weight

The 1U passive/2U active combination heat sink solution and the 2U passive heat sink solution will not exceed a mass of 1050 grams. Note that this is per processor, so a dual processor system will have up to 2100 grams total mass in the heat sinks. This large mass will require a minimum chassis stiffness to be met in order to withstand force during shock and vibration.

See Section 3 for details on the processor weight.

8.2.3 Boxed Processor Retention Mechanism and Heat Sink Support (CEK)

Baseboards and chassis designed for use by a system integrator should include holes that are in proper alignment with each other to support the boxed processor. Refer to the *Server System Infrastructure Specification (SSI-EEB 3.6, TEB 2.1 or CEB 1.1).* These specification can be found at: http://www.ssiforum.org.

Figure 8-3 illustrates the Common Enabling Kit (CEK) retention solution. The CEK is designed to extend air-cooling capability through the use of larger heat sinks with minimal airflow blockage and bypass. CEK retention mechanisms can allow the use of much heavier heat sink masses compared to legacy limits by using a load path directly attached to the chassis pan. The CEK spring on the secondary side of the baseboard provides the necessary compressive load for the thermal interface material. The baseboard is intended to be isolated such that the dynamic loads from the heat sink are transferred to the chassis pan via the stiff screws and standoffs. The retention scheme reduces the risk of package pullout and solder joint failures.

All components of the CEK heat sink solution will be captive to the heat sink and will only require a Phillips screwdriver to attach to the chassis pan. When installing the CEK, the CEK screws should be tightened until they will no longer turn easily. This should represent approximately 8 inch-pounds of torque. Avoid applying more than 10 inch-pounds of torque; otherwise, damage may occur to retention mechanism components.

8.3 Electrical Requirements

8.3.1 Fan Power Supply (Active CEK)

The 4-pin PWM/T-diode controlled active thermal solution is being offered to help provide better control over pedestal chassis acoustics. This is achieved though more accurate measurement of processor die temperature through the processor's temperature diode (T-diode). Fan RPM is modulated through the use of an ASIC located on the baseboard that sends out a PWM control signal to the 4th pin of the connector labeled as *Control*. This thermal solution requires a constant +12 V supplied to pin 2 of the active thermal solution and does not support variable voltage control or 3-pin PWM control. See Table 8-2 for details on the 4-pin active heat sink solution connectors.

If the 4-pin active fan heat sink solution is connected to an older 3-pin baseboard CPU fan header it will default back to a thermistor controlled mode, allowing compatibility with legacy 3-wire designs. When operating in thermistor controlled mode, fan RPM is automatically varied based on the T_{INLET} temperature measured by a thermistor located at the fan inlet of the heat sink solution.

The fan power header on the baseboard must be positioned to allow the fan heat sink power cable to reach it. The fan power header identification and location must be documented in the suppliers platform documentation, or on the baseboard itself. The baseboard fan power header should be positioned within 177.8 mm [7 in.] from the center of the processor socket.

Table 8-1. PWM Fan Frequency Specifications for 4-Pin Active CEK Thermal Solution

Description	Min Frequency	Nominal Frequency	Max Frequency	Unit
PWM Control Frequency Range	21,000	25,000	28,000	Hz

Table 8-2. Fan Specifications for 4-pin Active CEK Thermal Solution

Description	Min	Typ Steady	Max Steady	Max Startup	Unit
+12 V: 12 volt fan power supply	10.8	12	12	13.2	V
IC: Fan Current Draw	N/A	1	1.25	1.5	A
SENSE: SENSE frequency	2	2	2	2	Pulses per fan revolution

Figure 8-11. Fan Cable Connector Pin Out for 4-Pin Active CEK Thermal Solution

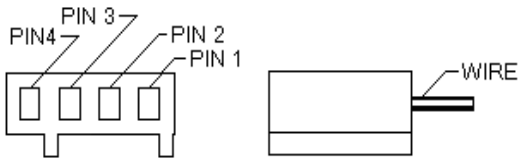


Table 8-3. Fan Cable Connector Pin Out for 4-Pin Active CEK Thermal Solution

Pin Number	Signal	Color
1	Ground	Black
2	**Power:** (+12 V)	Yellow
3	**Sense:** 2 pulses per revolution	Green
4	**Control:** 21 KHz-28 KHz	Blue

8.3.2 Boxed Processor Cooling Requirements

As previously stated the boxed processor will be available in two product configurations. Each configuration will require unique design considerations. Meeting the processor's temperature specifications is also the function of the thermal design of the entire system, and ultimately the responsibility of the system integrator. The processor temperature specifications are found in Chapter 6, "Thermal Specifications" of this document.

8.3.2.1 1U Passive / 2U Active Combination Heat Sink Solution (1U Rack Passive)

In the 1U configuration it is assumed that a chassis duct will be implemented to provide sufficient airflow to pass through the heat sink fins. Currently the actual airflow target is within the range of 15-27 CFM. The duct should be designed as precisely as possible and should not allow any air to bypass the heat sink (0" bypass) and a back pressure of 0.38 in. H_2O. It is assumed that a 40°C T_{LA} is met. This requires a superior chassis design to limit the T_{RISE} at or below 5°C with an external ambient temperature of 35°C. Following these guidelines will allow the designer to meet Thermal Profile B and conform to the thermal requirements of the processor.

8.3.2.2 1U Passive / 2U Active Combination Heat Sink Solution (Pedestal Active)

The active configuration of the combination solution is designed to help pedestal chassis users to meet the thermal processor requirements without the use of chassis ducting. It may be still be necessary to implement some form of chassis air guide or air duct to meet the T_{LA} temperature of 40°C depending on the pedestal chassis layout. Also, while the active thermal solution is designed to mechanically fit into a 2U volumetric, it may require additional space at the top of the thermal solution to allow sufficient airflow into the heat sink fan. Therefore, additional design criteria may need to be considered if this thermal solution is used in a 2U rack mount chassis, or in a chassis that has drive bay obstructions above the inlet to the fan heat sink. Use of the active configuration in rackmount chassis is not recommended.

It is recommended that the ambient air temperature outside of the chassis be kept at or below 35°C. The air passing directly over the processor thermal solution should not be preheated by other system components. Meeting the processor's temperature specification is the responsibility of the system integrator.

8.3.2.3 2U Passive Heat Sink Solution (2U+ Rack or Pedestal)

A chassis duct is required for the 2U passive heat sink. In this configuration the thermal profile (see Section 6) should be followed by supplying 27 CFM of airflow through the fins of the heat sink with a 0" or no duct bypass and a back pressure of 0.182 in. H_2O. The T_{LA} temperature of 40°C should be met. This may require the use of superior design techniques to keep T_{RISE} at or below 5°C based on an ambient external temperature of 35°C.

8.4 Boxed Processor Contents

A direct chassis attach method must be used to avoid problems related to shock and vibration, due to the weight of the thermal solution required to cool the processor. The board must not bend beyond specification in order to avoid damage. The boxed processor contains the components necessary to solve both issues. The boxed processor will include the following items:

- Dual-Core Intel Xeon Processor 5000 series
- Unattached Heat Sink Solution
- 4 screws, 4 springs, and 4 heat sink standoffs (all captive to the heat sink)
- Thermal Interface Material (pre-applied on heat sink)
- Installation Manual
- Intel Branding Logo

The other items listed in Figure 8-3 that are required to compete this solution will be shipped with either the chassis or boards. They are as follows:

- CEK Spring (supplied by baseboard vendors)
- Heat sink standoffs (supplied by chassis vendors)

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9 Debug Tools Specifications

Please refer to the *eXtended Debug Port: Debug Port Design Guide for UP and DP Platforms* and the appropriate platform design guidelines for information regarding debug tool specifications. Section 1.3 provides collateral details.

9.1 Debug Port System Requirements

The Dual-Core Intel Xeon Processor 5000 series debug port is the command and control interface for the In-Target Probe (ITP) debugger. The ITP enables run-time control of the processors for system debug. The debug port, which is connected to the FSB, is a combination of the system, JTAG and execution signals. There are several mechanical, electrical and functional constraints on the debug port that must be followed. The mechanical constraint requires the debug port connector to be installed in the system with adequate physical clearance. Electrical constraints exist due to the mixed high and low speed signals of the debug port for the processor. While the JTAG signals operate at a maximum of 75 MHz, the execution signals operate at the common clock FSB frequency. The functional constraint requires the debug port to use the JTAG system via a handshake and multiplexing scheme.

In general, the information in this chapter may be used as a basis for including all run-control tools in Dual-Core Intel Xeon Processor 5000 series-based system designs, including tools from vendors other than Intel.

Note: The debug port and JTAG signal chain must be designed into the processor board to utilize the XDP for debug purposes except for interposer solutions.

9.2 Target System Implementation

9.2.1 System Implementation

Specific connectivity and layout guidelines for the Debug Port are provided in the *eXtended Debug Port: Debug Port Design Guide for UP and DP Platforms* and the appropriate platform design guidelines.

9.3 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging Dual-Core Intel Xeon Processor 5000 series systems. Tektronix and Agilent should be contacted to obtain specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of Dual-Core Intel Xeon Processor 5000 series-based multiprocessor systems, the LAI is critical in providing the ability to probe and capture FSB signals. There are two sets of considerations to keep in mind when designing a Dual-Core Intel Xeon Processor 5000 series-based system that can make use of an LAI: mechanical and electrical.

9.3.1 Mechanical Considerations

The LAI is installed between the processor socket and the processor. The LAI plugs into the socket, while the processor plugs into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. Note that it is possible that the keepout volume reserved for the LAI may include differerent requirements from the space normally occupied by the heatsink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

9.3.2 Electrical Considerations

The LAI will also affect the electrical performance of the FSB, therefore it is critical to obtain electrical load models from each of the logic analyzer vendors to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.

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