Am29CPL154H-25/30

CMOS 512-Word Field-Programmable Controller (FPC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Implements complex state machines**
- **High-speed, low-power CMOS EPROM technology**
- **Functional upgrade from the Am29CPL151**
- **Eight conditional inputs (each can be registered as a programmable option), 16 outputs**
- **Up to 30-MHz maximum frequency**
- **512-word by 36-bit CMOS EPROM**
- **Space-saving 28-pin OTP plastic SKINNYDIP® and PLCC packages and windowed ceramic SKINNYDIP package**
- **28 instructions**
  - Conditional branching, conditional looping, conditional subroutine call, multiway branch

GENERAL DESCRIPTION

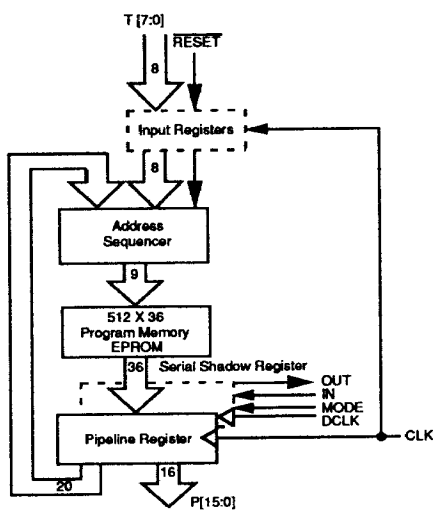
The Am29CPL154 is a CMOS, single-chip Field Programmable Controller (FPC). It allows implementation of complex state machines and controllers by programming the appropriate sequence of instructions. Jumps, loops, and subroutine calls, conditionally executed based on the test inputs, provide the designer with powerful control flow primitives.

Intelligent control may be distributed throughout the system by using FPCs to control various self-contained functional units, such as register file/ALU, I/O, interrupt, diagnostic, and bus control units. An address sequencer, the heart of the FPC, provides the address to an internal 512-word by 36-bit EPROM.

The Am29CPL154 is manufactured in CMOS technology and offers a space-saving 300-mil SKINNYDIP package. A pin-compatible smaller FPC is offered as the Am29CPL151 with a 64 x 32 memory.

This UV-erasable and reprogrammable device utilizes proven floating-gate CMOS EPROM technology to ensure high reliability, easy programming, and better than 99.9% programming yields. The Am29CPL154 is offered in both windowed and One-Time Programmable (OTP) packages. OTP plastic SKINNYDIP and PLCC devices are ideal for volume production.

SIMPLIFIED BLOCK DIAGRAM



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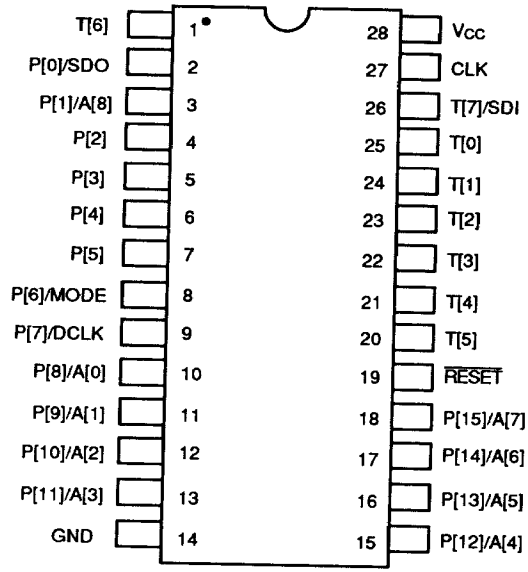
CONNECTION DIAGRAMS
Top View

SKINNYDIP



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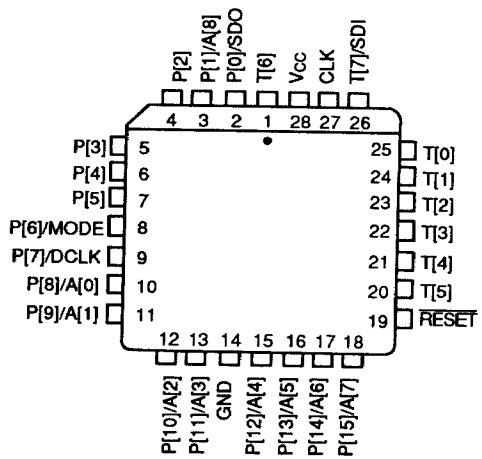
PLCC/LCC



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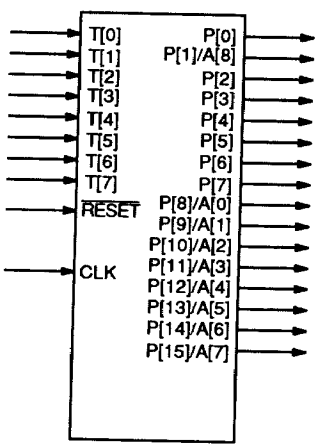
Note:
Pin 1 is marked for orientation.

LOGIC SYMBOLS

Normal Configuration



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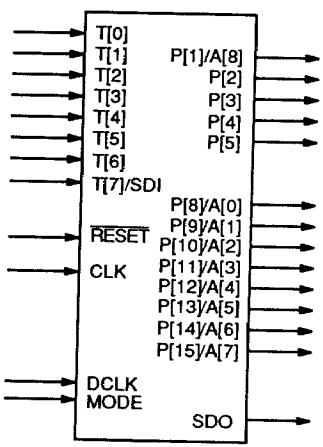
SSR® Diagnostics Configuration



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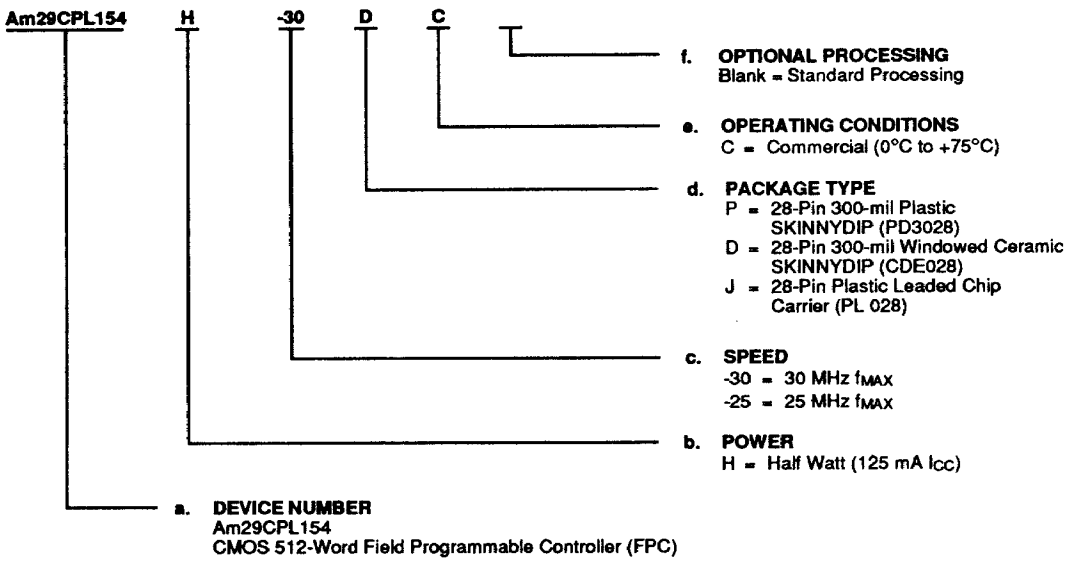
ORDERING INFORMATION
Commercial Products

AMD products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Power
c. Speed
d. Package Type
e. Operating Conditions
f. Optional Processing



Valid Combinations	
Am29CPL154H-30	PC, DC, JC
Am29CPL154H-25	

Valid Combinations

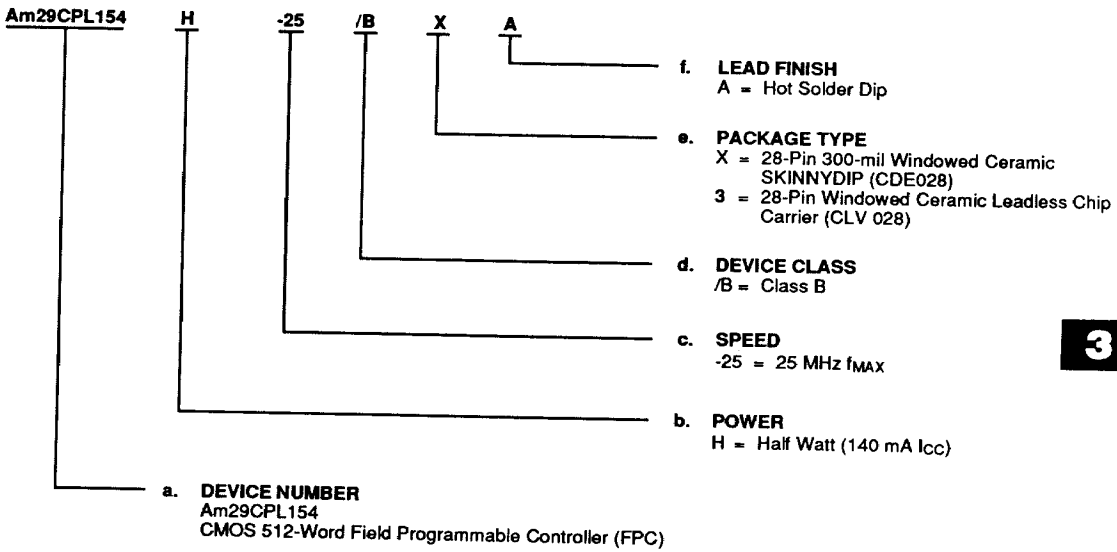
The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.

ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Power**
c. **Speed**
d. **Device Class**
e. **Package Type**
f. **Lead Finish**



Valid Combinations	
Am29CPL154H-25	/BXA, /B3A

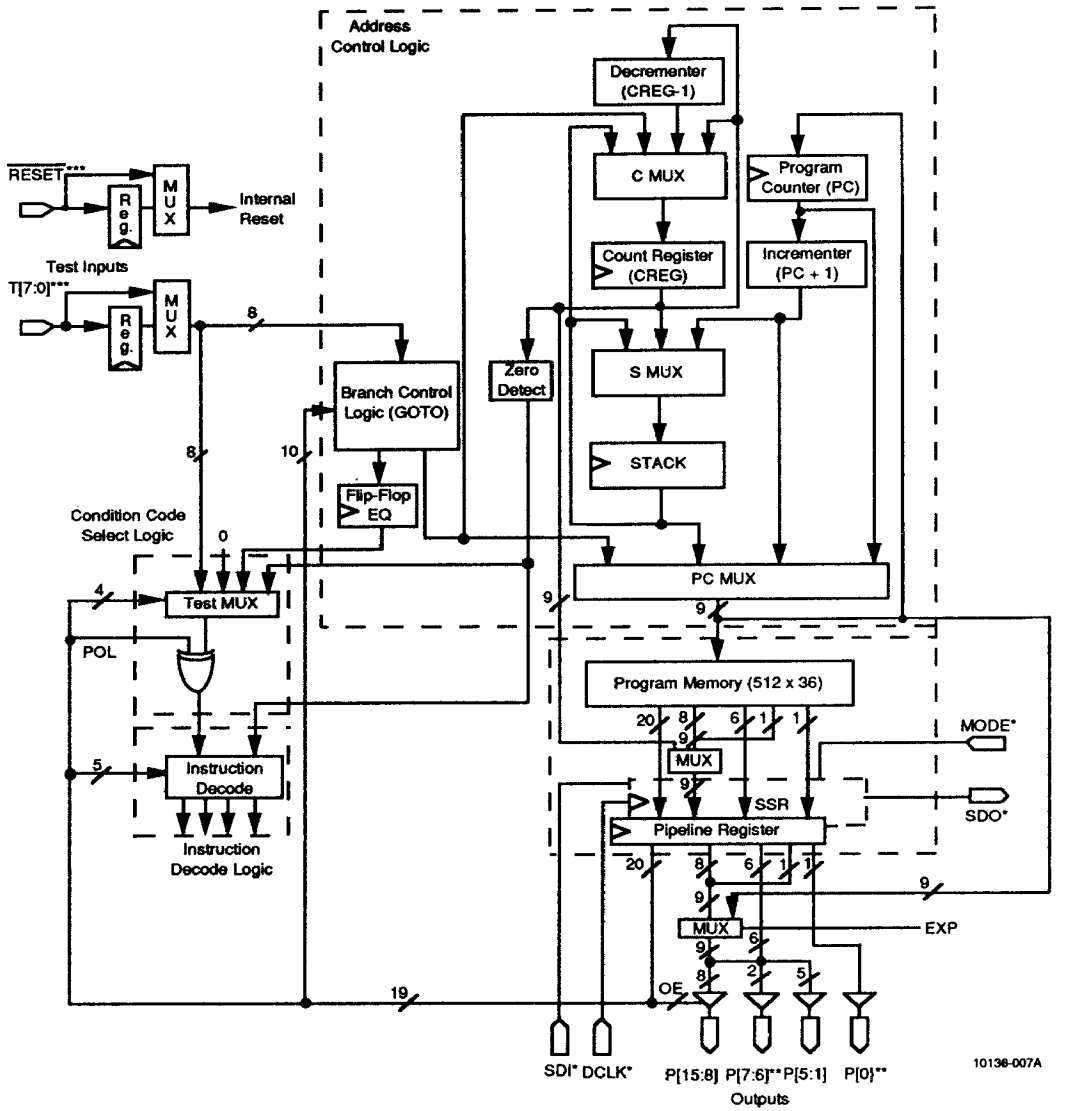
Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.

Group A Tests

Group A tests consists of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.



* These pins available only in SSR mode.
** These pins available only in normal mode.
*** Each of the T[7:0] and $\overline{\text{RESET}}$ inputs can be individually registered or left unregistered as a programmable option.

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Figure 1. Am29CPL154 Detailed Block Diagram

PIN DESCRIPTION

CLK
Clock Input

The rising edge of the clock latches the program counter, count register (CREG), subroutine register (SREG), pipeline register, and EQ flag. The rising edge of the clock also latches the test input registers and the $\overline{\text{RESET}}$ register if their respective configuration bits are set to enable internal synchronizing registers.

P[15:8]/A[7:0]
Outputs

The upper eight general-purpose control outputs are enabled by the OE signal from the pipeline register. When OE is HIGH, P[15:8] are enabled and when LOW, P[15:8] are disabled.

A controller Expansion (EXP) cell can be programmed to set pins P[1] and P[15:8] to output the program address A[8] and A[7:0] from the PC MUX. These can be used to address external registered memories to provide more control outputs.

The contents of the internal count register (CREG) can also be routed to the control output pins P[1] and P[15:8], using the OUTPUT instruction. Thus, the control outputs can be changed dynamically.

P[7:0] [DCLK, MODE, SDO]
Outputs

The lower eight general-purpose control outputs are permanently enabled. In the SSR diagnostic configuration, P[7] becomes the diagnostic clock input DCLK, P[6] becomes the diagnostic control input MODE, and P[0] becomes the serial Data Output [SDO].

$\overline{\text{RESET}}$
Optionally Registered $\overline{\text{Reset}}$ Input; Active LOW

When the reset input is LOW, the output of the PC MUX is forced to the uppermost program address (511). On the next rising edge of the clock, this address (511) is loaded into the program counter; the instruction at location 511 is loaded into the pipeline register, and the EQ flag is cleared. A programmable configuration bit allows the option of making this a registered input. If $\overline{\text{RESET}}$ is internally registered, the first rising edge of the clock latches it. On the next rising edge of the clock, the EQ flip-flop is cleared and the contents of memory location 511 are loaded into the pipeline register. The default state of this input is registered.

T[7:0] [SDI]
Optionally Registered Test Inputs

In conditional instructions, the TEST inputs can be used as individual condition codes selected by the TEST field in the pipeline register. The T[7:0] inputs can also be used as a branch address when performing a program branch or as a count value to be loaded into the CREG. When this is done, a ninth bit from the microword is added as the MSB of the test inputs to yield a nine-bit value. Each of these inputs has an EPROM bit associated with it. This bit may be programmed such that the corresponding input becomes an unregistered input. The default state of these inputs is registered. In SSR diagnostics mode, T[7] becomes the Serial Data Input (SDI).

FUNCTIONAL DESCRIPTION

Figure 1, the detailed block diagram of the Am29CPL154, shows logic blocks and interconnecting buses that permit parallel performance of different operations in a single instruction. The FPC consists of four main logic blocks: the program memory, address control logic, condition code selection logic, and instruction decode. A fifth optional block is the Serial Shadow Register (SSR).

The program memory contains the user-defined instruction flow and output sequence. The address control logic addresses the program memory. This control logic supports high-level instruction functions including conditional branches, subroutine calls and returns, loops, and multiway branches. The condition code selection logic selects the condition code input to be tested when a conditional instruction is executed. The polarity of the selected condition code input is controlled by the POL bit in the microword. The instruction decode generates the control signals necessary to perform the instruction specified by the instruction part (P[35:16]) of the microword. The SSR enables in-system testing to isolate problems down to the IC level.

Program Memory

The FPC program memory is a 512-word by 36-bit EPROM with a 36-bit pipeline register at its output. The upper 20 bits (P[35:16]) of the pipeline register are internal to the FPC and form the instruction to control address sequencing. The format for instructions is: a one-bit synchronous Output Enable OE, a five-bit OPCODE, a one-bit test polarity select POL, a four-bit TEST condition select field, and a nine-bit immediate DATA field. The DATA field is used to provide branch addresses, test input masks, and counter values.

The lower 16 bits (P[15:0]) of the pipeline register are brought out as user-defined, general-purpose control outputs. The upper eight control outputs (P[15:8]) are disabled when OE is programmed as a LOW. The lower eight control bits (P[7:0]) are always enabled.

Outputs P[1] and P[15:8] will contain the next instruction address when the optional bit EXP is set. The contents of the count register are also available at P[1] and P[15:18] by using the OUTPUT instruction regardless of whether the EXP bit is set.

Controlling External PROM

By programming the EXP bit, PC MUX is output over pins P[1,15:8]/A[8:0]. This feature can be used to extend the width of the output control word when external registered memories are used. In the diagram below, the Am29CPL154 controls external registered PROMs to provide an output control word (7 + N) bits wide (where N is the bit width of the PROMs).

When the OUTPUT instruction is executed, the CREG contents are output over pins P[1], P[15:8]/A[8], A[7:0] on the following cycle. Consequently, if the CREG contents must be read after programming the EXP cell, the system design should be modified to handle this exception.

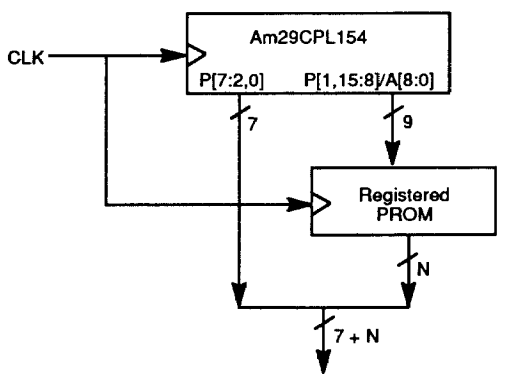

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Figure 2. Controlling External PROM

Address Control Logic

The address control logic consists of four smaller logic blocks. These are:

PC GRP – Program counter multiplexer (PCMUX), program counter register (PC) and combinatorial incrementer (PC + 1)

STACK – 17-word by 9-bit-wide stack with subroutine mux (S MUX)

CNTR – Count register (CREG) with counter mux (C MUX), combinatorial decrementer (CREG–1), and zero detect

GOTO – Multifunction branch control logic

PC GRP

The PC GRP consists of a 4:1 multiplexer, a program counter (PC) register, and a 9-bit combinatorial incrementer (PC + 1). It selects the PC, PC + 1, the branch address, or the top of stack as the next instruction address input to the program memory and the PC.

When $\overline{\text{RESET}}$ is internally registered, the first clock edge after $\overline{\text{RESET}}$ goes LOW latches $\overline{\text{RESET}}$ internally. The next clock edge loads the contents of location 511 decimal into the instruction-pipeline register and clears the EQ flag. A programmable configuration bit allows the option of bypassing the synchronizing register. In this case, after $\overline{\text{RESET}}$ goes LOW, the output of the PC MUX is forced to all "1"s (address 511 decimal) during the setup time, and the first clock edge loads the contents of location 511 decimal into the instruction-pipeline register and clears the EQ flag. Note: by default, the $\overline{\text{RESET}}$ input is registered.

STACK

This 17-deep, 9-bit-wide stack block consists of a 3:1 multiplexer (S MUX) that stores the data into the topmost location of the stack. The STACK register is incremented by one after an item is written onto the STACK (post-incremented) and decremented by one before an item is read from the STACK (pre-decremented). The S MUX chooses from three sources: PC +1 , count register, and the top of the stack (for holding). PC + 1 is the input source when doing subroutine calls. PC MUX is the output destination when a return-from-subroutine instruction is performed. The PSHCNTR and POPCNTR instructions can be used for nested counts up to the depth of the STACK. Table 1 shows how the stack operates when more than 17 values are pushed. Table 2 shows how the stack operates when more than 17 values are popped.

CNTR

The CNTR block consists of a nine-bit, four-to-one multiplexer (C MUX), driving a nine-bit register (CREG); a six-bit combinatorial decrementer (CREG-1); and a zero-detection circuit. The CNTR logic block is typically used for timing functions and iterative loop counting.

The CMUX has the following input sources: top of stack, the branch-logic output, CREG – 1, and the CREG (for holding).

GOTO

The GOTO logic block serves three functions:

1. It provides a nine-bit count value from the DATA field in the pipeline register (P[24:16]) or from the TEST inputs T[7:0] masked by the DATA field P[23:16]. This is represented by T*M.
2. It provides a branch address from the DATA field in the pipeline register P[24:16] or from the TEST inputs T[7:0] masked by the 8 LSBs of the DATA field P[23:16]. This is represented by T*M. The MSB or ninth bit of the branch address will be the MSB of the DATA field.
3. It compares T[7:0] masked by the MASK field P[23:16], called T*M, to the CONSTANT field from the pipeline register P[31:24]. If a match occurs, the EQ flip-flop is set. EQ remains unchanged if there is no match. Constant field bits that correspond to masked test bits must be zero.

The EQ flag can be tested by the condition code selection logic. Multiple tests of any group of T inputs in a manner analogous to sum-of-products can be performed since a no-match comparison does not reset the EQ flag. Any conditional branch on EQ will reset the EQ flag. Conditional returns on EQ will not change the EQ flag. $\overline{\text{RESET}}$ input LOW will reset the EQ flag.

Note: A zero in the MASK field blocks the corresponding bit in the TEST field; a one activates the corresponding bit.

The constant field bits that correspond to masked test field bits must be zero. A zero is substituted for masked test field bits. The "POL" bit is a "don't care" when using test inputs to load registers.

Note that when the inputs are internally registered (programmable option) they must meet the register setup time on the cycle preceding the one in which they are to be used.

Condition Code Selection Logic

The condition code selection logic consists of a 16:1 multiplexer. The 16 condition inputs are the eight test bits, the EQ flag, CREG ZERO status, and six UNCOND test conditions connected to zero for the unconditional mode. The TEST field in the pipeline register (P[28:25]) selects one of the 16 conditions. If one of the UNCOND is chosen, and the POL bit is a one, the instruction is executed with a "forced PASS" condition. If one of the UNCOND is chosen, and the POL bit is zero, the instruction is executed with a "forced FAIL" condition. See opcode descriptions for more details.

The polarity bit POL in the instruction allows the user to test for either a pass or fail condition. Refer to Table 3 for details.

Note that when the inputs are internally registered (programmable option) they must meet the register setup time on the cycle preceding the one in which they are to be used.

Instruction Decode

The instruction decoder is a PLA that generates the control for 28 different instructions. The decoder inputs include the OPCODE field P[34:30], the zero detection flag from the CNTR, and the selected test condition code from the condition code selection logic.

Operational Modes

The Am29CPL154 operates as a nine-bit microcontroller in normal mode, and there are several configuration bits that can be programmed to modify this normal operation. The EXP bit allows the nine program address lines from the PC MUX to be output on the output pins (P[1,15:8]) so that a user can expand the width of the control lines by using external registered memories. The SSR bit allows on-chip diagnostic capabilities for in-system testing. The remaining bits serve to individually select whether the input pins will be synchronized or not. The default setting of these bits (unprogrammed,1) will cause each pin to be synchronized, and so programming a given bit (to 0) will cause that corresponding input to become internally unsynchronized.

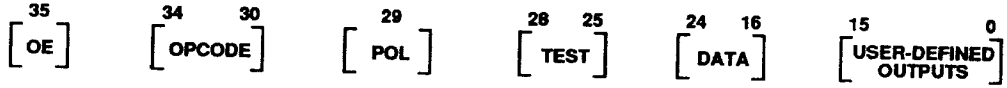
TABLE 1.

STACK LOCATION	PSH	PSH	PSH	PSH	PSH	PSH	PSH	PSH	PSH	PSH	PSH	PSH	PSH	PSH	PSH	PSH	PSH	PSH	PSH
1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
2	X	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
3	X	X	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
4	X	X	X	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
5	X	X	X	X	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
6	X	X	X	X	X	1	2	3	4	5	6	7	8	9	10	11	12	13	14
7	X	X	X	X	X	X	1	2	3	4	5	6	7	8	9	10	11	12	13
8	X	X	X	X	X	X	X	1	2	3	4	5	6	7	8	9	10	11	12
9	X	X	X	X	X	X	X	X	1	2	3	4	5	6	7	8	9	10	11
10	X	X	X	X	X	X	X	X	X	1	2	3	4	5	6	7	8	9	10
11	X	X	X	X	X	X	X	X	X	X	1	2	3	4	5	6	7	8	9
12	X	X	X	X	X	X	X	X	X	X	X	1	2	3	4	5	6	7	8
13	X	X	X	X	X	X	X	X	X	X	X	X	1	2	3	4	5	6	7
14	X	X	X	X	X	X	X	X	X	X	X	X	X	1	2	3	4	5	6
15	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	2	3	4	5
16	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	2	3	4
17	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	2	3

TABLE 2.

STACK LOCATION	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP
1	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	18	17
2	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	18	17	16
3	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	18	17	16	15
4	16	15	14	13	12	11	10	9	8	7	6	5	4	3	18	17	16	15	14
5	15	14	13	12	11	10	9	8	7	6	5	4	3	10	17	16	15	14	13
6	14	13	12	11	10	9	8	7	6	5	4	3	18	17	16	15	14	13	12
7	13	12	11	10	9	8	7	6	5	4	3	18	17	16	15	14	13	12	11
8	12	11	10	9	8	7	6	5	4	3	18	17	16	15	14	13	12	11	10
9	11	10	9	8	7	6	5	4	3	18	17	16	15	14	13	12	11	10	9
10	10	9	8	7	6	5	4	3	18	17	16	15	14	13	12	11	10	9	8
11	9	8	7	6	5	4	3	18	17	16	15	14	13	12	11	10	9	8	7
12	8	7	6	5	4	3	18	17	16	15	14	13	12	11	10	9	8	7	6
13	7	6	5	4	3	18	17	16	15	14	13	12	11	10	9	8	7	6	5
14	6	5	4	3	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4
15	5	4	3	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3
16	4	3	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	18
17	3	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	18	17

Am29CPL154 General Instruction Format



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WHERE:

OE = Synchronous Output Enable for P[15:8].
OPCODE = A five-bit opcode field for selecting one of the 27 single-data-field instructions.
POL = A one-bit test condition polarity select (refer to Table 3).
TEST = A four-bit test condition select.

TEST[28:25]	UNDER TEST
0000	T [0]
0001	T [1]
0010	T [2]
0011	T [3]
0100	T [4]
0101	T [5]
0110	T [6]
0111	T [7]
1000	EQ
1001	CREG ZERO
1010-1111	UNCONDITIONAL [0]

DATA = A nine-bit conditional branch address, test input mask, or counter value field designated as PL in instruction mnemonics.

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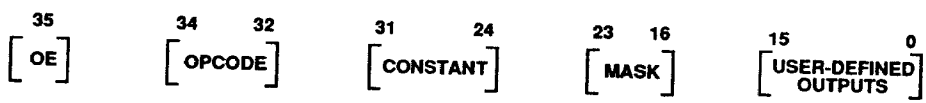
Table 3

Input Condition Being Tested	POL	Test Result
0	0	Fail
0	1	Pass
1	0	Pass
1	1	Fail

Am29CPL154 Comparison Instruction Format



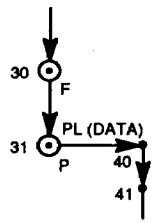
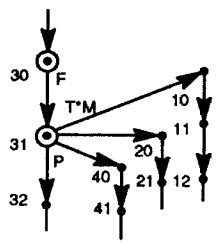
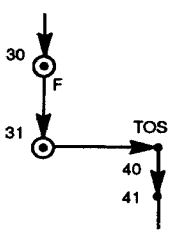
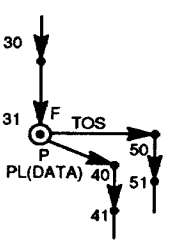
10136-009A

WHERE:

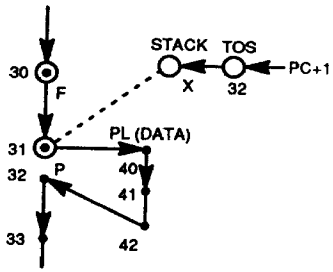
OE = Synchronous Output Enable for P[15:8].
OPCODE = Compare instruction (binary 100).
CONSTANT = An eight-bit constant for equal-to comparison with T*M.
MASK = An eight-bit mask field for masking the incoming T[7:0] inputs.

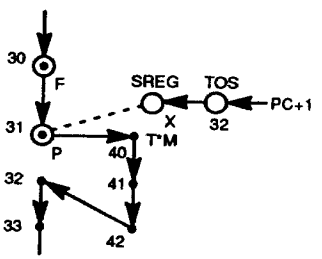
• = Other instruction
⊙ = Instruction being described
◯ = Register in part

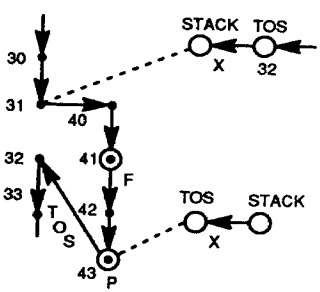
P = Test Pass
F = Test Fail
X,Y are arbitrary values in the CREG or STACK

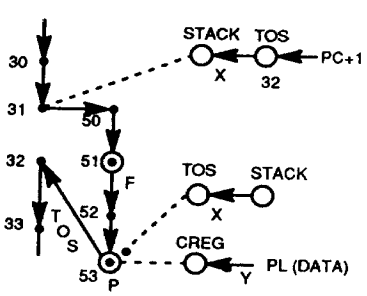
Opcode	Mnemonic	Description	Execution Example	Register Transfer Description
19	GOTOPL	**IF (cond) THEN GOTO PL (data)** Conditional branch to the address in the PL (DATA field). The EQ flag will be reset if the test field selects it and the condition passes. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.	 10135-009A	If (cond = true) Then PC = PL(data) Else PC = PC + 1
IF	GOTOTM	**IF (cond) THEN GOTO TM (data)** Conditional branch to the address defined by the T*M (T[7:0] under bitwise mask from the 8 LSBS of the DATA field). This instruction is intended for multiway branches. The EQ flag will be reset if the test field selects it and the condition passes. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0. The MSB of the branch address will be the MSB of the DATA field.	 10135-011A	If (cond = true) Then PC = T*M Else PC = PC + 1
03	GOTOSTK	**IF (cond) THEN GOTO (STACK)** Conditional branch to the address at the top of the stack, or else continue. The EQ flag will be reset if the test field selects it and the condition passes. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.	 10136-010A	If (cond = true) Then PC = TOS Else PC = PC + 1
18	FORK	**IF (cond) THEN GOTO PL (data) ELSE GOTO (STACK)** Conditional branch to the address in the PL (DATA field) or the TOS. A branch to PL is taken if the condition is true and a branch to TOS if false. The EQ flag will be reset if the test field selects it and the condition passes. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.	 10136-011A	If (cond = true) Then PC = PL(data) Else PC = TOS

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

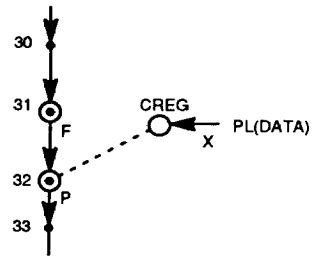
1C	CALPL	**IF (cond) THEN CALL PL (data)** Conditional jump to subroutine at the address in the PL (DATA field). The PC + 1 is pushed into the TOS as the return address. The EQ flag will be reset if the test field selects it and the condition passes. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is exe cuted with a forced FAIL condition if the test field is UNCOND and POL = 0.		If (cond = true) Then
				STACK = TOS
				TOS = PC + 1
				PC = PL(data)
				Else
				PC = PC + 1
				10136-012A

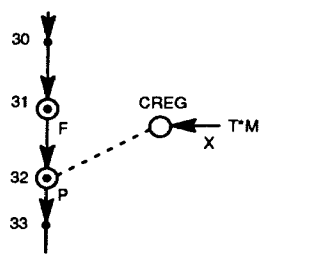
1E	CALTM	**IF (cond) THEN CALL TM (data),** Conditional jump to subroutine at the address specified by the T*M (T[7:0] under bitwise mask from the 8 LSBs of the DATA field). The PC + 1 is pushed into the TOS as the return address. The EQ flag will be reset if the test field selects it and the condition passes. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.The MSB of the branch address will be the MSB of the DATA field.		If (cond = true) Then
				STACK = TOS
				TOS = PC + 1
				PC = T*M
				Else
				PC = PC + 1
				10136-013A

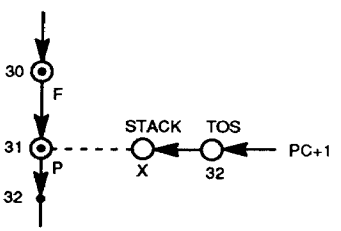
02	RET	**IF (cond) THEN RET** Conditional return from subroutine. The TOS provides the return from subroutine address and the stack is popped. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.		If (cond = true) Then
				PC = TOS
				TOS = STACK
				Else
				PC = PC + 1
				10136-014A

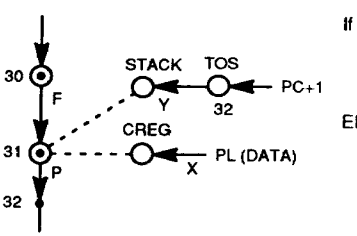
00	RETPL	**IF (cond) THEN RET, LOAD PL (data)** Conditional return from subroutine and load the CREG from the PL (DATA field). The TOS provides the return from subroutine address and the STACK is popped. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.	
			10136-015A
				If (cond = true) Then
				PC = TOS
				TOS = STACK
				CREG = PL(data)
				Else
				PC = PC + 1
				10136-015A

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

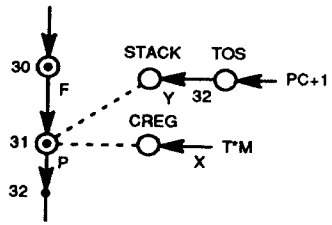
04	LDPL	**IF (cond) THEN LOAD PL (data)** Conditional load the CREG from the PL (DATA field). The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.	 10135-017A	If (cond = true) Then
				CREG = PL(data)
				PC = PC + 1
				Else
				PC = PC + 1

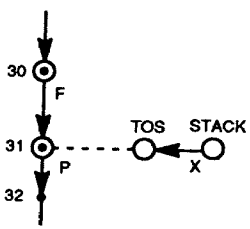
06	LDTM	**IF (cond) THEN LOAD TM (data)** Conditional load the CREG from the T*M (T[7:0] inputs under bitwise mask from the 8 LSBS of the DATA field). The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0. The MSB of the branch address will be the MSB of the DATA field.	 10135-019A	If (cond = true) Then
				CREG = T*M
				PC = PC + 1
				Else
				PC = PC + 1

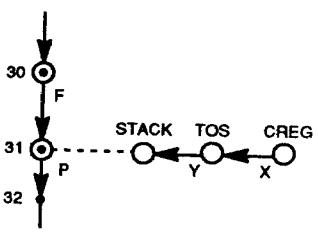
15	PSH	**IF (cond) THEN PUSH** Conditional push the PC + 1 into the TOS. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.	 10136-017A	If (cond = true) Then
				STACK = TOS
				TOS = PC + 1
				PC = PC + 1
				Else
				PC = PC + 1

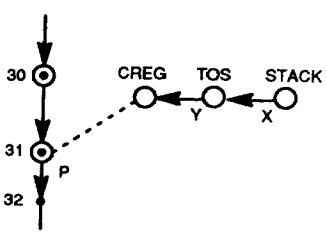
14	PSHPL	**IF (cond) THEN PUSH, LOAD PL (data)** Conditional push the PC + 1 into the TOS and load the CREG from the PL (DATA field). The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.	 10136-018A	If (cond = true) Then
				CREG = PL(data)
				STACK = TOS
				TOS = PC + 1
				PC = PC + 1
				Else
				PC = PC + 1

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

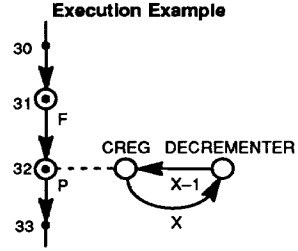
16	PSHTM	**IF (cond) THEN PUSH, LOAD TM (data)**
		Conditional push the PC + 1 into the TOS and load the CREG from the T*M (T[7:0] under bitwise mask from the 8 LSBs of the DATA field). The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0. The MSB of the branch address will be the MSB of the DATA field.
			
			10136-019A
				If (cond = true) Then
				CREG = T*M
				STACK = TOS
				TOS = PC + 1
				PC = PC + 1
				Else
				PC = PC + 1

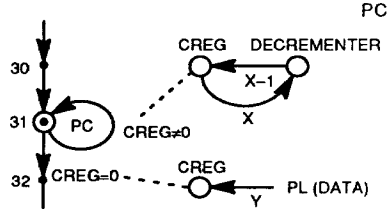
07	POP	**IF (cond) THEN POP**
		Conditional Pop the TOS. The instruction is executed with a forced PASS condition, if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition, if the test field is UNCOND and POL = 0.
			
			10136-020A
				If (cond = true) Then
				TOS = STACK
				PC = PC + 1
				Else
				PC = PC + 1

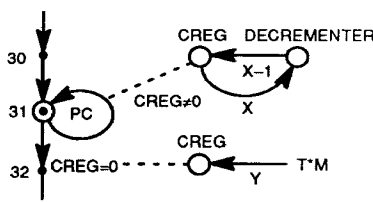
05	PSHCNTR	**IF (cond) THEN PUSH (CREG)**
		Conditional push CREG contents to top of stack. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.
			
			10136-021A
				If (cond = true) Then
				STACK = TOS
				TOS = CREG
				PC = PC + 1
				Else
				PC = PC + 1

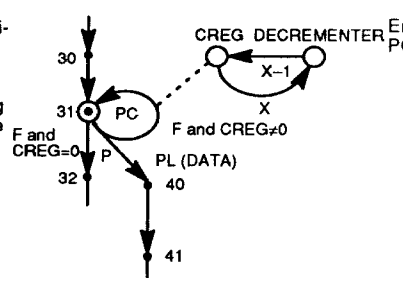
17	POPCNTR	**IF (cond) THEN POP TO (CREG)**
		Conditional pop TOS into CREG. The instruction is executed with a forced PASS condition, if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition, if the test field is UNCOND and POL = 0.
			
			10136-022A
				If (cond = true) Then
				CREG = TOS
				TOS = STACK
				PC = PC +1
				Else
				PC = PC + 1

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

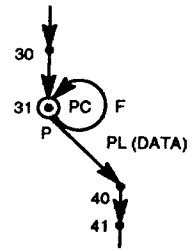
0B	DEC	**IF (cond) THEN DEC**
		Conditional decrement of the CREG. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.
			
			10135-029A
				If (cond = true) Then
				CREG = CREG –1
				PC = PC + 1
				Else
				PC = PC + 1

0C	DECPL	**WHILE (CREG < > 0) WAIT ELSE LOAD PL (data)**
		Conditional Hold until the counter is equal to zero, then load CREG from the PL (DATA field). This instruction is intended for timing waveform generation. If the CREG is not equal to zero, the same instruction is refetched while CREG is decremented. Timing is complete when the CREG is equal to zero, causing the next instruction to be fetched and the CREG to be reloaded from PL. This instruction does not depend on the pass/fail condition.
			
			10135-030A
				While (CREG < > 0)
				CREG = CREG –1
				PC = PC
				End While
				CREG = PL(data)
				PC = PC + 1

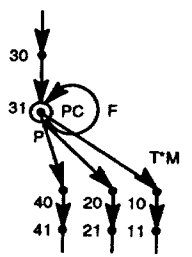
0E	DECTM	**WHILE (CREG < > 0) WAIT ELSE LOAD TM (data)**
		Conditional Hold until the counter is equal to zero, then load CREG from the T*M (T[7:0] under bitwise mask from the 8 LSBs of the DATA field). This instruction is intended for timing waveform generation. If the CREG is not equal to zero, the same instruction is refetched while the CREG is decremented. Timing is complete when the CREG is equal to zero, causing the next instruction to be fetched and the CREG to be reloaded from T*M. This instruction does not depend on the pass/fail condition. The MSB of the branch address will be the MSB of the DATA field.
			
			10135-031A
				While (CREG < > 0)
				CREG = CREG –1
				PC = PC
				End While
				CREG = T*M
				PC = PC + 1

1D	DECGOPL	**If (cond) THEN GOTO PL (data) ELSE WHILE (CREG < > 0) WAIT**
		Conditional Hold/Count. The current instruction will be refetched and the CREG decremented until the condition under test becomes true or the counter is equal to zero. If the condition becomes true, a branch to the address in the PL (DATA field) is executed. If the counter becomes zero without the condition becoming true, a CONTINUE is executed. The EQ flag will be reset if the test field selects it and the condition passes. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.
			
			10135-032A
				While (cond = false)
				If (CREG < > 0)
				CREG = CREG –1
				PC = PC
				Else
				PC = PC + 1
				End While
				PC = PL (data)

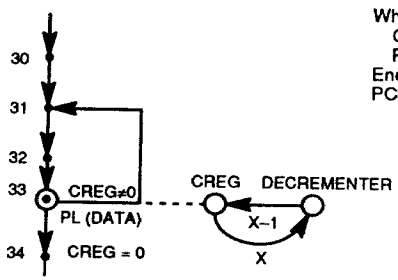
Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

1A	WAITPL	**IF (cond) THEN GOTO PL (data) ELSE WAIT**
		Conditional Hold. The current instruction will be refetched and executed until the condition under test becomes true. When true, a branch to the address in the PL (DATA field) is executed. The EQ flag will be reset if the test field selects it and the condition passes. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.
				If (cond = true) Then
				PC = PL (data)
				Else
				PC = PC

10135-033A

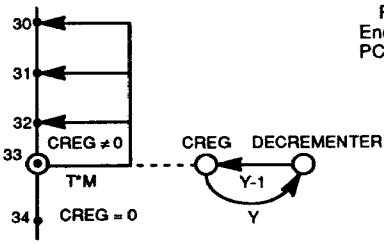
1B	WAITTM	**IF (cond) THEN GOTO TM (data), ELSE WAIT**
		Conditional Hold. The current instruction will be refetched and executed until the condition under test becomes true. When the condition is true, a branch to the T*M address (T[7:0] under bitwise mask from the eight LSBs of the DATA field) is executed. The EQ flag will be reset if the test field selects it and the condition passes. The instruction is executed with a forced PASS condition, if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition, if the test field is UNCOND and POL = 0. The MSB of the branch address will be the MSB of the DATA field.
				If (cond = true) Then
				PC = T*M
				Else
				PC = PC

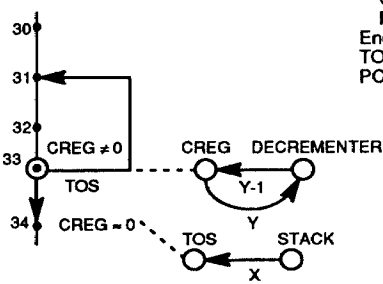
10136-023A

08	LPPL	**WHILE (CREG < > 0) LOOP TO PL (data)**
		Conditional loop to the address in the PL (DATA field). This instruction is intended to be placed at the bottom of an iterative loop. If the CREG is not equal to zero, it is decremented (signifying completion of an iteration), and a branch to the PL (DATA field) (top of the loop) is executed. If the CREG is equal to zero, looping is complete and the next sequential instruction is executed. This instruction does not depend on the pass/fail condition. The EQ flag will be reset if the test field selects it and CREG is not equal to zero.
				While (CREG < > 0)
				CREG = CREG –1
				PC = PL (data)
				End While
				PC = PC + 1

10135-034A

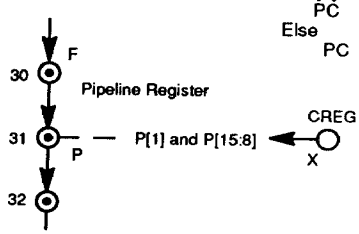
Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

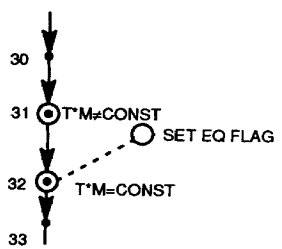
0A	LPTM	**WHILE (CREG < > 0) LOOP TO TM (data)**
		Conditional loop to the address T*M (T[7:0] under bitwise mask from the eight LSBs of the DATA field). This instruction should be placed at the bottom of an iterative loop. If CREG is not equal to zero, it is decremented (signifying completion of an iteration), and a branch to the address specified by T*M (top of the loop) is executed. If CREG is equal to zero, looping is complete and the next sequential instruction is executed. This does not depend on the pass/fail condition. The EQ flag will be reset if the test field selects it and CREG is not equal to zero. The MSB of the branch address will be the MSB of the DATA field.
			
			10136-024A
				While (CREG < > 0)
				CREG = CREG –1
				PC = T*M
				End While
				PC = PC + 1

0F	LPSTK	**WHILE (CREG < > 0) LOOP TO (STACK)**
		Conditional loop to the address in the TOS. If CREG ≠ 0, the CREG is decremened and a branch to the TOS address is executed. If the CREG = 0, looping is complete, the stack is popped, and the next sequential instruction is executed. This instruction does not depend on the pass/fail condition. The EQ flag will be reset if the test field selects it and CREG is not equal to zero.
			
			10136-025A
				While (CREG < > 0)
				CREG = CREG –1
				PC = TOS
				End While
				TOS = STACK
				PC = PC + 1

0D	CONT	**CONTINUE** The next sequential instruction is fetched unconditionally. This instruction can be used to reset the EQ flag by selecting EQ in the TEST field.	 10135-036A	PC = PC + 1

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

01	OUTPUT	**IF (cond) THEN OUTPUT**
		The CREG contents will be output on pins P[1] and P[15:8] during the next clock cycle. Care should be taken to ensure that the outputs are enabled for the next sequential instruction by setting the microcode bit OE = 1. The instruction is executed with a forced PASS condition, if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition, if the test field is UNCOND and POL = 0.
			
			10136-026A
				If (cond = ture) Then
				P[1] and P[15:8] = CREG
				PC = PC + 1
				Else
				PC = PC + 1

10–13 (100XX binary)	CMP	**CMP TM (mask) TO PL (constant)** This instruction performs bitwise Exclusive-OR of T*M (T[7:0] under bitwise mask from the MASK field) with CONSTANT (P[31:24]). If T*M equals CONSTANT, the EQ flag is set to one, which may be branched on in a following instruction. If not equal, the EQ flag is unaffected. This allows sequences of compares, in a manner analogous to sum-to-products, to be performed which can be followed by a single conditional branch if one or more of the comparisons are true. Note: The EQ flag is set to zero on reset or when EQ is selected as the test condition in a branch. Conditional returns on EQ leave the flag unchanged. Constant field bits that correspond to masked test field bits must be zero. This instruction does not depend on the pass/fail condition.	 10135-037A	Compare T*M and CONSTANT EQ = ((T [7:0] .AND. MASK) .XNOR. CONSTANT) .OR. EQ PC = PC + 1

INSTRUCTIONS BASED ON TEST CONDITIONS

Op-code	Mnemonic	Assembler Statement	Condition Pass				Condition Fail				Notes
			PC MUX	STACK	CREG	EQ FLAG	PC MUX	STACK	CREG	EQ FLAG	
00	RETPL	IF (cond) THEN RET, LOAD PL (data)	TOS	Pop	Load PL	NC	PC + 1	Hold	Hold	NC	5
01	OUTPUT	IF (cond) THEN OUTPUT	PC + 1	Hold	Hold	NC	PC + 1	Hold	Hold	NC	1
02	RET	IF (cond) THEN RET	TOS	Pop	Hold	NC	PC + 1	Hold	Hold	NC	5
03	GOTOSTK	IF (cond) THEN GOTO (STACK)	TOS	Hold	Hold	Reset	PC + 1	Hold	Hold	NC	3
04	LDPL	IF (cond) THEN LOAD PL (data)	PC + 1	Hold	Load PL	NC	PC + 1	Hold	Hold	NC	
05	PSHCNTR	IF (cond) THEN PUSH (CREG)	PC + 1	Push CREG	Hold	NC	PC + 1	Hold	Hold	NC	6
06	LDTM	IF (cond) THEN LOAD TM (data)	PC + 1	Hold	Load TM	NC	PC + 1	Hold	Hold	NC	
07	POP	IF (cond) THEN POP	PC + 1	Pop	Hold	NC	PC + 1	Hold	Hold	NC	5
0B	DEC	IF (cond) THEN DEC	PC + 1	Hold	DEC	NC	PC + 1	Hold	Hold	NC	
14	PSHPL	IF (cond) THEN PUSH, LOAD PL (data)	PC + 1	Push PC + 1	Load PL	NC	PC + 1	Hold	Hold	NC	6
15	PSH	IF (cond) THEN PUSH	PC + 1	Push PC + 1	Hold	NC	PC + 1	Hold	Hold	NC	6
16	PSHTM	IF (cond) THEN PUSH, LOAD TM (data)	PC + 1	Push PC + 1	Load TM	NC	PC + 1	Hold	Hold	NC	6
17	POPCNTR	IF (cond) THEN POP TO (CREG)	PC + 1	Pop	Load TOS	NC	PC + 1	Hold	Hold	NC	5
18	FORK	IF (cond) THEN GOTO PL (data) ELSE GOTO (STACK)	PL	Hold	Hold	Reset	TOS	Hold	Hold	NC	3
19	GOTOPL	IF (cond) THEN GOTO PL (data)	PL	Hold	Hold	Reset	PC + 1	Hold	Hold	NC	3
1A	WAITPL	IF (cond) THEN GOTO PL (data) ELSE WAIT	PL	Hold	Hold	Reset	PC	Hold	Hold	NC	3
1B	WAITTM	IF (cond) THEN GOTO TM (data), ELSE WAIT	TM	Hold	Hold	Reset	PC	Hold	Hold	NC	3
1C	CALPL	IF (cond) THEN CALL PL (data)	PL	Push PC + 1	Hold	Reset	PC + 1	Hold	Hold	NC	3,6
1E	CALTM	IF (cond) THEN CALL TM (data)	TM	Push PC + 1	Hold	Reset	PC + 1	Hold	Hold	NC	3,6
1F	GOTOTM	IF (cond) THEN GOTO TM (data)	TM	Hold	Hold	Reset	PC + 1	Hold	Hold	NC	3

Key:
- PC = Program Counter
- TOS = Top of Stack
- CREG = Counter Register
- PL = Pipeline (data) Field
- TM (data) = Test Inputs Masked by DATA Field
- TM (mask) = Test Inputs Masked by MASK Field
- DEC = Decrement
- NC = No Change

Notes:

1. If condition Passes, Output CREG contents on next clock cycle.
2. If Condition = EQ, reset EQ flag.
3. If Condition = EQ and Conditon Passes, reset EQ flag.
4. If Condition = EQ and CREG ≠ 0, reset EQ flag.
5. When Stack is popped, the next value in the Stack is transferred to TOS.
6. When Stack is pushed, TOS is transferred to next available Stack location before value is written into TOS.
7. Set EQ Flag if CONST field = T*M.

INSTRUCTIONS DEPENDENT ON CREG

			CREG = 0				CREG ≠ 0				
Op-code	Mnemonic	Assembler Statement	PC MUX	STACK	CREG	EQ FLAG	PC MUX	STACK	CREG	EQ FLAG	Notes
08	LPPL	WHILE (CREG < > 0) LOOP TO PL (data)	PC + 1	Hold	Hold	NC	PL	Hold	DEC	Reset	4
0A	LPTM	WHILE (CREG < > 0) LOOP TO TM (data)	PC + 1	Hold	Hold	NC	TM	Hold	DEC	Reset	4
0C	DECPL	WHILE (CREG < > 0) WAIT ELSE LOAD PL (data)	PC + 1	Hold	Load PL	NC	PC	Hold	DEC	NC	
0E	DECTM	WHILE (CREG < > 0) WAIT ELSE LOAD TM (data)	PC + 1	Hold	Load TM	NC	PC	Hold	DEC	NC	
0F	LPSTK	WHILE (CREG < > 0) LOOP TO (STACK)	PC + 1	Pop	Hold	NC	TOS	Hold	DEC	Reset	4

INSTRUCTIONS DEPENDENT ON TEST CONDITION AND CREG VALUE

Op-code	Mnemonic	Assembler Statement	CREG Content	PC MUX	Condition Pass			Condition Fail				Notes
					STACK	CREG	EQ FLAG	PC MUX	STACK	CREG	EQ FLAG	
1D	DECGOPL	IF (cond) THEN GOTO PL (data) ELSE WHILE (CREG < > 0) WAIT	≠ 0	PL	Hold	Hold	Reset	PC	Hold	DEC	NC	3
			= 0	PL	Hold	Hold	Reset	PC + 1	Hold	Hold	NC	

UNCONDITIONAL INSTRUCTIONS

Opcode	Mnemonic	Assembler Statement	PC MUX	STACK	CREG	EQ FLAG	Notes
0D	CONT	CONTINUE	PC + 1	Hold	Hold	NC	2
10-13 (Binary 100XX)	CMP	CMP TM (mask) TO PL (constant)	PC + 1	Hold	Hold	Set	7

Key:
- PC = Program Counter
- SREG = Stack Register
- CREG = Counter Register
- PL = Pipeline (data) Field
- TM (data) = Test Inputs Masked by DATA Field
- TM (mask) = Test Inputs Masked by MASK Field
- DEC = Decrement
- NC = No Change

Notes:

1. If condition Passes, Output CREG contents on next clock cycle.
2. If Condition = EQ, reset EQ flag.
3. If Condition = EQ and Conditon Passes, reset EQ flag.
4. If Condition = EQ and CREG ≠ 0, reset EQ flag.
5. When Stack is popped, the next value in the Stack is transferred to TOS.
6. When Stack is pushed, TOS is transferred to next available Stack location before value is written into TOS.
7. Set EQ Flag if CONST field = T*M.

Am29CPL154 SSR Diagnostics Option

As a programmable option, the Am29CPL154 FPC may be configured to contain Serial Shadow Register (SSR) diagnostics capability. SSR diagnostics is a simple, straightforward method of in-system testing to isolate problems down to the IC level.

The SSR diagnostics configuration activates a 36-bit-wide D-type register called a "shadow" register, on the pipeline register inputs. The shadow register can be serially loaded from the SDI pin, parallel loaded from the pipeline register, or held. The pipeline register can be loaded from the Program Memory in normal mode or from the shadow register during diagnostics. A redefinition of four device pins is required to control the different diagnostics functions. T[7] also functions as the Serial Data Input (SDI), P[0] becomes the Serial Data Output (SDO), P[7] becomes the diagnostic clock (DCLK), and P[6] becomes the diagnostic mode control (MODE). The various diagnostic and normal modes are shown in table 4.

Serially loading a test instruction into the shadow register and parallel loading the shadow register contents into the pipeline register forces execution of the test instruction. The test result can then be clocked into the pipeline register as in normal operation mode, parallel loaded into the shadow register, and serially shifted out for system diagnostics.

Table 4

Inputs				Outputs			Operation
SDI	MODE	DCLK	CLK	SDO	Shadow Register	Pipeline Register	
X	L	↑	H, L, ↓	S_0	$S_{i-1} \leftarrow S_i$ $S_{35} \leftarrow$ SDI	Hold	Serial Right – Shift Shadow Register
T [7] (Note 1)	L	H, L, ↓	↑	S_0	Hold	$P_i \leftarrow EPROM_i$	Normal Operation; Load Pipeline Register from EPROM
L	H	↑	H, L, ↓	L	$S_i \leftarrow P_i$	Hold	Load Shadow Register from Pipeline Register (Note 2)
X	H	H, L, ↓	↑	SDI	Hold	$P_i \leftarrow S_i$	Load Pipeline Register from Shadow Register
H	H	↑	H, L, ↓	H	Hold	Hold	Hold Shadow Register

Notes:

1. During normal operation, this pin behaves as the T[7] test input.
2. S7, S6 are undefined. S[15:8] load from the source driving pins P[15:8]. If P[35] in the microword is a ONE, S[15:8] are loaded from the pipeline register. If P[35] in the microword is a ZERO, S[15:8] are loaded from an external source.

Key: H = HIGH
L = LOW
X = Don't Care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition

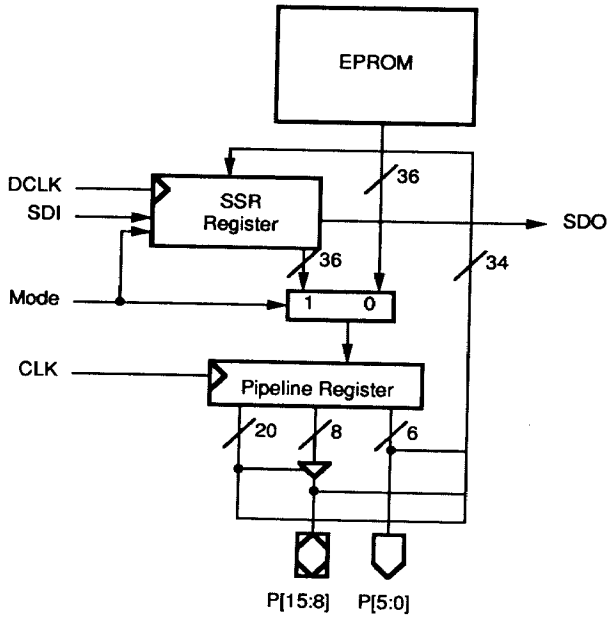


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Figure 3. SSR Diagnostics Logic

Erasure

In order to fully erase all memory locations, it is necessary to expose the memory array to a standard ultraviolet light source having a wavelength of 2537 angstroms. The minimum recommended dose (UV intensity x exposure time) is 15 Wsec/cm^2. For a UV lamp with a 12 mW/cm^2 power rating, the exposure time would be about 30 minutes. The device should be located one inch from the source in a direct line.

It should be noted that erasure will begin with exposure to light having wavelengths less than 4000 angstroms.

To prevent exposure to sunlight or fluorescent lighting, an opaque label should be affixed over the window after programming.

OTP (One-Time Programmable) Am29CPL154 devices are available in plastic and are ideal for volume production. They can be inventoried unprogrammed and used with current software revisions; there is no window to be covered to prevent light from changing data.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.3 V to V_{CC} + 0.3 V
DC Output or I/O Pin Voltage	–0.3 V to V_{CC} + 0.3 V
DC Input Current	–10 mA to +10 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.0 mA	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)				0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC} – 0.5 V, V_{CC} = Max. (Note 2)				10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0.5 V, V_{CC} = Max. (Note 2)				–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)				10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)				–10	µA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.	CMOS	V_{IN} = GND or V_{CC}		115	mA
			TTL	V_{IN} = 0.5 V or 2.4 V		125	
C_{PD}	Power Dissipation Capacitance (Note 3)	V_{CC} = Max. T_A = 25°C No Load			100 pF Typical		

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. The dynamic current consumption is:
   I_{CC} (Total) = I_{CC} (Static) + (C_{PD} + nC_L) V_{CC} (f/2), where f is the clock frequency, C_L = the output load capacitance, and n is the number of loads.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Max.	Unit
C_{IN}	Input Capacitance	$\overline{RESET}$	V_{IN} = 2.0 V	V_{CC} = 4.5 V to 5.5 V	25	pF
		Others		T_A = –55°C to +125°C	15	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	15	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Note 2)

No.	Parameter Symbol	Parameter Description		H-30 Min.	H-30 Max.	H-25 Min.	H-25 Max.	Unit
1	t_{CO}	CLK to P[15:0]			18		20	ns
2		CLK to A[8:0]			30		36	ns
3	t_S	T[7:0] to CLK, Registered		8		8		ns
4		T[7:0] to CLK, Asynchronous (Note 3)		33		40		ns
5		$\overline{RESET}$ to CLK, Registered		12		12		ns
6		$\overline{RESET}$ to CLK, Asynchronous (Note 3)		30		40		ns
7	t_H (Note 4)	CLK to T[7:0]		0		0		ns
8		CLK to $\overline{RESET}$		0		0		ns
9	t_{PZX}	CLK to P[15:8] Enable			33		40	ns
10	t_{PXZ}	CLK to P[15:8] Disable			33		40	ns
11	t_{WL}	CLK Width	LOW	14		16		ns
12	t_{WH}		HIGH	14		16		ns
13	t_P	CLK Period (Note 3)		33		40		ns
14	f_{MAX}	Maximum Frequency ($1/t_P$)		30		25		MHz

Note:

2. See Switching Test Circuit for test conditions.
3. These parameters are measured indirectly on unprogrammed devices. They are determined as follows:
   a. Measure delay from input (T[7:0], $\overline{RESET}$, or CLK) to EPROM address out in test mode. This will measure the delay through the sequence logic.
   b. Measure setup time from T[7:0] input through EPROM test columns to pipeline register in verify test column mode. This will measure the delay through the EPROM and register setup.
   c. Measure delay from T[7:0] input to EPROM address out in verify test column mode. This will measure the delay through the logic and P[15:0] outputs.

   To calculate the desired parameter measurement, the following formula is used:
   Measurement (a) + Measurement (b) – Measurement (c)

   CLK PERIOD:
   CLK (a) + (b) – (c) = CLK PERIOD
   T[7:0] to CLK setup time:
   T[7:0] (a) + (b) – (c) = T[7:0] to CLK setup time
   $\overline{RESET}$ to CLK setup time:
   $\overline{RESET}$ (a) + (b) – (c) = $\overline{RESET}$ to CLK setup time
4. These hold time parameters are tested on a sample basis.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Continued)

No.	Parameter Symbol	Parameter Description		H-30 Min.	H-30 Max.	H-25 Min.	H-25 Max.	Unit
SSR Configuration								
15	t_{PD}	Mode to SDO			25		30	ns
16		SDI to SDO			25		30	ns
17	t_{CO}	DCLK to SDO			32		36	ns
18	t_S	Mode to CLK		25		30		ns
19		Mode to DCLK		25		30		ns
20		SDI to DCLK		25		30		ns
21		P[15:8] to DCLK		25		30		ns
22	t_H	CLK to Mode		6		6		ns
23	(Note 1)	DCLK to Mode		0		0		ns
24		DCLK to SDI		0		0		ns
25		DCLK to P[15:8]		0		0		ns
26	t_{WL}	DCLK Width	LOW	20		25		ns
27	t_{WH}		HIGH	20		25		ns
28	t_P	DCLK Period		40		50		ns

Note:

1. These hold time parameters are tested on a sample basis.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.3 V to V_{CC} + 0.3 V
DC Output or I/O Pin Voltage	–0.3 V to V_{CC} + 0.3 V
DC Input Current	–10 mA to +10 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices

Ambient Temperature (T_A) Operating in Free Air	–55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = 25°C, 125°C and –55°C.

DC CHARACTERISTICS over MILITARY operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –1.0 mA	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)				0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC} – 0.5 V, V_{CC} = Max. (Note 2)				10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0.5 V, V_{CC} = Max. (Note 2)				–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)				10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)				–10	µA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.	CMOS	V_{IN} = GND or V_{CC}		130	mA
			TTL	V_{IN} = 0.5 V or 2.4 V		140	
C_{PD}	Power Dissipation Capacitance (Note 3)	V_{CC} = Max. T_A = 25°C No Load			100 pF Typical		

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. The dynamic current consumption is:
   I_{CC} (Total) = I_{CC} (Static) + (C_{PD} + nC_L) V_{CC} (f/2), where f is the clock frequency, C_L = the output load capacitance, and n is the number of loads.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Max.	Unit
C_{IN}	Input Capacitance	$\overline{RESET}$	V_{IN} = 2.0 V	V_{CC} = 4.5 V to 5.5 V	25	pF
		Others		T_A = –55°C to +125°C	15	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	15	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Note 2)

No.	Parameter Symbol	Parameter Description		H-25 Min.	H-25 Max.	Unit
1	t_{CO}	CLK to P[15:0]			25	ns
2		CLK to A[8:0]			40	ns
3	t_S	T[7:0] to CLK, Registered		10		ns
4		T[7:0] to CLK, Asynchronous (Note 3)		40		ns
5		$\overline{RESET}$ to CLK, Registered		16		ns
6		$\overline{RESET}$ to CLK, Asynchronous (Note 2)		40		ns
7	t_H	CLK to T[7:0]		0		ns
8	(Note 4)	CLK to $\overline{RESET}$		0		ns
9	t_{PZX}	CLK to P[15:8] Enable			40	ns
10	t_{PXZ}	CLK to P[15:8] Disable			35	ns
11	t_{WL}	CLK Width	LOW	20		ns
12	t_{WH}		HIGH	20		ns
13	t_P	CLK Period (Note 3)		40		ns
14	f_{MAX}	Maximum Frequency (1/t_P)		25		MHz

Note:

2. See Switching Test Circuit for test conditions.
3. These parameters are measured indirectly on unprogrammed devices. They are determined as follows:
   a. Measure delay from input (T[7:0], $\overline{RESET}$, or CLK) to EPROM address out in test mode. This will measure the delay through the sequence logic.
   b. Measure setup time from T[7:0] input through EPROM test columns to pipeline register in verify test column mode. This will measure the delay through the EPROM and register setup.
   c. Measure delay from T[7:0] input to EPROM address out in verify test column mode. This will measure the delay through the logic and P[15:0] outputs.

   To calculate the desired parameter measurement, the following formula is used:
   Measurement (a) + Measurement (b) – Measurement (c)

   CLK PERIOD:
   CLK (a) + (b) – (c) = CLK PERIOD
   T[7:0] to CLK setup time:
   T[7:0] (a) + (b) – (c) = T[7:0] to CLK setup time

   $\overline{RESET}$ to CLK setup time:
   $\overline{RESET}$ (a) + (b) – (c) = $\overline{RESET}$ to CLK setup time
4. These hold time parameters are tested on a sample basis.

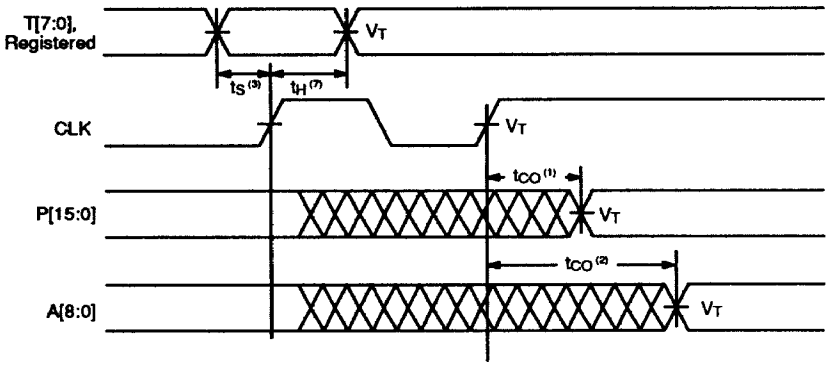
SWITCHING CHARACTERISTICS over MILITARY operating range (Continued)

No.	Parameter Symbol	Parameter Description		H-25 Min.	H-25 Max.	Unit
SSR Configuration						
15	t_{PD}	Mode to SDO			30	ns
16		SDI to SDO			30	ns
17	t_{CO}	DCLK to SDO			30	ns
18	t_S	Mode to CLK		30		ns
19		Mode to DCLK		30		ns
20		SDI to DCLK		30		ns
21		P[15:8] to DCLK		30		ns
22	t_H	CLK to Mode		6		ns
23	(Note 1)	DCLK to Mode		0		ns
24		DCLK to SDI		0		ns
25		DCLK to P[15:8]		0		ns
26	t_{WL}	DCLK Width	LOW	30		ns
27	t_{WH}		HIGH	30		ns
28	t_P	DCLK Period		60		ns

Note:

1. These hold time parameters are tested on a sample basis.

SWITCHING WAVEFORMS
Normal Configuration



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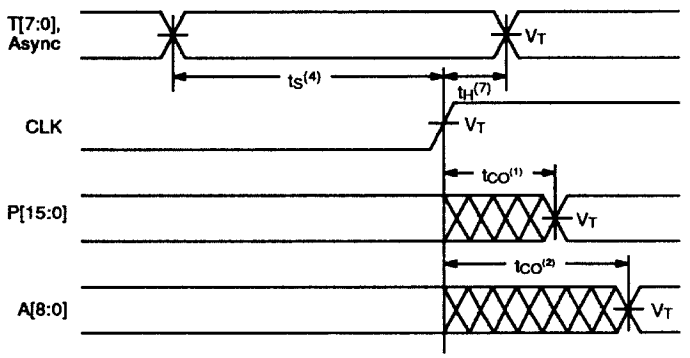
Registered Test Inputs



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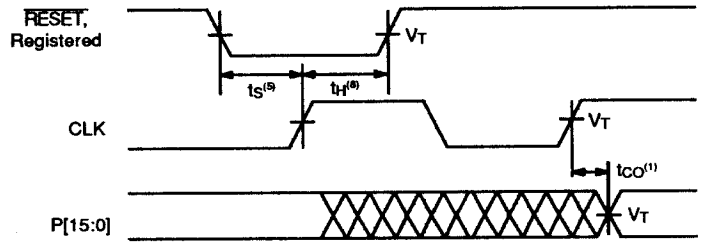
Asynchronous Test Inputs

SWITCHING WAVEFORMS (Continued)

Normal Configuration



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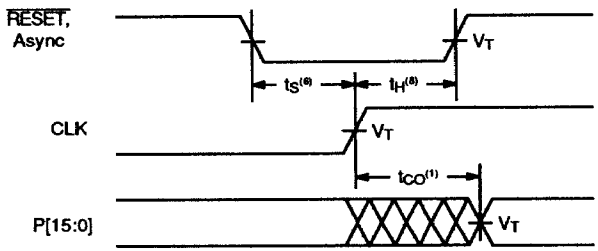
Registered $\overline{\text{RESET}}$



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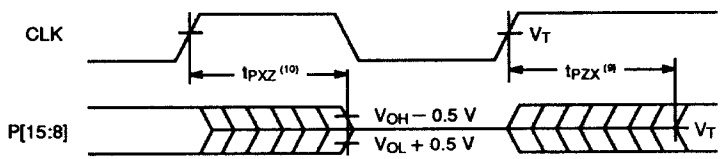
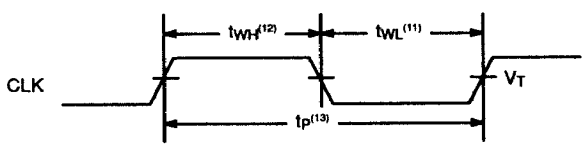
Asynchronous $\overline{\text{RESET}}$



10136-032A

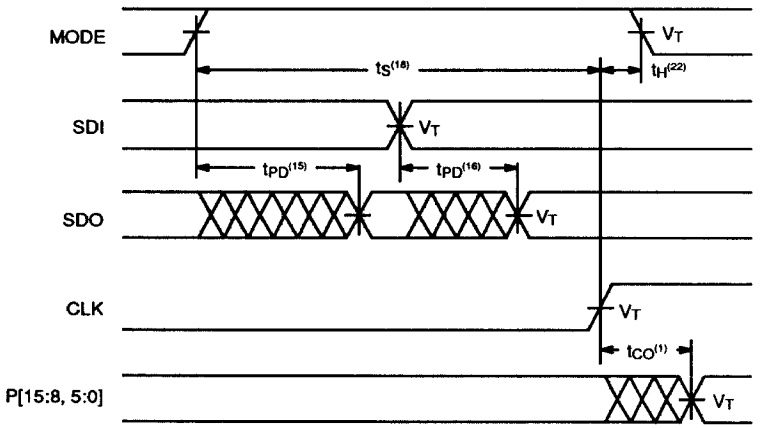
CLK to Output Disable/Enable



10136-033A

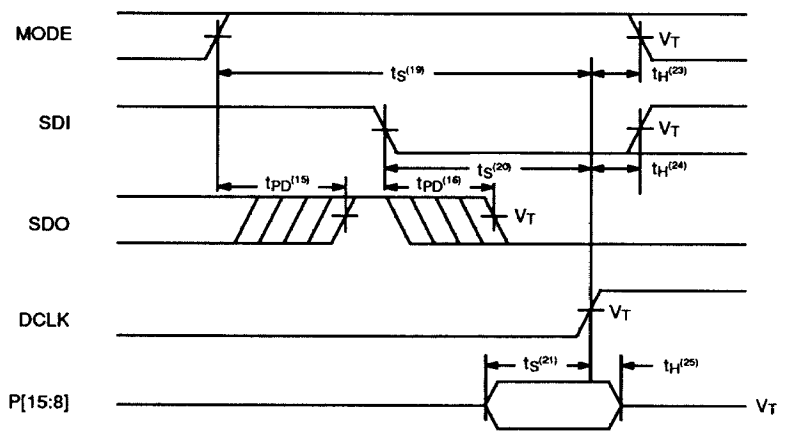
Clock Width/Period

SWITCHING WAVEFORMS (Continued)
SSR Configuration



10136-034A

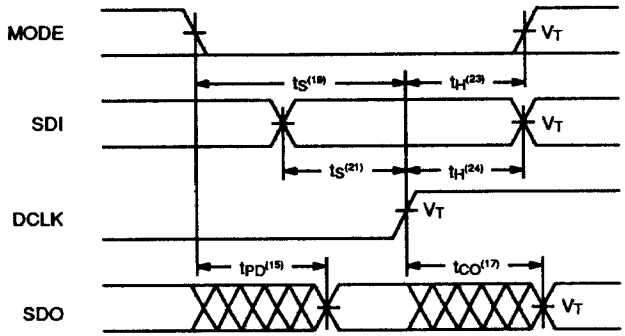
Load Pipeline Register from Shadow Register



10136-035A

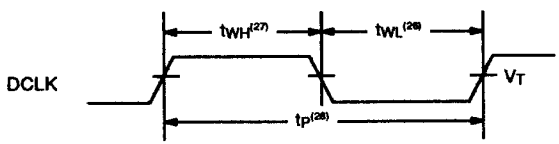
Load Shadow Register from Pipeline Register and/or Pins

SWITCHING WAVEFORMS (Continued)
SSR Configuration



10136-036A

Shift Shadow Register



10136-037A

DCLK Width/Period

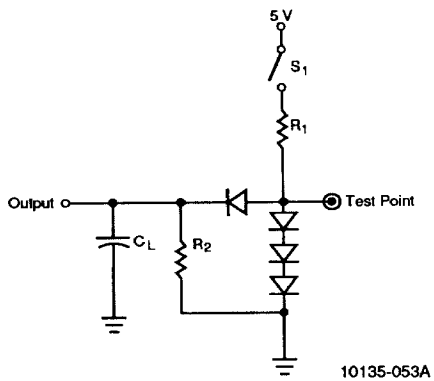
3

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

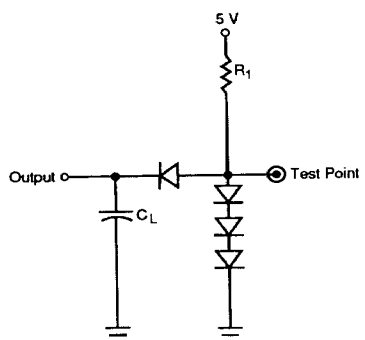
KS000010-PAL

SWITCHING TEST CIRCUIT



10135-053A

Three-State Outputs



10135-054A

Two-State Outputs

Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	667 Ω	5 kΩ	667 Ω	5 kΩ	1.5 V
t_{PZX}	Z → H: Open Z → L: Closed						1.5 V
t_{PXZ}	H → Z: Open L → Z: Closed	5 pF					H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

Note:

Pulse generator for all pulses: Rate ≤ 1.0 MHz; Z_O = 50 Ω; t_r ≤ 2.5 ns.

TEST PHILOSOPHY AND METHODS

The following eight points describe AMD's philosophy for high volume, high speed automatic testing.

1. Ensure that the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.

2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.

3. Do not attempt to perform threshold tests at high speed. Following an output transition, ground current may change by as much as 400 mA in 5–8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily.

4. Use extreme care in defining point input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0$ V and $V_{IH} \geq 3.0$ V for AC tests.

5. To simplify failure analysis, programs should be designed to perform DC, function, and AC tests as three distinct groups of tests.

6. Capacitive Loading for AC Testing

   Automatic testers and their associated hardware have stray capacitance that varies from one type of tester to another but is generally around 50 pF. This, of course, makes it impossible to make direct measurements of parameters which call for smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays," which measure the propagation delays into the high-impedance state and are usually specified at a load capacitance of 5.0 pF. In these cases, the test is performed at the higher load capacitance (typically 50 pF), and engineering correlations based on data taken with a bench setup are used to predict the result at the lower capacitance.

7. Threshold Testing

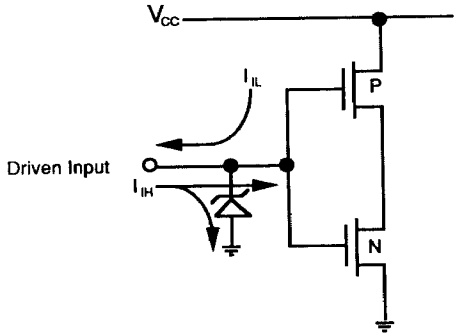
   The noise associated with automatic testing (due to the long, inductive cables) and the high gain of the tested device when in the vicinity of the actual device threshold, frequently give rise to oscillations when testing high-speed circuits. These oscillations are not indicative of a reject device but instead of an overtaxed test system. To minimize this problem, thresholds are tested at least once for each input pin. Thereafter, "hard" high and low levels are used for other tests. Generally this means that function and AC testing are performed at "hard" input levels rather than at V_{IL} Max. and V_{IH} Min.

8. AC Testing

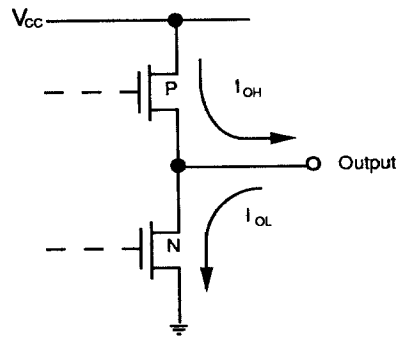
   Occasionally, parameters are specified that cannot be measured directly on automatic testers because of tester limitations. Data input hold times often fall into this category. In these cases, the parameter in question is guaranteed by correlating these tests with other AC tests that have been performed. These correlations are arrived at by the cognizant engineer by using precise bench measurements in conjunction with the knowledge that certain DC parameters have already been measured and are within spec.

   In some cases, certain AC tests are redundant, since they can be shown to be predicted by some other tests which have already been performed. In these cases, the redundant tests are not performed.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



10135-050A



10135-051A

Thermal Inpedance Values (θ_{JA}), Typical	
28-Pin Plastic SKINNYDIP (PD3028)	50°C/W
28-Pin Windowed Ceramic SKINNYDIP (CDE028)	40°C/W
28-Pin Plastic Leaded Chip Carrier (PL 028)	55°C/W
28-Pin Windowed Ceramic Leadless Chip Carrier (CLV028)	55°C/W