HD74LS221 ●Dual Monostable Multivibrators

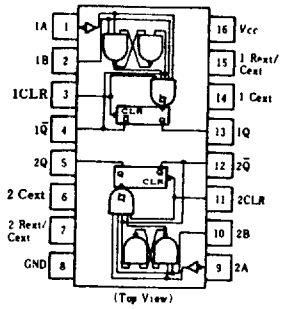
This multivibrator features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input. Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1V/s, providing the circuit with excellent noise immunity of typically 1.2V. A high immunity to V_{CC} noise of typically 1.5V is also provided by internal latching circuitry. Once fired, the outputs are independent of further transitions of the A and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses may be of any duration relative to the output pulse. Output rise and fall times are TTL compatible and independent of pulse length.

Typical triggering and clearing sequence are illustrated as a part of the switching characteristics waveforms. Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature.

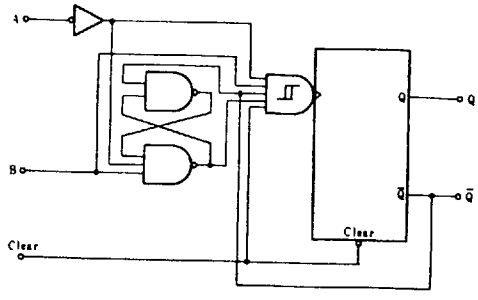
In most applications, pulse stability will only be limited by the accuracy of external timing components. Jitter-free operation is maintained over the full temperature and V_{CC} range for more than six decades of timing capacitance (10pF to 10μF) and more than one decade of timing resistance (2kΩ to 100kΩ).

Throughout these ranges, pulse width is defined by the relationship: $t_w(out)$=Cext·Rext·1n$_e$2.

■PIN ARRANGEMENT



■BLOCK DIAGRAM (½)



■FUNCTION TABLE

Inputs			Outputs	
Clear	A	B	Q	Q̄
L	×	×	L	H
×	H	×	L	H
×	×	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

H; high level, L; low level, X; irrelevant.
↓; Transition from high to low level.
↑; Transition from low to high level.
⎍; one high-level pulse.
⎎; one low-level pulse.

■RECOMMENDED OPERATING CONDITIONS

Item		Symbol	min	typ	max	Unit
Rate of rise or fall of input pulse	Schmitt input, B	dV/dt	1	–	–	V/s
	logic input, A		1	–	–	V/μs
Input pulse width	A or B	$t_{w(in)}$	40	–	–	ns
	Clear	$t_{w(clear)}$	40	–	–	
Setup time		t_{su}	15	–	–	ns
External timing resistance		R_{ext}	1.4	–	100	kΩ
External timing capacitance		C_{ext}	0	–	1,000	μF
Duty cycle	R_T=2kΩ		–	–	50	%
	R_T=100kΩ		–	–	90	

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■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item		Symbol	Test Conditions		min	typ*	max	Unit
Threshold voltage	A	V_{T+}	$V_{CC}=4.75V$		–	1.0	2.0	V
		V_{T-}	$V_{CC}=4.75V$		0.8	1.0	–	V
	B	V_{T+}	$V_{CC}=4.75V$		–	1.0	2.0	V
		V_{T-}	$V_{CC}=4.75V$		0.8	0.9	–	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $I_{OH}=-400\mu A$		2.7	–	–	V
		V_{OL}	$V_{CC}=4.75V$	$I_{OL}=4mA$	–	–	0.4	V
				$I_{OL}=8mA$	–	–	0.5	
Input current		I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		–	–	20	μA
	A	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		–	–	−0.4	mA
	B, Clear				–	–	−0.8	
		I_I	$V_{CC}=5.25V$, $V_I=7V$		–	–	0.1	mA
Short-circuit output current		I_{OS}	$V_{CC}=5.25V$		−20	–	−100	mA
Supply current		I_{CC}	$V_{CC}=5.25V$	Quiescent	–	4.7	11	mA
				Triggered	–	19	27	
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		–	–	−1.5	V

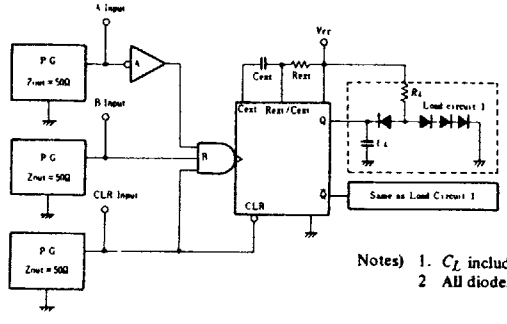
* $V_{CC}=5V$, $Ta=25°C$

■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

Item	Symbol	Inputs	Outputs	Test Conditions		min	typ	max	Unit
Propagation delay time	t_{PLH}	A	Q	$C_L=15pF$, $R_L=2k\Omega$	$C_{ext}=80pF$, $R_{ext}=2k\Omega$	–	45	70	ns
		B	Q			–	35	55	
	t_{PHL}	A	$\overline{Q}$			–	50	80	ns
		B	$\overline{Q}$			–	40	65	
	t_{PHL}	Clear	Q			–	35	55	ns
	t_{PLH}	Clear	$\overline{Q}$			–	44	65	ns
Output pulse width	$t_{w(out)}$	A or B	Q or $\overline{Q}$		$C_{ext}=80pF$, $R_{ext}=2k\Omega$	70	120	150	ns
					$C_{ext}=0$, $R_{ext}=2k\Omega$	20	47	70	
					$C_{ext}=100pF$, $R_{ext}=10k\Omega$	600	670	750	
					$C_{ext}=1\mu F$, $R_{ext}=10k\Omega$	6	6.7	7.5	ms

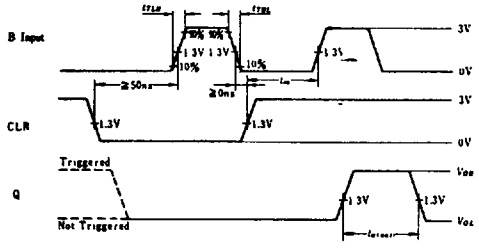
■TESTING METHOD

1) Test Circuit

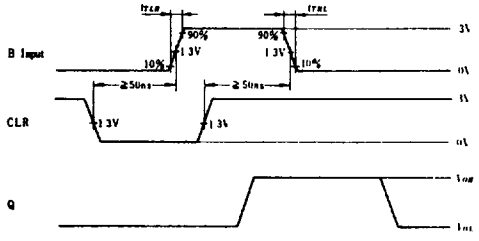


Notes) 1. C_L includes probe and jig capacitance.
2 All diodes are 1S2074 Ⓗ.

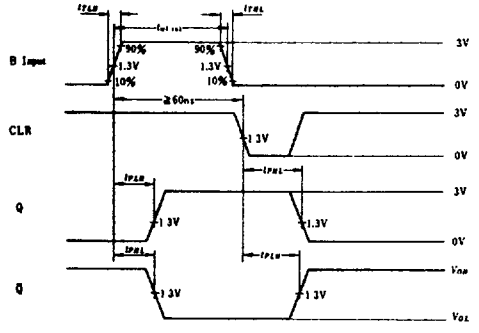
Waveform



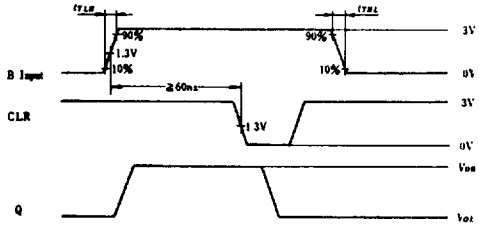
Trigger from B, then clear (A input is low).



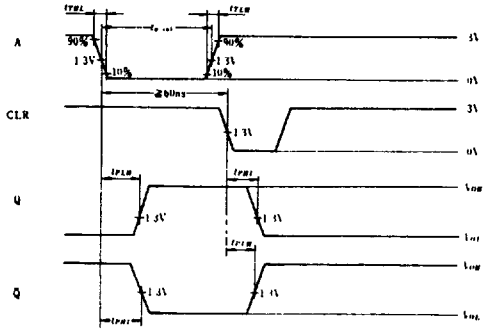
Trigger from B, then clear (A input is low).



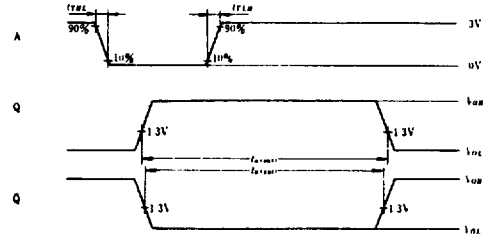
Clear overriding B, then trigger from B.



Triggering from positive transition of Clear.



Trigger from A, then clear (B input is high).



Trigger from A (B an clear inputs are high).

Note) Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR = 1$MHz

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PACKAGING INFORMATIONS

T-90-20

Factory orders for circuits described in this databook should include a three-part type number as explained in the following example.

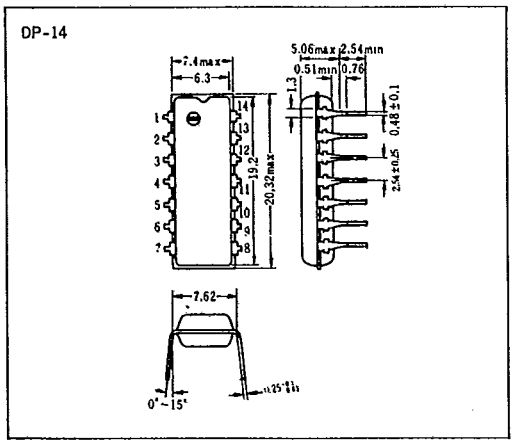
HD 74LS00 P

- P — Package ; Plastic DIP ; letters P / Cerdip ; non-letters
- 74LS00 — Circuit description
- HD — Prefix : HD ; Hitachi Digital IC

■Plastic DIP

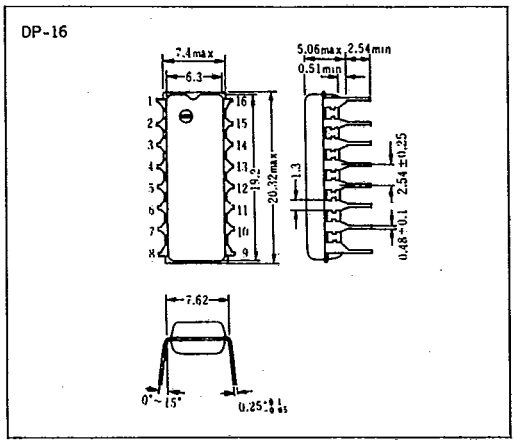
●14 Pin

DP-14



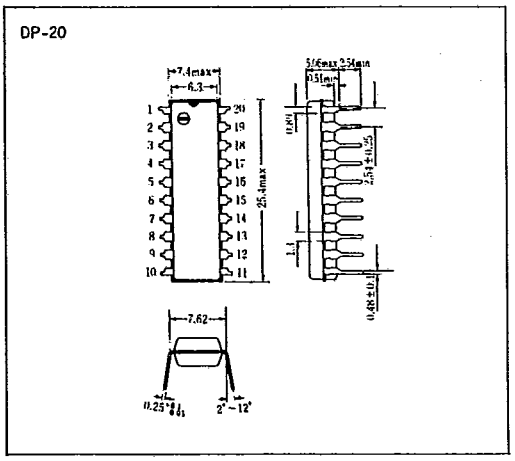
●16 Pin

DP-16



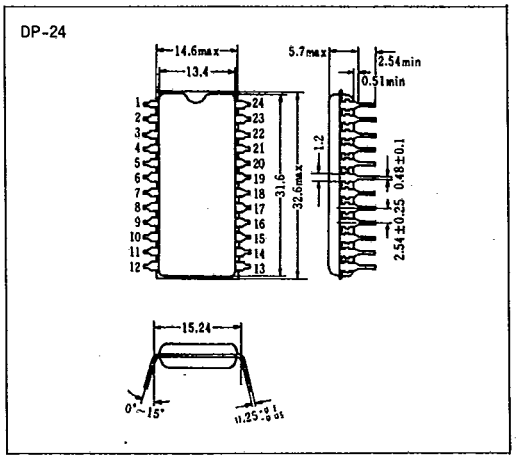
●20 Pin

DP-20



●24 Pin

DP-24



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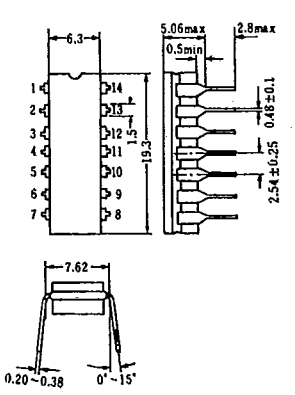
PACKAGING INFORMATIONS

■Cerdip

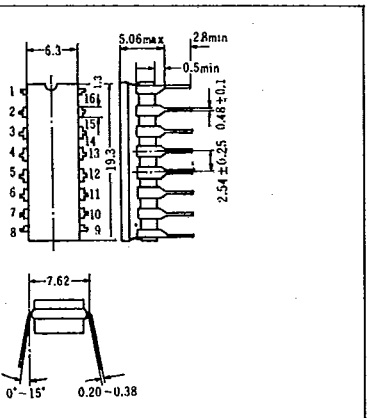
●14 Pin

DG-14



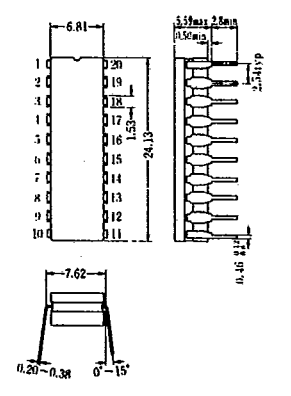
●16 Pin

DG-16



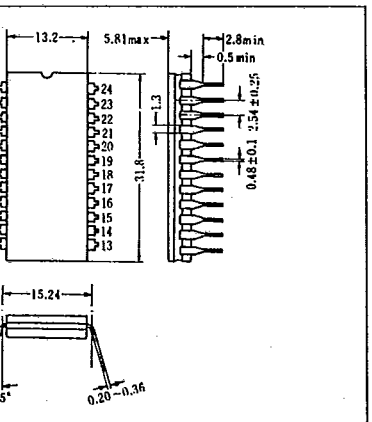
●20 Pin

DG-20



●24 Pin

DG-24



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