

Octal Buffers and Line Drivers with 3-State Outputs

These high-speed octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has the choice of combinations of inverting/non inverting outputs and symmetrical/complementary input controls (both active-low, or one active-low, the other active-high).

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

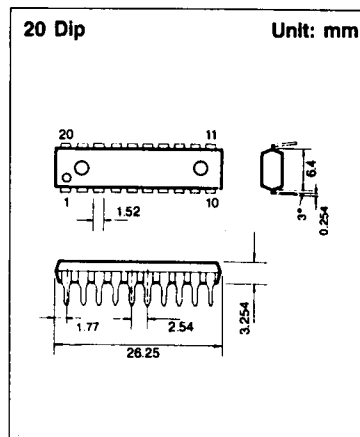
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FEATURES

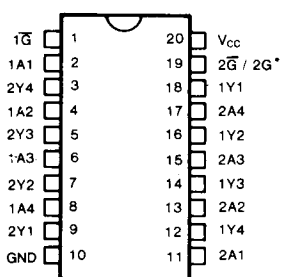
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ($I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to $+85^{\circ}\text{C}$

KS54HCTLS: -55°C to $+125^{\circ}\text{C}$



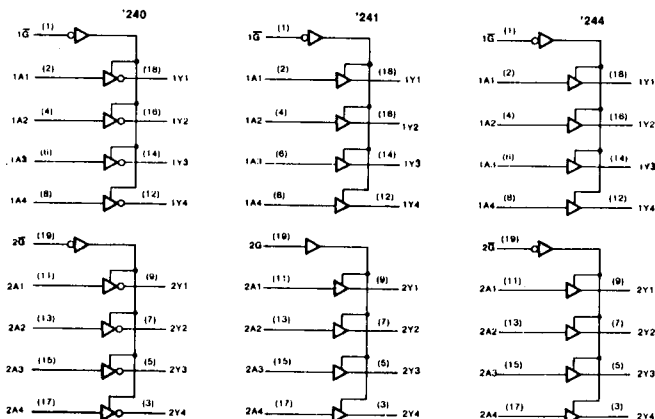
PIN CONFIGURATION



*2G for '240 and '244

2G for '241

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

| Characteristic | Symbol | Ratings | Unit |
|--|-----------------------------|--------------|------|
| Supply Voltage Range | V _{CC} | -0.5 to +7.0 | V |
| DC Input Diode Current (V _I < -0.5V or V _I > V _{CC} + 0.5V) | I _{IK} | ±20 | mA |
| DC Output Diode Current (V _O < -0.5V or V _O > V _{CC} + 0.5V) | I _{OK} | ±20 | mA |
| Continuous Output Current Per Pin (-0.5V < V _O < V _{CC} + 0.5V) | I _O | ±70 | mA |
| Continuous Current Through V _{CC} or GND pins | | ±250 | mA |
| Storage Temperature Range | T _{STG} | -65 to +150 | °C |
| Power Dissipation Per Package | P _D [†] | 500 | mW |

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
 Plastic Package (N): -12mW/°C from 65°C to 85°C
 Ceramic Package (J): -12mW/°C from 100°C to 125°C

RECOMMENDED OPERATING CONDITIONS

| Characteristic | Symbol | Value | | | Unit |
|-----------------------------|------------------------------------|-------|-----|-----------------|------|
| | | Min | Typ | Max | |
| Supply Voltage | V _{CC} | 4.5 | 5.0 | 5.5 | V |
| DC Input & Output Voltages* | V _{IN} , V _{OUT} | 0 | | V _{CC} | V |
| Operating Temperature Range | T _A | -40 | | +85 | °C |
| | | -55 | | +125 | °C |
| Input Rise & Fall Times | t _r , t _f | | | 500 | ns |

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

KS54HCTLS KS54HCTLS KS54HCTLS
 KS74HCTLS **240** KS74HCTLS **241** KS74HCTLS **244**

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

| Characteristic | Symbol | Test Conditions | $T_A = 25^\circ\text{C}$ | | KS74HCTLS $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | | KS54HCTLS $T_A = -55^\circ\text{C to } +125^\circ\text{C}$ | | Unit |
|-----------------------------------|----------|--|--------------------------|------------------------|--|-----------------------|---|-----------------------|---------------|
| | | | Typ | Guaranteed Limits | | | | | |
| Minimum High-Level Input Voltage | V_{IH} | | | 2.0 | 2.0 | 2.0 | 2.0 | 2.0 | V |
| Maximum Low-Level Input Voltage | V_{IL} | | | 0.8 | 0.8 | 0.8 | 0.8 | 0.8 | V |
| Minimum High-Level Output Voltage | V_{OH} | $V_{IN}=V_{IH}$ or V_{IL} $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$ | V_{CC} 4.2 | $V_{CC} - 0.1$ 3.98 | $V_{CC} - 0.1$ 3.84 | $V_{CC} - 0.1$ 3.7 | $V_{CC} - 0.1$ 3.7 | $V_{CC} - 0.1$ 3.7 | V |
| Maximum Low-Level Output Voltage | V_{OL} | $V_{IN}=V_{IH}$ or V_{IL} $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$ | 0 | 0.1 0.26 0.39 | 0.1 0.33 0.5 | 0.1 0.33 0.5 | 0.1 0.4 | 0.1 0.4 | V |
| Maximum Input Current | I_{IN} | $V_{IN}=V_{CC}$ or GND | | ± 0.1 | ± 1.0 | ± 1.0 | ± 1.0 | ± 1.0 | μA |
| Maximum 3-State Leakage Current | I_{OZ} | Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND | | ± 0.5 | ± 5.0 | ± 5.0 | ± 10.0 | ± 10.0 | μA |
| Maximum Quiescent Supply Current | I_{CC} | $V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$ | | 8.0 | 80.0 | 80.0 | 160.0 | 160.0 | μA |

AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 6$ ns, HCTLS240/241/244)

| Characteristic | Symbol | Conditions† | $T_A = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$ | | KS74HCTLS $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$ | | KS54HCTLS $T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$ | | Unit | | |
|---|-----------|--|--|----------|---|----------|--|----------|------|----|--|
| | | | Typ | | Guaranteed Limits | | | | | | |
| | | | | | | | | | | | |
| Maximum Propagation Delay, A to Y | t_{PLH} | $C_L = 50\text{pF}$ $C_L = 150\text{pF}$ | 13 19 | 18 25 | 22 31 | | 27 38 | | ns | | |
| | t_{PHL} | $C_L = 50\text{pF}$ $C_L = 150\text{pF}$ | 13 19 | 18 25 | 22 31 | | 27 38 | | | | |
| Maximum Output Enable Time, Enable to Y | t_{PZH} | $R_L = 1\text{k}\Omega$ | $C_L = 50\text{pF}$ $C_L = 150\text{pF}$ | 17 23 | 23 30 | 29 38 | | 34 45 | | ns | |
| | t_{PZL} | | $C_L = 50\text{pF}$ $C_L = 150\text{pF}$ | 17 23 | 23 30 | 29 38 | | 34 45 | | | |
| Maximum Output Disable Time, Enable to Y | t_{PHZ} | $R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$ | | 16 | 21 | 26 | | 32 | | ns | |
| | t_{PLZ} | | | 16 | 21 | 26 | | 32 | | | |
| Maximum Input Capacitance | C_{IN} | | 5 | | | | | | pF | | |
| Maximum Output Capacitance | C_{OUT} | Output Disabled | 10 | | | | | | pF | | |
| Power Dissipation Capacitance* (per stage) | C_{PD} | $\bar{G} = V_{CC}$ $\bar{G} = \text{GND}$ | 5 | | | | | | pF | | |
| | | | 30 | | | | | | | | |

* C_{PD} determines the no-load dynamic power consumption: $P_D = C_{PD}V_{CC}^2 f + I_{CC} V_{CC}$.

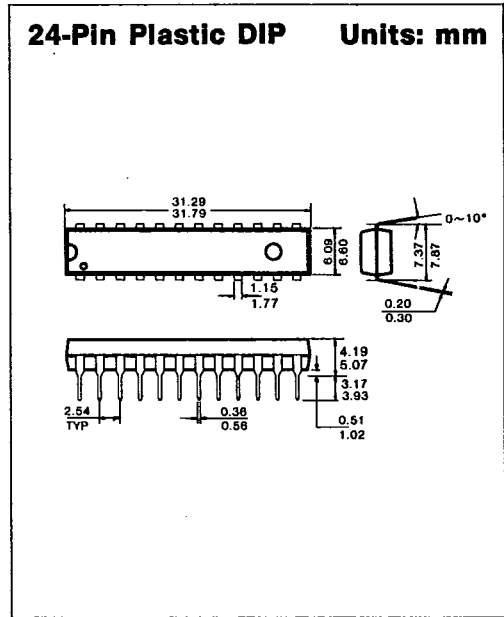
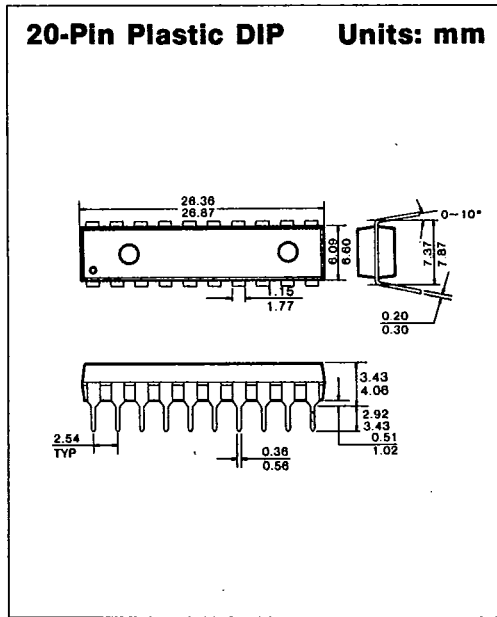
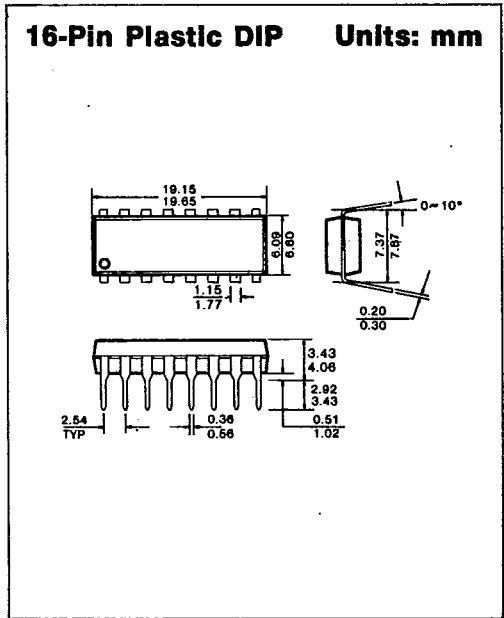
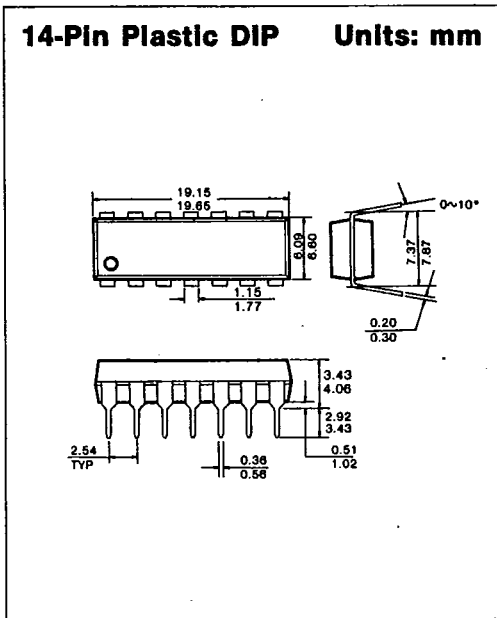
† For AC switching test circuits and timing waveforms see section 2.



PACKAGE DIMENSIONS

T-90-20

1. PLASTIC PACKAGES

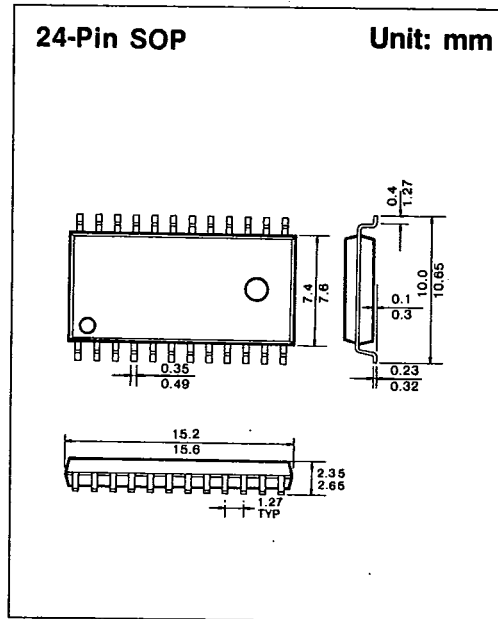
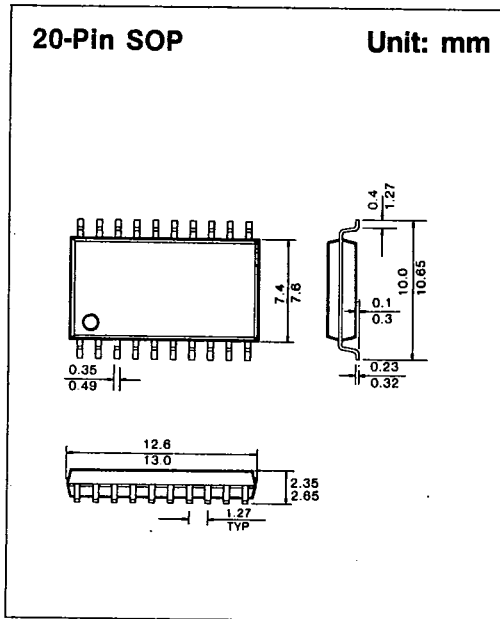
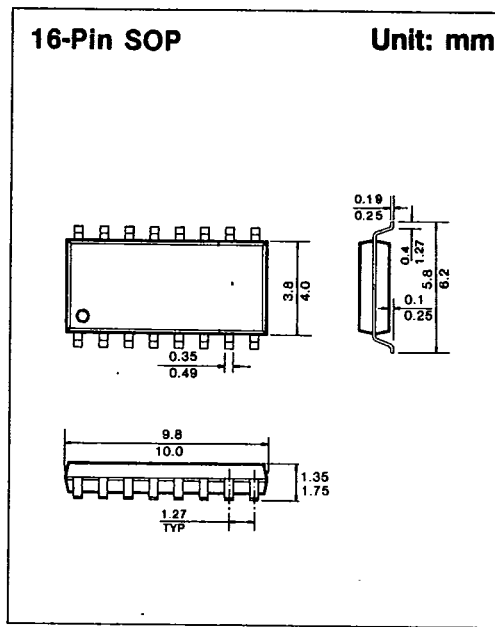
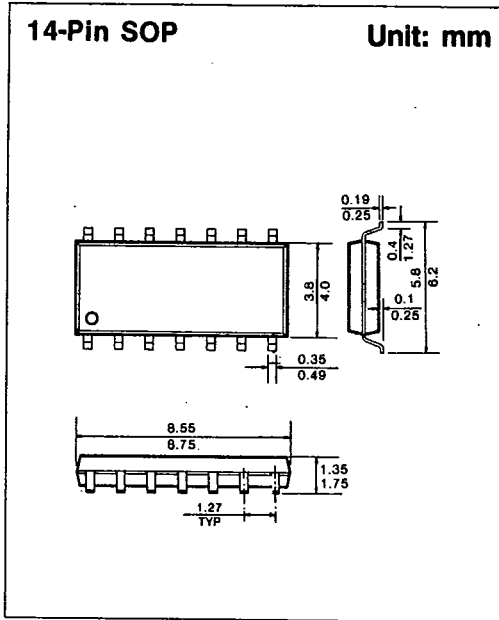


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PACKAGE DIMENSIONS

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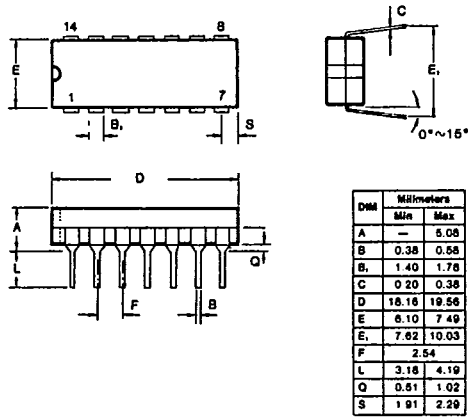


PACKAGE DIMENSIONS

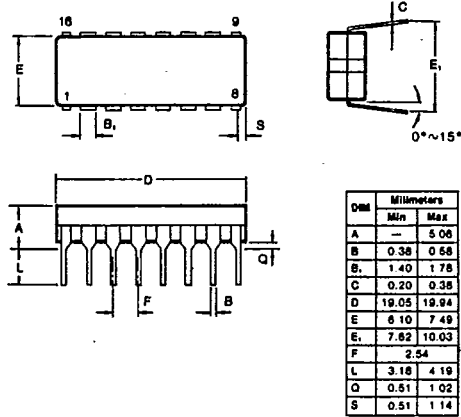
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2. CERAMIC PACKAGES

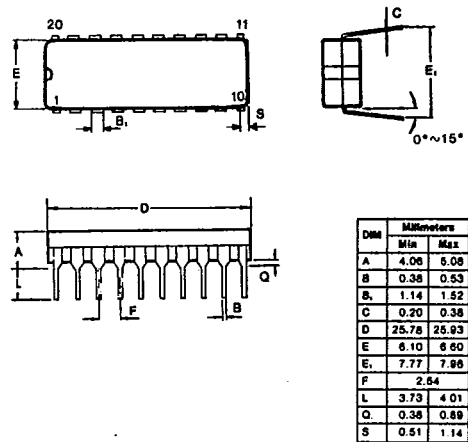
14-Pin Ceramic DIP Units: mm



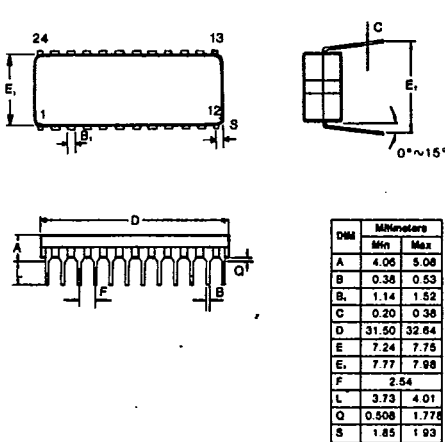
16-Pin Ceramic DIP Units: mm



20-Pin Ceramic DIP Units: mm



24-Pin Ceramic DIP Units: mm



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