T-46-13-47

CY7C340 EPLD Family

CYPRESS SEMICONDUCTOR

Multiple Array MatriX High-Density EPLDs

Features

- Erasable, user-configurable CMOS EPLDs capable of implementing high-density custom logic functions
- Advanced 0.8-micron double-metal CMOS EPROM technology
- Multiple Array MatriX architecture optimized for speed, density, and straightforward design implementation
  - Typical clock frequency = 50 MHz
  - Programmable Interconnect Array (PIA) simplifies routing
  - Flexible macrocells increase utilization
  - Programmable clock control
  - Expander product terms implement complex logic functions
- MAX+PLUS® development system eases design
  - Runs on IBM PC/AT® and compatible machines
  - Hierarchical schematic capture with 7400 series TTL and custom macrofunctions
  - State machine and Boolean entry
  - Graphical delay path calculator
  - Automatic error location
  - Timing simulation
  - Graphical interactive entry of waveforms

General Description

The Cypress Multiple Array MatriX (MAX®) family of EPLDs provides a user-configurable, high-density solution to general-purpose logic integration requirements. With the combination of innovative architecture and state-of-the-art process, the MAX EPLDs offer LSI density without sacrificing speed.

The MAX architecture makes it ideal for replacing large amounts of TTL SSI and MSI logic. For example, a 74161 counter utilizes only 3% of the 128 macrocells available in the CY7C342. Similarly, a 74151 8-to-1 multiplexer consumes less than 1% of the over 1,000 product terms in the CY7C342. This allows the designer to replace 50 or more TTL packages with just one MAX EPLD. The family comes in a range of densities, shown below. By standardizing on a few MAX building blocks, the designer can replace hundreds of different 7400 series part numbers currently used in most digital systems.

The family is based on an architecture of flexible macrocells grouped together into Logic Array Blocks (LABs). Within the LAB is a group of additional product terms called expander product terms. These expanders are used and shared by the macrocells, allowing complex functions, up to 35 product terms, to be easily mplemented in a single macrocell. A Programmable Interconnect Array (PIA) globally routes all signals within devices containing more than one LAB. This architecture is fabricated on the Cypress advanced 0.8-micron, double-layer-metal CMOS EPROM process, yielding devices with significantly higher integration density and system clock speed than the largest of previous generation EPLDs.

The density and flexibility of the CY7C340 family is accessed using the MAX+PLUS development system. A PC-based design system, MAX+PLUS is optimized specifically for the CY7C340 family architecture, providing efficient design processing. A hierarchical schematic entry mechanism is used to capture the design. State machine, truth table, and Boolean equation entry mechanisms are also supported, and may be mixed with schematic capture. The powerful design processor performs minimization and logic synthesis, then automatically fits the design into the desired EPLD. Design verification is done using a timing simulator, which provides full A.C. simulation, along with an interactive graphic waveform editor package to speed waveform creation and debugging. During design processing a sophisticated automatic error locator shows exactly where the error occurred by popping the designer back into the schematic at the exact error location.

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Max Family Members

Feature	CY7C344	CY7C343	CY7C342	CY7C341
Macrocells	32	64	128	192
MAX Flip-Flops	32	64	128	192
MAX Latches[1]	64	128	256	384
MAX Inputs[2]	23	35	59	71
MAX Outputs	16	28	52	64
Packages	28H,J 28W,D	44H,J	68H,J 68R,G	84H,J 84R,G

Key: D—DIP G—Pin Grid Array H—Windowed Ceramic Leaded Chip Carrier J—J-Lead Chip Carrier R—Windowed Pin Grid Array W—Windowed Ceramic DIP

Notes:
1. When all expander product terms are used to implement latches. 2. With one output.

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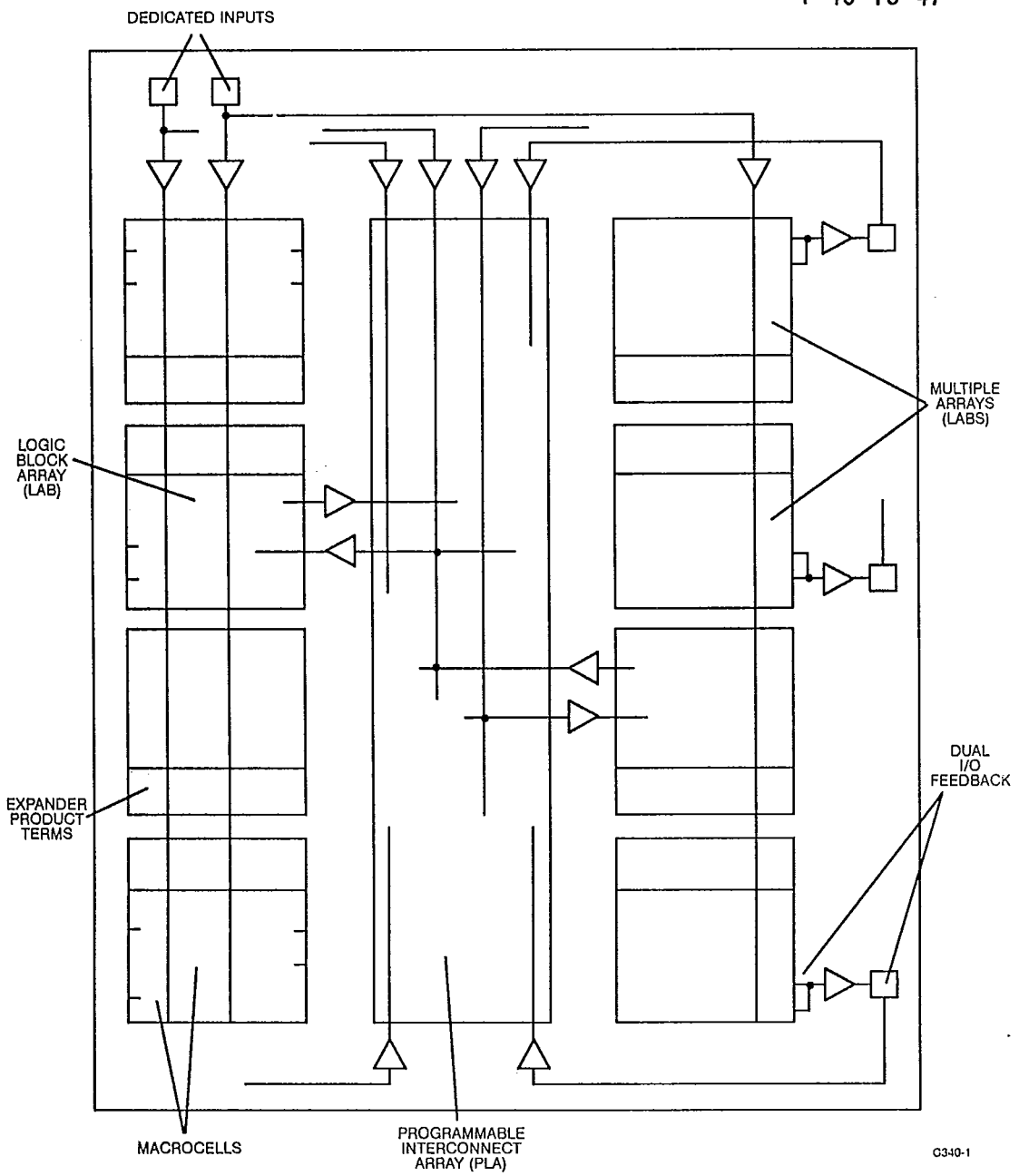

Figure 1. Key MAX Features

Functional Description

The Logic Array Block

The logic array block, shown in *Figure 2*, is the heart of the MAX architecture. It consists of a macrocell array, expander product term array, and an I/O block. The number of macrocells, expanders, and I/O vary, depending upon the device used. Global feedback of all signals is provided within a LAB, giving each functional block complete access to the LAB resources. The LAB itself is fed by the programmable interaconnect array and dedicated input bus. The feedbacks of the macrocells and I/O pins feed the PIA, providing access to them through other LABs in the device. The CY7C340 family of EPLDs that have a single LAB use a global bus and a PIA is not needed (see *Figure 3*).

The MAX Macrocell

Traditionally, PLDs have been divided into either PLA (programmable AND, programmable OR), or PAL® (programmable AND, fixed OR) architectures. PLDs of the latter type provide faster input-to-output delays, but can be inefficient due to fixed allocation of product terms. Statistical analysis of PLD logic designs has shown that 70% of all logic functions (per macrocell) require three product terms or less.

The macrocell structure of MAX has been optimized to handle variable product term requirements. As shown in *Figure 4*, each macrocell consists of a product term array and a configurable register. In the macrocell, combinatorial logic is implemented with three product terms ORed together, which then feeds an XOR gate. The second input to the XOR gate is also controlled by a product term, providing the ability to control active HIGH or active LOW logic and to implement T- and JK-type flip-flops. The Max+PLUS sofware will aso use this gate to implement complex mutually exclusive-OR arithmetic logic functions, or to do DeMorgan's Inversion, reducing the number of product terms required to implement a function.

If more product terms are required to implement a given function, they may be added to the macrocell from the expander product term array. These additional product terms may be added to any macrocell, allowing the designer to build gate-intensive logic, such as address decoders, adders, comparators, and complex state machines, without using extra macrocells.

The register within the macrocell may be programmed for either D, T, JK, or RS operation. It may alternately be configured as a flow-through latch for minimum input-to-output delays, or bypassed entirely for purely combinatorial logic. In addition, each register supports both asynchronous preset and clear, allowing asynchronous loading of counters of shift registers, as found in many standard TTL functions. These registers may be clocked with a synchronous system clock, or clocked independently from the logic array.

Expander Product Terms

The expander product terms, as shown in *Figure 5*, are fed by the dedicated input bus, the programmable interconnect array, the macrocell feedback, the expanders themselves, and the I/O pin feedbacks. The outputs of the expanders then go to each and every product term in the macrocell array. This allows expanders to be "shared" by the product terms in the logic array block. One expander may feed all macrocells in the LAB, or even multiple product terms in the same macrocell. Since these expanders feed the secondary product terms (preset, clear, clock, and output enable) of each macrocell, complex logic funcitons may be implemented without utilizing another macrocell. Likewise, expanders may feed

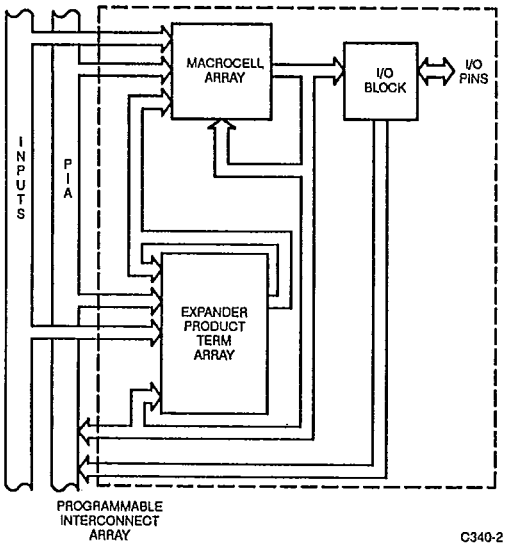

Figure 2. Typical LAB Block Diagram

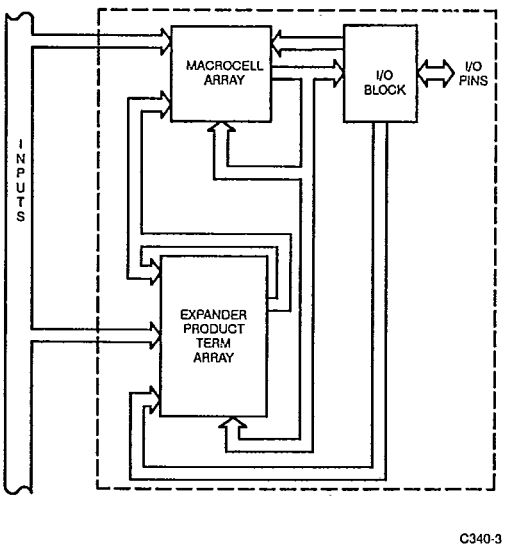

Figure 3. 7C344 LAB Block Diagram

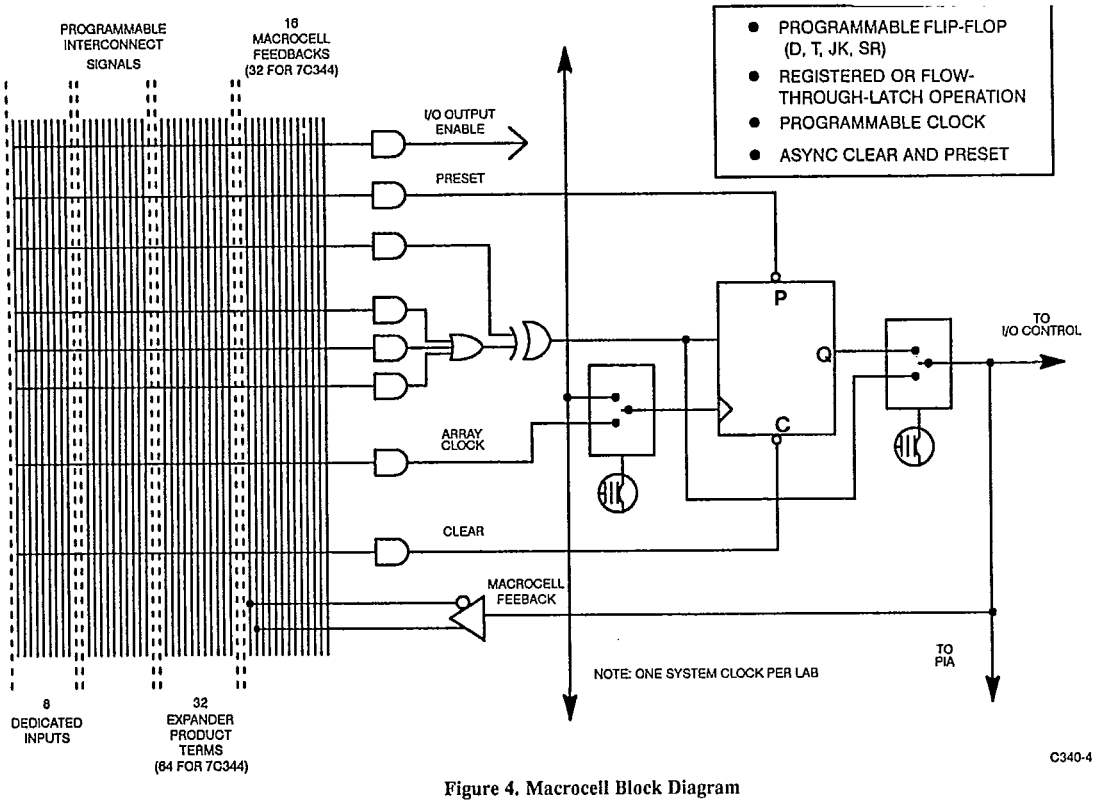

Figure 4. Macrocell Block Diagram

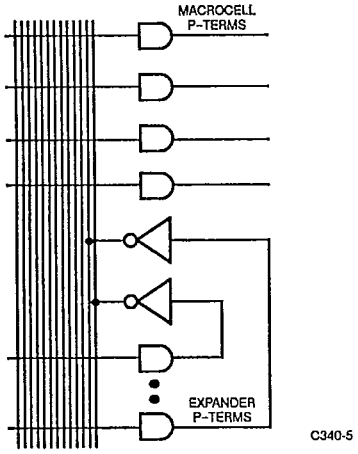

Figure 5. Expander Product Terms

Functional Description (continued)

and be shared by other expanders, to implement complex multi-level logic and input latches.

I/O Block

Separate from the macrocell array is the I/O control block of the LAB. *Figure 6* shows the I/O block diagram. The three-state buffer is controlled by a macrocell product term and the drives the I/O pad. The input of this buffer comes from a macrocell within the associated LAB. The feedback path from the I/O pin may feed other blocks within the LAB, as well as the PIA.

By decoupling the I/O pins from the flip-flops, all the registers in the LAB are "buried," allowing the I/O pins to be used as dedicated outputs, bidirectional outputs, or as additional dedicated inputs. Therefore, applications requiring many buried flip-flops, such as counters, shift registers, and state machines, no longer consume both the macrocell register and the assoicated I/O pin, as in earlier devices.

The Programmable Interconnect Array

PLD density and speed has traditionally been limited by signal routing; i.e., getting signals from one macrocell to another. For smaller devices, a single array is used and all signals are available to all macrocells. But as the devices increase in density, the number of signals being routed becomes very large, increasing the amount

Functional Description (continued)

of silicon used for interconnections. Also, because the signal must be global, the added loading on the internal connection path reduces the overall speed performance of the device. The MAX architecture solves these problems. It is based on the concept of small, flexible logic array blocks, which, in the later devices, are interconnected by a PIA.

The PIA solves interconnect limitations by routing only the signals needed by each LAB. The architecture is designed so that every signal on the chip is within the PIA. The PIA is then programmed to give each LAB access to the signals that it requires. Consequently, each LAB receives only the signals needed. This effectively solves any routing problems that may arise in a design without degrading the performance of the device. Unlike masked or programmable gate arrays, which induce variable delays dependent on routing, the PIA has a fixed delay from point to point. This eliminates undesired skews among logic signals, which may cause glitches in internal or external logic.

MAX+PLUS Development System Description

The PLDS-MAX+PLUS (Programmable Logic Design System) is a unified CAE system for designing logic with Cypress's CY7C340 family of EPLDs (*Figure 7*). PLDS-MAX+PLUS includes design entry, design processing, timing simulation, and device programming support. PLDS-MAX+PLUS runs on IBM PS/2, PC-AT, or compatible machines, and provides tools to quickly and efficiently create and verify complex logic designs.

The MAX+PLUS software compiles designs for MAX EPLDs in minutes. Designs may be entered with a variety of design entry mechanisms. MAX+PLUS supports hierarchical entry of both Graphic Design Files (GDFs) with the MAX+PLUS Graphic Editor, and Text Design Files (TDFs) with the Advanced Hardware Description Language (AHDL). The Graphic Editor offers advanced features such as multiple hierarchy levels, symbol editing, and a library of 7400 series devices as well as basic SSI gates. AHDL designs may be mixed into any level of the hierarchy or used on a standalone basis. AHDL is tailored especially for EPLD designs and includes support for complex Boolean and arithmetic functions, relational comparisons, multiple hierarchy levels, state machines with automatic state variable assignment, truth tables, and function calls.

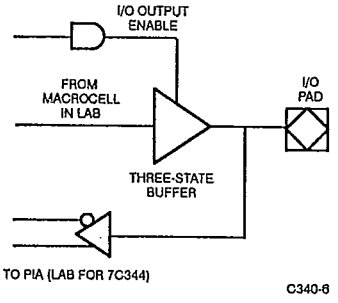

Figure 6. I/O Block Diagram

In addition to multiple design entry mechanisms, MAX+PLUS includes a sophisticated compiler that uses advanced logic synthesis and minimization techniques in conjunction with heuristic fitting rules to efficiently place designs within MAX EPLDs. A programming file created by the compiler is then used by MAX+PLUS to program MAX devices with the QP2-MAX programming hardware.

Simulations may be performed with a powerful, event-driven timing simulator. The MAX+PLUS Simulator interactively displays timing results in the MAX+PLUS Waveform Editor. Hardcopy table and waveform output is also available. With the Waveform Editor, input vector waveforms may be entered, modified, grouped, and ungrouped. In addition, the Waveform Editor compares simulation runs and highlights the differences.

The integrated structure of MAX+PLUS provides features such as automatic error location and delay prediction. If a design contains an error in either a schematic or a text file, MAX+PLUS flags the error *and* takes the user to the actual location of the error in the original schematic or text file. In addition, propagation delays of critical paths may be determined in both the Graphic and Text Editors with the delay predictor. After the source and destination nodes are tagged, the shortest and longest timing delays are calculated.

MAX+PLUS provides a seamless design framework using a consistent graphical user interface throughout. This framework simplifies all stages of the design cycle: design entry, processing, verification, and programming. In addition, MAX+PLUS offers online help to aid the user.

Design Entry

MAX+PLUS offers both graphic and text design entry methods. GDFs are entered with the MAX+PLUS Graphic Editor; Boolean equations, state machines, and truth tables may be entered with the MAX+PLUS Test Editor using AHDL. The ability to freely mix graphics and text files at all levels of the design hierarchy and to use either a top-down or bottom-up design method makes design entry simple and versatile.

Graphic Editor

The Graphic Editor provides a mouse-driven, multi-windowed environment in which commands are entered with pop-up menus or simple keystrokes. The Hierarchy Display window, shown at the top, lists all schematics used in a design. The designer navigates the hierarchy by placing the cursor on the name of the design to be edited and clicking the left mouse button. The Total View window (next to the Hierarchy window) shows the entire design. By clicking on an area in this window, the user is moved to that area of the schematic. The Error Report window lists all warnings and errors inthe compiled design; selecting an error with the cursor highlights the problem node and symbol. A design is edited in the main area, which may be enlarged by closing the auxiliary windows.

When entering a design, the user may choose from a library of over 200 7400 series and special-purpose macrofunctions that are all optimized for MAX architecture. In addition, the designer my create custom functions that can be used in any MAX+PLUS design.

To take advantage of the hierarchy features, the user first saves the entered design so the Graphic Editor can automatically create a symbol representing the design. This symbol may be used in a higher-level schematic or in another design. It may also be modified with the Symbol Editor.

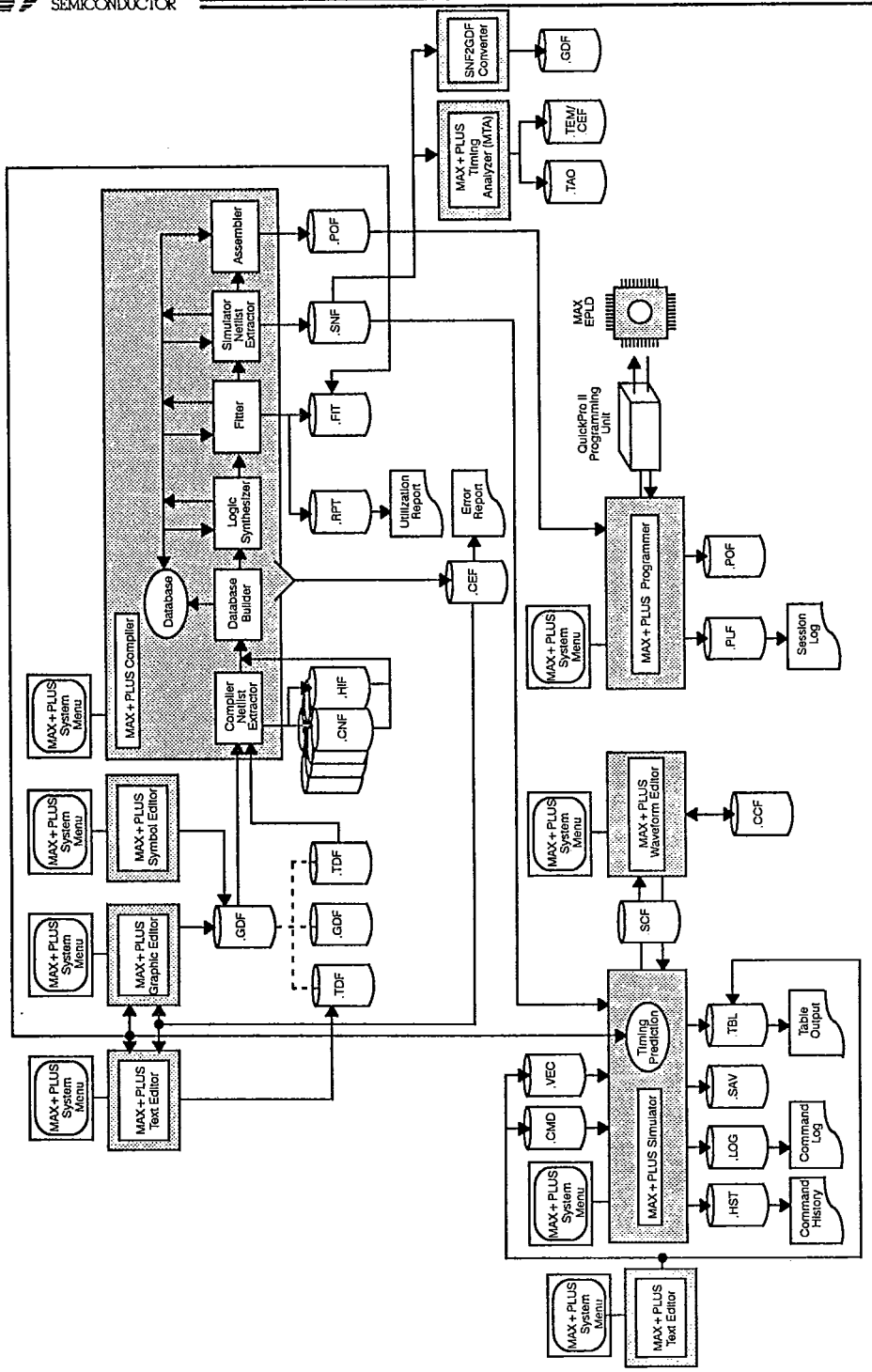

Figure 7. MAX+PLUS Block Diagram

Graphic Editor (continued)

Tag-and-drag editing is used to move individual symbols or entire areas. Lines stay connected with orthogonal rubberbanding. A design may be printed on an Epson FX-compatible printer, or plotted on an HP- or Houston Instruments-compatible plotter.

Symbol Editor

The MAX + PLUS Symbol Editor enables the designer to create or modify a custom symbol representing a GDF or TDF. It is also possible to modify input and output pin placement of an automatically generated symbol.

The created symbol represents a lower-level design, described by a GDF or TDF. The lower-level design represented by the symbol may be displayed with a single command that invokes either the Graphic Editor for schematics or the Text Editor for AHDL designs.

AHDL

The Advanced Hardware Description Language (AHDL) is a high-level, modular language used to create logic designs for MAX EPLDs. It is completely integrated into MAX + PLUS, so AHDL files may be created, edited, compiled, simulated, and programmed from within MAX + PLUS.

AHDL provides support for state machine, truth tables, and Boolean equations, as well as srithmetic and relational operations. AHDL is hierarchical, which allows frequently used functions such as TTL and bus macrofunctions to be incorporated in a design. AHDL supports complex arithmetic and relational opeartions, such as addition, subtraction, equality, and magnitude comparisons, with the logic functions automatically generated. Standard Boolean functions, including AND, OR, NAND, NOR, XOR, and SNOR are also included. Groups are fully supported so operations may be performed on groups as well as on single variables. AHDL also allows the designer to specify the location of nodes within MAX EPLDs. Together, these features enable complex designs to be implemented in a concise, high-level description.

Text Editor

The MAX + PLUS Text Editor enables the user to view and edit text files within the MAX + PLUS environment. Any ASCII text file, including Vector Files, Table Files, Report Files, and AHDL Text Design Files (TDFs) may be viewed and edited wihtout having to exit to DOS.

The Text Editor parallels the Graphic Editor's menu structure. It has a Hierarchy Display and a Total View window for moving through the hierarchy levels and around the design. It includes automatic error location and hierarchy traversal. If an error is found in a TDF during compilation, the Text Editor is automatically invoked and the line of AHDL code where the error occurred is highlighted. In addition, a design may use both text and graphic files. As the designer t4raverses the hierarchy, the Text Editor is invoked for text files, and the Graphic Editor is invoked for schematics.

Symbol Libraries

The library provided with MAX + PLUS contains the most commonly used 7400 series devices such as counters, decoders, encoders, shift registers, flip-flops, latches, and multipliers, as well as special bus macrofunctions, all of which increase design productivity. Because of the flexible architecture of MAX EPLDs (that includes asynchronous preset and clear), true TTL device emulation is achieved. Cypress also provides special-purpose bus macrofunctions for designs that use buses. All macrofunctions have been optimized to maximize speed and utilization. Refer to the *MAX + PLUS TTL MacroFunctions* manual for more information on TTL macrofunctions.

Design Processing

The MAX + PLUS Compiler processes MAX designs. The Compiler offers options that speed the processing and analysis of a design. The user can set the degree of detail of the Report File and the maximum number of errors generated. In addition, the user may select whether or not to extract a netlist file for simulation.

The Compiler compiles a design in increments. If a design has been previously processed, only the portion of the design that has been changed is re-extracted, which decreases the compilation time. This "Make" facility is an automatic feature of the Compile command.

The first module of the Compiler, the Compiler Netlist Extractor, extracts the netlist that is used to define the design from each file. At this time, design rules are checked for any errors. If errors are found, the Graphic Editor is invoked when the error appears in a GDF, and the Text Editor is invoked when the error appears in a TDF. The Error Report window in both editors highlights the location of the error. A successfully extracted design is built into a database to be used by the Logic Synthesizer.

The Logic Synthesizer module translates and optimizes the user-defined logic for the MAX architecture. Any unused logic within the design is automatically removed. The Logic Synthesizer uses expert system synthesis rules to factor and map logic within the multilevel MAX architecture. It then chooses the approach that ensures the most efficient use of silicon resources.

The next module, the Fitter, uses heuristic rules to optimally place the synthesized design into the chosen MAX EPLD. For MAX devices that have a Programmable Interconnect Array (PIA), the Fitter also routes the signals across this interconnect structure, so the designer doesn't have to worry about placement and routing issues. A Report File (.RPT) is issued by the Fitter, which shows design implementation as well as any unused resources in the EPLD. The designer can then determine how much additional logic may be placed in the EPLD.

A Simulator Netlist File (.SNF) may be extracted from the compiled design by the Simulator Netlist Extractor if simulation is desired. Finally, the Assembler creates a Programmer Object File (.POF) from the compiled design. This file is used with the QP2-MAX programming hardware to program the desired part.

Delay Prediction and Probes

MAX + PLUS includes powerful analysis tools to verify and analyze the completed design. Delay analysis with the delay predictor may be performed interactively in the Graphic Editor, or in the Simulator. The Simulator is interactive and event-driven, yielding true timing and functional charactersitics of the compiled design.

The delay predictor provides instant feedback about the timing of the processed design. After selecting the start point and end point of a path, the designer may determine the shortest and longest propagation delays of speed-critical paths.

Also, a designer may use probes to mark internal nodes in a design. The designer may enter a probe by placing the cursor on any node in a graphic design, selecting the SPE (Symbol:Probe:Enter) command, and then entering a unique name to define the probe. This name may then be used in the Graphic Editor, Simulator, and Waveform Editor to reference that node, so that lengthy hierarchical path names are avoided.

Simulator

Input stimuli can be defined with a straightforward vector input language, or waveforms can be directly drawn using the Waveform Editor. Outputs may also be viewed in the Waveform Editor, or hardcopy table and waveform files may be printed.

The Simulator used the Simulator Netlist File (SNF) extracted from the compiled design to perform timing simulation with 1/10-nanosecond resolution. A Command File may be used for batch operation, or commands may be entered interactively. Simulator commands allow the user to halt the simulation dependent on user-defined conditions, to force and group nodes, and perform AC detection.

If flip-flop set-up or hold times have been violated, the Simulator warns the user. In addition, the minimum pulse width and period of oscillation may be defined. If a pulse is shorter than the minimum pulse width specified, or if a node oscillates for longer than the specified time, the Simulator issues a warning.

Waveform Editor

The MAX + PLUS Waveform Editor provides a mouse-driven environment in which timing waveforms may be viewed and edited. It functions as a logic analyzer, enabling the user to observe simulation results. Simulated waveforms may be viewed and manipulated at multiple zoom levels. Nodes may be added, deleted, and combined into buses, which may contain up to 32 signals represented in binary, octal, decimal, or hexadecimal format. Logical opeartors may also be performed on pairs of waveforms, so that waveforms may be inverted, ORed, ANDed, or XORed together.

The Waveform Editor includes sophisticated editing features to define and modify input vectors. Input waveforms are created with the mouse and familiar text editing commands. Waveforms may be copied, patterns may be repeated, and blocks may be moved and copied. For example, all or part of a waveform may be contracted to simulate the increase in clock frequency.

The Waveform Editor also compares and highlights the difference between two different simulations. A user may simulate a design, observe and edit the results, and then resimulate the design, and the Waveform Editor will show the results superimposed upon each other to highlight the differences.

MAX + PLUS Timing Analyzer (MTA)

The MAX + PLUS Timing Analyzer (MTA) provides user-configurable reports that assist the designer in analyzing critical delay paths, set-up and hold timing, and overall system performance of any MAX EPLD design. Critical paths identified by these reports may be desplayed and highlighted.

Timing delays between multiple source and destination nodes may be calculated, thus creating a connection matrix giving the shortest and longest delay paths between all source and destination nodes specified. Or, the designer may specify that the detailed paths and delays between specific sources and destinations be shown.

The set-up/hold option provides set-up and hold requirements at the device pins for all pins that feed the D, CLK, or ENABLE inputs of flip-flops and latches. Critical source nodes may be specified individually, or set-up and hold at all pins may be calculated. This information is then displayed in a table, one set of set-up and hold times per flip-flop/latch.

The MTA also allows the user to print a complete list of all accessible nodes in a design,; i.e., all nodes that may be displayed during simulation or delay prediction.

All MTA options may be listed in an MTA command file. With this file, the user may specify all information needed to configure the output.

SNF2GDF Converter

SNF2GDF converts the SNF into logic schematics represented with basic gates and flip-flop elements. It uses the SNF's delay and connection information and creates a series of schematics fully annotated with propagation delay and set-up and hold information at each logic gate. Certain speed paths of a design may be specified for conversion, so the user may graphically analyze only the paths considered critical.

If State Machine or Boolean Equation design entry is used, SNF2GDF shows how the high-level description has been synthesized and placed into the MAX architecture.

Device Programming

PLDS-MAX contains the basic hardware and software for programming the MAX EPLD family. Adpaters are included for programming the CY7C344 (DIP and PLCC) and CY7C342 (PLCC) devices. Additional adapters supporting other MAX devices may be purchased separately. MAX + PLUS programming software drives the QP2-MAX programming hardware. The designer can use MAX + PLUS to program and verify MAX EPLDs. If the security bit of the device is not set to ON, the designer may also read the contents of a MAX device and use this information to program additional devices.

System Requirements

Minimum System Configuration

IBM PS/2 model 50 or higher, PC/AT or compatible computer.

PC-DOS version 3.1 or higher.

640 kbytes RAM.

EGA, VGA or Hercules monochrome display.

20-MB hard disk drive.

1.2-MB 5¼" or 1.44-MB 3½" floppy disk drive.

3-button serial port mouse.

Recommended System Configuration

IBM PS/2 model 70 or higher, or Compaq 386 20-Mhz computer.

PC-DOS version 3.3.

640 kbytes of RAM plus 1 MB of expanded memory with LIM 3.2-compatible EMS driver.

VGA graphics display.

20-MB hard disk drive.

1.2-MB 5¼" or 1.44-MB 3½" floppy disk drive.

3-button serial port mouse.

Ordering Information

CY3200	PLDS-MAX + PLUS System including:	
	CY3201	MAX + PLUS software, manuals and key.
	CY3202	QP2-MAX PLD programmer with CY3342 & CY3344 adapters.

Device Adapters

CY3340	Adapter for CY7C341 in PLCC packages.
CY3342	Adapter for CY7C342 in PLCC packages.
CY3344	Adapter for CY7C344 in DIP and PLCC packages.
CY3342R	Adapter for CY7C342 in PGA packages.
CY33435	Adapter for CY7C343 in PLCC packages.

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PRELIMINARY **CY7C341**

CYPRESS SEMICONDUCTOR

192-Macrocell MAX® EPLD

Features

- **192 macrocells in 12 LABs**
- **8 dedicated inputs, 64 bidirectional I/O pins**
- **Programmable interconnect array**
- **384 expander product terms**
- **Available in 84-pin JLCC, PLCC, and PGA packages**

Functional Description

The CY7C341 is an Erasable Programmable Logic Device (EPLD) in which CMOS EPROM cells are used to configure logic functions within the device. The MAX architecture is 100% user configurable allowing the devices to accommodate a variety of independent logic functions.

The 192 macrocells in the CY7C341 are divided into 12 Logic Array Blocks (LABs), 16 per LAB. There are 384 expander product terms, 32 per LAB, to be used and shared by the macrocells within each LAB. Each LAB is interconnected with a programmable interconnect array, allowing all signals to be routed throughout the chip.

The speed and density of the CY7C341 allows it to be used in a wide range of applications, from replacement of large amounts of 7400 series TTL logic, to complex controllers and multifunction chips. With greater than 37 times the functionality of 20-pin PLDs, the CY7C341 allows the replacement of over 75 TTL devices. By replacing large amounts of logic, the CY7C341 reduces board space, part count, and increases system reliability.

Each LAB contains 16 macrocells. In LABs A, F, G, and L, 8 macrocells are connected to I/O pins and 8 are buried, while for LABs B, C, D, E, H, I, J, and K, 4 macrocells are connected to I/O pins and 12 are buried. Moreover. in addition to the I/O and buried macrocells, there are 32 single product term logic expanders in each LAB. Their use greatly enhances the capability of the macrocells without increasing the number of product terms in each macrocell.

Logic Array Blocks

There are 12 logic array blocks in the CY7C341. Each LAB consists of a macrocell array containing 16 macrocells, an expander product term array containing 32 expanders, and an I/O block. The LAB is fed by the programmable interconnect array and the dedicated input bus. All macrocell feedbacks go to the macrocell array, the expander array, and the programmable interconnect array. Expanders feed themselves and the macrocell array. All I/O feedbacks go to the programmable interconnect array so that they may be accessed by macrocells in other LABs as well as the macrocells in the LAB in which they are situated.

Externally, the CY7C341 provides 8 dedicated inputs, one of which may be used as a system clock. There are 64 I/O pins that may be individually configured for input, output, or bidirectional data flow.

Programmable Interconnect Array

The Programmable Interconnect Array (PIA) solves interconnect limitations by routing only the signals needed by each logic array block. The inputs to the PIA are the outputs of every macrocell within the device and the I/O pin feedback of every pin on the device.

Unlike masked or programmable gate arrays, which induce variable delay dependent on routing, the PIA has a fixed delay. This eliminates undesired skews among logic signals, which may cause glitches in internal or external logic. The fixed delay, regardless of programmable interconnect array configuration, simplifies design by assuring that internal signal skews or races are avoided. The result is ease of design implementation, often in a single pass, without the multiple internal logic placement and routing iterations required for a programmable gate array to achieve design timing objectives.

Timing Delays

Timing delays within the CY7C341 may be easily determined using MAX+PLUS® software or by the model shown in *Figure 1*. The CY7C341 has fixed internal delays, allowing the user to determine the worst case timing delays for any design. For complete timing information, the MAX+PLUS software provides a timing simulator.

Design Recommendations

For proper operation, input and output pins must be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 µF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled to GND, directly at the device. Decoupling capacitors should have good frequency response, such as monolithic ceramic types.

Design Security

The CY7C341 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

The CY7C341 is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

The erasable nature of these devices allows test programs to be used and erased during early stages of the production flow. The devices also contain on-board logic test circuitry to allow verification of function and AC specification once encapsulated in non-windowed packages.

Selection Guide

		7C341-30	7C341-35	7C341-40
Maximum Access Time (ns)		30	35	40
Maximum Operating Current (mA)	Commercial	310	310	40
	Military		320	320
Maximum Standby Current (mA)	Commercial	200	200	
	Military		240	240

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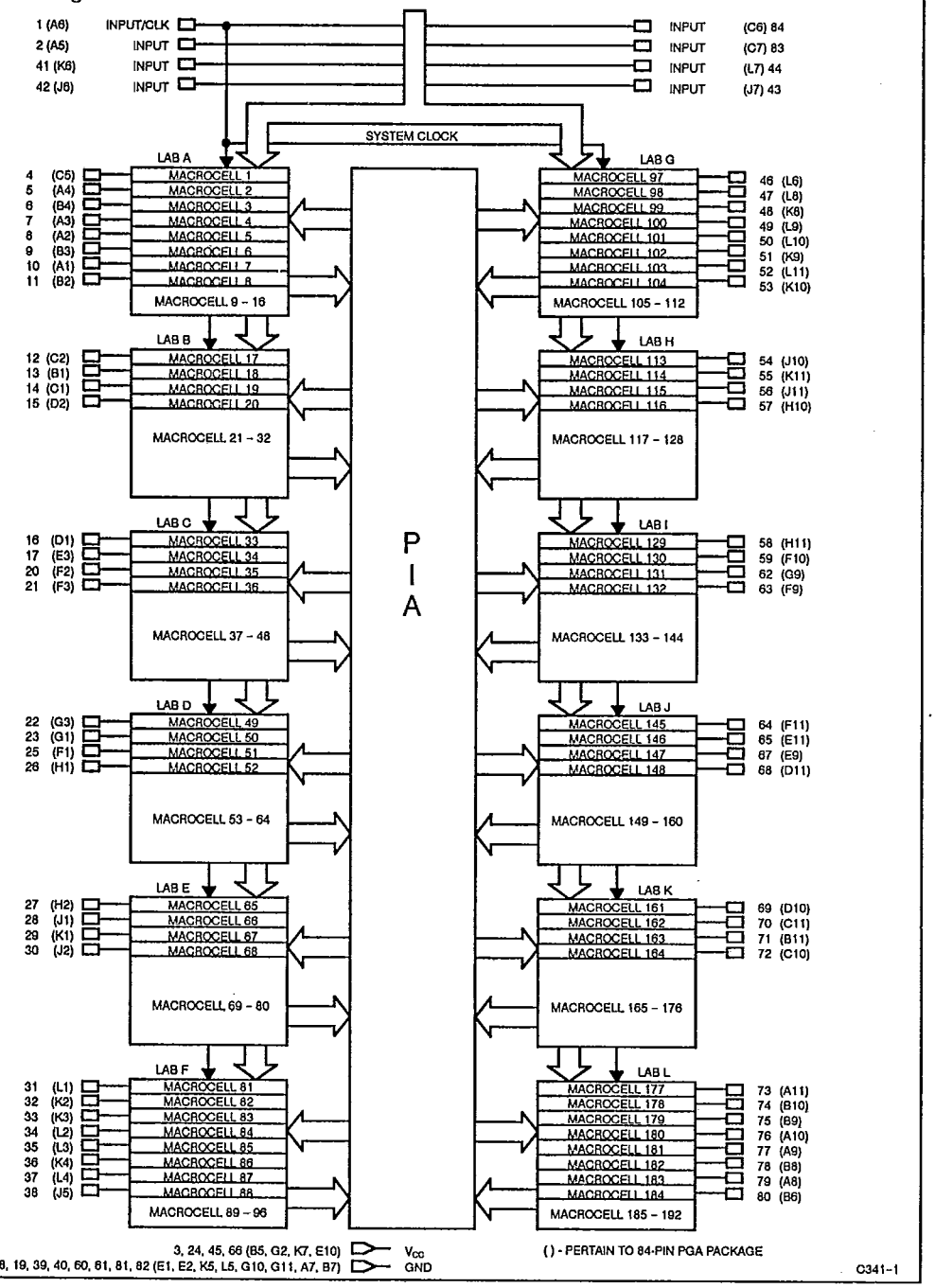
Logic Block Diagram



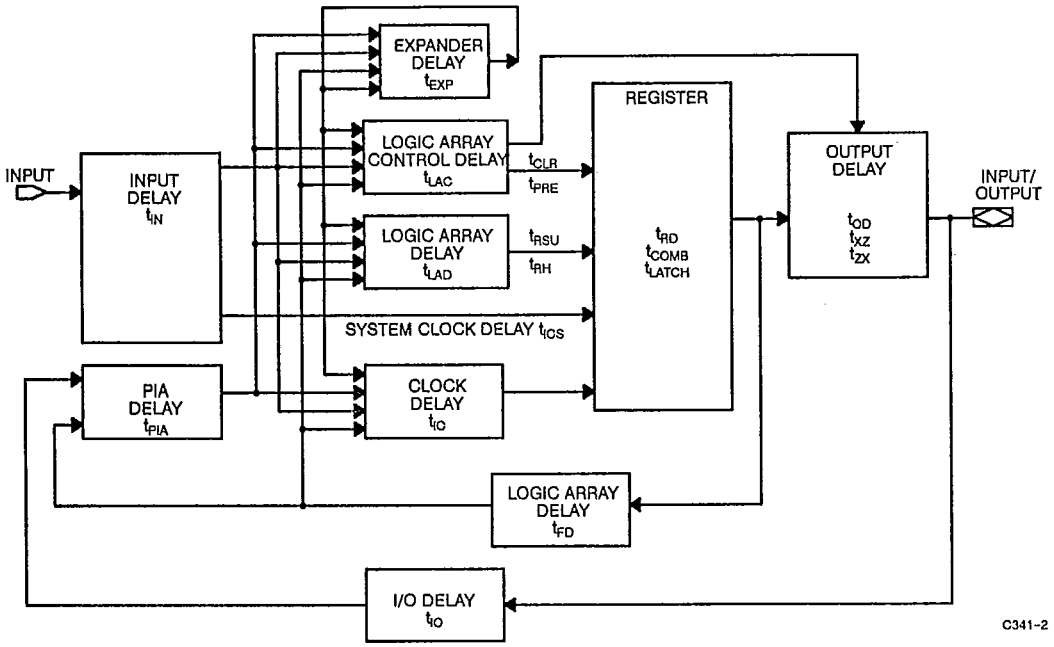


Figure 1. CY7C341 Internal Timing Model

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... 0°C to +70°C

Maximum Junction Temperature (Under Bias) ..... 150°C

Supply Voltage to Ground Potential ..... −2.0V to +7.0V

Maximum Power Dissipation ..... 2500 mW

DC V_{CC} or GND Current ..... 500 mA

DC Output Current, per Pin ..... −25 mA to +25 mA

DC Input Voltage[1] ..... −2.0V to +7.0V

DC Program Voltage ..... −2.0V to +13.5V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 5%
Industrial	−40°C to + 85°C	5V ± 10%
Military	−55°C to + 125°C (Case)	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C341 Min.	7C341 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA			0.45	V
V_{IH}	Input HIGH Level			2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Level			−0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	µA
I_{OZ}	Output Leakage Current	V_O = V_{CC} or GND		−40	+40	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		−30	−90	mA
I_{CC1}	Power Supply Current (Standby)	V_I = V_{CC} or GND (No Load)	Com'l		200	mA
			Mil		240	mA
I_{CC2}	Power Supply Current[3]	V_I = V_{CC} or GND (No Load) f = 1.0 MHz[3]	Com'l		310	mA
			Mil		320	mA

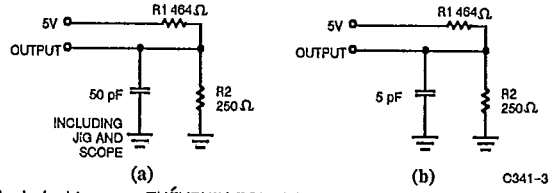
Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

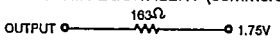
Notes:

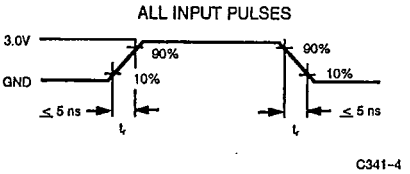
1. Minimum DC input is −0.3V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.
2. Typical values are for T_A = 25°C and V_{CC} = 5V.
3. This parameter is measured with device programmed as a 16-bit counter in each LAB and is tested periodically by sampling production material.
4. Part (a) in AC Test Load and Waveforms is used for all parameters except t_{ER} and t_{XZ}, which is used for part (b) in AC Test Load and Waveforms. All external timing parameters are measured referenced to external pins of the device.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT (commercial/military)





External Synchronous Switching Characteristics Over the Operating Range[4]

Parameters	Description		7C341-30		7C341-35		7C341-40		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[5]	Com'l		30		35			ns
		Mil				35		40	
t_{PD2}	I/O Input to Combinatorial Output Delay[6]	Com'l		45		55			ns
		Mil				55		65	
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[7]	Com'l		44		55			ns
		Mil				55		65	
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[8]	Com'l		60		75			ns
		Mil				75		90	
t_{EA}	Input to Output Enable Delay[5]	Com'l		30		35			ns
		Mil				35		40	
t_{ER}	Input to Output Disable Delay[5]	Com'l		30		35			ns
		Mil				35		40	
t_{CO1}	Synchronous Clock Input to Output Delay	Com'l		16		20			ns
		Mil				20		23	
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[9]	Com'l		35		42			ns
		Mil				42		50	
t_{S1}	Dedicated Input or Feedback Set-up Time to Synchronous Clock Output[5,10]	Com'l	22		25				ns
		Mil			25		28		
t_{S2}	I/O Input Set-up Time to Synchronous Clock Input[6]	Com'l	39		45				ns
		Mil			45		52		
t_H	Input Hold Time from Synchronous Clock Input[5]	Com'l	0		0				ns
		Mil			0		0		
t_{WH}	Synchronous Clock Input High Time	Com'l	10		12.5				ns
		Mil			12.5		15		
t_{WL}	Synchronous Clock Input Low Time	Com'l	10		12.5				ns
		Mil			12.5		15		
t_{RW}	Asynchronous Clear Width[5]	Com'l	30		35				ns
		Mil			35		40		
t_{RR}	Asynchronous Clear Recovery[5]	Com'l	30		35				ns
		Mil			35		40		
t_{RO}	Asynchronous Clear to Registered Output Delay[5]	Com'l	30		35				ns
		Mil			35		40		
t_{PW}	Asynchronous Preset Width[5]	Com'l	30		35				ns
		Mil			35		40		
t_{PR}	Asynchronous Preset Recovery Time[5]	Com'l	30		35				ns
		Mil			35		40		

External Synchronous Switching Characteristics Over the Operating Range[4](continued)

Parameters	Description		7C341-30 Min.	7C341-30 Max.	7C341-35 Min.	7C341-35 Max.	7C341-40 Min.	7C341-40 Max.	Units
t_{PO}	Asynchronous Preset to Registered Output Delay[5]	Com'l		30		35			ns
		Mil				35		40	
t_{CF}	Synchronous Clock to Local Feedback Input[11]	Com'l		3		6			ns
		Mil				6		9	
t_P	External Synchronous Clock Period ($t_{CO1} + t_{S1}$)	Com'l	38		45				ns
		Mil			45		51		
f_{MAX1}	External Feedback Maximum Frequency ($1/(t_{CO1} + t_{S1})$)[12]	Com'l	26.3		22.2				MHz
		Mil			22.2		19.6		
f_{MAX2}	Internal Local Feedback Maximum Frequency, lesser of ($1/(t_{S1} + t_{CF})$) or ($1/t_{CO1}$)[13]	Com'l	40.0		32.2				MHz
		Mil			32.2		28.5		
f_{MAX3}	Data Path Maximum Frequency, least of $1/(t_{WL} + t_{WH})$, $1/(t_{S1} + t_H)$, or ($1/t_{CO1}$)[14]	Com'l	45.4		40.0				MHz
		Mil			40.0		33.3		
f_{MAX4}	Maximum Register Toggle Frequency ($1/(t_{WL} + t_{WH})$)[15]	Com'l	50.0		40.0				MHz
		Mil			40.0		33.3		
t_{OH}	Output Data Stable Time from Synchronous Clock Input[16]	Com'l	3		3				ns
		Mil			3		3		

Notes:

5. This specification is a measure of the delay from input signal applied to a dedicated input (68-pin PLCC input pin 1, 2, 32, 34, 35, 66, or 68) to combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function.
   When this note is applied to any parameter specification it indicates that the signal (data, asynchronous clock, asynchronous clear, and/or asynchronous preset) is applied to a dedicated input only and no signal path (either clock or data) employs expander logic.
   If an input signal is applied to an I/O pin an additional delay equal to t_{PIA} should be added to the comparable delay for a dedicated input. If expanders are used, add the maximum expander delay t_{EXP} to the overall delay for the comparable delay without expanders.
6. This specification is a measure of the delay from input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
7. This specification is a measure of the delay from an input signal applied to a dedicated input (68-pin PLCC input pin 1, 2, 32, 34, 35, 36, 66, or 68) to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic functions and includes the worst-case expander logic delay for one pass through the expander logic.
8. This specification is a measure of the delay from an input signal applied to an I/O macrocell pin to any output. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
9. This specification is a measure of the delay from synchronous register clock to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used, register is synchronously clocked and all feedback is within the same LAB. This parameter is tested periodically by sampling production material.
10. If data is applied to an I/O input for capture by a macrocell register, the I/O pin set-up time minimums should be observed. These parameters are t_{S2} for synchronous operation and t_{AS2} for asynchronous operation.
11. This specification is a measure of the delay associated with the internal register feedback path. This is the delay from synchronous clock to LAB logic array input. This delay plus the register set-up time, t_{S1}, is the minimum internal period for an internal synchronous state machine configuration. This delay is for feedback within the same LAB. This parameter is tested periodically by sampling production material.
12. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which a state machine configuration with external feedback can operate. It is assumed that all data inputs and feedback signals are applied to dedicated inputs. All feedback is assumed to be local originating within the same LAB.
13. This specification indicates the guaranteed maximum frequency at which a state machine, with internal-only feedback, can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{CO1}$.
14. This frequency indicates the maximum frequency at which the device may operate in data path mode (dedicated input pin to output pin). This assumes data input signals are applied to dedicated input pins and no expander logic is used. If any of the data inputs are I/O pins, t_{S2} is the appropriate t_S for calculation.
15. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which an individual output or buried register can be cycle by a clock signal applied to the dedicated clock input pin.
16. This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.

External Asynchronous Switching Characteristics Over the Operating Range[4] (continued)

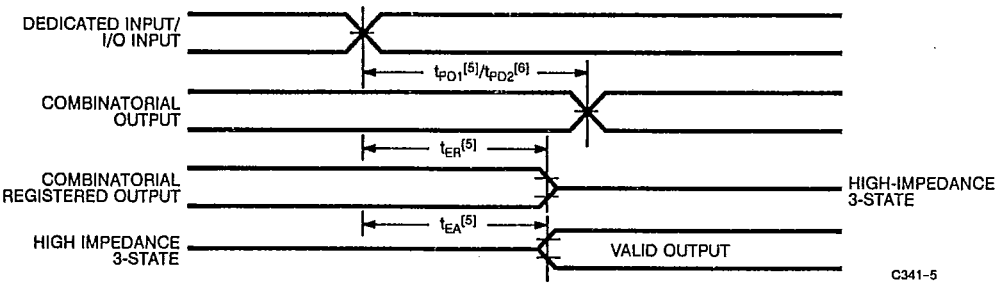
Parameters	Description		7C341-30		7C341-35		7C341-40		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACO1}	Dedicated Clock Input to Output Delay[5]	Com'l		30		35			ns
		Mil				35		45	
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output [17]	Com'l		46		55			ns
		Mil				55		64	
t_{AS1}	Dedicated Input or Feedback Set-up Time to Asynchronous Clock Input[5]	Com'l	10		10				ns
		Mil			10		10		
t_{AS2}	I/O Input Set-Up Time to Asynchronous Clock Input[5]	Com'l	27		30				ns
		Mil			30		33		
t_{AH}	Input Hold Time from Asynchronous Clock Input[5]	Com'l	15		15				ns
		Mil			15		15		
t_{AWH}	Asynchronous Clock Input High Time[5]	Com'l	25		30				ns
		Mil			30		35		
t_{AWL}	Asynchronous Clock Input Low Time[5]	Com'l	25		30				ns
		Mil			30		35		
t_{ACF}	Aynchronous Clock to Local Feedback Input[18]	Com'l		18		22			ns
		Mil				22		26	
t_{AP}	External Asynchronous Clock Period ($t_{ACO1} + t_{AS1}$) or ($t_{AWH} + t_{AWL}$)	Com'l	50		60				ns
		Mil			60		70		
f_{MAXA1}	External Feedback Maximum Frequency in Asynchronous Mode[19]	Com'l	20		16.6				MHz
		Mil			16.6		14.2		
f_{MAXA2}	Maximum Internal Asynchronous Frequency[20]	Com'l	20		16.6				MHz
		Mil			16.6		14.2		
f_{MAXA3}	Data Path Maximum Frequncy in Asynchronous Mode[21]	Com'l	20		16.6				MHz
		Mil			16.6		14.2		
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[22]	Com'l	20		16.6				MHz
		Mil			16.6		14.2		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[23]	Com'l	15		15				ns
		Mil			15		15		

Notes:

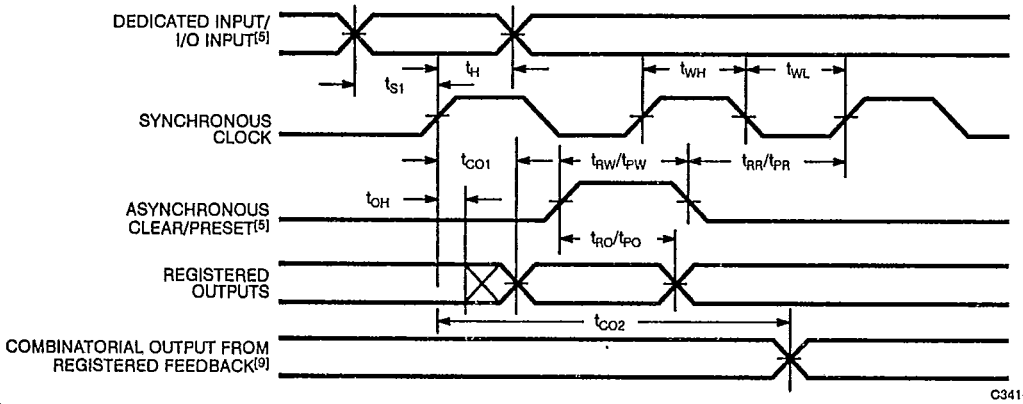
17. This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used in the logic of combinatorial output or the asynchronous clock input. The clock signal is applied to the dedicated clock input pin and all feedback is within a single LAB. This parameter is tested periodically by sampling production material.
18. This specification is a measure of the delay associated with the internal register feedback path for an asynchronous clock to LAB logic array input. This delay plus the asynchronous register set-up time, t_{AS1}, is the minimum internal period for an internal asynchronously clocked state machine configuration. This delay is for feedback within the same LAB, and assumes no expander logic in the clock path and the clock input signal is applied to a dedicated input pin. This parameter is tested periodically by sampling production material.
19. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that all data inputs, clock inputs, and feedback signals are applied to dedicated inputs, and that no expander logic is employed in the clock signal path or data path.
20. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal-only feedback can operate. This parameter is determined by the lesser of $(1/t_{ACF} + t_{AS})$ or $(1/(t_{AWH} + t_{AWL}))$. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO1}$.
21. This frequency is the maximum frequency at which the device may operate in the asynchronously clocked data path mode. This specification is determined by the least of $1/(t_{AWH} + t_{AWL})$, $1/(t_{AS1} + t_{AH})$ or $1/t_{ACO1}$. It assumes data and clock input signals are applied to dedicated input pins and no expander logic is used.
22. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input pin.
23. This parameter indicates the minimum time that the previous register output data is maintained on the output after an asynchronous register clock input applied to an external dedicated input pin.

Switching Waveforms

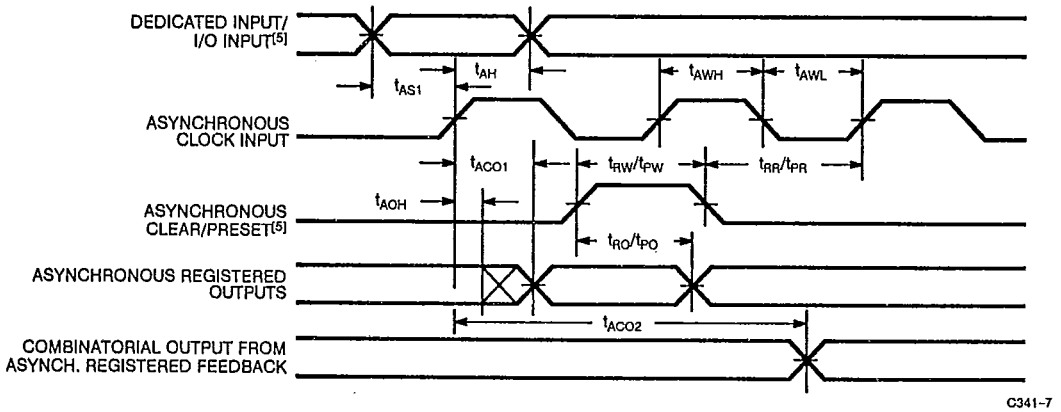
External Combinatorial



External Synchronous



External Asynchronous



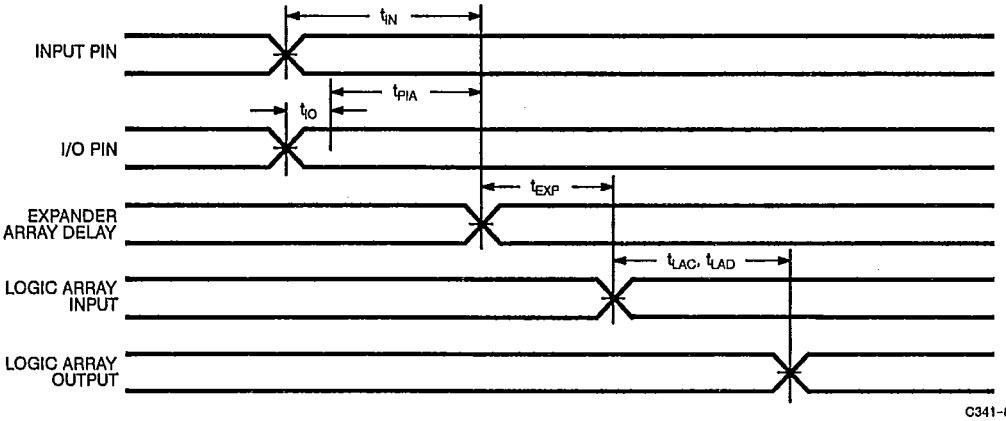
Internal Switching Characteristics Over the Operating Range[1]

Parameters	Description		7C341-30		7C341-35		7C341-40		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l		7		9			ns
		Mil				9		11	
t_{IO}	I/O Input Pad and Buffer Delay	Com'l		6		9			ns
		Mil				9		12	
t_{EXP}	Expander Array Delay	Com'l		14		20			ns
		Mil				20		25	
t_{LAD}	Logic Array Data Delay	Com'l		14		16			ns
		Mil				16		18	
t_{LAC}	Logic Array Control Delay	Com'l		12		13			ns
		Mil				13		14	
t_{OD}	Output Buffer and Pad Delay	Com'l		5		6			ns
		Mil				6		7	
t_{ZX}	Output Buffer Enable Delay[24]	Com'l		11		13			ns
		Mil				13		15	
t_{XZ}	Output Buffer Disable Delay	Com'l		11		13			ns
		Mil				13		15	
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	Com'l	8		10				ns
		Mil			10		12		
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l	8		10				ns
		Mil			10		12		
t_{LATCH}	Flow-Through Latch Delay	Com'l		4		4			ns
		Mil				4		4	
t_{RD}	Register Delay	Com'l		2		2			ns
		Mil				2		2	
t_{COMB}	Transparent Mode Delay[25]	Com'l		4		4			ns
		Mil				4		4	
t_{CH}	Clock High Time	Com'l	10		12.5				ns
		Mil			12.5		15		
t_{CL}	Clock Low Time	Com'l	10		12.5				ns
		Mil			12.5		15		
t_{IC}	Asynchronous Clock Logic Delay	Com'l		16		18			ns
		Mil				18		20	
t_{ICS}	Synchronous Clock Delay	Com'l		2		3			ns
		Mil				3		4	
t_{FD}	Feedback Delay	Com'l		1		2			ns
		Mil				2		3	
t_{PRE}	Asynchronous Register Preset Time	Com'l		6		7			ns
		Mil				7		8	
t_{CLR}	Asynchronous Register Clear Time	Com'l		6		7			ns
		Mil				7		8	
t_{PCW}	Asynchronous Preset and Clear Pulse Width	Com'l	6		7				ns
		Mil			7		8		
t_{PCR}	Asynchronous Preset and Clear Recovery Time	Com'l	6		7				ns
		Mil			7		8		
t_{PIA}	Programmable Interconnect Array Delay Time	Com'l		16		20			ns
		Mil				20		24	

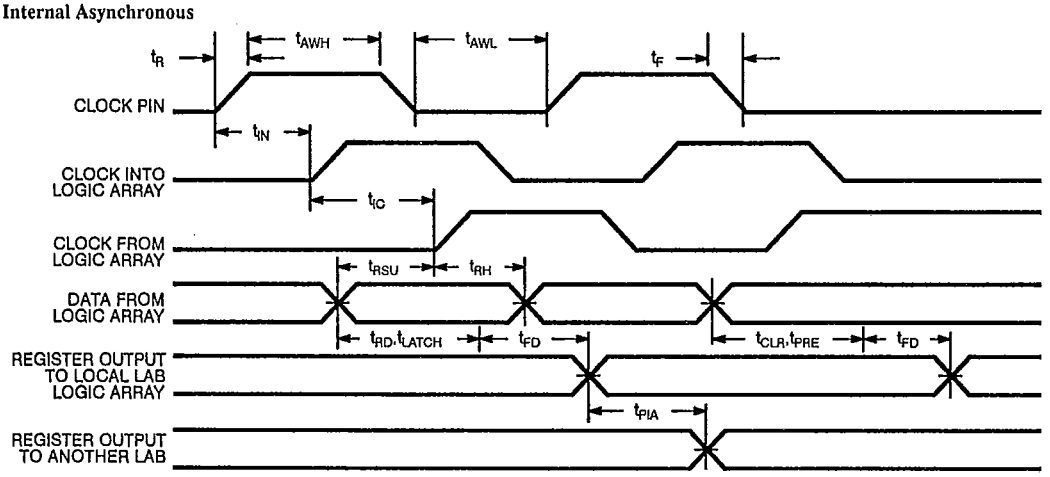
Notes:
24. Sample tested only for an output change of 500 mV.
25. This specification guarantees the maximum combinatorial delay associated with the macrocell register bypass when the macrocell is configured for combinatorial operation.

Switching Waveforms (continued)

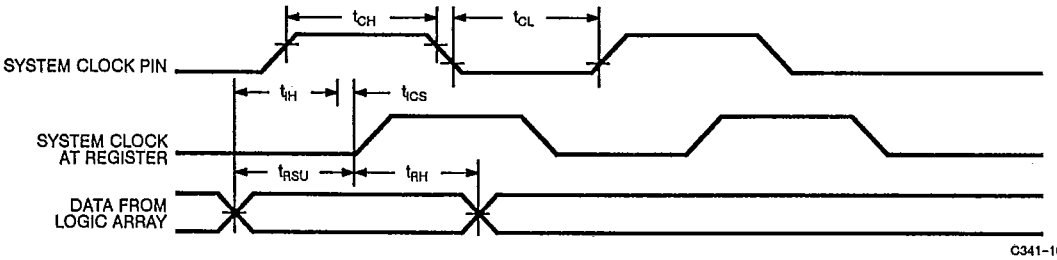
Internal Combinatorial



Internal Asynchronous

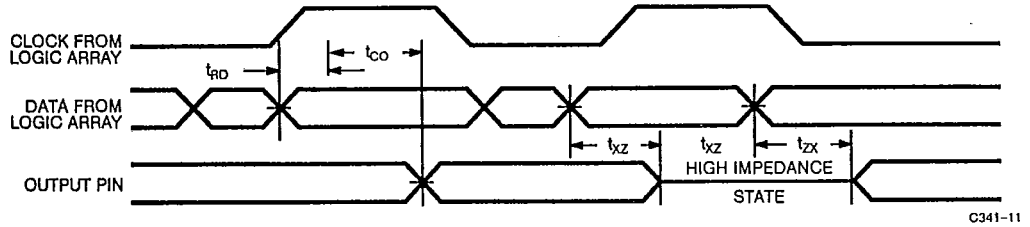


External Asynchronous



Switching Waveforms (continued)

Internal Synchronous



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
30	CY7C341-30HC		Commercial
	CY7C341-30JC		
	CY7C341-30RC		
	CY7C341-30GC		
35	CY7C341-35HC		Commercial
	CY7C341-35JC		
	CY7C341-35RC		
	CY7C341-35GC		
	CY7C341-35HMB		Military
	CY7C341-35RMB		
40	CY7C341-40HC		Commercial
	CY7C341-40JC		
	CY7C341-40RC		
	CY7C341-40GC		
	CY7C341-40HMB		Military
	CY7C341-40RMB		

Document #: 38-00137-B

T-46-13-47

CY7C342

CYPRESS SEMICONDUCTOR

128-Macrocell MAX™ EPLDs

Features

- 128 macrocells in 8 LABs
- 8 dedicated inputs, 52 bidirectional I/O pins
- Programmable interconnect array
- Available in 68-pin HLCC, PLCC, and PGA

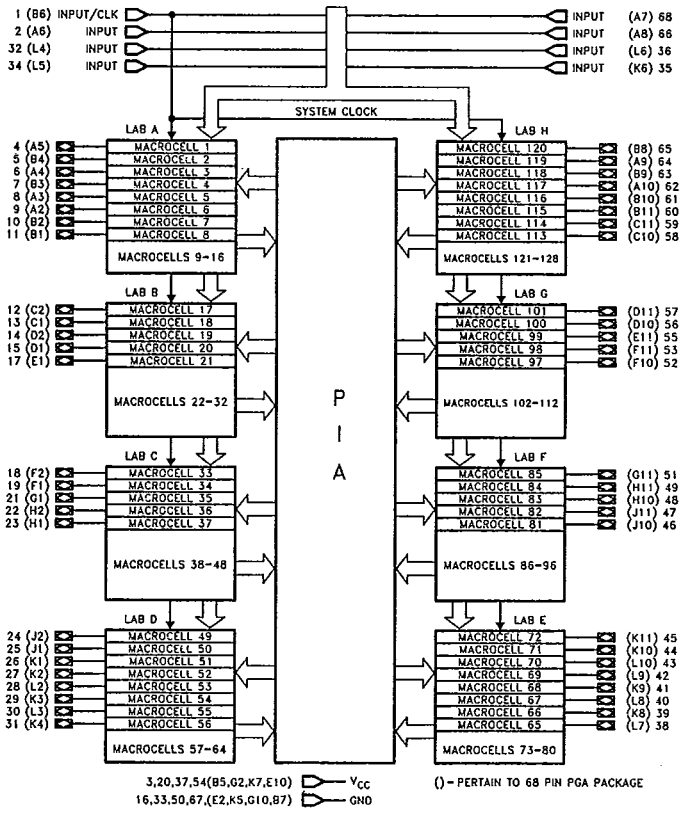
Functional Description

The CY7C342 is an Erasable Programmable Logic Device (EPLD) in which CMOS EPROM cells are used to configure logic functions within the device. The MAX architecture is 100% user configurable, allowing the devices to accommodate a variety of independent logic functions.

The 128 macrocells in the CY7C342 are divided into 8 Logic Array Blocks (LABs), 16 per LAB. There are 256 expander product terms, 32 per LAB, to be used and shared by the macrocells within each LAB. Each LAB is interconnected with a programmable interconnect array, allowing all signals to be routed throughout the chip.

The speed and density of the CY7C342 allows it to be used in a wide range of applications, from replacement of large amounts of 7400 series TTL logic, to complex controllers and multi-function chips. With greater than 25 times the functionality of 20-pin PLDs, the CY7C342 allows the replacement of over 50 TTL devices. By replacing large amounts of logic, the CY7C342 reduces board space, part count, and increases system reliability.

Logic Block Diagram



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CYPRESS SEMICONDUCTOR

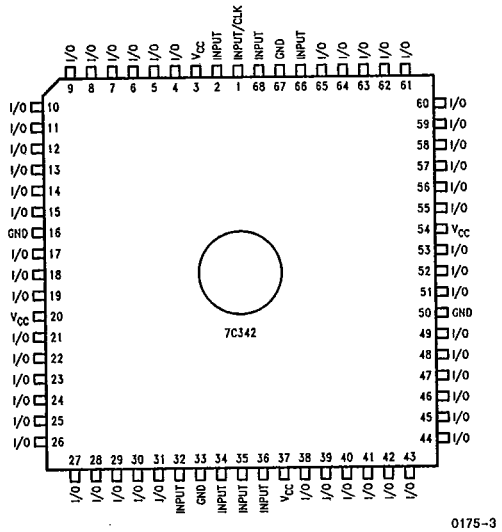
CY7C342

T-46-13-47

Selection Guide

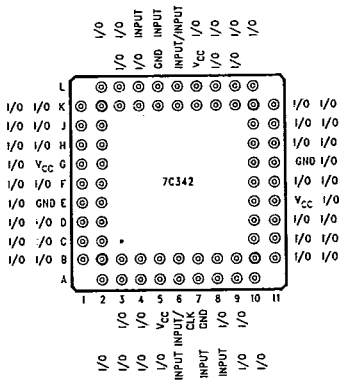
		7C342-30	7C342-35	7C342-40
Maximum Access Time (ns)		30	35	40
Maximum Operating Current (mA)	Commercial	310	310	
	Military		320	320
	Industrial	320	320	320
Maximum Standby Current (mA)	Commercial	200	200	
	Military		240	240
	Industrial	240	240	240

Pin Configurations



0175-3

PGA
Bottom View



0175-4

Logic Array Blocks

There are eight logic array blocks in the CY7C342. Each LAB consists of a macrocell array containing 16 macrocells, an expander product term array containing 32 expanders, and an I/O block. The LAB is fed by the programmable interconnect array and the dedicated input bus. All macrocell feedbacks go to the macrocell array, the expander array, and the programmable interconnect array. Expanders feed themselves and the macrocell array. All I/O feedbacks go to the programmable interconnect array so that they may be accessed by macrocells in other LABs as well as the macrocells in the LAB in which they are situated.

Externally, the CY7C342 provides eight dedicated inputs, one of which may be used as a system clock. There are 52 I/O pins which may be individually configured for input, output, or bidirectional data flow.

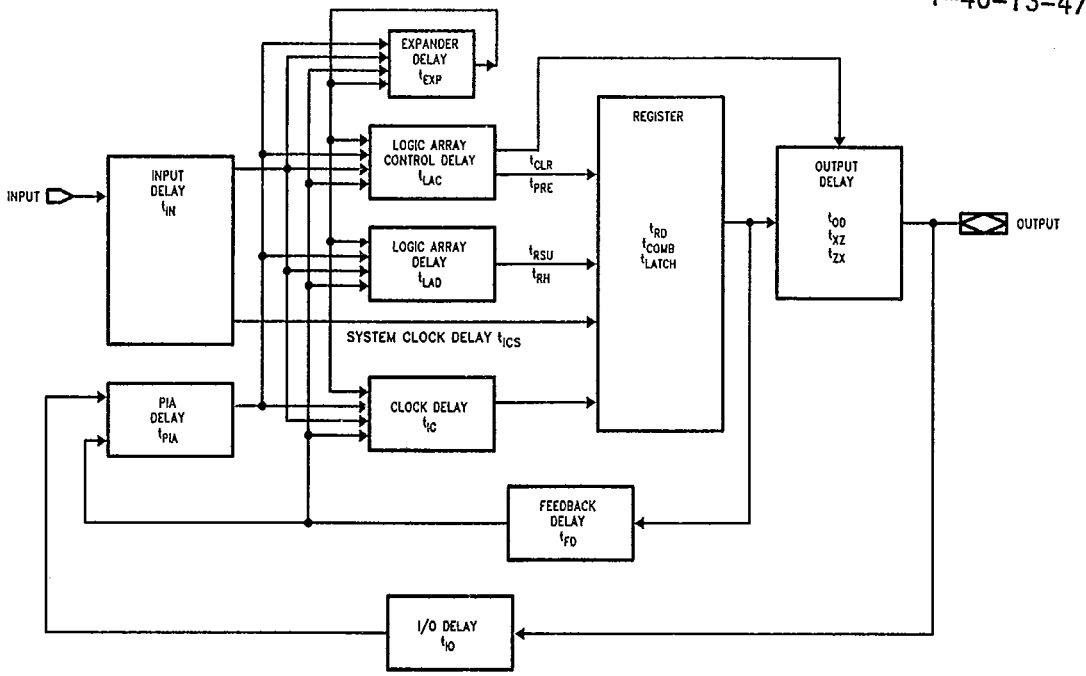


Figure 3. CY7C342 Internal Timing Model

Programmable Interconnect Array

The Programmable Interconnect Array (PIA) solves interconnect limitations by routing only the signals needed by each logic array block. The inputs to the PIA are the outputs of every macrocell within the device and the I/O pin feedback of every pin on the device.

Unlike masked or programmable gate arrays, which induce variable delay dependent on routing, the PIA has a fixed delay. This eliminates undesired skews among logic signals, which may cause glitches in internal or external logic. The fixed delay, regardless of programmable interconnect array configuration, simplifies design by assuring that internal signal skews or races are avoided. The result is ease of design implementation, often in a single pass, without the multiple internal logic placement and routing iterations required for a programmable gate array to achieve design timing objectives.

Timing Delays

Timing delays within the CY7C342 may be easily determined using MAX + PLUS™ software or by the model shown in *Figure 3*. The CY7C342 has fixed internal delays, allowing the user to determine the worst case timing delays for any design. For complete timing information the MAX + PLUS software provides a timing simulator.

Design Recommendations

Operation of the devices described herein with conditions above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability. The CY7C342 contains circuitry to protect device pins from high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

For proper operation, input and output pins must be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 μF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled to GND, directly at the device. Decoupling capacitors should have good frequency response, such as monolithic ceramic types.

Design Security

The CY7C342 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a propriety design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

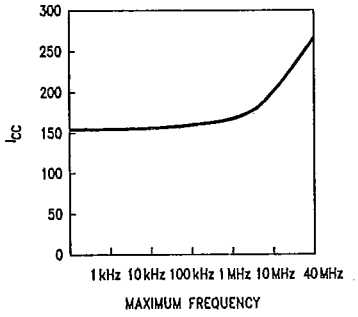


Figure 4. Typical I_{CC} vs f_{MAX}

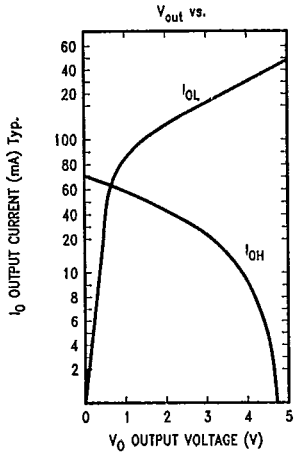


Figure 5. Output Drive Current

The CY7C342 is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

The erasable nature of these devices allows test programs to be used and erased during early stages of the production flow. The devices also contain on-board logic test circuitry to allow verification of function and AC specification once encapsulated in non-windowed packages.

Timing Considerations

Unless otherwise stated, propagation delays do not include expanders. When using expanders add the maximum expander delay t_{EXP} to the overall delay. Similarly, there is an additional t_{PIA} delay for an input from an I/O pin when compared to a signal from a straight input pin.

When calculating synchronous frequencies, use t_{S_1} if all inputs are on dedicated input pins. The parameter t_{S_2} should be used if data is applied at an I/O pin. If t_{S_2} is greater than t_{CO_1}, $1/t_{S_2}$ becomes the limiting frequency in the data path mode unless $1/(t_{WH} + t_{WL})$ is less than $1/t_{S_2}$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{S_1}. Determine which of $1/(t_{WH} + t_{WL})$, $1/t_{CO_1}$, or $1/(t_{EXP} + t_{S_1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the synchronous configuration.

When calculating external asynchronous frequencies, use t_{AS_1} if all inputs are on the dedicated input pins. If any data is applied to an I/O pin, t_{AS_2} must be used as the required set up time. If $(t_{AS_2} + t_{AH})$ is greater than t_{ACO_1}, $1/(t_{AS_2} + t_{AH})$ becomes the limiting frequency in the data path mode unless $1/(t_{AWH} + t_{AWL})$ is less than $1/(t_{AS_2} + t_{AH})$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{AS_1}. Determine which of $1/(t_{AWH} + t_{AWL})$, $1/t_{ACO_1}$, or $1/(t_{EXP} + t_{AS_1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the asynchronous configuration.

The parameter t_{OH} indicates the system compatibility of this device when driving other synchronous logic with positive input hold times, which is controlled by the same synchronous clock. If t_{OH} is greater than the minimum required input hold time of the subsequent synchronous logic, then the devices are guaranteed to function properly with a common synchronous clock under worst-case environmental and supply voltage conditions.

The parameter t_{AOH} indicates the system compatibility of this device when driving subsequent registered logic with a positive hold time and using the same clock as the CY7C342.

In general, if t_{AOH} is greater than the minimum required input hold time of the subsequent logic (synchronous or asynchronous) then the devices are guaranteed to function properly under worst-case environmental and supply voltage conditions, provided the clock signal source is the same. This also applies if expander logic is used in the clock signal path of the driving device, but not for the driven device. This is due to the expander logic in the second device's clock signal path adding an additional delay (t_{EXP}) causing the output data from the preceding device to change prior to the arrival of the clock signal at the following device's register.

CYPRESS SEMICONDUCTOR

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... 0°C to +70°C

Maximum Junction Temperature (Under Bias) ..... 150°C

Supply Voltage to Ground Potential .... −2.0V to +7.0V

Maximum Power Dissipation ..... 2500 mW

DC V_{CC} or GND Current ..... 500 mA

DC Output Current, per Pin ..... −25 mA to +25 mA

DC Input Voltage[1] ..... −2.0V to +7.0V

DC Program Voltage..... −2.0V to +13.5V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±5%
Industrial	−40°C to +85°C	5V ±10%
Military	−55°C to + 125°C (Case)	5V ±10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA			0.45	V
V_{IH}	Input HIGH Level			2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Level			−0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Leakage Current	V_O = V_{CC} or GND		−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3, 4]		−30	−90	mA
I_{CC_1}	Power Supply Current (Standby)	V_I = V_{CC} or GND (No Load)	Commercial		200	mA
			Military/Industrial		240	mA
I_{CC_2}	Power Supply Current[5]	V_I = V_{CC} or GND (No Load) f = 1.0 MHz[4]	Commercial		310	mA
			Military/Industrial		320	mA

Capacitance[6]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 2V, f = 1.0 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, f = 1.0 MHz	10	

Notes:

1. Minimum DC input is −0.3V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.
2. Typical values are for T_A = 25°C and V_{CC} = 5V.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Guaranteed but not 100% tested.
5. This parameter is measured with device programmed as a 16-bit counter in each LAB.
6. *Figure 1a* in AC Test Load and Waveforms is used for all parameters except t_{ER} and t_{XZ}, which is used for *Figure 1b* in AC Test Load and Waveforms. All external timing parameters are measured referenced to external pins of the device.

AC Test Loads and Waveforms[6]

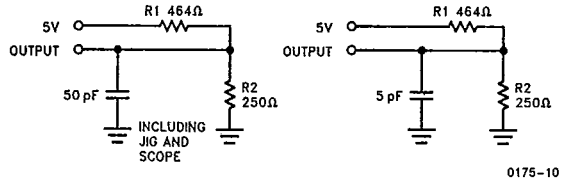
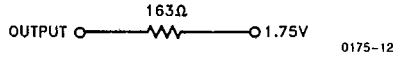


Figure 1a

Figure 1b

Equivalent to: THÉVENIN EQUIVALENT (Commercial/Military)



Input Pulses

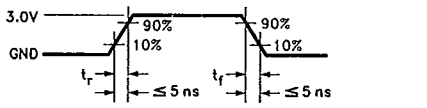


Figure 2

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External Synchronous Switching Characteristics[6] Over Operating Range

Parameters	Description		CY7C342-30		CY7C342-35		CY7C342-40		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD_1}	Dedicated Input to Combinatorial Output Delay[7]	Com'l/Ind		30		35			ns
		Mil				35		40	
t_{PD_2}	I/O Input to Combinatorial Output Delay[8]	Com'l/Ind		45		55			ns
		Mil				55		65	
t_{PD_3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[9]	Com'l/Ind		44		55			ns
		Mil				55		65	
t_{PD_4}	I/O Input to Combinatorial Output Delay with Expander Delay[4, 10]	Com'l/Ind		60		75			ns
		Mil				75		90	
t_{EA}	Input to Output Enable Delay[4, 7]	Com'l/Ind		30		35			ns
		Mil				35		40	
t_{ER}	Input to Output Disable Delay[4, 7]	Com'l/Ind		30		35			ns
		Mil				35		40	
t_{CO_1}	Synchronous Clock Input to Output Delay	Com'l/Ind		16		20			ns
		Mil				20		23	
t_{CO_2}	Synchronous Clock to Local Feedback to Combinatorial Output[4, 11]	Com'l/Ind		35		42			ns
		Mil				42		50	
t_{S_1}	Dedicated Input or Feedback Setup Time to Synchronous Clock Input[7, 12]	Com'l/Ind	22		25				ns
		Mil			25		28		
t_{S_2}	I/O Input Setup Time to Synchronous Clock Input[7]	Com'l/Ind	39		45				ns
		Mil			45		52		
t_H	Input Hold Time from Synchronous Clock Input[7]	Com'l/Ind	0		0				ns
		Mil			0		0		
t_{WH}	Synchronous Clock Input High Time	Com'l/Ind	10		12.5				ns
		Mil			12.5		15		
t_{WL}	Synchronous Clock Input Low Time	Com'l/Ind	10		12.5				ns
		Mil			12.5		15		
t_{RW}	Asynchronous Clear Width[4, 7]	Com'l/Ind	30		35				ns
		Mil			35		40		
t_{RR}	Asynchronous Clear Recovery Time[4, 7]	Com'l/Ind	30		35				ns
		Mil			35		40		
t_{RO}	Asynchronous Clear to Registered Output Delay[7]	Com'l/Ind		30		35			ns
		Mil				35		40	
t_{PW}	Asynchronous Preset Width[4, 7]	Com'l/Ind	30		35				ns
		Mil			35		40		
t_{PR}	Asynchronous Preset Recovery Time[4, 7]	Com'l/Ind	30		35				ns
		Mil			35		40		
t_{PO}	Asynchronous Preset to Registered Output Delay[7]	Com'l/Ind		30		35			ns
		Mil				35		40	
t_{CF}	Synchronous Clock to Local Feedback Input[4, 13]	Com'l/Ind		3		6			ns
		Mil				6		9	
t_P	External Synchronous Clock Period ($t_{CO_1} + t_{S_1}$)[4]	Com'l/Ind	38		45				ns
		Mil			45		51		

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External Synchronous Switching Characteristics[6] Over Operating Range (Continued)

Parameters	Description		CY7C342-30		CY7C342-35		CY7C342-40		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX_1}	External Feedback Maximum Frequency $(1/(t_{CO_1} + t_{S_1}))$[4, 14]	Com'l/Ind	26.3		22.2				MHz
		Mil			22.2		19.6		
f_{MAX_2}	Internal Local Feedback Maximum Frequency, lesser of $1/(t_{S_1} + t_{CF})$ or $(1/t_{CO_1})$[4, 15]	Com'l/Ind	40.0		32.2				MHz
		Mil			32.2		28.5		
f_{MAX_3}	Data Path Maximum Frequency, least of $(1/(t_{WL} + t_{WH}))$, $(1/(t_{S_1} + t_H))$ or $(1/t_{CO_1})$[4, 16]	Com'l/Ind	45.4		40.0				MHz
		Mil			40.0		33.3		
f_{MAX_4}	Maximum Register Toggle Frequency $(1/(t_{WL} + t_{WH}))$[4, 17]	Com'l/Ind	50.0		40.0				MHz
		Mil			40.0		33.3		
t_{OH}	Output Data Stable Time from Synchronous Clock Input[4, 18]	Com'l/Ind	3		3				ns
		Mil			3		3		

Notes:

7. This specification is a measure of the delay from input signal applied to a dedicated input, (68-pin PLCC input pin 1, 2, 32, 34, 35, 66, or 68) to combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function.
   When this note is applied to any parameter specification it indicates that the signal (data, asynchronous clock, asynchronous clear, and/or asynchronous preset) is applied to a dedicated input only and no signal path (either clock or data) employs expander logic.
   If an input signal is applied to an I/O pin an additional delay equal to t_{PIA} should be added to the comparable delay for a dedicated input. If expanders are used add the maximum expander delay t_{EXP} to the overall delay for the comparable delay without expanders.
8. This specification is a measure of the delay from input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
9. This specification is a measure of the delay from an input signal applied to a dedicated input, (68-pin PLCC input pin 1, 2, 32, 34, 35, 36, 66, or 68) to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic.
10. This specification is a measure of the delay from an input signal applied to an I/O macrocell pin to any output. This delay assumes expander terms are used to form the logic function and includes the worst case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
11. This specification is a measure of the delay from synchronous register clock to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used, register is synchronously clocked and all feedback is within the same LAB. This parameter is tested periodically by sampling production material.
12. If data is applied to an I/O input for capture by a macrocell register, the I/O pin input set-up time minimums should be observed. These parameters are t_{S_2} for synchronous operation and t_{AS_2} for asynchronous operation.
13. This specification is a measure of the delay associated with the internal register feedback path. This is the delay from synchronous clock to LAB logic array input. This delay plus the register set-up time, t_{S_1}, is the minimum internal period for an internal synchronous state machine configuration. This delay is for feedback within the same LAB. This parameter is tested periodically by sampling production material.
14. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which a state machine configuration with external feedback can operate. It is assumed that all data inputs and feedback signals are applied to dedicated inputs. All feedback is assumed to be local originating within the same LAB.
15. This specification indicates the guaranteed maximum frequency at which a state machine with internal only feedback can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{CO_1}$.
16. This frequency indicates the maximum frequency at which the device may operate in data path mode (dedicated input pin to output pin). This assumes data input signals are applied to dedicated input pins and no expander logic is used. If any of the data inputs are I/O pins, t_{S_2} is the appropriate t_S for calculation.
17. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which an individual output or buried register can be cycled by a clock signal applied to the dedicated clock input pin.
18. This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.

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External Asynchronous Switching Characteristics[6] Over Operating Range

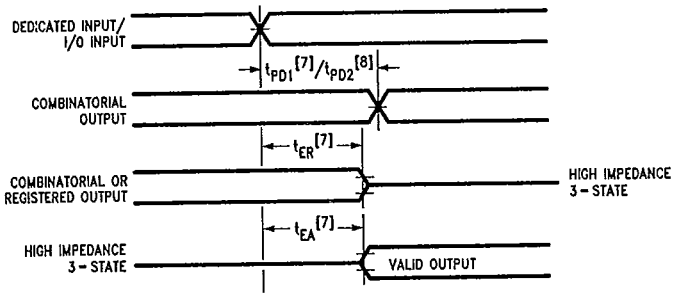
Parameters	Description		CY7C342-30		CY7C342-35		CY7C342-40		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACO1}	Asynchronous Clock Input to Output Delay[7]	Com'l/Ind		30		35			ns
		Mil				35		45	
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[19]	Com'l/Ind		46		55			ns
		Mil				55		64	
t_{AS1}	Dedicated Input or Feedback Setup Time to Asynchronous Clock Input[7]	Com'l/Ind	10		10				ns
		Mil			10		10		
t_{AS2}	I/O Input Setup Time to Asynchronous Clock Input[7]	Com'l/Ind	27		30				ns
		Mil			30		33		
t_{AH}	Input Hold Time from Asynchronous Clock Input[7]	Com'l/Ind	15		15				ns
		Mil			15		15		
t_{AWH}	Asynchronous Clock Input High Time[7]	Com'l/Ind	25		30				ns
		Mil			30		35		
t_{AWL}	Asynchronous Clock Input Low Time[7]	Com'l/Ind	25		30				ns
		Mil			30		35		
t_{ACF}	Asynchronous Clock to Local Feedback Input[4, 20]	Com'l/Ind		18		22			ns
		Mil				22		26	
t_{AP}	External Asynchronous Clock Period ($t_{ACO1} + t_{AS1}$) or ($t_{AWH} + t_{AWL}$)[4]	Com'l/Ind	50		60				ns
		Mil			60		70		
f_{MAXA1}	External Feedback Maximum Frequency in Asynchronous Mode ($1/t_{AP}$)[4, 21]	Com'l/Ind	20		16.6				MHz
		Mil			16.6		14.2		
f_{MAXA2}	Maximum Internal Asynchronous Frequency[4, 24]	Com'l/Ind	20		16.6				MHz
		Mil			16.6		14.2		
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[4, 23]	Com'l/Ind	20		16.6				MHz
		Mil			16.6		14.2		
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[4, 22]	Com'l/Ind	20		16.6				MHz
		Mil			16.6		14.2		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[4, 25]	Com'l/Ind	15		15				ns
		Mil			15		15		

Notes:

19. This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used in the logic of combinatorial output or the asynchronous clock input. The clock signal is applied to the dedicated clock input pin and all feedback is within a single LAB. This parameter is tested periodically by sampling production material.
20. This specification is a measure of the delay associated with the internal register feedback path for an asynchronous clock to LAB logic array input. This delay plus the asynchronous register setup time, t_{AS1}, is the minimum internal period for an internal asynchronously clocked state machine configuration. This delay is for feedback within the same LAB, assumes no expander logic in the clock path and assumes that the clock input signal is applied to a dedicated input pin. This parameter is tested periodically by sampling production material.
21. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that all data inputs, clock inputs, and feedback signals are applied to dedicated inputs and that no expander logic is employed in the clock signal path or data path.
22. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input pin.
23. This frequency is the maximum frequency at which the device may operate in the asynchronously clocked data path mode. This specification is determined by the least of $1/(t_{AWH} + t_{AWL})$, $1/(t_{AS1} + t_{AH})$ or $1/t_{ACO1}$. It asssumes data and clock input signals are applied to dedicated input pins and no expander logic is used.
24. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal only feedback can operate. This parameter is determined by the lesser of $(1/(t_{ACF} + t_{AS}))$ or $(1/(t_{AWH} + t_{AWL}))$. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO1}$.
    This specification assumes no expander logic is utilized, all data inputs and clock inputs are applied to dedicated inputs, and all state feedback is within a single LAB. This parameter is tested periodically by sampling production material.
25. This parameter indicates the minimum time that the previous register output data is maintained on the output after an asynchronous register clock input applied to an external dedicated input pin.

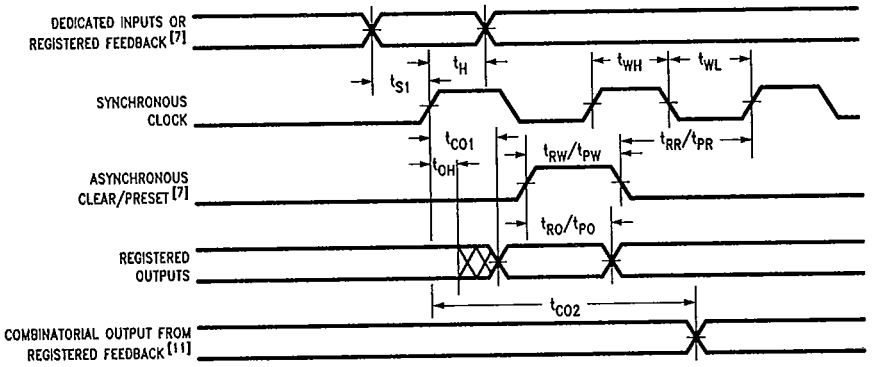
Switching Waveforms

External Combinatorial



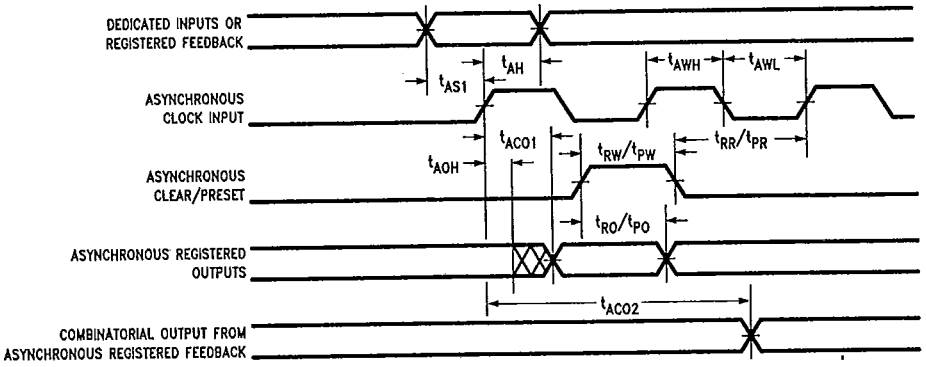
0175-13

External Synchronous



0175-14

External Asynchronous



0175-15

Typical Internal Switching Characteristics Over Operating Range

Parameters	Description		CY7C342-30		CY7C342-35		CY7C342-40		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l/Ind		7		9			ns
		Mil				9		11	
t_{IO}	I/O Input Pad and Buffer Delay	Com'l/Ind		6		9			ns
		Mil				9		12	
t_{EXP}	Expander Array Delay	Com'l/Ind		14		20			ns
		Mil				20		25	
t_{LAD}	Logic Array Data Delay	Com'l/Ind		14		16			ns
		Mil				16		18	
t_{LAC}	Logic Array Control Delay	Com'l/Ind		12		13			ns
		Mil				13		14	
t_{OD}	Output Buffer and Pad Delay	Com'l/Ind		5		6			ns
		Mil				6		7	
t_{ZX}	Output Buffer Enable Delay[26]	Com'l/Ind		11		13			ns
		Mil				13		15	
t_{XZ}	Output Buffer Disable Delay	Com'l/Ind		11		13			ns
		Mil				13		15	
t_{RSU}	Register Setup Time Relative to Clock Signal at Register	Com'l/Ind	8		10				ns
		Mil			10		12		
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l/Ind	8		10				ns
		Mil			10		12		
t_{LATCH}	Flow Through Latch Delay	Com'l/Ind		4		4			ns
		Mil				4		4	
t_{RD}	Register Delay	Com'l/Ind		2		2			ns
		Mil				2		2	
t_{COMB}	Transparent Mode Delay[27]	Com'l/Ind		4		4			ns
		Mil				4		4	
t_{CH}	Clock High Time	Com'l/Ind	10		12.5				ns
		Mil			12.5		15		
t_{CL}	Clock Low Time	Com'l/Ind	10		12.5				ns
		Mil			12.5		15		
t_{IC}	Asynchronous Clock Logic Delay	Com'l/Ind		16		18			ns
		Mil				18		20	
t_{ICS}	Synchronous Clock Delay	Com'l/Ind		2		3			ns
		Mil				3		4	
t_{FD}	Feedback Delay	Com'l/Ind		1		2			ns
		Mil				2		3	
t_{PRE}	Asynchronous Register Preset Time	Com'l/Ind		6		7			ns
		Mil				7		8	
t_{CLR}	Asynchronous Register Clear Time	Com'l/Ind		6		7			ns
		Mil				7		8	
t_{PCW}	Asynchronous Preset and Clear Pulse Width	Com'l/Ind	6		7				ns
		Mil			7		8		
t_{PCR}	Asynchronous Preset and Clear Recovery Time	Com'l/Ind	6		7				ns
		Mil			7		8		
t_{PIA}	Programmable Interconnect Array Delay Time	Com'l/Ind		16		20			ns
		Mil				20		24	

Notes:

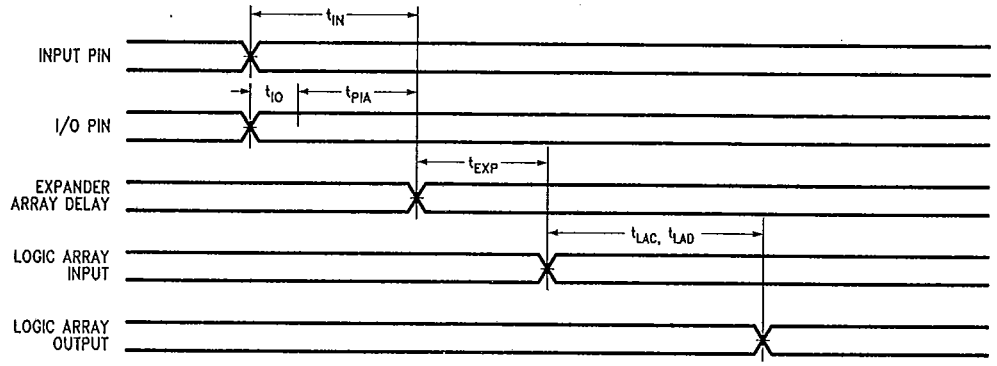
26. Sample tested only for an output change of 500 mV.

27. This specification guarantees the maximum combinatorial delay associated with the macrocell register bypass when the macrocell is configured for combinatorial operation.

Switching Waveforms (Continued)

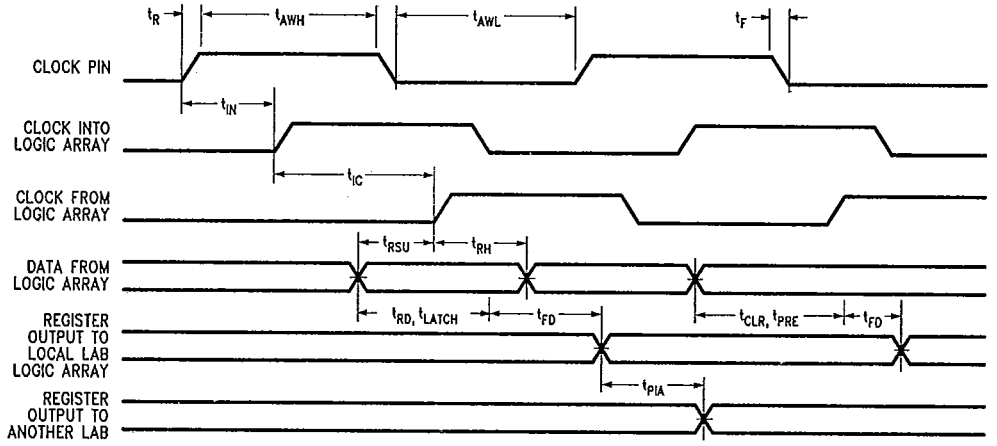
T-46-13-47

Internal Combinatorial



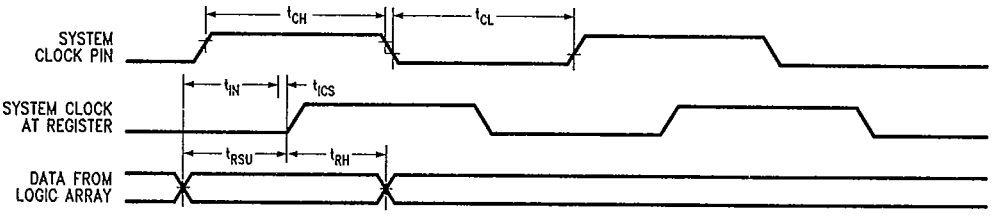
0175-16

Internal Asynchronous



0175-17

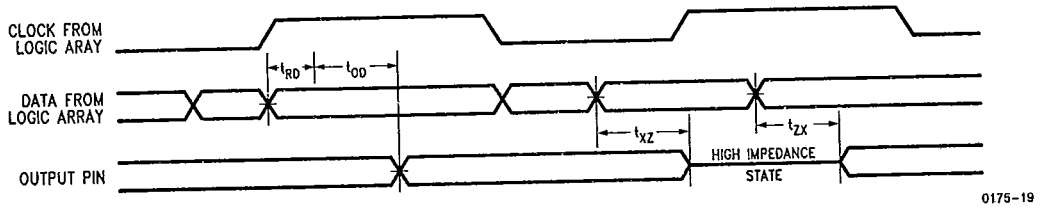
Internal Synchronous



0175-18

Switching Waveforms (Continued)

Internal Synchronous



0175-19

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
30	CY7C342-30HC/HI	H81	Commercial/ Industrial
	CY7C342-30JC/JI	J81	
	CY7C342-30RC/RI	R68	
	CY7C342-30GC/GI	G68	
35	CY7C342-35HC/HI	H81	Commercial/ Industrial
	CY7C342-35JC/JI	J81	
	CY7C342-35RC/RI	R68	
	CY7C342-35GC/GI	G68	
	CY7C342-35HMB	H81	Military
	CY7C342-35RMB	R68	
40	CY7C342-40HC/HI	H81	Commercial/ Industrial
	CY7C342-40JC/JI	J81	
	CY7C342-40RC/RI	R68	
	CY7C342-40GC/GI	G68	
	CY7C342-40HMB	H81	Military
	CY7C342-40RMB	R68	

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MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC1}	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{PD1}	7,8,9,10,11
t_{PD2}	7,8,9,10,11
t_{PD3}	7,8,9,10,11
t_{CO1}	7,8,9,10,11
t_{S1}	7,8,9,10,11
t_{S2}	7,8,9,10,11
t_{H}	7,8,9,10,11
t_{WH}	7,8,9,10,11
t_{WL}	7,8,9,10,11
t_{RO}	7,8,9,10,11
t_{PO}	7,8,9,10,11
t_{ACO1}	7,8,9,10,11
t_{ACO2}	7,8,9,10,11
t_{AS1}	7,8,9,10,11
t_{AS2}	7,8,9,10,11
t_{AH}	7,8,9,10,11
t_{AWH}	7,8,9,10,11
t_{AWL}	7,8,9,10,11

Document #: 38-00119-A

PRELIMINARY **CY7C343**

CYPRESS SEMICONDUCTOR

64-Macrocell MAX® EPLD

Features

- 64 MAX macrocells in 4 LABs
- 8 dedicated inputs, 28 three-stateable, bidirectional I/O pins
- Programmable interconnect array
- Available in 44-pin HLCC, PLCC

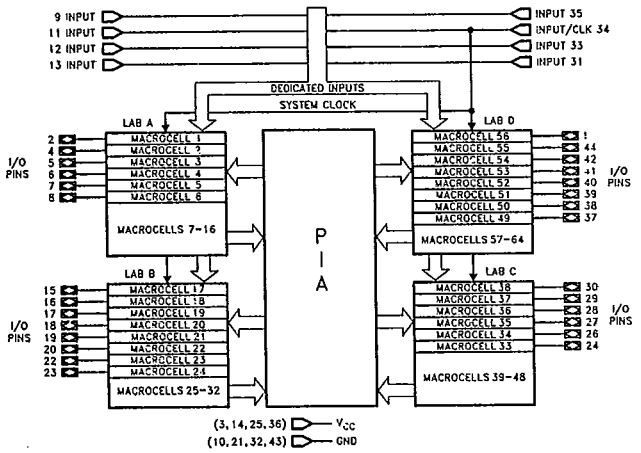
Functional Description

The CY7C343 is a high-performance, high-density erasable programmable logic device, available in 44-pin PLCC and HLCC packages.

The CY7C343 contains 64 highly flexible macrocells and 128 expander product terms. These resources are divided into four Logic Array Blocks (LABs) connected through the Programmable Interconnect Array (PIA). There are 8 input pins, one of which doubles as a clock pin if needed. The CY7C343 also has 28 I/O pins, each connected to a macrocell (six for LABs A and C, and eight for LABs B and D). The remaining 36 macrocells are used for embedded logic.

The CY7C343 is excellent for a wide range of applications both synchronous and asynchronous.

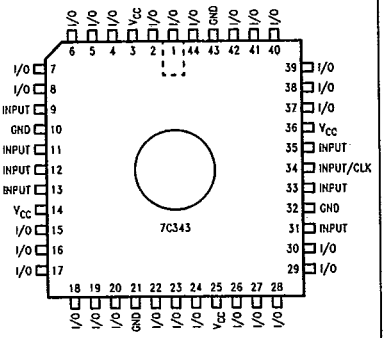
Logic Block Diagram



0185-1

Pin Configuration

HLCC
Top View



0185-2

Selection Guide

		7C343-30	7C343-35	7C343-40
Maximum Access Time (ns)		30	35	40
Maximum Operating Current (mA)	Commercial	135	135	
	Military		225	225
	Industrial	225	225	225
Maximum Standby Current (mA)	Commercial	120	120	
	Military		200	200
	Industrial	200	200	200

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... 0°C to +70°C

Maximum Junction Temperature (Under Bias) ..... 150°C

Supply Voltage to Ground Potential .... −2.0V to +7.0V

Maximum Power Dissipation ..... 2500 mW

DC V_{CC} or GND Current ..... 500 mA

DC Output Current, per Pin ..... −25 mA to +25 mA

DC Input Voltage[1] ..... −2.0V to +7.0V

DC Program Voltage..... −2.0V to +13.5V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±5%
Industrial	−40°C to +85°C	5V ±10%
Military	−55°C to +125°C (Case)	5V ±10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA			0.45	V
V_{IH}	Input HIGH Level			2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Level			−0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Leakage Current	V_O = V_{CC} or GND		−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[2A]		−30	−90	mA
I_{CC_1}	Power Supply Current (Standby)	V_I = V_{CC} or GND (No Load)	Commercial		120	mA
			Military/Industrial		200	mA
I_{CC_2}	Power Supply Current[3]	V_I = V_{CC} or GND (No Load) f = 1.0 MHz[3]	Commercial		135	mA
			Military/Industrial		225	mA

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 2V, f = 1.0 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, f = 1.0 MHz	10	

Notes:

1. Minimum DC input is −0.3V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.
2. Typical values are for T_A = 25°C and V_{CC} = 5V.
2A. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
3. Measured with device programmed as a 16-bit counter in each LAB. This parameter is tested periodically by sampling production material.
4. Part (a) in AC Test Load and Waveforms is used for all parameters except t_{ER} and t_{XZ}, which is used for part (b) in AC Test Load and Waveforms. All external timing parameters are measured referenced to external pins of the device.

AC Test Loads and Waveforms[4]

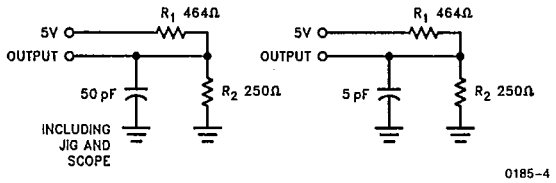


Figure 1a Figure 1b

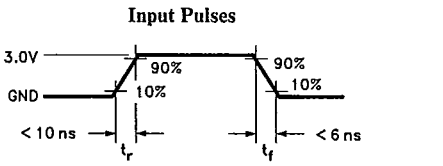
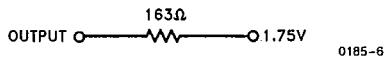
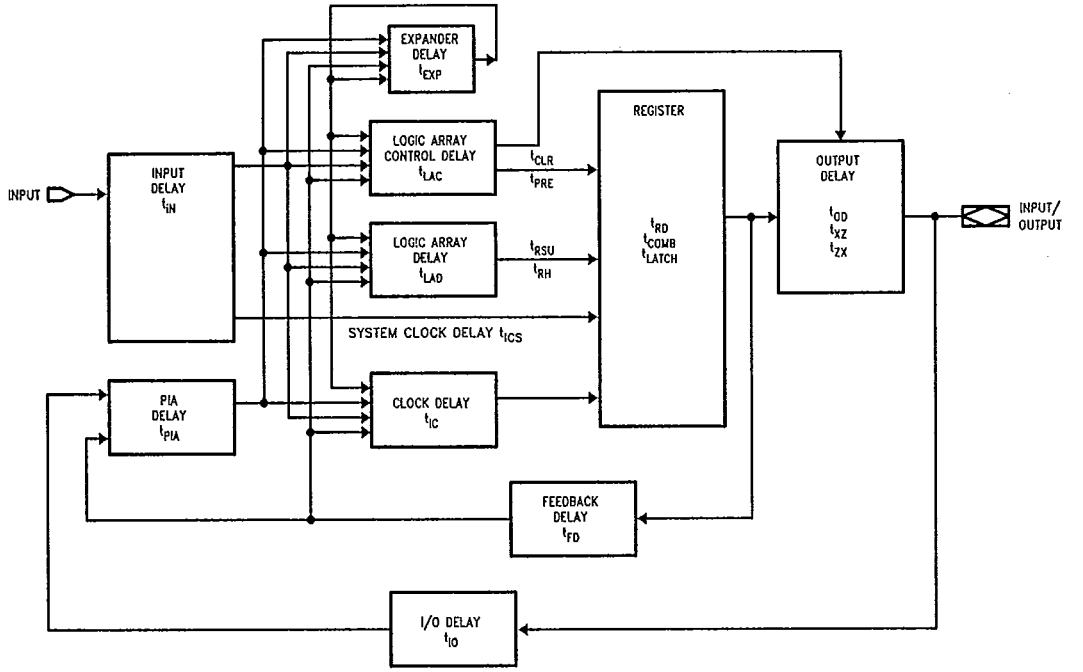


Figure 2

Equivalent to: THÉVENIN EQUIVALENT (Commercial/Military)



CY7C343 Timing Model



0185-3

Programmable Interconnect Array

The Programmable Interconnect Array (PIA) solves interconnect limitations by routing only the signals needed by each logic array block. The inputs to the PIA are the outputs of every macrocell within the device and the I/O pin feedback of every pin on the device.

Unlike masked or programmable gate arrays, which induce variable delay dependent on routing, the PIA has a fixed delay. This eliminates undesired skews among logic signals, which may cause glitches in internal or external logic. The fixed delay, regardless of programmable interconnect array configuration, simplifies design by assuring that internal signal skews or races are avoided. The result is ease of design implementation, often in a single pass, without the multiple internal logic placement and routing iterations required for a programmable gate array to achieve design timing objectives.

Timing Delays

Timing delays within the CY7C343 may be easily determined using MAX + PLUS™ software or by the model shown in *Figure 3*. The CY7C343 has fixed internal delays, allowing the user to determine the worst case timing delays for any design. For complete timing information the MAX + PLUS software provides a timing simulator.

Design Recommendations

Operation of the devices described herein with conditions above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability. The CY7C343 contains circuitry to protect device pins from high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

For proper operation, input and output pins must be constrained to the range GND (V_{IN} or V_{OUT}) V_{CC}. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 μF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled to GND, directly at the device. Decoupling capacitors should have good frequency response, such as monolithic ceramic types.

Timing Considerations

Unless otherwise stated, propagation delays do not include expanders. When using expanders add the maximum expander delay t_{EXP} to the overall delay. Similarly, there is an additional t_{PIA} delay for an input from an I/O pin when compared to a signal from a straight input pin.

When calculating synchronous frequencies, use ts_1 if all inputs are on the input pins. ts_2 should be used if data is applied at an I/O pin. If ts_2 is greater than t_{CO_1}, $1/ts_2$ becomes the limiting frequency in the data path mode unless $1/(t_{WH} + t_{WL})$ is less than $1/ts_2$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to ts_1. Determine which of $1/(t_{WH} + t_{WL})$, $1/t_{CO_1}$, or $1/(t_{EXP} + ts_1)$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the synchronous configuration.

When calculating external asynchronous frequencies, use t_{AS_1} if all inputs are on dedicated input pins. If any data is applied to an I/O pin, t_{AS_2} must be used as the required set up time. If $(t_{AS_2} + t_{AH})$ is greater than t_{ACO_1}, $1/(t_{AS_2} + t_{AH})$ becomes the limiting frequency in the data path mode unless $1/(t_{AWH} + t_{AWL})$ is less than $1/(t_{AS_2} + t_{AH})$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{AS_1}. Determine which of $1/(t_{AWH} + t_{AWL})$, $1/t_{ACO_1}$, or $1/(t_{EXP} + t_{AS_1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the asynchronous configuration.

The parameter t_{OH} indicates the system compatibility of this device when driving other synchronous logic with positive input hold times, which is controlled by the same synchronous clock. If t_{OH} is greater than the minimum required input hold time of the subsequent synchronous logic, then the devices are guaranteed to function properly with a common synchronous clock under worst-case environmental and supply voltage conditions.

The parameter t_{AOH} indicates the system compatibility of this device when driving subsequent registered logic with a positive hold time and using the same clock as the CY7C343.

In general, if t_{AOH} is greater than the minimum required input hold time of the subsequent logic (synchronous or asynchronous) then the devices are guaranteed to function properly under worst-case environmental and supply voltage conditions, provided the clock signal source is the same. This also applies if expander logic is used in the clock signal path of the driving device, but not for the driven device. This is due to the expander logic in the second device's clock signal path adding an additional delay (t_{EXP}) causing the output data from the preceding device to change prior to the arrival of the clock signal at the following device's register.

External Synchronous Switching Characteristics[4] Over Operating Range

Parameters	Description		CY7C343-30		CY7C343-35		CY7C343-40		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD_1}	Dedicated Input to Combinatorial Output Delay[5]	Com'l & Ind		30		35			ns
		Mil				35		40	
t_{PD_2}	I/O Input to Combinatorial Output Delay[6]	Com'l & Ind		45		55			ns
		Mil				55		65	
t_{PD_3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[7]	Com'l & Ind		47		55			ns
		Mil				55		62	
t_{PD_4}	I/O Input to Combinatorial Output Delay with Expander Delay[8]	Com'l & Ind		64		72			ns
		Mil				72		80	
t_{EA}	Input to Output Enable Delay[5]	Com'l & Ind		30		35			ns
		Mil				35		40	
t_{ER}	Input to Output Disable Delay[5]	Com'l & Ind		30		35			ns
		Mil				35		40	
t_{CO_1}	Synchronous Clock Input to Output Delay	Com'l & Ind		16		20			ns
		Mil				20		23	
t_{CO_2}	Synchronous Clock to Local Feedback to Combinatorial Output[9]	Com'l & Ind		40		45			ns
		Mil				45		50	
t_{S_1}	Dedicated Input or Feedback Setup Time to Synchronous Clock Input[5, 10]	Com'l & Ind	22		25				ns
		Mil			25		28		
t_{S_2}	I/O Input Setup Time to Synchronous Clock Input[5]	Com'l & Ind	39		42				ns
		Mil			42		45		
t_H	Input Hold Time from Synchronous Clock Input[5]	Com'l & Ind	0		0				ns
		Mil			0		0		
t_{WH}	Synchronous Clock Input High Time	Com'l & Ind	10		12.5				ns
		Mil			12.5		15		
t_{WL}	Synchronous Clock Input Low Time	Com'l & Ind	10		12.5				ns
		Mil			12.5		15		
t_{RW}	Asynchronous Clear Width[5]	Com'l & Ind	30		35				ns
		Mil			35		40		
t_{RR}	Asynchronous Clear Recovery Time[5]	Com'l & Ind	30		35				ns
		Mil			35		40		
t_{RO}	Asynchronous Clear to Registered Output Delay[5]	Com'l & Ind		30		35			ns
		Mil				35		40	
t_{PW}	Asynchronous Preset Width[5]	Com'l & Ind	30		35				ns
		Mil			35		40		
t_{PR}	Asynchronous Preset Recovery Time[5]	Com'l & Ind	30		35				ns
		Mil			35		40		
t_{PO}	Asynchronous Preset to Registered Output Delay[5]	Com'l & Ind		30		35			ns
		Mil				35		40	
t_{CF}	Synchronous Clock to Local Feedback Input[11]	Com'l & Ind		3		6			ns
		Mil				6		9	
t_P	External Synchronous Clock Period ($t_{CO_1} + t_{S_1}$)	Com'l & Ind	37		43				ns
		Mil			45		51		

External Synchronous Switching Characteristics[4] Over Operating Range (Continued)

T-46-13-47

Parameters	Description		CY7C343-30		CY7C343-35		CY7C343-40		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX_1}	External Maximum Frequency $(1/(t_{CO_1} + t_{S_1}))$[12]	Com'l & Ind	27.0		23.2				MHz
		Mil			22.2		19.6		
f_{MAX_2}	Internal Local Feedback Maximum Frequency, lesser of $1/(t_{S_1} + t_{CF})$ or $(1/t_{CO_1})$[13]	Com'l & Ind	40.0		32.2				MHz
		Mil			33.3		28.5		
f_{MAX_3}	Data Path Maximum Frequency, least of $(1/(t_{WL} + t_{WH}))$, $(1/(t_{S_1} + t_H))$ or $(1/t_{CO_1})$[14]	Com'l & Ind	45.4		40.0				MHz
		Mil			40.0		30.0		
f_{MAX_4}	Maximum Register Toggle Frequency $1/(t_{WL} + t_{WH})$[15]	Com'l & Ind	50.0		40.0				MHz
		Mil			40.0		30.0		
t_{OH}	Output Data Stable Time from Synchronous Clock Input[16]	Com'l & Ind	3		3				ns
		Mil			3		3		

Notes:

5. This specification is a measure of the delay from input signal applied to a dedicated input, (44-pin PLCC input pin 9, 11, 12, 13, 31, 33, 34, or 35) to combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function.
   When this note is applied to any parameter specification it indicates that the signal (data, asynchronous clock, asynchronous clear, and/or asynchronous preset) is applied to a dedicated input only and no signal path (either clock or data) employs expander logic.
   If an input signal is applied to an I/O pin an additional delay equal to t_{PIA} should be added.
   If expanders are used add the maximum expander delay t_{EXP} to the overall delay.
6. This specification is a measure of the delay from input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
7. This specification is a measure of the delay from an input signal applied to a dedicated input, (44-pin PLCC input pin 9, 11, 12, 13, 31, 33, 34, or 35) to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
8. This specification is a measure of the delay from an input signal applied to an I/O macrocell pin to any output. This delay assumes expander terms are used to form the logic function and includes the worst case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
9. This specification is a measure of the delay from synchronous register clock to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used, register is synchronously clocked and all feedback is within the same LAB. This parameter is tested periodically by sampling production material.
10. If data is applied to an I/O input for capture by a macrocell register, the I/O pin input set-up time minimums should be observed. These parameters are t_{S_1} for synchronous operation and t_{AS_2} for asynchronous operation.
11. This specification is a measure of the delay associated with the internal register feedback path. This is the delay from synchronous clock to LAB logic array input. This delay plus the register set-up time, t_{S_1}, is the minimum internal period for an internal synchronous state machine configuration. This delay is for feedback within the same LAB. This parameter is tested periodically by sampling production material.
12. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which a state machine configuration with external feedback can operate. It is assumed that all data inputs and feedback signals are applied to dedicated inputs.
13. This specification indicates the guaranteed maximum frequency at which a state machine with internal only feedback can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{CO_1}$. All feedback is assumed to be local, originating within the same LAB.
14. This frequency indicates the maximum frequency at which the device may operate in data path mode. This delay assumes data input signals are applied to dedicated inputs and no expander logic is used.
15. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which an individual output or buried register can be cycled.
16. This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.

T-46-13-47

External Asynchronous Switching Characteristics[4] Over Operating Range

Parameters	Description		CY7C343-30		CY7C343-35		CY7C343-40		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACO_1}	Asynchronous Clock Input to Output Delay[5]	Com'l & Ind		30		35			ns
		Mil		30		35		45	
t_{ACO_2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[17]	Com'l & Ind		50		60			ns
		Mil				60		70	
t_{AS_1}	Dedicated Input or Feedback Setup Time to Asynchronous Clock Input[5]	Com'l & Ind	10		10				ns
		Mil			10		10		
t_{AS_2}	I/O Input Setup Time to Asynchronous Clock Input[5]	Com'l & Ind	27		30				ns
		Mil			30		33		
t_{AH}	Input Hold Time from Asynchronous Clock Input[5]	Com'l & Ind	15		15				ns
		Mil			15		15		
t_{AWH}	Asynchronous Clock Input High Time[5]	Com'l & Ind	25		30				ns
		Mil			30		35		
t_{AWL}	Asynchronous Clock Input Low Time[5]	Com'l & Ind	25		30				ns
		Mil			30		35		
t_{ACF}	Asynchronous Clock to Local Feedback Input[18]	Com'l & Ind		18		22			ns
		Mil				22		26	
t_{AP}	External Asynchronous Clock Period ($t_{ACO_1} + t_{AS_1}$) or ($t_{AWH} + t_{AWL}$)	Com'l & Ind	50		60				ns
		Mil			60		70		
f_{MAXA_1}	External Maximum Frequency in Asynchronous Mode ($1/t_{AP}$)[19]	Com'l & Ind	20		16.6				MHz
		Mil			16.6		14.2		
f_{MAXA_2}	Maximum Internal Asynchronous Frequency[22]	Com'l & Ind	20		16.6				MHz
		Mil			16.6		14.2		
f_{MAXA_3}	Data Path Maximum Frequency in Asynchronous Mode[21]	Com'l & Ind	20		16.6				MHz
		Mil			16.6		14.2		
f_{MAXA_4}	Maximum Asynchronous Register Toggle Frequency ($1/(t_{AWH} + t_{AWL})$)[20]	Com'l & Ind	20		16.6				MHz
		Mil			16.6		14.2		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[23]	Com'l & Ind	15		15				ns
		Mil			15		15		

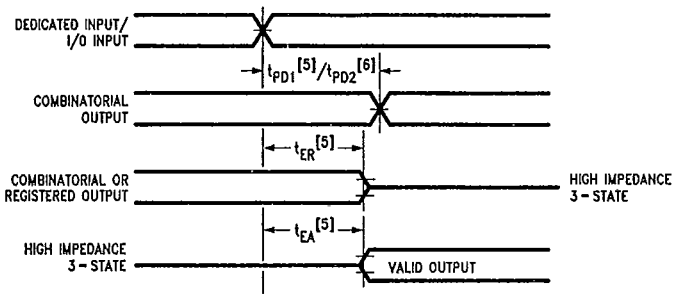
Notes:

17. This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used in the logic of combinatorial output or the asynchronous clock input. The clock signal is applied to a dedicated input pin and all feedback is within a single LAB. This parameter is tested periodically by sampling production material.
18. This specification is a measure of the delay associated with the internal register feedback path for an asynchronous clock to LAB logic array input. This delay plus the asynchronous register setup time, t_{AS_1}, is the minimum internal period for an internal asynchronously clocked state machine configuration. This delay is for feedback within the same LAB, assumes no expander logic in the clock path and assumes that the clock input signal is applied to a dedicated input pin. This parameter is tested periodically by sampling production material.
19. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that all data inputs, clock inputs, and feedback signals are applied to dedicated inputs and that no expander logic is employed in the clock signal path or data path.
20. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input pin.
21. This frequency is the maximum frequency at which the device may operate in the asynchronously clocked data path mode. This specification is determined by the least of $1/(t_{AWH} + t_{AWL})$, $1/(t_{AS_1} + t_{AH})$ or $1/t_{ACO_1}$. It asssumes data and clock input signals are applied to dedicated input pins and no expander logic is used.
22. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal only feedback can operate. This parameter is determined by the lesser of $(1/(t_{ACF} + t_{AS}))$ or $(1/(t_{AWH} + t_{AWL}))$. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO_1}$.
    This specification assumes no expander logic is utilized, all data inputs and clock inputs are applied to dedicated inputs, and all state feedback is within a single LAB. This parameter is tested periodically by sampling production material.
23. This parameter indicates the minimum time that the previous register output data is maintained on the output after an asynchronous register clock input.

Switching Waveforms

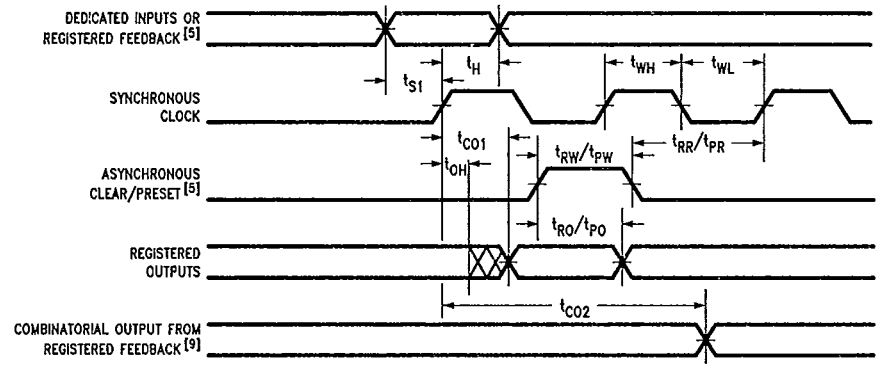
T-46-13-47

External Combinatorial



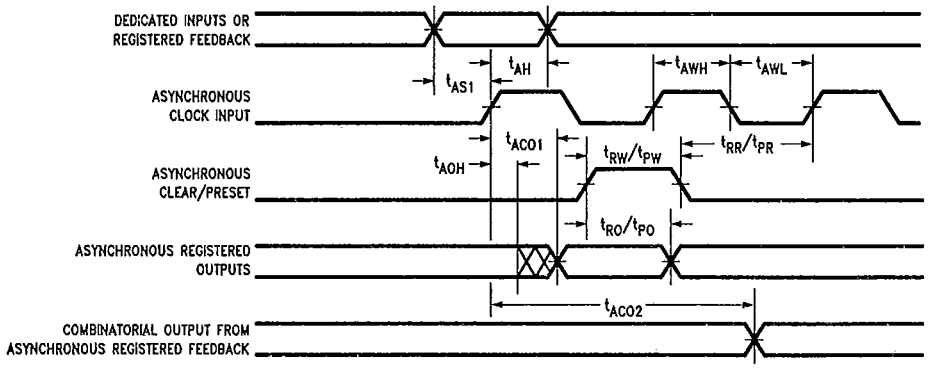
0185-7

External Synchronous



0185-8

External Asynchronous



0185-9

Internal Switching Characteristics[1] Over Operating Range

Parameters	Description		CY7C343-30		CY7C343-35		CY7C343-40		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l & Ind		7		9			ns
		Mil				9		11	
t_{IO}	I/O Input Pad and Buffer Delay	Com'l & Ind		5		7			ns
		Mil				7		9	
t_{EXP}	Expander Array Delay	Com'l & Ind		14		20			ns
		Mil				20		25	
t_{LAD}	Logic Array Data Delay	Com'l & Ind		14		16			ns
		Mil				16		18	
t_{LAC}	Logic Array Control Delay	Com'l & Ind		12		13			ns
		Mil				13		14	
t_{OD}	Output Buffer and Pad Delay	Com'l & Ind		5		6			ns
		Mil				6		7	
t_{ZX}	Output Buffer Enable Delay[24]	Com'l & Ind		11		13			ns
		Mil				13		15	
t_{XZ}	Output Buffer Disable Delay	Com'l & Ind		11		13			ns
		Mil				13		15	
t_{RSU}	Register Setup Time Relative to Clock Signal at Register	Com'l & Ind	8		8				ns
		Mil			8		8		
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l & Ind	8		12				ns
		Mil			12		14		
t_{LATCH}	Flow Through Latch Delay	Com'l & Ind		4		4			ns
		Mil				4		4	
t_{RD}	Register Delay	Com'l & Ind		2		2			ns
		Mil				2		2	
t_{COMB}	Transparent Mode Delay[25]	Com'l & Ind		4		4			ns
		Mil				4		4	
t_{CH}	Clock High Time	Com'l & Ind	10		12.5				ns
		Mil			12.5		15		
t_{CL}	Clock Low Time	Com'l & Ind	10		12.5				ns
		Mil			12.5		15		

Notes:

24. Sample tested only for an output change of 500 mV.

25. This specification guarantees the maximum combinatorial delay associated with the macrocell register bypass when the macrocell is configured for combinatorial operation.

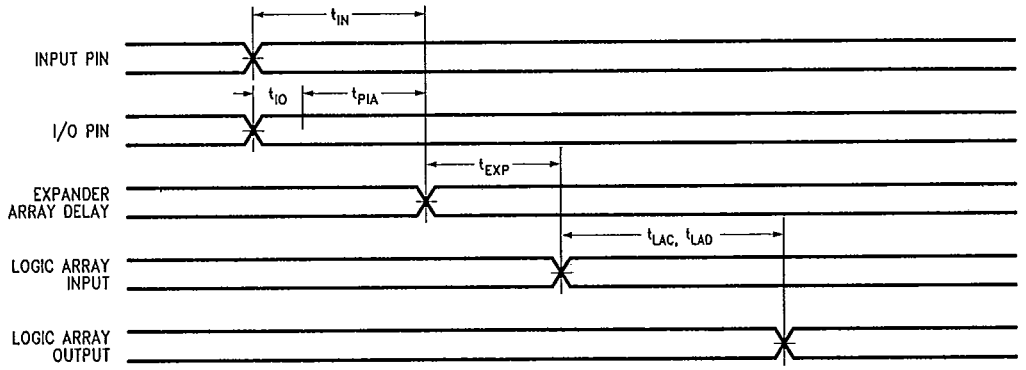
Internal Switching Characteristics[19] Over Operating Range (Continued)

Parameters	Description		CY7C343-30		CY7C343-35		CY7C343-40		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{IC}	Asynchronous Clock Logic Delay	Com'l & Ind		16		18			ns
		Mil				18		20	
t_{ICS}	Synchronous Clock Delay	Com'l & Ind		2		3			ns
		Mil				3		4	
t_{FD}	Feedback Delay	Com'l & Ind		1		2			ns
		Mil				2		3	
t_{PRE}	Asynchronous Register Preset Time	Com'l & Ind		6		7			ns
		Mil				7		8	
t_{CLR}	Asynchronous Register Clear Time	Com'l & Ind		6		7			ns
		Mil				7		8	
t_{PCW}	Asynchronous Preset and Clear Pulse Width	Com'l & Ind	6		7				ns
		Mil			7		8		
t_{PCR}	Asynchronous Preset and Clear Recovery Time	Com'l & Ind	6		7				ns
		Mil			7		8		
t_{PIA}	Programmable Interconnect Array Delay Time	Com'l & Ind		16		20			ns
		Mil				20		24	

Switching Waveforms

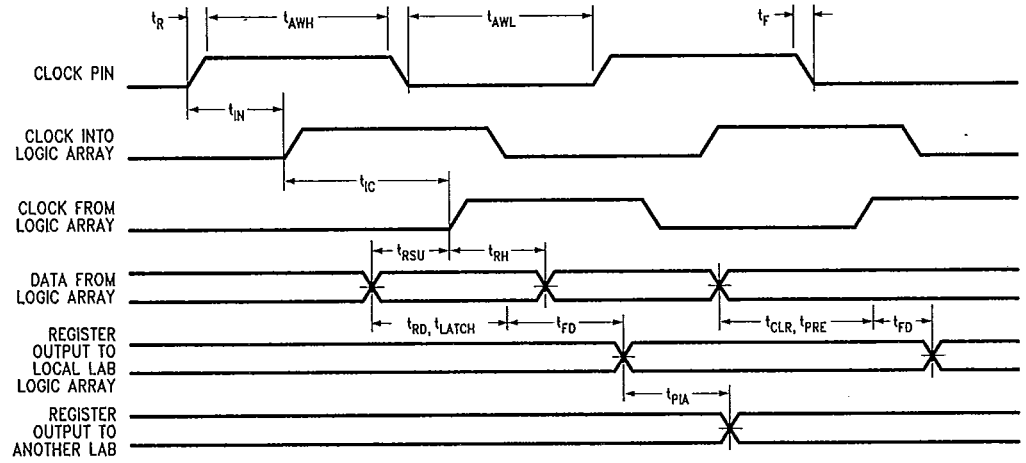
T-46-13-47

Internal Combinatorial



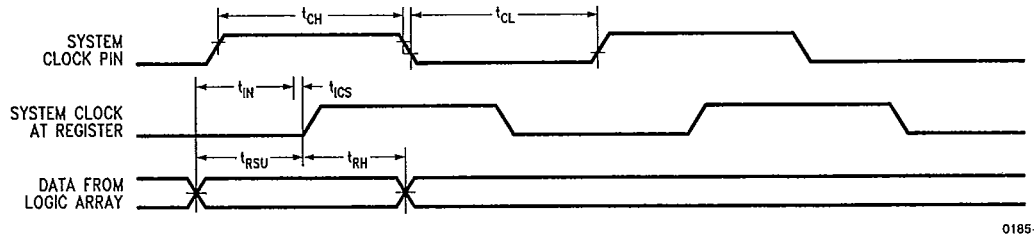
0185-10

Internal Asynchronous



0185-11

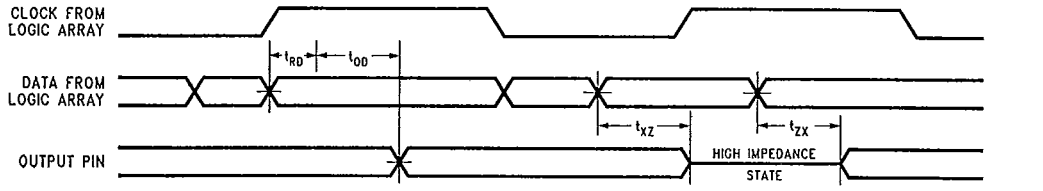
Internal Synchronous



0185-12

Switching Waveforms (Continued)

Output Mode



0185-13

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
30	CY7C343-30HC/HI	H67	Commercial/ Industrial
	CY7C343-30JC/JI	J67	
35	CY7C343-35HC/HI	H67	Commercial/ Industrial
	CY7C343-35JC/JI	J67	
	CY7C343-35HMB	H67	Military
40	CY7C343-40HMB	H67	Military

Document #: 38-00128

T-46-13-47

CY7C344

CYPRESS SEMICONDUCTOR

32-Macrocell MAX™ EPLD

Features

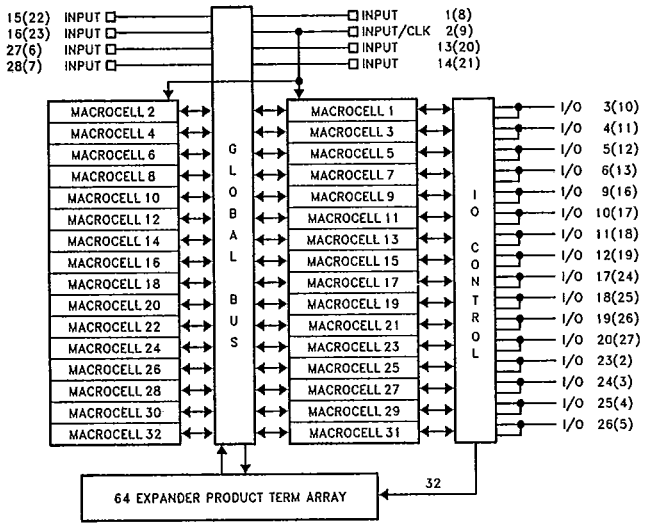
- **High-performance, high-density replacement for TTL, 74HC, and custom logic**
- **32 macrocells, 64 expander product terms in one LAB**
- **8 dedicated inputs, 16 I/O pins**
- **28-pin 300-mil DIP, Cerdip or 28-pin HLCC, PLCC package**

Functional Description

Available in a 28-pin 300-mil DIP or windowed J-leaded ceramic chip carrier (HLCC), the CY7C344 represents the densest EPLD of this size. 8 dedicated inputs and 16 bi-directional I/O pins communicate to one logic array block. In the CY7C344 LAB there are 32 macrocells and 64 expander product terms. When an I/O macrocell is used as an input, two expanders are used to create an input path. Even if all of the I/O pins are driven by macrocell registers, there are still 16 "buried" registers available. All inputs, macrocells, and I/O pins are interconnected within the LAB.

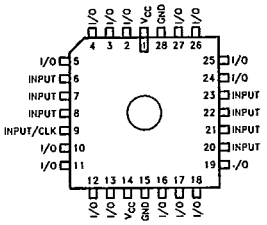
The speed and density of the CY7C344 makes it a natural for all types of applications. With just this one device, the designer can implement complex state machines, registered logic, and combinatorial "glue" logic, without using multiple chips. This architectural flexibility allows the CY7C344 to replace multi-chip TTL solutions, whether they are synchronous, asynchronous, combinatorial, or all three.

Logic Block Diagram[1]

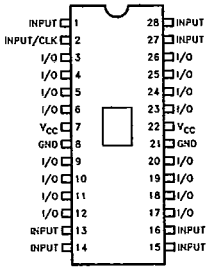


Pin Configurations

HLCC
Top View



Cerdip
Top View



Selection Guide

		7C344-20	7C344-25	7C344-35
Maximum Access Time (ns)		20	25	35
Maximum Operating Current (mA)	Commercial	200	200	
	Military		220	220
	Industrial	220	220	220
Maximum Standby Current (mA)	Commercial	150	150	
	Military		170	170
	Industrial	170	170	170

Note: 1. Figures in ( ) are for J-leaded packages.

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CYPRESS SEMICONDUCTOR

CY7C344

T-46-13-47

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... 0°C to +70°C

Maximum Junction Temperature (Under Bias) ..... 150°C

Supply Voltage to Ground Potential .... −2.0V to +7.0V

Maximum Power Dissipation ..... 1500 mW

DC V_{CC} or GND Current ..... 500 mA

DC Output Current, per Pin ..... −25 mA to +25 mA

DC Input Voltage[2] ..... −2.0V to +7.0V

DC Program Voltage..... −2.0V to +13.5V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±5%
Industrial	−40°C to +85°C	5V ±10%
Military	−55°C to +125°C (Case)	5V ±10%

Electrical Characteristics Over the Operating Range[5]

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA			0.45	V
V_{IH}	Input HIGH Level			2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Level			−0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Leakage Current	V_O = V_{CC} or GND		−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3, 4]		−30	−90	mA
I_{CC_1}	Power Supply Current (Standby)	V_I = V_{CC} or GND (No Load)	Commercial		150	mA
			Military/Industrial		170	mA
I_{CC_2}	Power Supply Current	V_I = V_{CC} or GND (No Load) f = 1.0 MHz[4, 6]	Commercial		200	mA
			Military/Industrial		220	mA

Capacitance

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 2V, f = 1.0 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, f = 1.0 MHz	10	

Notes:

2. Minimum DC input is −0.3V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Guaranteed but not 100% tested.
5. Typical values are for T_A = 25°C and V_{CC} = 5V.
6. Measured with device programmed as a 16-bit counter.
7. *Figure 1a* in AC Test Load and Waveforms is used for all parameters except t_{ER} and t_{XZ}, which is used for *Figure 1b* in AC Test Load and Waveforms. All external timing parameters are measured referenced to external pins of the device.

AC Test Loads and Waveforms[7]

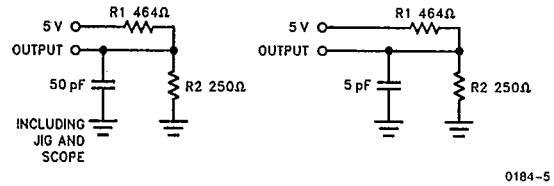


Figure 1a Figure 1b

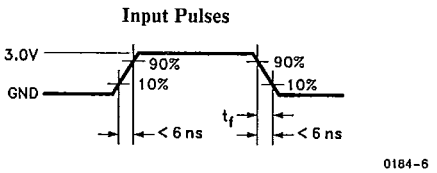
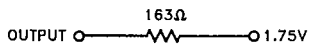
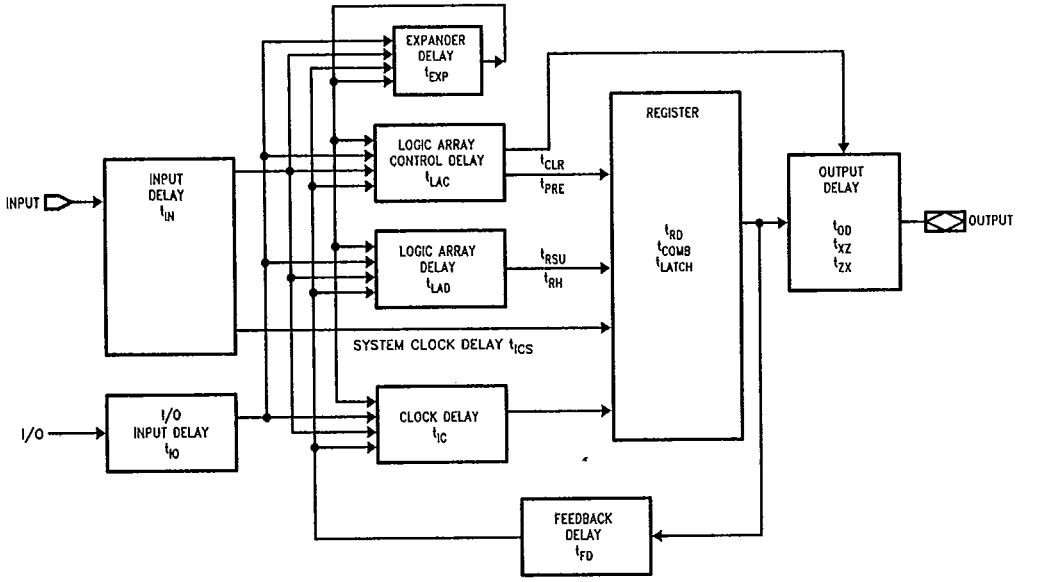


Figure 2

Equivalent to: THÉVENIN EQUIVALENT (Commercial/Military)



CY7C344 Timing Model



0184-4

Timing Delays

Timing delays within the CY7C344 may be easily determined using MAX+PLUS™ software or by the model shown in *Figure 3*. The CY7C344 has fixed internal delays, allowing the user to determine the worst case timing delays for any design. For complete timing information the MAX+PLUS software provides a timing simulator.

Design Recommendations

Operation of the devices described herein with conditions above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability. The CY7C344 contains circuitry to protect device pins from high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

For proper operation, input and output pins must be constrained to the range GND (V_{IN} or V_{OUT}) V_{CC}. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 μF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled.

Timing Considerations

Unless otherwise stated, propagation delays do not include expanders. When using expanders add the maximum expander delay t_{EXP} to the overall delay.

When calculating synchronous frequencies, use ts_1 if all inputs are on the input pins. ts_2 should be used if data is applied at an I/O pin. If ts_2 is greater than tco_1, $1/ts_2$ becomes the limiting frequency in the data path mode unless $1/(t_{WH} + t_{WL})$ is less than $1/ts_2$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to ts_1. Determine which of $1/(t_{WH} + t_{WL})$, $1/tco_1$, or $1/(t_{EXP} + ts_1)$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the synchronous configuration.

When calculating external asynchronous frequencies, use t_{AS_1} if all inputs are on dedicated input pins. If any data is applied to an I/O pin, t_{AS_2} must be used as the required set up time. If $(t_{AS_2} + t_{AH})$ is greater than t_{ACO_1}, $1/(t_{AS_2} + t_{AH})$ becomes the limiting frequency in the data path mode unless $1/(t_{AWH} + t_{AWL})$ is less than $1/(t_{AS_2} + t_{AH})$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{AS_1}. Determine which of $1/(t_{AWH} + t_{AWL})$, $1/t_{ACO_1}$, or $1/(t_{EXP} + t_{AS_1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the asynchronous configuration.

Timing Considerations (Continued)

The parameter t_{OH} indicates the system compatibility of this device when driving other synchronous logic with positive input hold times, which is controlled by the same synchronous clock. If t_{OH} is greater than the minimum required input hold time of the subsequent synchronous logic, then the devices are guaranteed to function properly with a common synchronous clock under worst-case environmental and supply voltage conditions.

The parameter t_{AOH} indicates the system compatibility of this device when driving subsequent registered logic with a positive hold time and using the same clock as the CY7C344.

In general, if t_{AOH} is greater than the minimum required input hold time of the subsequent logic (synchronous or asynchronous) then the devices are guaranteed to function properly under worst-case environmental and supply voltage conditions, provided the clock signal source is the same. This also applies if expander logic is used in the clock signal path of the driving device, but not for the driven device. This is due to the expander logic in the second device's clock signal path adding an additional delay (t_{EXP}) causing the output data from the preceding device to change prior to the arrival of the clock signal at the following device's register.

External Synchronous Switching Characteristics[7] Over Operating Range

Parameters	Description		CY7C344-20		CY7C344-25		CY7C344-35		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD_1}	Dedicated Input to Combinatorial Output Delay[8]	Com'l/Ind		20		25			ns
		Mil				25		35	
t_{PD_2}	I/O Input to Combinatorial Output Delay[9]	Com'l/Ind		20		25			ns
		Mil				25		35	
t_{PD_3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[10]	Com'l/Ind		30		40			ns
		Mil				40		60	
t_{PD_4}	I/O Input to Combinatorial Output Delay with Expander Delay[4, 11]	Com'l/Ind		30		40			ns
		Mil				40		60	
t_{EA}	Input to Output Enable Delay[4]	Com'l/Ind		20		25			ns
		Mil				25		35	
t_{ER}	Input to Output Disable Delay[4]	Com'l/Ind		20		25			ns
		Mil				25		35	
t_{CO_1}	Synchronous Clock Input to Output Delay	Com'l/Ind		12		15			ns
		Mil				15		23	
t_{CO_2}	Synchronous Clock to Local Feedback to Combinatorial Output[4, 12]	Com'l/Ind		22		30			ns
		Mil				30		46	
t_S	Dedicated Input or Feedback Setup Time to Synchronous Clock Input	Com'l/Ind	12		15				ns
		Mil			15		21		
t_H	Input Hold Time from Synchronous Clock Input[7]	Com'l/Ind	1		2.5				ns
		Mil			2.5		2.5		
t_{WH}	Synchronous Clock Input High Time[4]	Com'l/Ind	7		8				ns
		Mil			8		10		
t_{WL}	Synchronous Clock Input Low Time[4]	Com'l/Ind	7		8				ns
		Mil			8		10		
t_{RW}	Asynchronous Clear Width[4]	Com'l/Ind	23		28				ns
		Mil			28		33		
t_{RR}	Asynchronous Clear Recovery Time[4]	Com'l/Ind	20		25				ns
		Mil			25		35		
t_{RO}	Asynchronous Clear to Registered Output Delay[4]	Com'l/Ind		23		28			ns
		Mil				28		33	
t_{PW}	Asynchronous Preset Width[4]	Com'l/Ind	23		28				ns
		Mil			28		33		
t_{PR}	Asynchronous Preset Recovery Time[4]	Com'l/Ind		23		28			ns
		Mil				28		38	

External Synchronous Switching Characteristics[7] Over Operating Range (Continued)

Parameters	Description		CY7C344-20		CY7C344-25		CY7C344-35		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PO}	Asynchronous Preset to Registered Output Delay[4]	Com'l/Ind		23		28			ns
		Mil				28		33	
t_{CF}	Synchronous Clock to Local Feedback Input[4, 13]	Com'l/Ind		4		7			ns
		Mil				7		13	
t_P	External Synchronous Clock Period ($t_{CO_1} + t_S$)[4]	Com'l/Ind	24		30				ns
		Mil			30		44		
f_{MAX_1}	External Maximum Frequency ($1/(t_{CO_1} + t_S)$)[4, 14]	Com'l/Ind	41.6		33.3				MHz
		Mil			33.3		22.7		
f_{MAX_2}	Maximum Frequency with Internal Only Feedback ($1/(t_{CF} + t_S)$)[4, 15]	Com'l/Ind	62.5		45.4				MHz
		Mil			45.4		29.4		
f_{MAX_3}	Data Path Maximum Frequency, least of $1/(t_{WL} + t_{WH})$, $(1/(t_{S_1} + t_H))$ or $(1/t_{CO_1})$[4, 16]	Com'l/Ind	71.4		57.1				MHz
		Mil			57.1		42.5		
f_{MAX_4}	Maximum Register Toggle Frequency $1/(t_{WH} + t_{WL})$[4, 17]	Com'l/Ind	71.4		62.5				MHz
		Mil			62.5		50.0		
t_{OH}	Output Data Stable Time from Synchronous Clock Input[4, 18]	Com'l/Ind	3		3				ns
		Mil			3		3		

Notes:

8. This parameter is the delay from an input signal applied to a dedicated input pin to a combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function.
9. This parameter is the delay associated with an input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
10. This parameter is the delay associated with an input signal applied to a dedicated input pin to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
11. This parameter is the delay associated with an input signal applied to an I/O macrocell pin to any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
12. This specification is a measure of the delay from synchronous register clock input to internal feedback of the registered output signal to a combinatorial output for which the registered output signal is used as an input. This parameter assumes that no expanders are used in the logic of the combinatorial output and the register is synchronously clocked. This parameter is tested periodically by sampling production material.
13. This specification is a measure of the delay associated with the internal register feedback path. This delay plus the register setup time, t_S, is the minimum internal period for an internal state machine configuration. This parameter is tested periodically by sampling production material.
14. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external only feedback can operate.
15. This specification indicates the guaranteed maximum frequency at which a state machine with internal only feedback can operate. If register output states must also control external points, this frequency can still be observed as long as it is less than $1/t_{CO_1}$. This specification assumes no expander logic is used. This parameter is tested periodically by sampling production material.
16. This frequency indicates the maximum frequency at which the device may operate in data path mode (dedicated input pin to output pin). This assumes that no expander logic is used.
17. This specification indicates the guaranteed maximum frequency in synchronous mode, at which an individual output or buried register can be cycled by a clock signal applied to either a dedicated input pin or an I/O pin.
18. This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.

External Asynchronous Switching Characteristics[7] Over Operating Range

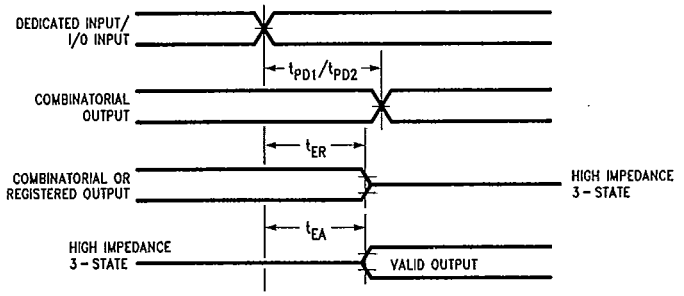
Parameters	Description		CY7C344-20		CY7C344-25		CY7C344-35		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACO_1}	Asynchronous Clock Input to Output Delay	Com'l/Ind		20		25			ns
		Mil				25		35	
t_{ACO_2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[19]	Com'l/Ind		38		46			ns
		Mil				46		62	
t_{AS}	Dedicated Input or Feedback Setup Time to Asynchronous Clock Input	Com'l/Ind	9		12				ns
		Mil			12		15		
t_{AH}	Input Hold Time from Asynchronous Clock Input	Com'l/Ind	9		12				ns
		Mil			12		17.5		
t_{AWH}	Asynchronous Clock Input High Time[4]	Com'l/Ind	15		20				ns
		Mil			20		30		
t_{AWL}	Asynchronous Clock Input Low Time[4]	Com'l/Ind	15		20				ns
		Mil			20		30		
t_{ACF}	Asynchronous Clock to Local Feedback Input[4, 20]	Com'l/Ind		18		21			ns
		Mil				21		27	
t_{AP}	External Asynchronous Clock Period ($t_{ACO_1} + t_{AS}$) or ($t_{AWH} + t_{AWL}$)[4]	Com'l/Ind	30		40				ns
		Mil			40		60		
f_{MAXA_1}	External Maximum Frequency in Asynchronous Mode ($1/t_{AP}$)[4, 21]	Com'l/Ind	33.3		25.0				MHz
		Mil			25.0		16.6		
f_{MAXA_2}	Maximum Internal Asynchronous Frequency $1/(t_{ACF} + t_{AS})$[4, 24]	Com'l/Ind	33.3		25.0				MHz
		Mil			25.0		16.6		
f_{MAXA_3}	Data Path Maximum Frequency in Asynchronous Mode[4, 23]	Com'l/Ind	33.3		25.0				MHz
		Mil			25.0		16.6		
f_{MAXA_4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[4, 22]	Com'l/Ind	33.3		25.0				MHz
		Mil			25.0		16.6		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[4, 25]	Com'l/Ind	15		15				ns
		Mil			15		15		

Notes:

19. This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the registered output signal to a combinatorial output for which the registered output signal is used as an input. Assumes no expanders are used in logic of combinatorial output or the asynchronous clock input. This parameter is tested periodically by sampling production material.
20. This specification is a measure of the delay associated with the internal register feedback path for an asynchronously clocked register. This delay plus the asynchronous register setup time, t_{AS}, is the minimum internal period for an asynchronously clocked state machine configuration. This delay assumes no expander logic in the asynchronous clock path. This parameter is tested periodically by sampling production material.
21. This parameter indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that no expander logic is employed in the clock signal path or data input path.
22. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to either a dedicated input or an I/O pin.
23. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode. If this frequency is less than $1/t_{ACO_1}$ or $1/(t_{AH} + t_{AS})$. It also indicates the maximum frequency at which the device may operate in the asynchronously clocked data path mode. Assumes no expander logic is used.
24. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal only feedback can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO_1}$. This specification assumes no expander logic is utilized. This parameter is tested periodically by sampling production material.
25. This parameter indicates the minimum time that the previous register output data is maintained on the output pin after an asynchronous register clock input to an external dedicated input or I/O pin.

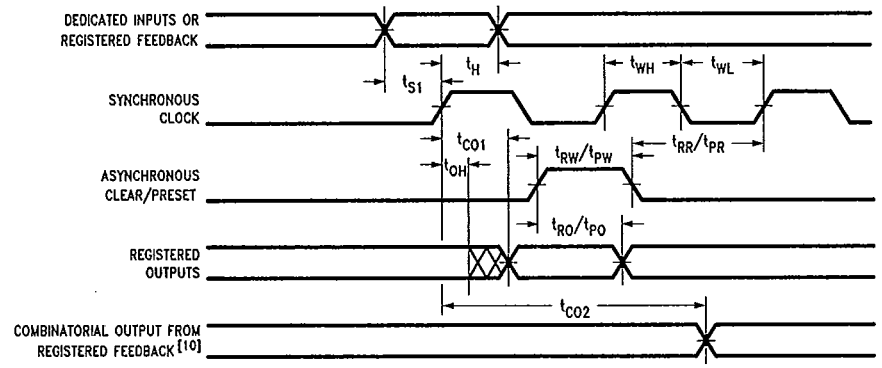
Switching Waveforms

External Combinatorial



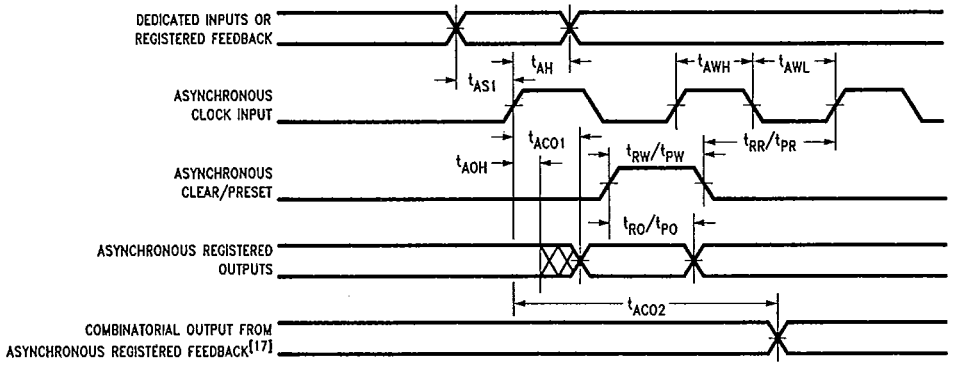
0184-8

External Synchronous



0184-9

External Asynchronous



0184-10

Typical Internal Switching Characteristics Over Operating Range

Parameters	Description		CY7C344-20		CY7C344-25		CY7C344-35		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l/Ind		5		7			ns
		Mil				7		11	
t_{IO}	I/O Input Pad and Buffer Delay	Com'l/Ind		5		7			ns
		Mil				7		11	
t_{EXP}	Expander Array Delay	Com'l/Ind		10		15			ns
		Mil				15		23	
t_{LAD}	Logic Array Data Delay	Com'l/Ind		9		10			ns
		Mil				10		12	
t_{LAC}	Logic Array Control Delay	Com'l/Ind		7		7			ns
		Mil				7		7	
t_{OD}	Output Buffer and Pad Delay	Com'l/Ind		5		5			ns
		Mil				5		5	
t_{ZX}	Output Buffer Enable Delay[26]	Com'l/Ind		8		11			ns
		Mil				11		17	
t_{XZ}	Output Buffer Disable Delay	Com'l/Ind		8		11			ns
		Mil				11		17	
t_{RSU}	Register Setup Time Relative to Clock Signal at Register	Com'l/Ind	5		8				ns
		Mil			8		14		
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l/Ind	9		12				ns
		Mil			12		18		
t_{LATCH}	Flow Through Latch Delay	Com'l/Ind		1		3			ns
		Mil				3		7	
t_{RD}	Register Delay	Com'l/Ind		1		1			ns
		Mil				1		1	
t_{COMB}	Transparent Mode Delay[27]	Com'l/Ind		1		3			ns
		Mil				3		7	
t_{CH}	Clock High Time	Com'l/Ind	7		8				ns
		Mil			8		9		
t_{CL}	Clock Low Time	Com'l/Ind	7		8				ns
		Mil			8		9		
t_{IC}	Asynchronous Clock Logic Delay	Com'l/Ind		8		10			ns
		Mil				10		12	
t_{ICS}	Synchronous Clock Delay	Com'l/Ind		2		3			ns
		Mil				3		5	
t_{FD}	Feedback Delay	Com'l/Ind		1		1			ns
		Mil				1		1	
t_{PRE}	Asynchronous Register Preset Time	Com'l/Ind		6		9			ns
		Mil				9		15	
t_{CLR}	Asynchronous Register Clear Time	Com'l/Ind		6		9			ns
		Mil				9		15	
t_{PCW}	Asynchronous Preset and Clear Pulse Width	Com'l/Ind	6		7				ns
		Mil			7		9		
t_{PCR}	Asynchronous Preset and Clear Recovery Time	Com'l/Ind	6		7				ns
		Mil			7		9		

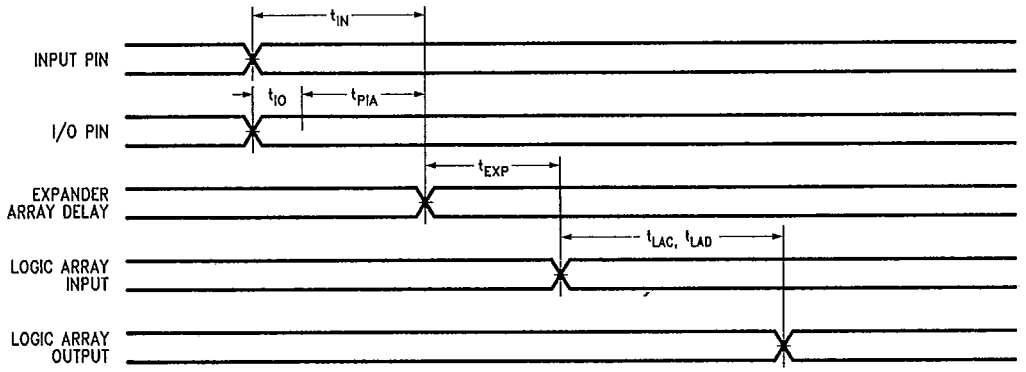
Notes:

26. Sample tested only for an output change of 500 mV.

27. This specification guarantees the maximum combinatorial delay associated with the macrocell register bypass when the macrocell is configured for combinatorial operation.

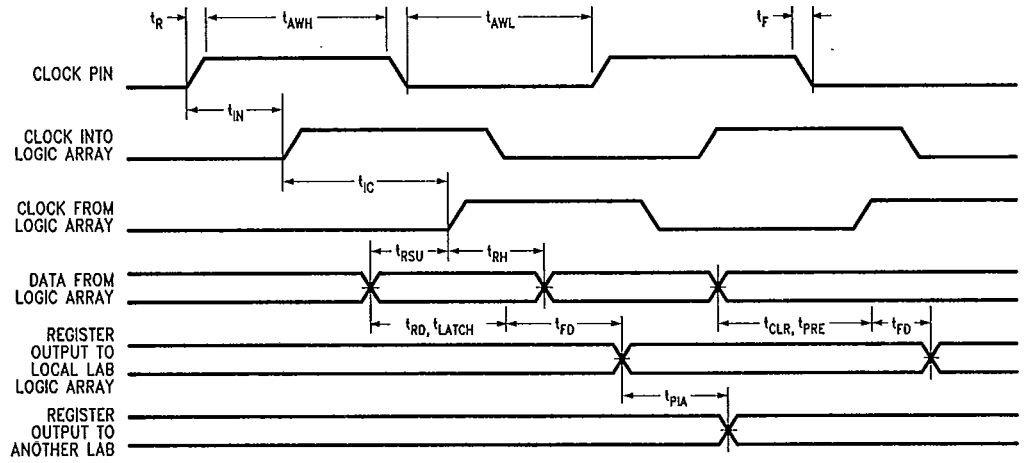
Switching Waveforms (Continued)

Internal Combinatorial



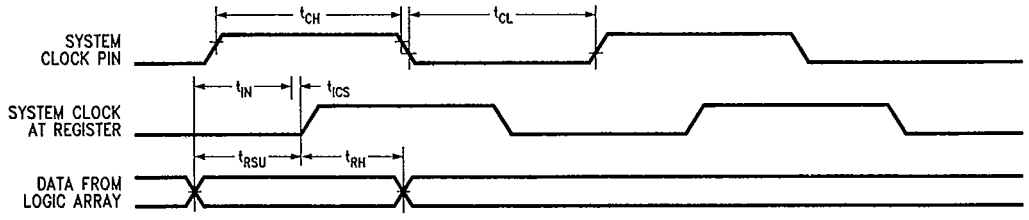
0184-11

Internal Asynchronous



0184-12

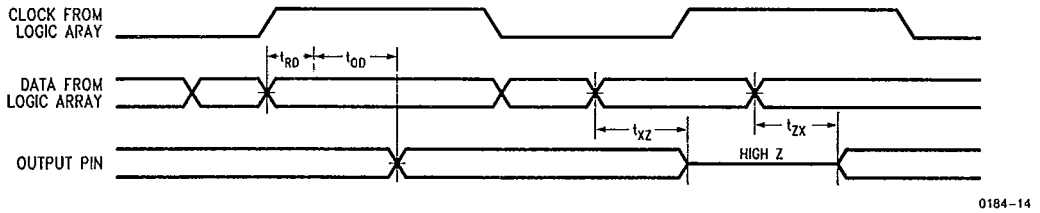
Internal Synchronous (Input Path)



0184-13

Switching Waveforms (Continued)

Internal Synchronous (Output Path)



0184-14

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY7C344-20PC/PI	P21	Commercial/ Industrial
	CY7C344-20DC/DI	D22	
	CY7C344-20WC/WI	W22	
	CY7C344-20HC/HI	H64	
	CY7C344-20JC/JI	J64	
25	CY7C344-25PC/PI	P21	Commercial/ Industrial
	CY7C344-25DC/DI	D22	
	CY7C344-25WC/WI	W22	
	CY7C344-25HC/HI	H64	
	CY7C344-25JC/JI	J64	
	CY7C344-25HMB	H64	Military
	CY7C344-25WMB	W22	
	CY7C344-25DMB	D22	
35	CY7C344-35HMB	H64	Military
	CY7C344-35WMB	W22	
	CY7C344-35DMB	D22	

MILITARY SPECIFICATIONS

T-46-13-47

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC1}	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{PD1}	7,8,9,10,11
t_{PD2}	7,8,9,10,11
t_{PD3}	7,8,9,10,11
t_{CO1}	7,8,9,10,11
t_S	7,8,9,10,11
t_H	7,8,9,10,11
t_{ACO1}	7,8,9,10,11
t_{ACO2}	7,8,9,10,11
t_{AS}	7,8,9,10,11
t_{AH}	7,8,9,10,11

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