

8080A SYSTEM CONTROLLER AND BUS DRIVER

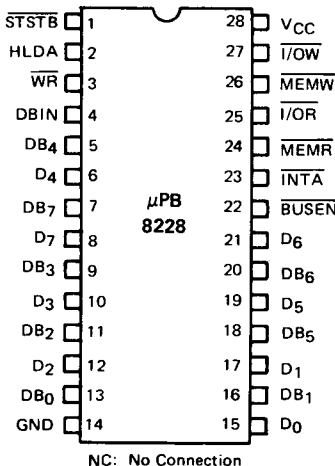
DESCRIPTION The μPB8228 is a single chip controller and bus driver for 8080A based systems. All the required interface signals necessary to connect RAM, ROM and I/O components to a μPD8080A are generated.

The μPB8228 provides a bi-directional three-state bus driver for high TTL fan-out and isolation of the processor data bus from the system data bus for increased noise immunity.

The system controller portion of the μPB8228 consists of a status latch for definition of processor machine cycles and a gating array to decode this information for direct interface to system components. The controller can enable gating of a multi-byte interrupt onto the data bus or can automatically insert a RESTART 7 onto the data bus without any additional components.

- FEATURES**
- System Controller for 8080A Systems
 - Bi-Directional Data Bus for Processor Isolation
 - 3.60V Output High Voltage for Direct Interface to 8080A Processor
 - Three State Outputs on System Data Bus
 - Enables Use of Multi-Byte Interrupt Instructions
 - Generates RST 7 Interrupt Instruction
 - μPB8228 for Small Memory Systems
 - Reduces System Package Count
 - Schottky Bipolar Technology

PIN CONFIGURATION



PIN NAMES

D7 - D0	Data Bus (Processor Side)
DB7 - DB0	Data Bus (System Side)
I/OR	I/O Read
I/OW	I/O Write
MEMR	Memory Read
MEMW	Memory Write
DBIN	DBIN (From Processor)
INTA	Interrupt Acknowledge
HLDA	HLDA (From Processor)
WR	WR (From Processor)
BUSEN	Bus Enable Input
STSTB	Status Strobe (From μPB8224)
VCC	+5V
GND	0 Volts

μPB8228

Bi-Directional Bus Driver

The eight bit, bi-directional bus driver provides buffering between the processor data bus and the system data bus. On the processor side, the μPB8228 exceeds the minimum input voltage requirements (3.0V) of the μPD8080A. On the system side, the driver is capable of adequate drive current (10 mA) for connection of a large number of memory and I/O devices to the bus. Single flow in the bus driver is controlled by the gating array and its outputs can be forced into a high impedance state by use of the BUSEN input.

Status Latch

The Status Latch in the μPB8228 stores the status information placed on the data bus by the 8080A at the beginning of each machine cycle. The information is latched when STSTB goes low and is then decoded by the gating array for the generation of control signals.

Gating Array

The Gating Array generates "active low" control signals for direct interfacing to system components by gating the contents of the status latch with control signals from the 8080A.

$\overline{MEM/R}$, $\overline{I/O R}$ and \overline{INTA} are generated by gating the DBIN signal from the processor with the contents of the status latch. $\overline{I/O R}$ is used to enable an I/O input onto the system data bus. $\overline{MEM/R}$ is used to enable a memory input.

\overline{INTA} is normally used to gate an interrupt instruction onto the system data bus. When used with the μPD8080A processor, the μPB8228 will decode an interrupt acknowledge status word during all three machine cycles for a multi-byte interrupt instruction. For 8080A type processors that do not generate an interrupt acknowledge status word during the second and third machine cycles of a multi-byte interrupt instruction, the μPB8228 will internally generate an \overline{INTA} pulse for those machine cycles.

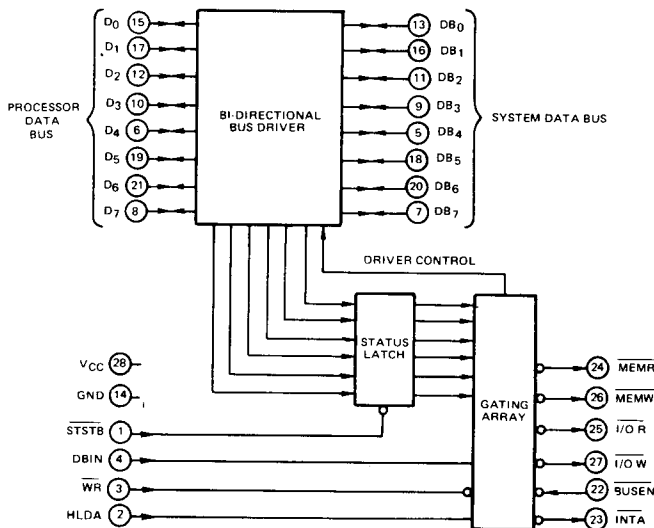
The μPB8228 also provides the designer the ability to place a single interrupt instruction onto the bus without adding additional components. By connecting the +12 volt supply to the \overline{INTA} output (pin 23) of the μPB8228 through a 1 K ohm series resistor, RESTART 7 will be gated onto the processor data bus when DBIN is active during an interrupt acknowledge machine cycle.

$\overline{MEM/W}$ and $\overline{I/O W}$ are generated by gating the \overline{WR} signal from the processor with the contents of the status latch. $\overline{I/O W}$ indicates that an output port write is about to occur. $\overline{MEM/W}$ indicates that a memory write will occur.

The data bus output buffers and control signal buffers can be asynchronously forced into a high impedance state by placing a high on the BUSEN pin of the μPB8228. Normal operation is performed with BUSEN low.

FUNCTIONAL DESCRIPTION

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Output or Supply Voltages	-0.5 to +7 Volts
All Input Voltages	-1.0 to +7.0 Volts
Output Currents	100 mA

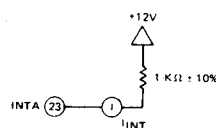
T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{CC} = 5V ± 5%

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Clamp Voltage, All Inputs	V _C			-1.0	V	V _{CC} = 4.75V; I _{CC} = -5 mA
Input Load Current, STSTB	I _F			500	μA	V _{CC} = 5.25V V _F = 0.45V
D ₂ and D ₆				750	μA	
D ₀ , D ₁ , D ₄ , D ₅ , and D ₇				250	μA	
All Other Inputs				250	μA	
Input Leakage Current, STSTB	I _R			100	μA	V _{CC} = 5.25V V _R = 5.0V
DB ₀ through DB ₇				20	μA	
All Other Inputs				100	μA	
Input Threshold Voltage, All Inputs	V _{TH}	0.8		2.0	V	V _{CC} = 5V
Power Supply Current	I _{CC}			190	mA	V _{CC} = 5.25V
Output Low Voltage, D ₀ through D ₇	V _{OL}			0.45	V	V _{CC} = 4.75V; I _{OL} = 2 mA
All Other Outputs				0.48	V	I _{OL} = 10 mA
Output High Voltage, D ₀ through D ₇	V _{OH}	3.6			V	V _{CC} = 4.75V; I _{OH} = -10 μA
All Other Outputs		2.4			V	I _{OH} = -1 mA
Short Circuit Current, All Outputs	I _{OS}	15		90	mA	V _{CC} = 5V
Off State Output Current, All Control Outputs	I _{O(off)}			100	μA	V _{CC} = 5.25V; V _O = 5.0V
				-100	μA	V _O = 0.45V
INTA Current	I _{INT}			5	mA	(See Figure below)



INTA TEST CIRCUIT

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CAPACITANCE

T_a = 25°C

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C _{IN}			12	pF	V _{BIAS} = 2.5V,
Output Capacitance Control Signals	C _{OUT}			15	pF	V _{CC} = 5.0V,
I/O Capacitance (D or DB)	C _{I/O}			15	pF	f = 1 MHz

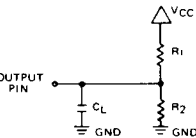
NOTE: This parameter is not 100% tested.

T_a = 0°C to 70°C, V_{CC} = 5V ± 5%

AC CHARACTERISTICS

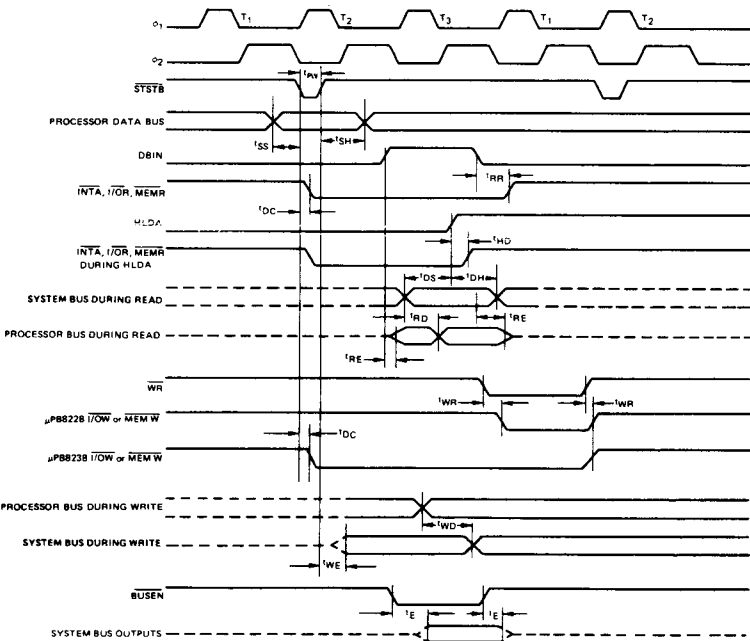
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Width of Status Strobe	t _{pw}	22			ns	
Setup Time, Status Inputs D ₀ -D ₇	t _{SS}	8			ns	
Hold Time, Status Inputs D ₀ -D ₇	t _{SH}	5			ns	
Delay from STSTB to any Control Signal	t _{DC}	20		60	ns	C _L = 100 pF
Delay from DBIN to Control Outputs	t _{RR}			30	ns	C _L = 100 pF
Delay from DBIN to Enable/Disable 8080A Bus	t _{RE}			45	ns	C _L = 25 pF
Delay from System Bus to 8080A Bus during Read	t _{RD}			30	ns	C _L = 25 pF
Delay from WR to Control Outputs	t _{WR}	5		45	ns	C _L = 100 pF
Delay to Enable System Bus DB ₀ -DB ₇ after STSTB	t _{WE}			30	ns	C _L = 100 pF
Delay from 8080A Bus D ₀ -D ₇ to System Bus DB ₀ -DB ₇ during Write	t _{WD}	5		40	ns	C _L = 100 pF
Delay from System Bus Enable to System Bus DB ₀ -DB ₇	t _E			30	ns	C _L = 100 pF
HLDA to Read Status Outputs	t _{HD}			25	ns	
Setup Time, System Bus Inputs to HLDA	t _{DS}	10			ns	
Hold Time, System Bus Inputs to HLDA	t _{DH}	20			ns	C _L = 100 pF

For D₀-D₇: R₁ = 4 KΩ, R₂ = ∞Ω.
C_L = 25 pF. For all other outputs:
R₁ = 500Ω, R₂ = 1 KΩ, C_L = 100 pF.



TEST CIRCUIT

TIMING WAVEFORMS



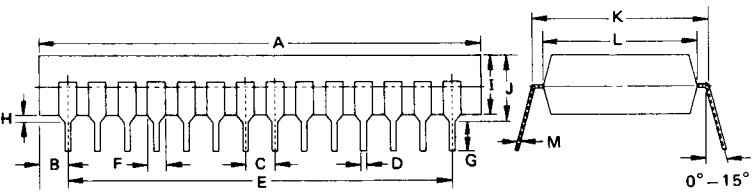
VOLTAGE MEASUREMENT POINTS: D₀-D₇ (when outputs) Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

STATUS WORD CHART

DATA BUS BIT		STATUS INFORMATION									
		INSTRUCTION INFORMATION									
		MEMORY FETCH									
		MEMORY READ									
		MEMORY WRITE									
		STACK READ									
		STACK WRITE									
		INPUT READ									
		OUTPUT WRITE									
		INTERRUPT ACKNOWLEDGE (M ₁)									
		INT. ACK. (M ₂ , M ₃)									
		HALT ACKNOWLEDGE									
		①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩
D ₀	INTA	0	0	0	0	0	0	0	1	0	1
D ₁	WO	1	1	0	1	0	1	0	1	1	1
D ₂	STACK	0	0	0	1	1	0	0	0	0	0
D ₃	HLTA	0	0	0	0	0	0	0	0	1	1
D ₄	OUT	0	0	0	0	0	0	1	0	0	0
D ₅	M ₁	1	0	0	0	0	0	0	1	0	1
D ₆	INP	0	0	0	0	0	1	0	0	0	0
D ₇	MEMR	1	1	0	1	0	0	0	0	1	0
24	MEMR	0	0	1	0	1	1	1	1	1	1
26	MEMW	1	1	0	1	0	1	1	1	1	1
25	I/OR	1	1	1	1	1	0	1	1	1	1
27	I/OW	1	1	1	1	1	1	0	1	1	1
23	INTA	1	1	1	1	1	1	1	0	0	1
PIN NO.		SIGNAL STATUS									
		μPB8228 CONTROL SIGNALS									

μPD8080A
OUTPUT

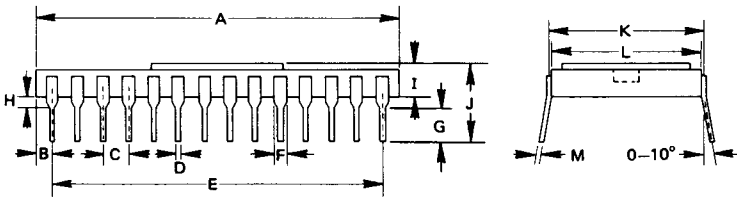
μPB8228
OUTPUT



PACKAGE OUTLINE
μPB8228C

(Plastic)

ITEM	MILLIMETERS	INCHES
A	38.0 MAX	1.496 MAX
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	0.25 ^{+0.10} _{-0.05}	0.01 ^{+0.004} _{-0.002}



μPB8228D

(Ceramic)

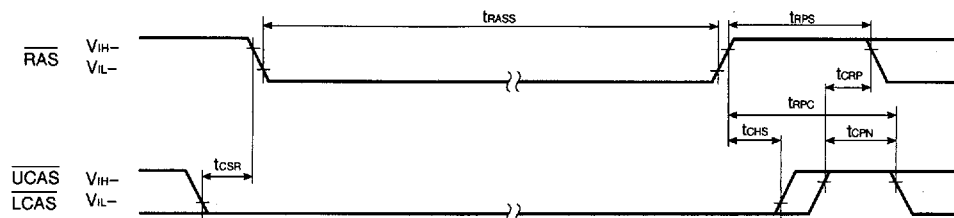
ITEM	MILLIMETERS	INCHES
A	36.2 MAX	1.43
B	1.59 MAX	0.06
C	2.54	0.1
D	0.46 ± 0.05	0.02 ± 0.004
E	33.02	1.3
F	1.02	0.04
G	3.2 MIN	0.13
H	1.0	0.04
I	3.5	0.14
J	4.5	0.18
K	15.24	0.6
L	14.93	0.59
M	0.25 ± 0.05	0.01 ± 0.002

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CAS Before RAS Self Refresh Cycle (Only for the μ PD42S18160)



Remark Address, \overline{WE} , \overline{OE} : Don't care L I/O, U I/O: Hi-Z

Cautions on Use of CAS Before RAS Self Refresh

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with long RAS only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh as follows just before and after setting CAS before RAS self refresh.

μ PD42S18160: 1,024 times within a 16 ms interval

(2) Normal Combined Use of CAS Before RAS Self Refresh and Long RAS Only Refresh

When CAS before RAS self refresh and RAS only refresh are used in combination, please perform RAS only refresh as follows just before and after setting CAS before RAS self refresh.

μ PD42S18160: 1,024 times within a 16 ms interval

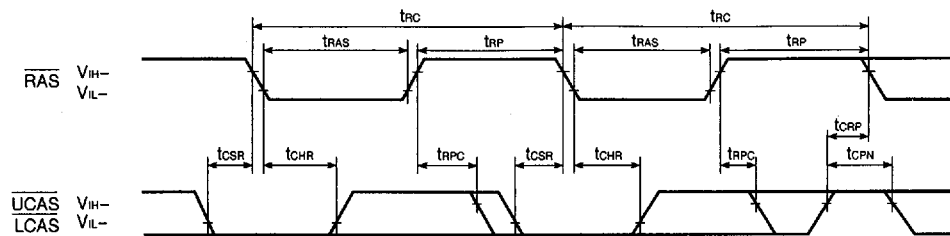
(3) If $t_{RASS} (MIN.)$ is not satisfied at the beginning of CAS before RAS self refresh cycles ($t_{RAS} < 100 \mu s$), CAS before RAS refresh cycles will be executed one time.

If $10 \mu s < t_{RAS} < 100 \mu s$, RAS precharge time for CAS before RAS self refresh (t_{RPS}) is applied. And refresh cycles as follows should be met.

μ PD42S18160: 1,024 times within a 128 ms interval

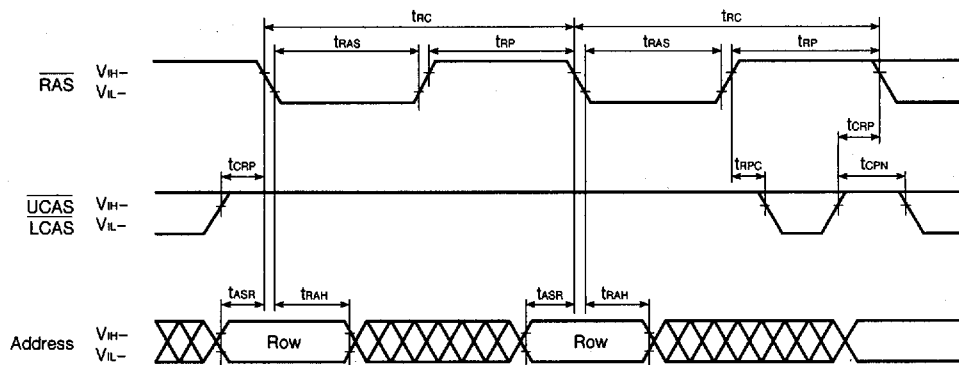
For details, please refer to **How to use DRAM** User's Manual.

CAS Before RAS Refresh Cycle



Remark Address, \overline{WE} , \overline{OE} : Don't care L I/O, U I/O: Hi-Z

RAS Only Refresh Cycle



Remark \overline{WE} , \overline{OE} : Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)

