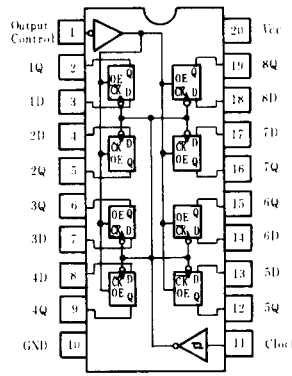
HD74LS374 ●Octal D-type Edge-triggered Flip-Flops (with three-state outputs)

The HD74LS374, 8-bit registers features totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide this register with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The eight flip-flops are edge-triggered D-type flip-flops. On the positive transition the clock, the Q outputs will be set to the logic states that were setup at the D inputs.

■PIN ARRANGEMENT



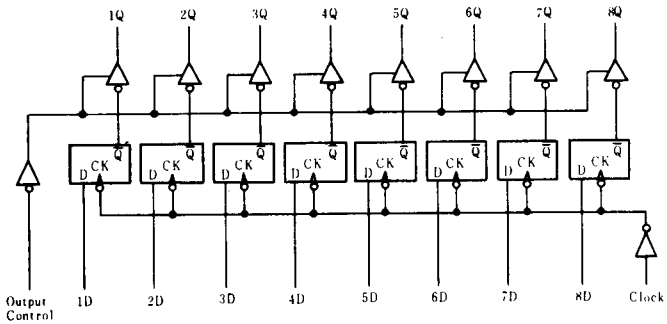
(Top View)

■FUNCTION TABLE

Inputs			Output
Output control	Clock	D	Q
L	↑	H	H
L	↑	L	L
L	L	×	Q_0
H	×	×	Z

Notes: H = high level, L = low level,
X = irrelevant
↑ = transition from low to high level
Q_0 = level of Q before the indicated steady-state input conditions were established
Z = off (high-impedance) state of a three-state output

■BLOCK DIAGRAM



■RECOMMENDED OPERATING CONDITION

Item		Symbol	min	typ	max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output voltage		V_{OH}	—	—	5.5	V
Output current		I_{OH}	—	—	−2.6	mA
		I_{OL}	—	—	24	mA
Clock pulse width	"H" level	t_w	15	—	—	ns
	"L" level		15	—	—	
Data setup time		t_{su}	20 ↑	—	—	ns
Data hold time		t_h	3 ↑	—	—	ns

Note) ↑ : The arrow indicates the rising edge of clock pulse.

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■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item	Symbol	Test Conditions		min	typ*	max	Unit
Input voltage	V_{IH}			2.0	—	—	V
	V_{IL}			—	—	0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-2.6mA$		2.4	—	—	V
	V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=12mA$	—	—	0.4	V
			$I_{OL}=24mA$	—	—	0.5	
Off-state output current	I_{OZH}	$V_{CC}=5.25V$, $V_{IH}=2V$	$V_O=2.7V$	—	—	20	μA
	I_{OZL}		$V_O=0.4V$	—	—	−20	
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		—	—	20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		—	—	−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$		—	—	0.1	mA
Short-circuit output current	I_{OS}	$V_{CC}=5.25V$		−30	—	−130	mA
Supply current	I_{CC}	$V_{CC}=5.25V$, $V_I=4.5V$ (Output control)		—	27	40	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		—	—	−1.5	V

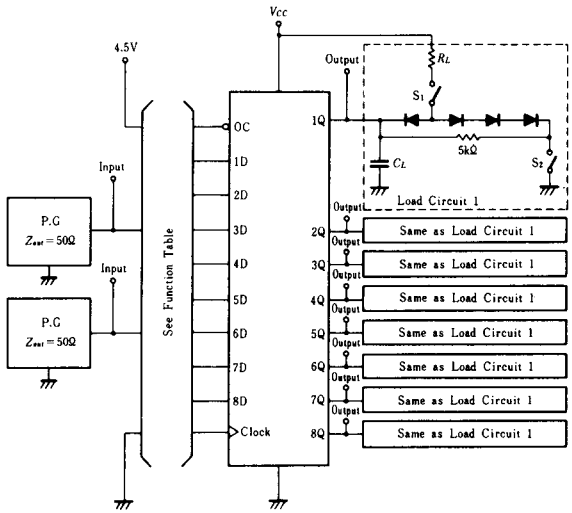
* $V_{CC}=5V$, $Ta=25°C$

■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

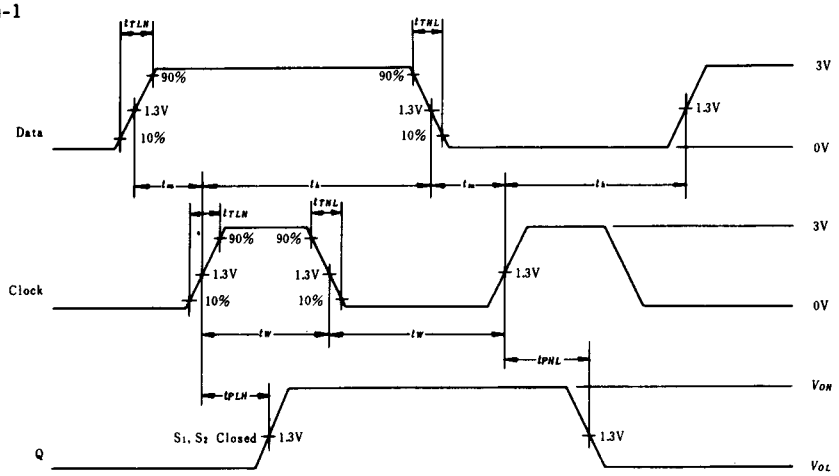
Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}	Clock	Q	$C_L=45pF$ $R_L=667\Omega$	35	50	—	MHz
Propagation delay time	t_{PLH}	Clock	Q		—	15	28	ns
	t_{PHL}				—	19	28	
Output enable time	t_{ZH}	OC	Q		—	20	28	
	t_{ZL}				—	21	28	
Output disable time	t_{HZ}	OC	Q	$C_L=5pF$ $R_L=667\Omega$	—	12	20	
	t_{LZ}				—	14	25	

■TESTING METHOD

Test Circuit

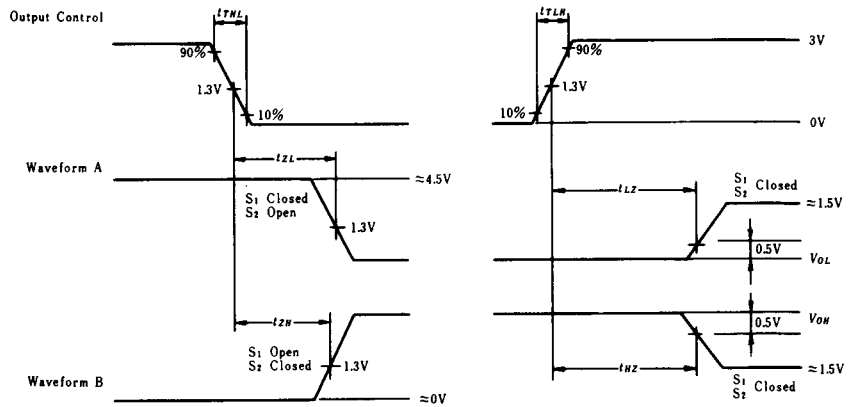


Waveform-1



Notes: 1. Input pulse; t_{TLH} = 15ns, t_{THL} = 6ns
Clock input; PRR = 1MHz, duty cycle 50%
Data input; PRR = 500kHz, duty cycle 50%
2. f_{max}: t_{TLH} = 2.5ns, t_{THL} = 2.5ns

Waveform-2



Notes: 1. Input pulse; t_{TLH} = 15ns, t_{THL} = 6ns, PRR = 1MHz, duty cycle 50%
2. Waveform A is for an output with internal conditions such that the output is low except when disable by the output control. Waveform B is for an output with internal conditions such that the output is high except when disabled by the output control.

PACKAGING INFORMATIONS

T-90-20

Factory orders for circuits described in this databook should include a three-part type number as explained in the following example.

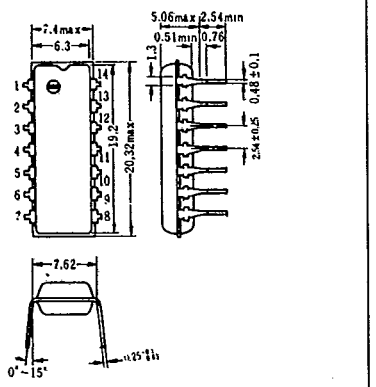
HD 74LS00 P

- Package ; Plastic DIP ; letters P
  Cerdip ; non-letters
- Circuit description
- Prefix : HD ; Hitachi Digital IC

■Plastic DIP

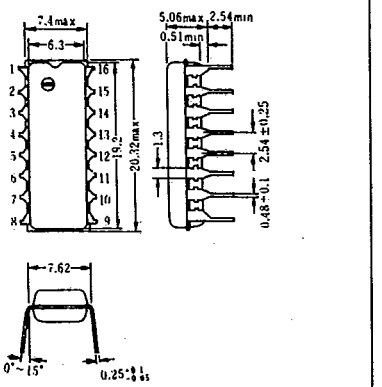
●14 Pin

DP-14



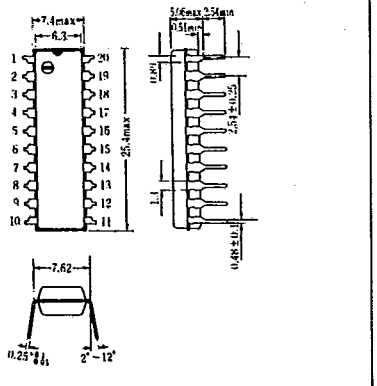
●16 Pin

DP-16



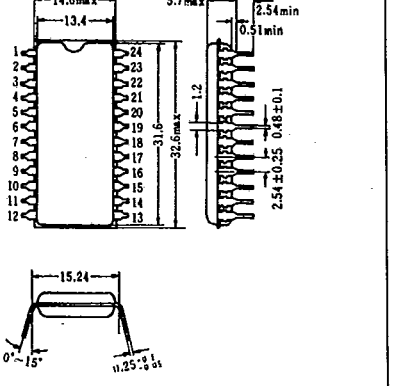
●20 Pin

DP-20



●24 Pin

DP-24

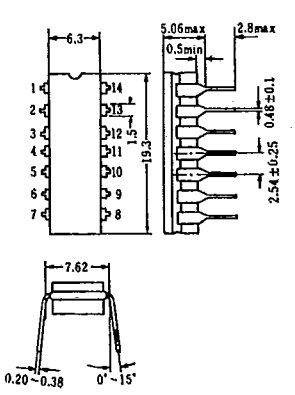


PACKAGING INFORMATIONS

■Cerdip

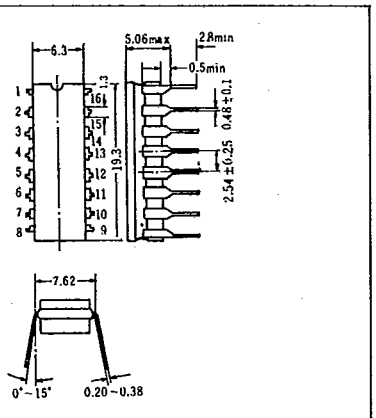
●14 Pin

DG-14



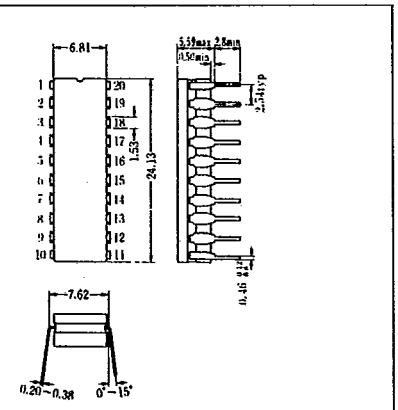
●16 Pin

DG-16



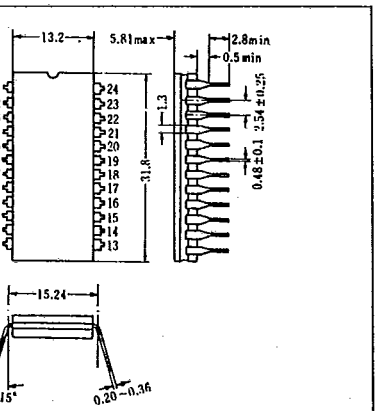
●20 Pin

DG-20



●24 Pin

DG-24



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