ANALOG DEVICES

CMOS 12-Bit Monolithic Multiplying CMOS D/A Converter

T-51-09-12 **PM-7541A**

2

FEATURES

- 7541 with Improved Accuracy and Ruggedness
- ±1/2 LSB Max Nonlinearity Over Full Temp. Range (12-Bit Linearity)
- ±1 LSB Max Gain Error – No User Adjustment Required
- Less Than 0.03 LSB Max Zero Scale Error (5nA)
- Low Gain Tempco .....5ppm/°C Max
- All Data Input Pins Designed with ESD Protective Circuitry
- Full Four-Quadrant Multiplication
- Low Power Consumption
- Low Feedthrough Error and Digital Charge Injection
- Superior Power Supply Rejection From +5V to +15V .....001%% Max
- Direct Replacement for AD7541 and AD7541A
- Both DIP Packages Suitable for Auto-Insertion, Surface Mount Packaging Available
- Available in Die Form

APPLICATIONS

- Digital/Synchro Conversion
- Programmable Amplifiers
- Ratiometric A/D Conversion
- Function Generators
- Digitally-Controlled Attenuators
- Digitally-Controlled Power Supplies
- Digitally-Controlled Filters

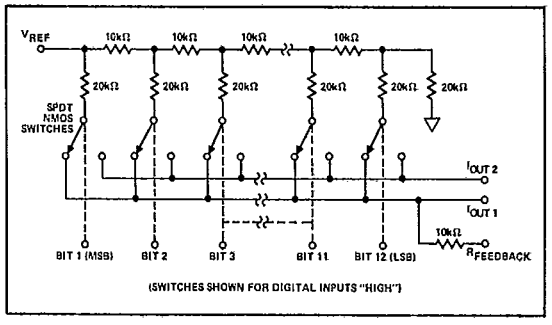
GENERAL DESCRIPTION

PMI's PM-7541A is a 12-bit resolution, current output, 4-quadrant multiplying digital-to-analog converter. Manufactured with advanced oxide-isolated, silicon-gate, monolithic CMOS technology, the PM-7541A features circuitry designed to protect data inputs against damage from electrostatic discharges.

Laser-trimmed thin-film resistors provide true 12-bit linearity with excellent absolute accuracy. The PM-7541A's low power dissipation, along with NMOS temperature compensating switches, insures high performance across the full temperature range.

The PM-7541A is a superior pin-compatible replacement for the industry standard 7541 and the AD7541A. Available in standard plastic and CerDIP packages, the PM-7541A is compatible with automatic insertion equipment. The improved performance of the PM-7541A permits upgrading existing designs with greater ruggedness and accuracy. Tighter linearity and gain error specifications may permit reduced system parts count by eliminating trimming circuitry.

FUNCTIONAL DIAGRAM



ORDERING INFORMATION †

GAIN ERROR	NON-LINEARITY	PACKAGE: MILITARY* TEMPERATURE –55°C to +125°C	PACKAGE: EXTENDED INDUSTRIAL TEMPERATURE –40°C to +85°C	PACKAGE: COMMERCIAL TEMPERATURE 0°C to +70°C
±1 LSB	±1/2 LSB	PM7541AAX	PM7541AEX	PM7541AGP
±2 LSB	±1/2 LSB	PM7541ABX	PM7541AFX	–
±2 LSB	±1/2 LSB	PM7541ABRC/883	PM7541AFP	–
±2 LSB	±1/2 LSB	–	PM7541AFPC	–
±2 LSB	±1/2 LSB	–	PM7541AFS	–

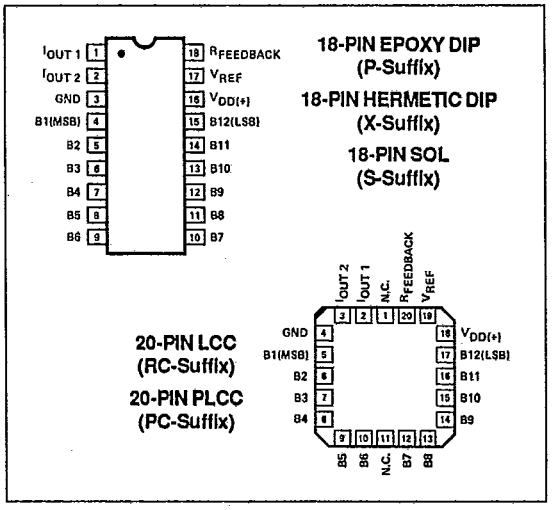
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7541AAX PM7541ABX	AD7541ATD AD7541ASD	MIL
PM7541AEX PM7541AFX	AD7541ABQ AD7541AAQ	IND
PM7541GP PM7541FPC PM7541AFP	AD7541AKN AD7541AKP AD7541AJN	COM

PIN CONNECTIONS



PM-7541A

T-51-09-12

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted)

V_{DD} (to GND) ..... ±17V
V_{REF} (to GND) ..... ±25V
V_{RFB} (to GND) ..... ±25V
Digital Input Voltage Range ..... V_{DD} to GND
Operating Temperature Range
AX/BX/ARC/BRC Versions ..... –55°C to +125°C
EX/FX/FP/FPC/FS Versions ..... –40°C to +85°C
GP Version ..... 0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
18-Pin Hermetic DIP (X)	79	11	°C/W
18-Pin Plastic DIP (P)	70	30	°C/W
20-Contact LCC (RC)	88	33	°C/W
18-Pin SOL (S)	88	25	°C/W
20-Contact PLCC (PC)	73	33	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL and PLCC packages.

CAUTION:
1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} (Pin 17) and R_{FB} (Pin 18).
2. The digital control inputs are zener protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper antistatic handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS

at V_{DD} = +15V, V_{REF} = +10V, $V_{OUT\,1}$ = $V_{OUT\,2}$ = 0V; T_A = –55°C to +125°C apply for PM-7541AAX/BX/ARC/BRC; T_A = –40°C to +85°C apply for PM-7541AEX/FX/FP/FPC/FS; and T_A = 0°C to +70°C apply for PM-7541AGP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution	N		12	—	—	LSB
Nonlinearity (Note 1)	INL		—	—	±1/2	LSB
Differential Nonlinearity (Note 2)	DNL	PM-7541AA/E/G	—	—	±1/2	LSB
		PM-7541AB/F	—	—	±1	
Gain Error (Note 3)	G_{FSE}	T_A = +25°C				LSB
		PM-7541AA/E/G	—	—	1	
		PM-7541AB/F	—	—	2	
		T_A = Full Temp. Range				
		PM-7541AA/E/G	—	—	2	
		PM-7541AB/F	—	—	3	
Gain Tempco (ΔGain/ΔTemp.) (Note 6)	TC_{GFS}		—	±2	±5	ppm/°C
Power Supply Rejection Ratio (ΔGain/ΔV_{DD})	PSRR	ΔV_{DD} = ±5%				%/%
		T_A = +25°C	—	—	±0.001	
		T_A = Full Temp. Range	—	—	±0.002	
Output Leakage Current (Notes 4, 5)	I_{LKG}	T_A = +25°C				nA
		PM-7541AA/B/E/F/G	—	—	5	
		T_A = Full Temp. Range				
		PM-7541AA/B	—	—	100	
		PM-7541AE/F/G	—	—	10	
Zero Scale Error (Notes 12, 13)	I_{ZSE}	T_A = +25°C				LSB
		PM-7541AA/B/E/G	—	0.002	—	
		T_A = Full Temp. Range				
		PM-7541AA/B	—	0.05	—	
		PM-7541AE/F/G	—	0.01	—	
REFERENCE INPUTS						
Input Resistance (Note 9)	R_{REF}		7	11	15	kΩ

ELECTRICAL CHARACTERISTICS at V_{DD} = +15V, V_{REF} = +10V, $V_{OUT\,1}$ = $V_{OUT\,2}$ = 0V; T_A = −55°C to +125°C apply for PM-7541AAX/BX/ARC/BRC; T_A = −40°C to +85°C apply for PM-7541AEX/FX/FP/FPC/FS; and T_A = 0°C to +70°C apply for PM-7541AGP, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
V_{DD} Range	V_{DD}	Accuracy is not guaranteed over this range	+5	15	+17	V
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL}	—	—	2	mA
		Digital Inputs = 0V or V_{DD}				
		T_A = +25°C	—	—	100	µA
		T_A = Full Temp. Range	—	—	100	
DIGITAL INPUTS						
Digital Input High	V_{IH}		2.4	—	—	V
Digital Input Low	V_{IL}		—	—	0.8	V
Input Leakage Current (Note 10)	I_{IL}	V_{IN} = 0 to +15V	—	—	±1	µA
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V	—	—	8	pF
DYNAMIC PERFORMANCE						
Propagation Delay (Notes 6, 7)	t_{PD}	From Digital Input Change to 90% of Final Analog Output T_A = +25°C	—	100	150	ns
Output Current Settling Time (Notes 6, 7, 8)	t_S	To ±1/2 LSB (±0.01% of Full Scale Range) T_A = +25°C	—	0.6	1	µs
Feedthrough Error (V_{REF} to I_{OUT}) (Note 6)	FT	V_{REF} = 20V_{p-p} @ f = 10kHz All Digital Inputs Low T_A = +25°C	—	2	5	mV_{p-p}
Digital to Analog Glitch Energy (Notes 6, 11)	Q	T_A = +25°C	—	700	1000	nVs
ANALOG OUTPUTS						
Output Capacitance (Note 6)	$C_{OUT\,1}$	Digital Inputs = V_{IH}	—	85	120	pF
	$C_{OUT\,2}$		—	30	50	
	$C_{OUT\,1}$	Digital Inputs = V_{IL}	—	30	50	
	$C_{OUT\,2}$		—	85	120	

NOTES:
1. ±1/2 LSB = ±0.012% of Full Scale.
2. All grades are monotonic to 12-bits over temperature.
3. Using internal feedback resistor.
4. Applies to $I_{OUT\,1}$; digital inputs = V_{IL}.
5. Specification also applies for $I_{OUT\,2}$ with all digital inputs = V_{IH}.
6. Guaranteed by design and not tested.
7. I_{OUT} Load = 100Ω, C_{EXT} = 13pF, digital inputs = 0V to V_{DD} or V_{DD} to 0V.
8. Extrapolated to 1/2 LSB: t_s = Propagation Delay (t_{PD}) + 9τ, where τ = measured first time constant of the final RC decay.
9. Absolute temperature coefficient is approximately +50 ppm/°C.
10. Digital inputs are CMOS gates; I_{IN} is typically 1nA at +25°C.
11. V_{REF} = 0V, all digital inputs = 0V to V_{DD} or V_{DD} to 0V.
12. V_{REF} = +10V, all digital inputs = 0V.
13. Calculated from: $I_{ZSE}(\text{in LSBs}) = \frac{R_{REF}(4096)I_{LKG}}{V_{REF}}$

PM-7541A

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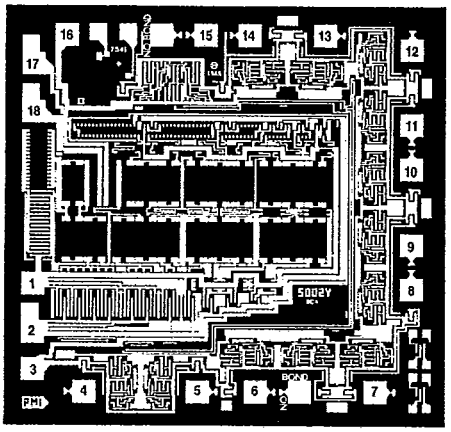
DICE CHARACTERISTICS



DIE SIZE 0.102 × 0.100 inch, 10,200 sq. mils
(2.59 × 2.54 mm, 6.58 sq. mm)

1. CURRENT OUTPUT 1
2. CURRENT OUTPUT 2
3. GROUND
4. DIGITAL INPUT (BIT 1) (MOST SIGNIFICANT BIT)
5. DIGITAL INPUT (BIT 2)
6. DIGITAL INPUT (BIT 3)
7. DIGITAL INPUT (BIT 4)
8. DIGITAL INPUT (BIT 5)
9. DIGITAL INPUT (BIT 6)
10. DIGITAL INPUT (BIT 7)
11. DIGITAL INPUT (BIT 8)
12. DIGITAL INPUT (BIT 9)
13. DIGITAL INPUT (BIT 10)
14. DIGITAL INPUT (BIT 11)
15. DIGITAL INPUT (BIT 12) (LEAST SIGNIFICANT BIT)
16. POSITIVE POWER SUPPLY
17. REFERENCE INPUT VOLTAGE
18. INTERNAL FEEDBACK RESISTOR

WAFER TEST LIMITS at V_{DD} = +15V, V_{REF} = +10V, AGND = DGND = 0V, $V_{OUT\,1}$ = $V_{OUT\,2}$ = 0V, T_A = +25°C.

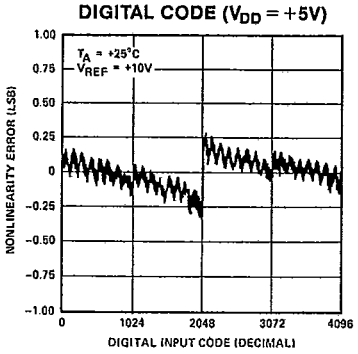
PARAMETER	SYMBOL	CONDITIONS	PM-7541AG LIMIT	UNITS
STATIC ACCURACY				
Resolution	N		12	Bits MIN
Nonlinearity	INL		±1/2	LSB MAX
Differential Nonlinearity	DNL		±1	LSB MAX
Gain Error (Note 1)	G_{FSE}		±1	LSB MAX
Power Supply Rejection	PSRR	ΔV_{DD} = ±5%	±0.001	%/% MAX
Output Leakage Current ($I_{OUT\,1}$) (Note 2)	I_{LKG}	Digital Inputs = V_{IL}	±5	nA MAX
REFERENCE INPUT				
Input Resistance	R_{REF}		7/15	kΩ MIN/MAX
DIGITAL INPUTS				
Digital Input High	V_{IH}		2.4	V MIN
Digital Input Low	V_{IL}		0.8	V MAX
Input Leakage Current	I_{IL}	V_{IN} = 0 to 15V	±1	μA MAX
POWER SUPPLY				
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL} Digital Inputs = 0V or V_{DD}	2 100	mA MAX μA MAX

NOTES:
1. Using internal feedback resistor.
2. Specification also applies for $I_{OUT\,2}$ but all Digital Inputs = V_{IH}.

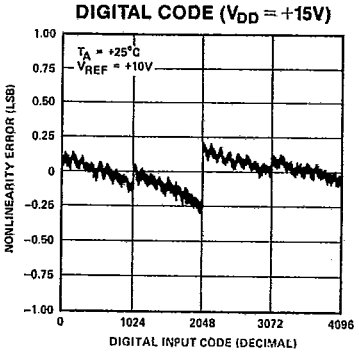
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

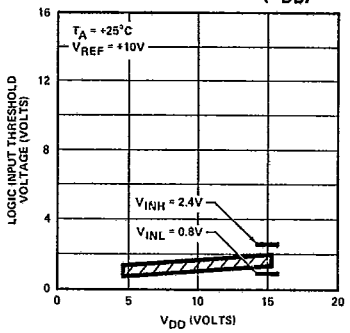
NONLINEARITY ERROR vs DIGITAL CODE (V_{DD} = +5V)



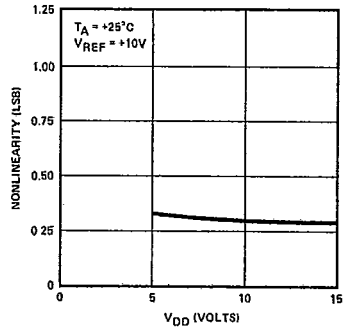
NONLINEARITY ERROR vs DIGITAL CODE (V_{DD} = +15V)



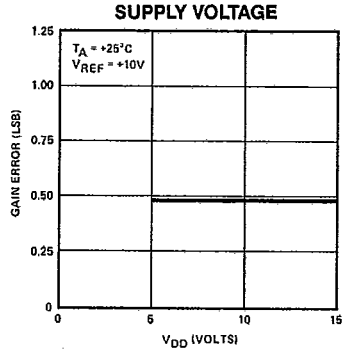
LOGIC INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE (V_{DD})



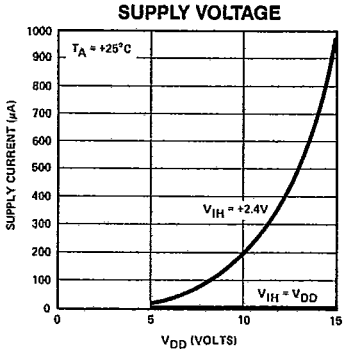
NONLINEARITY vs SUPPLY VOLTAGE



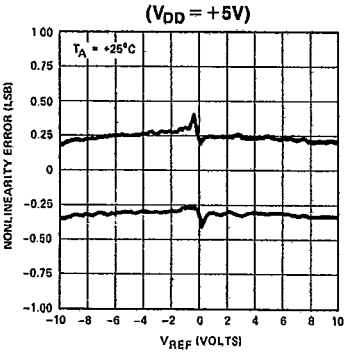
GAIN ERROR vs SUPPLY VOLTAGE



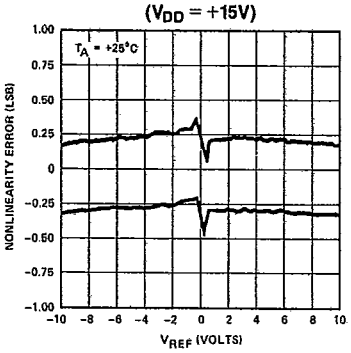
SUPPLY CURRENT vs SUPPLY VOLTAGE



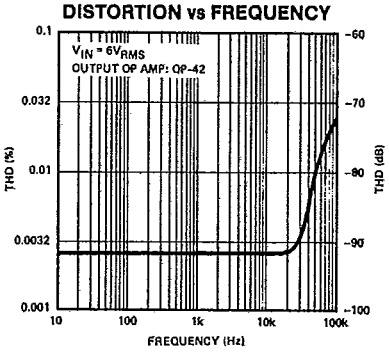
NONLINEARITY ERROR vs REFERENCE VOLTAGE (V_{DD} = +5V)



NONLINEARITY ERROR vs REFERENCE VOLTAGE (V_{DD} = +15V)



MULTIPLYING MODE TOTAL HARMONIC DISTORTION vs FREQUENCY



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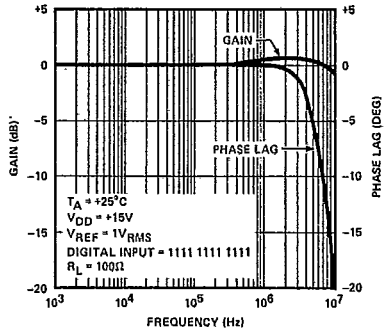
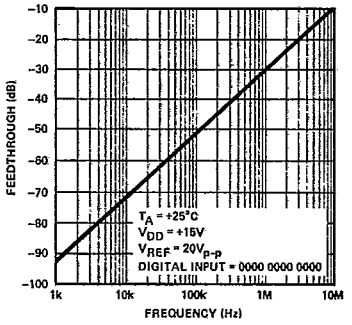
TYPICAL PERFORMANCE CHARACTERISTICS

V_{REF} PHASE LAG AND FREQUENCY RESPONSE



FEEDTHROUGH vs FREQUENCY



SPECIFICATION DEFINITIONS

RESOLUTION

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into, where "n" is equal to the number of bits.

SETTLING TIME

Time required for the analog output of the DAC to settle to within 1/2 LSB of its final value for a given digital input stimulus; i.e., zero to full scale.

GAIN

Ratio of the DAC's external operational amplifier output voltage to the V_{REF} input voltage when all digital inputs are HIGH.

FEEDTHROUGH ERROR

Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE

Capacitance from $I_{OUT\,1}$ or $I_{OUT\,2}$ terminals to ground.

OUTPUT LEAKAGE CURRENT

Current which appears on $I_{OUT\,1}$ terminal with all digital inputs LOW, or on $I_{OUT\,2}$ terminal when all inputs are HIGH.

CIRCUIT DESCRIPTION

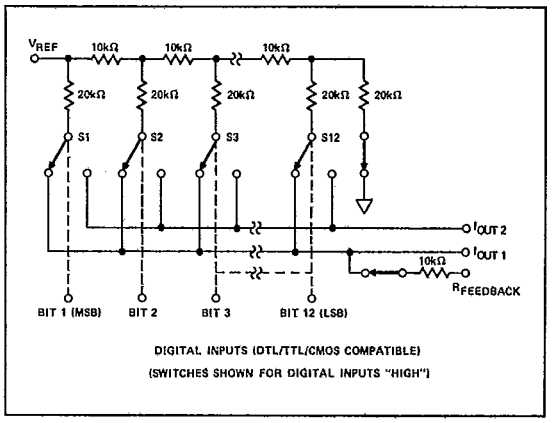
GENERAL CIRCUIT INFORMATION

The PM-7541A is a 12-bit multiplying D/A converter consisting of a highly-stable, silicon-chrome, thin film, R-2R resistor ladder network and twelve pairs of NMOS current steering switches on a monolithic chip. Most applications require the addition of a voltage or current reference and an output operational amplifier.

A simplified circuit of the PM-7541A is shown in Figure 1. The R-2R inverted ladder binarily divides the input currents that are switched between $I_{OUT\,1}$ and $I_{OUT\,2}$ bus lines. This switching allows a constant current to be maintained in each ladder leg independent of the input code.

The design includes a matching switch in series with the feedback (R_{FB}) and terminating resistors. These switches (Figure 1) provide improved gain and linearity performance over the operating temperature range.

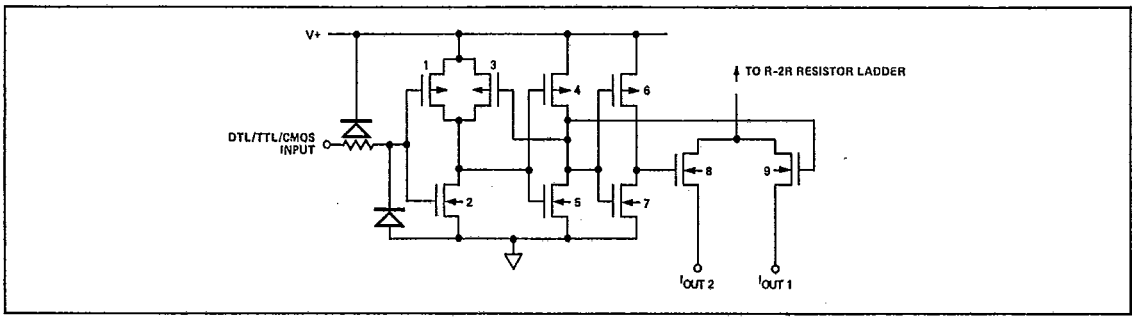
FIGURE 1: Simplified DAC Circuit



One of the twelve CMOS switches is shown in Figure 2. The digital input stage, devices 1, 2, and 3, drives the two inverters, devices 4, 5, 6, and 7; these inverters in turn drive the two output current steering switches, devices 8 and 9. Devices 1, 2, and 3 are designed such that the digital control inputs are DTL, TTL, and CMOS compatible over the full military temperature range.

The twelve output current-steering switches are in series with the R-2R resistor ladder, and therefore, can introduce bit errors. It is essential then, that the switch "ON" resistance be binarily scaled so that the voltage drop across each switch remains constant. If, for example, switch 1 of Figure 1 were designed with an "ON" resistance of 10 ohms, switch 2 for 20 ohms, etc., then with a 10 volt reference input, the current through switch 1 is 0.5mA, switch 2 is 0.25mA, etc., a constant 5mV drop will then be maintained across each switch.

FIGURE 2: CMOS Switch



To further insure accuracy across the full temperature range, permanently "ON" MOS switches are included in series with the feedback resistor and the R-2R ladder's terminating resistor. These series switches are equivalently scaled to two times switch 1 (MSB) and to switch 12 (LSB) respectively to maintain constant relative voltage drops with varying temperature. During any testing of the resistor ladder or $R_{FEEDBACK}$ (such as incoming inspection), V_{DD} must be present to turn "ON" these series switches.

ESD PROTECTION

In the design of the PM-7541A's data inputs, ESD resistance has been incorporated through careful layout and the inclusion of input protection circuitry.

Figure 2 shows the input protection diodes. High voltage static charges applied to the digital inputs are shunted to the supply and ground rails through forward biased diodes. These protection diodes clamp the inputs well below dangerous levels during static discharge conditions.

EQUIVALENT CIRCUIT ANALYSIS

Figures 3 and 4 show the equivalent circuits for all digital inputs LOW and HIGH respectively. The reference current is switched to $I_{OUT\,2}$ when all inputs are LOW and $I_{OUT\,1}$ when inputs are HIGH. The $I_{LEAKAGE}$ current source is the combination of surface and junction leakages to the substrate; the 1/4096 current source represents the constant 1-bit current drain through the ladder terminating resistor. The output capacitance is dependent upon the digital input code, and is therefore varied between the low and high values.

FIGURE 3: PM-7541A Equivalent Circuit (All Inputs LOW)

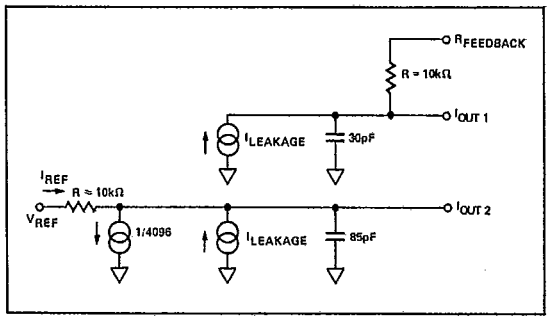
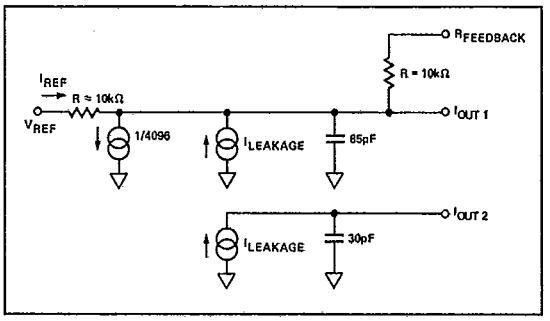


FIGURE 4: PM-7541A Equivalent Circuit (All Digital Inputs HIGH)



DYNAMIC PERFORMANCE

OUTPUT IMPEDANCE

The output resistance, as in the case of the output capacitance, varies with the digital input code. This resistance, looking back into the $I_{OUT\,1}$ terminal, may be between 10kΩ (the feedback resistor alone when all digital inputs are low) and 7.5kΩ (the feedback resistor in parallel with approximately 30kΩ of the R-2R ladder network resistance when any single bit logic is high). Static accuracy and dynamic performance will be affected by these variations. The gain and phase stability of the output amplifier, board layout, and power supply decoupling will all affect the dynamic performance of the PM-7541A. The use of a compensation capacitor may be required when high-speed operational amplifiers are used. It may be connected across the amplifiers feedback resistor to provide the necessary phase compensation to critically damp the output.

The considerations when using high-speed amplifiers are:

1. Phase compensation (See Figures 5 and 6).
2. Power supply decoupling at the device socket and use of proper grounding techniques.

PM-7541A

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FIGURE 5: Unipolar Binary Operation with High Accuracy Op Amp (2-Quadrant)

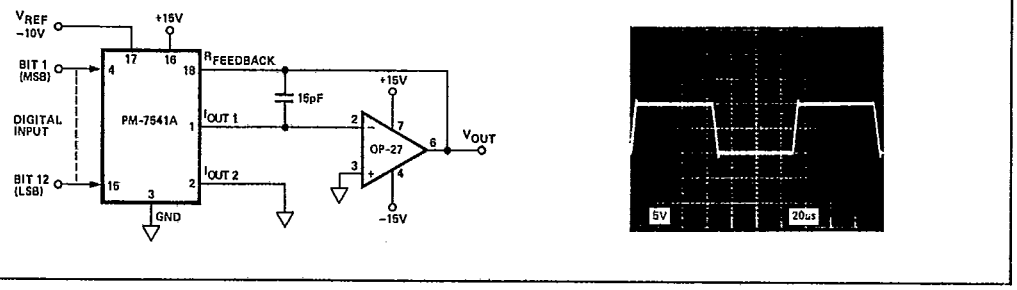
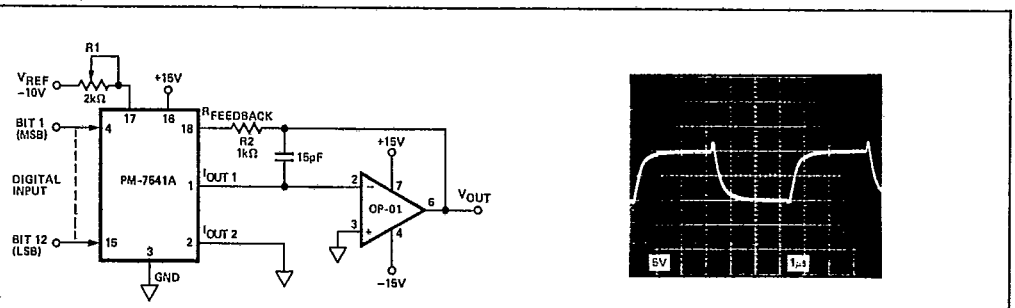
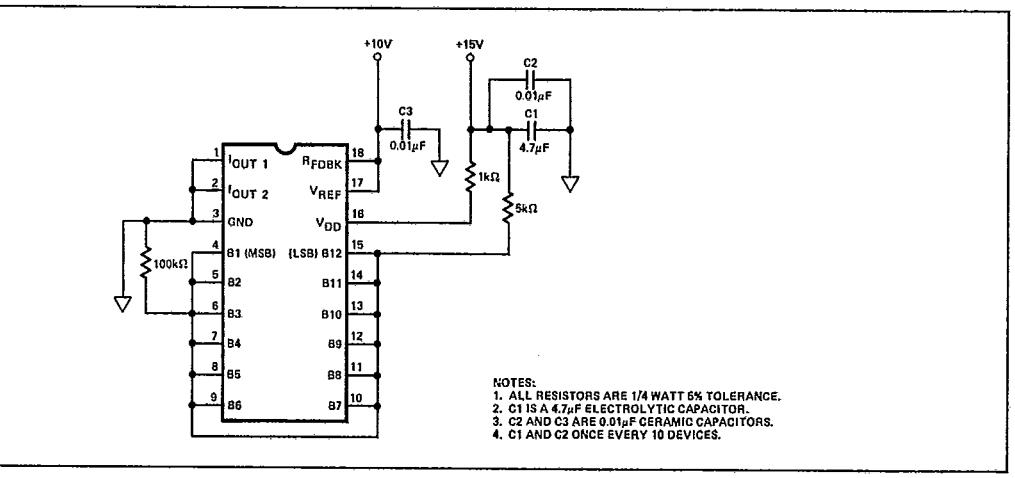


FIGURE 6: Unipolar Binary Operation with Fast Output Op Amp (2-Quadrant)



BURN-IN CIRCUIT



NOTES:
1. ALL RESISTORS ARE 1/4 WATT 5% TOLERANCE.
2. C1 IS A 4.7µF ELECTROLYTIC CAPACITOR.
3. C2 AND C3 ARE 0.01µF CERAMIC CAPACITORS.
4. C1 AND C2 ONCE EVERY 10 DEVICES.

APPLICATIONS INFORMATION

APPLICATION TIPS

Linearity depends upon the potential of $I_{OUT\,1}$ and $I_{OUT\,2}$ (pins 1 and 2) being exactly equal to GND (pin 3). In most applications, the DAC is connected to an external op amp with its noninverting input tied to ground, see Figures 5 and 6. The amplifier selected should have a low input bias current and low drift over temperature. The amplifier's input offset voltage should be nulled to less than $\pm 200\mu V$ (less than 10% of 1 LSB).

The operational amplifier's noninverting input should have a minimum resistance connection to ground; the usual bias current compensation resistor should not be used. This resistor can cause a variable offset voltage appearing as a varying output error. All grounded pins should tie to a common ground point, avoiding ground loops. The V_{DD} power supply should have a low noise level with no transients greater than +17V.

Unused digital inputs must always be grounded or taken to V_{DD}; this will prevent noise from triggering the high impedance digital input resulting in output errors. It is also recommended that the used digital inputs be taken to ground or V_{DD} via a high value (1MΩ) resistor; this will prevent the accumulation of static charge if the PC card is disconnected from the system.

Peak supply current flows as the digital inputs pass through the transition voltage. The supply current decreases as the input voltage approaches the supply rails (V_{DD} or DGND), i.e., rapidly slewing logic signals that settle very near the supply rails will minimize supply current.

OUTPUT AMPLIFIER CONSIDERATIONS

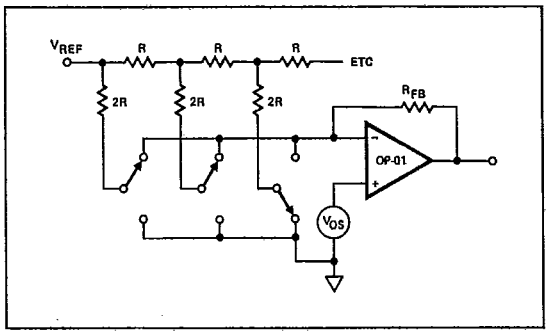
For low speed or static applications, AC specifications of the amplifier are not very critical. In high-speed applications, slew rate, settling time, open-loop gain, and gain/phase margin specifications of the amplifier should be selected for the desired performance. It has already been noted that an offset can be caused by including the usual bias current compensation resistor in the amplifier's noninverting input-terminal. This resistor should not be used. Instead, the amplifier should have a bias current which is low over the temperature range of interest.

The static accuracy is affected by the variation in the DAC's output resistance. This variation is best illustrated by using the circuit of Figure 7 and the equation:

$$\text{Error Voltage} = V_{OS}\left(1 + \frac{R_{FB}}{R_O}\right)$$

where R_O is a function of the digital code, and:
$R_O \cong 10k\Omega$ for more than 4-bits of logic 1
$R_O \cong 30k\Omega$ for any single bit logic 1

FIGURE 7: Simplified Circuit



Therefore, the offset gain varies as follows:

$$\text{At code 0011 1111 1111: } V_{ERROR\,1} = V_{OS}\left(1 + \frac{10k\Omega}{10k\Omega}\right) = 2\,V_{OS}$$

$$\text{At code 0100 0000 0000: } V_{ERROR\,2} = V_{OS}\left(1 + \frac{10k\Omega}{30k\Omega}\right) = \frac{4}{3}V_{OS}$$

The error difference is 2/3 V_{OS}.

Since one LSB has a weight (for $V_{REF} = +10V$) of 2.5mV for the PM-7541A DAC, it is clearly important that V_{OS} be minimized, either using the amplifier's nulling pins, an external nulling network, or by selection of an amplifier with inherently low V_{OS}. Amplifiers with sufficiently low V_{OS} include PMI's OP-77, OP-07, and OP-27.

APPLICATIONS

Figures 5, 6, and 8 show simple unipolar and bipolar circuits with their associated waveforms using the PM-7541A and two types of PMI output amplifiers. A small feedback capacitor should be used across the amplifier to help prevent overshoot and ringing when using high-speed op amps. Resistor R1 is used to trim for full scale. Low tempco (approximately 50ppm/°C) resistors or trimpots should be selected when gain adjustments are required.

UNIPOLAR BINARY OPERATION (2-QUADRANT)

The circuits of Figures 5 and 6 can be used either as a fixed reference D/A converter, or as an attenuator with an AC input voltage. In the fixed reference mode, the DAC provides an analog output voltage in the range of zero to plus or minus V_{REF}, depending on V_{REF} polarity. The reference input voltage can range between –20V to +20V; this is due to the ability of V_{REF} to exceed V_{DD}, the limiting factor being the op amp's voltage range. Table 1 shows the code relationship for the circuit of Figures 5 and 6. R_1 can be omitted with a resulting maximum gain error of 0.02% of full scale.

TABLE 1: Unipolar Binary Code Table

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figures 5 and 6)
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0001	$-V_{REF}\left(\frac{2049}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -\frac{V_{REF}}{2}$
0111 1111 1111	$-V_{REF}\left(\frac{2047}{4096}\right)$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{0}{4096}\right) = 0$

NOTES:
1. Nominal full scale for the circuits of Figures 5 and 6 is given by $FS = -V_{REF}\left(\frac{4095}{4096}\right)$.
2. Nominal LSB magnitude for the circuits of Figures 5 and 6 is given by $LSB = V_{REF}\left(\frac{1}{4096}\right)$ or $V_{REF}(2^{-n})$.

BIPOLAR BINARY OPERATION (4-QUADRANT)

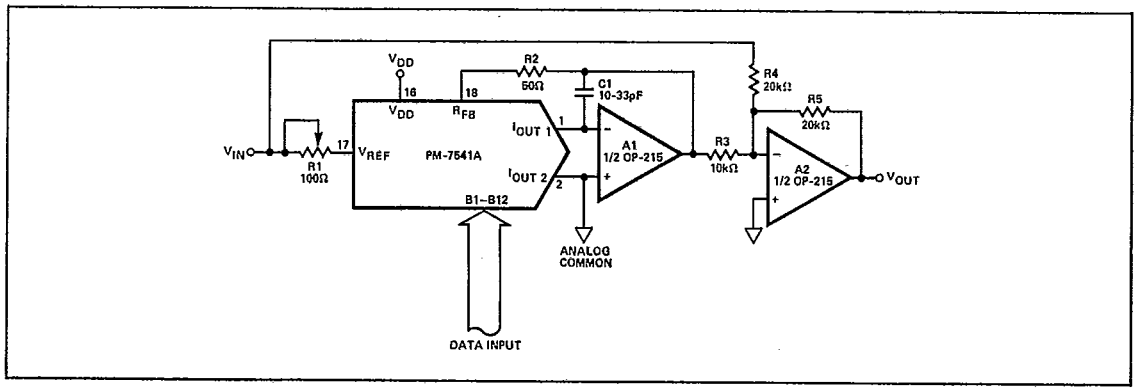
Figure 8 shows a simple bipolar output circuit using the PM-7541A and a PMI OP-215 dual op amp. The circuit uses offset binary coding and a fixed DC voltage for V_{REF}. Digitally-controlled attenuation of an AC signal occurs when the signal is used as the signal source at V_{REF}. Negative output full-scale is adjusted by setting the digital inputs to all zeros and adjusting the value of the V_{IN} voltage or R_5. The zero-scale output voltage is adjusted while the digital inputs are set to 1000 0000 0000 by adjusting R_1 for a zero output voltage (less than 10% of 1 LSB). Resistors R_3, R_4, and R_5 must be selected for matching and tracking in order to keep offset and full scale errors to a minimum. Resistors R_1 and R_2 temperature coefficients must be taken into account if they are used. C_1 phase compensation capacitor may not be needed and should be selected empirically. The digital input code versus analog output voltage is shown in Table 2.

TABLE 2: Bipolar (Offset Binary) Code Table

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 8)
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0
1111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0001	$-V_{REF}\left(\frac{2047}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

NOTES:
1. Nominal full scale for the circuit of Figure 8 is given by $FS = V_{REF}\left(\frac{2047}{2048}\right)$.
2. Nominal LSB magnitude for the circuit of Figure 8 is given by $LSB = V_{REF}\left(\frac{1}{2048}\right)$.

FIGURE 8: Bipolar Operation (4-Quadrant Multiplication)



2

ANALOG/DIGITAL DIVISION

The transfer function for the PM-7541A connected in the multiplying mode as shown in Figures 5 and 6 is:

$$V_O = -V_{IN}\left(\frac{A_1}{2^1}+\frac{A_2}{2^2}+\frac{A_3}{2^3}+\ldots\ldots\ldots\frac{A_{12}}{2^{12}}\right)$$

where A_X assumes a value of 1 for an "ON" bit and 0 for an "OFF" bit. The transfer function is modified when the DAC is connected in the feedback of an operational amplifier as shown in Figure 9. It now is:

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1}+\frac{A_2}{2^2}+\frac{A_3}{2^3}+\ldots\ldots\ldots\frac{A_{12}}{2^{12}}}\right)$$

The above transfer function is the division of an analog voltage (V_{REF}) by a digital word. The amplifier goes to the rails with all bits "OFF" since division by zero is infinity. With all bits "ON," the gain is 1 (±1 LSB). The gain becomes 4096 with the LSB, bit 12, "ON."

FIGURE 9: Analog/Digital Divider