



LXT6251A

21 E1 SDH Mapper

Datasheet

The LXT6251A 21E1 Mapper performs asynchronous mapping and demapping of 21 E1 PDH signals into SDH. The PDH side interfaces with E1 LIUs and framers via NRZ Clock & Data, while the SDH side uses a standard Telecom bus interface. Further processing by the companion LXT6051 Overhead Terminator chip creates the final STM-0 or STM-1 signal. One mapper provides complete processing of 21 E1s in STM-0, while three mappers can process 63 E1s in STM-1.

The LXT6251A is compliant with the latest releases of ITU-T G.703 and G.707. It provides all the alarm and control features to easily implement the multiplexer specified in ITU-T G.783.

Applications

- 21 or 63 E1 Terminal or ADM SDH Multiplexer
- Digital Cross Connect System
- Digital Loop Carrier Systems (NGDLC)
- Microwave Radio System

Product Features

- Maps and Demaps 21 E1 signals between PDH and SDH networks via VC-12 asynchronous mapping.
- Multiplexes the 21 VC-12 signals into seven interleaved TUG-2 structures for STM-0 or a TUG-3 structure for STM-1 applications.
- Configurable as a flexible Add/Drop Multiplexer for up to 21 E1 tributaries, with each E1 I/O port assignable to any TU time slot within an AU-3 or TUG-3.
- Performs VC-12 path overhead processing for all 21 VC-12s, including V5, J2 Path Trace, and K4 Enhanced RDI.
- Records TU pointer alarms (TU-AIS, TU-LOP), BIP-2 and REI error counts, TIM and PLM alarms, and all other V5 POH alarms for all 21 tributaries.
- NRZ Data and Clock interface for E1 tributary access.
- Microprocessor/SEMF interface to set Signal Label, J2 Path Trace, access alarms and counters
- Low power CMOS technology with 3.3V core and 5V I/O, available in PQFP-208 package.
- IEEE 1149.1 (JTAG) support.



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Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

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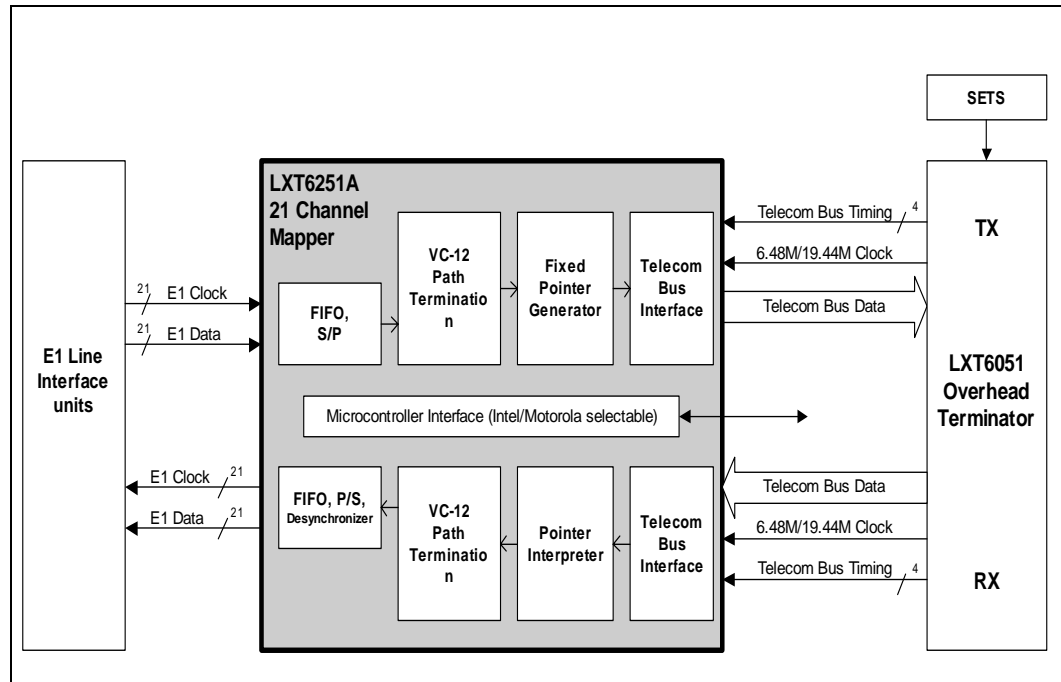
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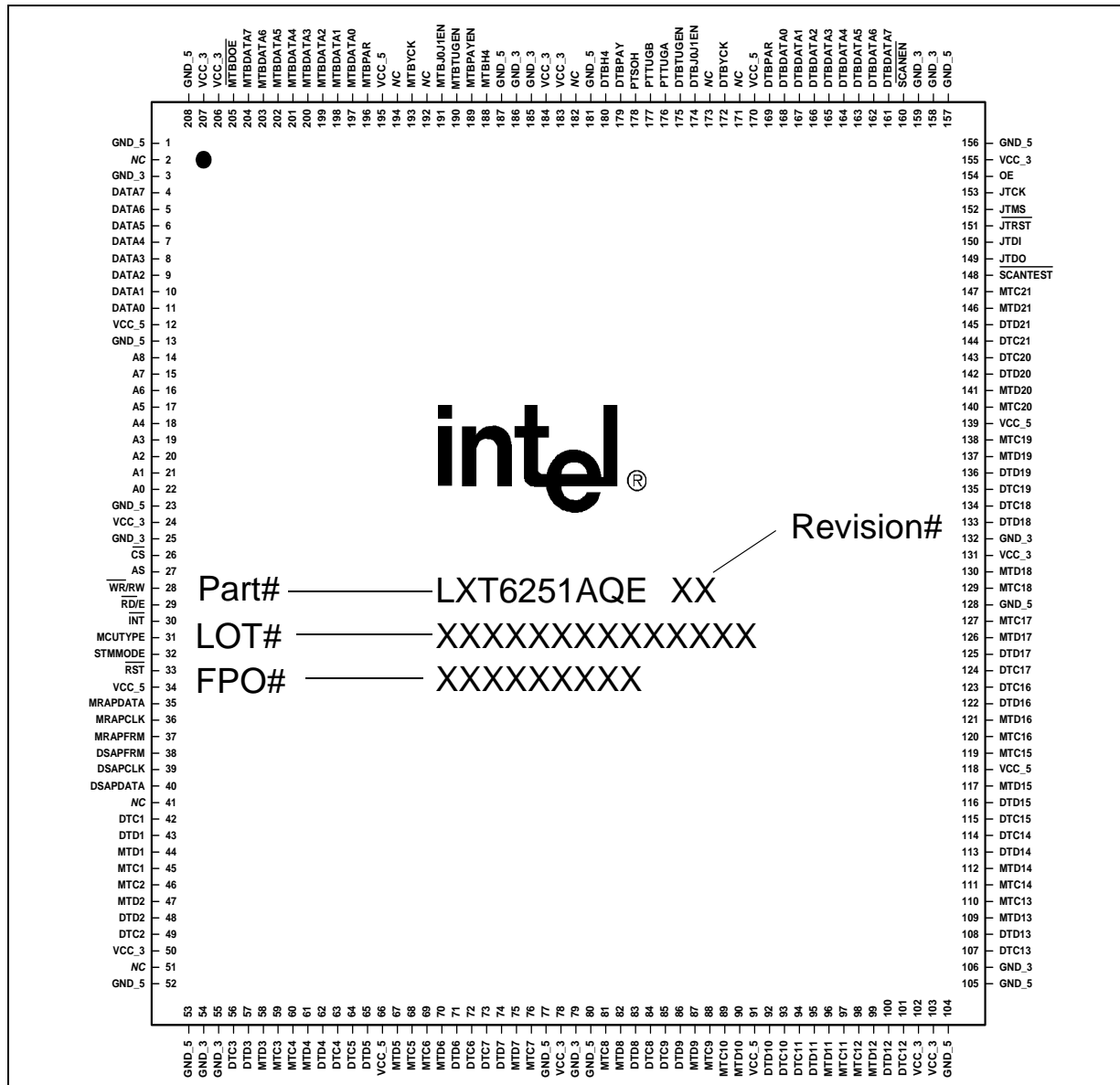
1.0 Block Diagram

Figure 1. LXT6251A Block Diagram



2.0 Pin Assignments and Signal Descriptions

Figure 2. LXT6251A Pin Assignments



Revision#

Part# ————— LXT6251AQE XX
 LOT# ————— XXXXXXXXXXXXXXXX
 FPO# ————— XXXXXXXXXX

Package Topside Markings

Marking	Definition
Part #	LXT6251A is the unique identifier for this product family. QE indicates the family member.
Rev #	Identifies the particular silicon "stepping" — refer to the specification update for additional stepping information.
Lot #	Identifies the batch.
FPO #	Identifies the Finish Process Order.

Table 1. Signal Description Nomenclature

Type	Description
I	Standard input signal
O	Standard output signal
I/O	Input and output signal
TTLin ¹	Supports TTL input levels
HiZ ¹	High Impedance
1. Some signals indicate buffer strength. For example, HiZ-4ma indicates a high-impedance buffer capable of sourcing 4 ma.	

Table 2. Pin Descriptions (Sheet 1 of 7)

Pin #	Name	Type	Function
E1 Transmit and Receive Ports			
44	MTD1	I TTL in	Transmit Tributary NRZ Data Port # 1. Input E1 NRZ data input at 2.048 Mbit/s
47	MTD2	I TTL in	Transmit Tributary NRZ Data Port # 2
58	MTD3	I TTL in	Transmit Tributary NRZ Data Port # 3
61	MTD4	I TTL in	Transmit Tributary NRZ Data Port # 4
67	MTD5	I TTL in	Transmit Tributary NRZ Data Port # 5
70	MTD6	I TTL in	Transmit Tributary NRZ Data Port # 6
75	MTD7	I TTL in	Transmit Tributary NRZ Data Port # 7
82	MTD8	I TTL in	Transmit Tributary NRZ Data Port # 8
87	MTD9	I TTL in	Transmit Tributary NRZ Data Port # 9
90	MTD10	I TTL in	Transmit Tributary NRZ Data Port # 10
96	MTD11	I TTL in	Transmit Tributary NRZ Data Port # 11
99	MTD12	I TTL in	Transmit Tributary NRZ Data Port # 12
109	MTD13	I TTL in	Transmit Tributary NRZ Data Port # 13
112	MTD14	I TTL in	Transmit Tributary NRZ Data Port # 14
117	MTD15	I TTL in	Transmit Tributary NRZ Data Port # 15
121	MTD16	I TTL in	Transmit Tributary NRZ Data Port # 16

Table 2. Pin Descriptions (Continued) (Sheet 2 of 7)

Pin #	Name	Type	Function
126	MTD17	I TTL in	Transmit Tributary NRZ Data Port # 17
130	MTD18	I TTL in	Transmit Tributary NRZ Data Port # 18
137	MTD19	I TTL in	Transmit Tributary NRZ Data Port # 19
141	MTD20	I TTL in	Transmit Tributary NRZ Data Port # 20
146	MTD21	I TTL in	Transmit Tributary NRZ Data Port # 21
45	MTC1	I TTL in	Transmit Tributary Clock Port # 1 Input E1 clock at 2.048 MHz
46	MTC2	I TTL in	Transmit Tributary Clock Port # 2
59	MTC3	I TTL in	Transmit Tributary Clock Port # 3
60	MTC4	I TTL in	Transmit Tributary Clock Port # 4
68	MTC5	I TTL in	Transmit Tributary Clock Port # 5
69	MTC6	I TTL in	Transmit Tributary Clock Port # 6
76	MTC7	I TTL in	Transmit Tributary Clock Port # 7
81	MTC8	I TTL in	Transmit Tributary Clock Port # 8
88	MTC9	I TTL in	Transmit Tributary Clock Port # 9
89	MTC10	I TTL in	Transmit Tributary Clock Port # 10
97	MTC11	I TTL in	Transmit Tributary Clock Port # 11
98	MTC12	I TTL in	Transmit Tributary Clock Port # 12
110	MTC13	I TTL in	Transmit Tributary Clock Port # 13
111	MTC14	I TTL in	Transmit Tributary Clock Port # 14
119	MTC15	I TTL in	Transmit Tributary Clock Port # 15
120	MTC16	I TTL in	Transmit Tributary Clock Port # 16
127	MTC17	I TTL in	Transmit Tributary Clock Port # 17
129	MTC18	I TTL in	Transmit Tributary Clock Port # 18

Table 2. Pin Descriptions (Continued) (Sheet 3 of 7)

Pin #	Name	Type	Function
138	MTC19	I TTL in	Transmit Tributary Clock Port # 19
140	MTC20	I TTL in	Transmit Tributary Clock Port # 20
147	MTC21	I TTL in	Transmit Tributary Clock Port # 21
43	DTD1	O HiZ - 2mA	Receive Tributary NRZ Data Port # 1 Received E1 NRZ data output from the demapped VC-12 at 2.048Mbit/s
48	DTD2	O HiZ - 2mA	Receive Tributary NRZ Data Port # 2
57	DTD3	O HiZ - 2mA	Receive Tributary NRZ Data Port # 3
62	DTD4	O HiZ - 2mA	Receive Tributary NRZ Data Port # 4
65	DTD5	O HiZ - 2mA	Receive Tributary NRZ Data Port # 5
71	DTD6	O HiZ - 2mA	Receive Tributary NRZ Data Port # 6
74	DTD7	O HiZ - 2mA	Receive Tributary NRZ Data Port # 7
83	DTD8	O HiZ - 2mA	Receive Tributary NRZ Data Port # 8
86	DTD9	O HiZ - 2mA	Receive Tributary NRZ Data Port # 9
92	DTD10	O HiZ - 2mA	Receive Tributary NRZ Data Port # 10
95	DTD11	O HiZ - 2mA	Receive Tributary NRZ Data Port # 11
100	DTD12	O HiZ - 2mA	Receive Tributary NRZ Data Port # 12
108	DTD13	O HiZ - 2mA	Receive Tributary NRZ Data Port # 13
113	DTD14	O HiZ - 2mA	Receive Tributary NRZ Data Port # 14
116	DTD15	O HiZ - 2mA	Receive Tributary NRZ Data Port # 15
122	DTD16	O HiZ - 2mA	Receive Tributary NRZ Data Port # 16
125	DTD17	O HiZ - 2mA	Receive Tributary NRZ Data Port # 17
133	DTD18	O HiZ - 2mA	Receive Tributary NRZ Data Port # 18
136	DTD19	O HiZ - 2mA	Receive Tributary NRZ Data Port # 19
142	DTD20	O HiZ - 2mA	Receive Tributary NRZ Data Port # 20

Table 2. Pin Descriptions (Continued) (Sheet 4 of 7)

Pin #	Name	Type	Function
145	DTD21	O HiZ - 2mA	Receive Tributary NRZ Data Port # 21
42	DTC1	O HiZ - 2mA	Receive Tributary Clock Port # 1. Received E1 clock at 2.048 MHz recovered from VC-12. This clock is gapped, data is valid on the falling edge.
49	DTC2	O HiZ - 2mA	Receive Tributary Clock Port # 2
56	DTC3	O HiZ - 2mA	Receive Tributary Clock Port # 3
63	DTC4	O HiZ - 2mA	Receive Tributary Clock Port # 4
64	DTC5	O HiZ - 2mA	Receive Tributary Clock Port # 5
72	DTC6	O HiZ - 2mA	Receive Tributary Clock Port # 6
73	DTC7	O HiZ - 2mA	Receive Tributary Clock Port # 7
84	DTC8	O HiZ - 2mA	Receive Tributary Clock Port # 8
85	DTC9	O HiZ - 2mA	Receive Tributary Clock Port # 9
93	DTC10	O HiZ - 2mA	Receive Tributary Clock Port # 10
94	DTC11	O HiZ - 2mA	Receive Tributary Clock Port # 11
101	DTC12	O HiZ - 2mA	Receive Tributary Clock Port # 12
107	DTC13	O HiZ - 2mA	Receive Tributary Clock Port # 13
114	DTC14	O HiZ - 2mA	Receive Tributary Clock Port # 14
115	DTC15	O HiZ - 2mA	Receive Tributary Clock Port # 15
123	DTC16	O HiZ - 2mA	Receive Tributary Clock Port # 16
124	DTC17	O HiZ - 2mA	Receive Tributary Clock Port # 17
134	DTC18	O HiZ - 2mA	Receive Tributary Clock Port # 18
135	DTC19	O HiZ - 2mA	Receive Tributary Clock Port # 19
143	DTC20	O HiZ - 2mA	Receive Tributary Clock Port # 20
144	DTC21	O HiZ - 2mA	Receive Tributary Clock Port # 21
Telecom Bus Interface			

Table 2. Pin Descriptions (Continued) (Sheet 5 of 7)

Pin #	Name	Type	Function
204-197	MTBDATA <7:0>	O HiZ - 4mA	Multiplex Telecom Bus Data 7 to 0. This is a byte wide data output at 19.44 Mbit/s for STM-1 or 6.48 Mbit/s for STM-0. The output in STM-1 may be tri-stated for certain bytes depending on the configuration of the device.
196	MTBPAR	O HiZ - 4mA	Multiplex Telecom Bus Parity. This is the parity check signal calculated on the MTBDATA byte only. It is an odd parity and is always a calculated value (i.e. the value is not passed through in ADM).
193	MTBYCK	I TTLin	Multiplexer Telecom Bus Clock. This clock drives the multiplexer section at 6.48 MHz for STM-0 or 19.44MHz for STM-1.
191	MTBJ0J1EN	I/O TTLin - 4mA	Multiplex Telecom Bus Frame indicator. This indicates the presence of the J0 and J1 bytes on the MTBDATA bus. Optionally configurable to also indicate H4 multiframe position, instead of using MTBH4EN.
188	MTBH4EN	I/O TTLin - 4mA	Multiplex Telecom Bus H4 multiframe Indicator. An output in ADM mode, this is a 2 KHz signal that indicates the location of the 00 value of H4. As input in terminal mode, the signal is sampled during the J1 byte position given by MTBJ0J1EN.
189	MTBPAYEN	I/O TTLin - 4mA	Multiplex Telecom Bus Payload Enable. Indicates the position of VC-4 in the STM-1 mode or VC-3 in the STM-0 mode. In an ADM configuration the pin is an output while in the terminal mode it is an input.
190	MTBTUGEN	I TTLin	Multiplexer Telecom Bus TUG Enable. This pin is used in STM-1 terminal applications and controls the TUG-3 in which the LXT6251A will generate data. This pin should be tied to Vcc for STM-0 terminal applications.
205	MTBDOE	O HiZ - 4mA	Multiplexer Telecom Bus Output Enable. Active Low output enable signal that mirrors the internal MTBDATA data bus control. Its function is to enable an <i>external</i> tri-state bus driver that should be used when the device is installed in a multi-card/backplane environment. Usually reserved for STM-1 use, the signal is always active in STM-0
161 - 168	DTBDATA <7:0>	I TTLin	Demultiplexer Telecom Bus Data 7. This is a byte wide data input at 19.44 Mbit/s for STM-1 or 6.48 Mbit/s for STM-0. In STM-1 mode, the data is ignored if DTBTUGEN is Low.
169	DTBPAR	I TTLin	Telecom Bus Parity. This is parity check calculated on the DTBDATA byte only. It is an odd parity.
172	DTBYCK	I TTLin	Demultiplexer Telecom Bus Clock. This clock drives the demultiplexer section at 6.48 MHz for STM-0 or 19.44MHz for STM-1
174	DTBJ0J1EN	I TTLin	Demultiplexer Telecom Bus Frame Indicator. This indicates the position of J0 and J1 bytes on the DTBDATA bus. Optionally configurable to also detect H4 multiframe position, instead of using DTBH4EN.
180	DTBH4EN	I TTLin	Demultiplexer Telecom Bus H4 multiframe Indicator. This is a 2 KHz signal that indicates the location of the 00 value of H4. This signal is sampled during the J1 pulse from DTBJ0J1EN.
179	DTBPAYEN	I TTL-in	Demultiplexer Telecom Bus Payload Enable. Indicates the position of VC-4 in the STM-1 mode or VC-3 in the STM-0 mode. This pin is always an input.
175	DTBTUGEN	I TTLin	Demultiplexer Telecom Bus TUG Enable. This pin is used in STM-1 applications and indicates the proper TUG-3 payload the demultiplexer section should process. This pin is tied to VCC for STM-0 applications.

Table 2. Pin Descriptions (Continued) (Sheet 6 of 7)

Pin #	Name	Type	Function
176	PTTUGA	I TTLin	Pass-Trough TUG Enable-A. A High on this pin indicates the TUG data received coincident with the pulse is to be passed through to the MTBDATA output. Refer to “Add/Drop Configuration” on page 30 for use of this pin. This pin should be tied Low in STM-0 configuration or if unused.
177	PTTUGB	I TTLin	Pass-Trough TUG Enable-B. A High on this pin indicates the TUG data received coincident with the pulse is to be passed through to the MTBDATA output. Refer to “Add/Drop Configuration” on page 30 for use of this pin. This pin should be tied Low in STM-0 configuration or if unused.
178	PTSOH	I TTLin	Pass-Trough SOH Enable. A High on this pin indicates the SOH data, HPOH data, and VC-4 fixed stuff (STM-1) received on the telecom bus is to be passed through to the MTBDATA output. Refer to “Add/Drop Configuration” on page 30 for use of this pin. This pin should be tied to ground in STM-0 or STM-1 terminal configurations or if unused.
Serial Alarm Indication Ports			
40	DSAPDATA	O HiZ - 2mA	Serial Alarm Data. Output which provides a rapid indication of the V5 byte parity error, TU-AIS, TU-Loss of pointer, Unequipped detect, Trace ID mismatch, Signal Label mismatch and VC-AIS alarm status for all 21 VC-12 channels. Refer to “Serial/Remote Alarm Processing Port” on page 40 for details.
39	DSAPCLK	O HiZ - 2mA	Serial Alarm Clock. Clock frequency is nominally 1.62MHz.
38	DSAPFRM	O HiZ - 2mA	Serial Alarm Frame. Frame indicator active during the first bit of the DSAPDATA data frame.
35	MRAPDATA	I TTLin	Serial Alarm Data. Input that contains indication of alarm status resulting from the V5 byte parity error, TU-AIS, TU-Loss of pointer, Unequipped detect, Trace ID mismatch, and Signal Label mismatch, and VC-AIS for all 21 VC-12 channels. Refer to “Serial/Remote Alarm Processing Port” on page 40 for details.
36	MRAPCLK	I TTLin	Serial Alarm Clock input. The clock frequency is nominally 1.62MHz
37	MRAPFRM	I TTLin	Serial Alarm Frame. Frame indicator that must be active during the first bit of the data frame on MRAPDATA.
Microprocessor Bus			
14-22	A<8:0>	I TTLin	Address Bus. A nine bit address port for microprocessor access.
4-11	DATA<7:0>	I/O TTLin-6mA	Data Bus. Eight bit I/O data port for the microprocessor to read and write data, commands, and status information to and from the device.
28	$\overline{WR}/\overline{RW}$	I TTLin	Write signal (Intel); Read/Write signal (Motorola)
29	\overline{RD}/E	TTLin	Read signal (Intel); Enable signal (Motorola)
26	CS	I	Chip Select. Active Low signal to enable microprocessor RD or WR action.
31	MCUTYPE	I TTLin	Motorola/Intel Interface Mode Select. Low = Intel, High = Motorola
30	INT	O HiZ - 4mA	Interrupt. Active Low interrupt indication.

Table 2. Pin Descriptions (Continued) (Sheet 7 of 7)

Pin #	Name	Type	Function
27	AS	TTLin	Address Latch Enable. Used by chip for systems where address and data busses are multiplexed. Latches A<8:0> on the falling edge. If address and data are not multiplexed, this pin should be tied High.
JTAG Boundary Scan Test Functions			
148	SCANTEST	TTLin-48PU	Active Low Scan Test mode select with ~48 KOhm Pull-up resistor. Should be left unconnected for normal operation.
160	SCANEN	ITTLin-48PU	Active Low Scan Enable with ~48 KOhm Pull-up resistor. Controls all Scan FF muxes. Should be left unconnected for normal operation.
153	JTCK	I TTLin-48PU	JTAG Clock. This signal has a ~48 KΩ Pull-up resistor. Clock for the boundary scan circuitry. See “IEEE 1149.1 Boundary Scan Description” on page 66 for details.
152	JTMS	I TTLin-48PU	Test Mode Select. This signal has a ~48KΩ Pull-up resistor. This pin determine state of TAP controller.
151	JTRS	I TTLin-35PD	Active low Reset. This signal has a ~35KΩ Pull-down resistor. Should be left unconnected for normal device usage.
150	JTDI	ITTLin-48PU	Data Input. This signal has a ~48KΩ Pull-up resistor. Input signal used to shift in instructions and data. Should be left unconnected for normal device usage.
149	JTDO	O HiZ-2mA	Data Output. Output signal used to shift out instruction and data.
Control Functions			
154	OEN	I TTLin-48PU	Output Enable. This signal has a ~48KOhm Pull-up resistor. Used to disable all output pins for bed of nails type testing or other applications. When Low, all outputs are in high impedance and all bi-directional pins are inputs. Should be left unconnected for normal operation.
33	RST	I TTLin-108PUS	Chip Master Reset. This signal has a ~108KOhm Pull-up resistor. A low will reset all registers to default conditions. Input logic is a schmidt trigger type.
32	STMMODE	I TTLin	STM Mode Select. Low = STM-0, High = STM-1

Table 3. Power, Ground, and No Connects

Pin #	Name	Type	Power Supply
12, 34, 66, 91, 118, 139, 170, 195	VCC_5		5V Supply for I/O ring
1, 13, 23, 52, 53, 77, 80, 104, 105, 128, 156, 157, 181, 187, 208	GND_5		GND 5 Volts. Ground pins for 5 Volt supply.
24, 50, 78, 102, 103, 131, 155, 183, 184, 206, 207	VCC_3		3 V supply for core
3, 25, 54, 55, 79, 106, 132, 158, 159, 185, 186	GND_3		GND 3 Volts. Ground pins for 3 Volt supply.
2, 41, 51, 171, 173, 182, 192, 194	NC		Not Connected. Unused

3.0 Functional Description

3.1 Introduction

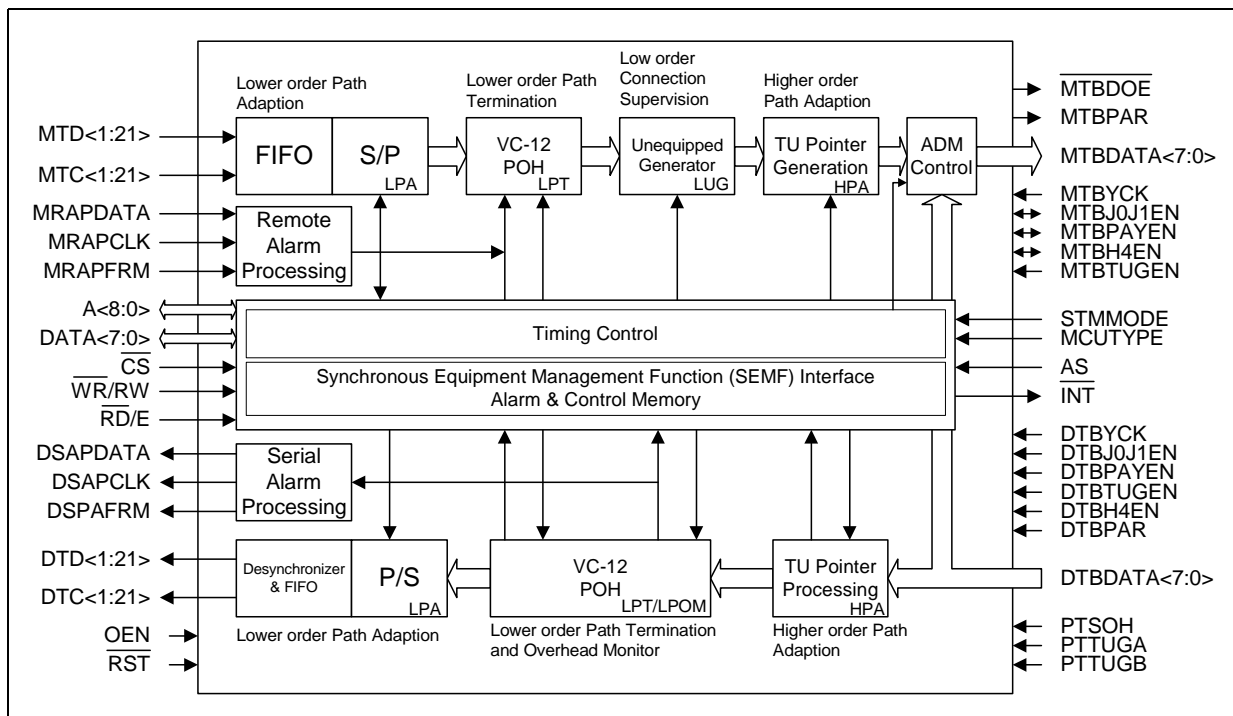
The LXT6251A performs mapping and demapping of 21 channels of E1 PDH tributaries into and out of the SDH hierarchy. It supports two system configurations, terminal or Add/Drop multiplexing, and two operating frequencies, STM-0 or STM-1. In the terminal configuration, the transmit section maps 21 tributaries of E1 data into 21 VC-12 virtual containers, formatted as a C-3 in STM-0 or as a TUG-3 in STM-1. The terminal receiver processes either a C3 or a TUG-3 payload and outputs 21 E1 tributaries after processing the VC-12 path overhead. In the Add/Drop configuration, the receiver processes any number of TU-12 containers up to its capacity of 21, and passes the non-dropped portion of the payload to the transmitter where the added E1/TU-12 tributaries are multiplexed and output.

The discussion will focus first on the terminal functions, which describe the E1 to SDH process used in the terminal mode as well as those E1 channels in the add/drop mode. Following the terminal functions, the configuration details of the add/drop mode are presented. Further details about the configuration of the LXT6251A with the LXT6051 in different system configurations can be found in a companion document, Application Note LXT6051/LXT6251A SDH Chipset.”

3.2 Receive Section, Terminal Mode

At the Telecom Bus input point (DTBDATA), the Mapper expects to receive byte wide data that has been processed by the LXT6051 OHT or an other overhead terminator up to the higher order path terminator (HPT) point. The Mapper thus receives data that minimally contains C-3 or C-4 payload data along with the Telecom Bus timing signals DTBJ0J1EN, DTBPAYEN, DTBH4EN, and DTBTUGEN (STM-1 only) which synchronize the internal timing generator to the data. The timing generator in turn drives 21 identical demapper blocks to process the appropriate TU-12 signals.

Refer to “[Telecom Bus Interface](#)” on page 35 for a detailed discussion of the Telecom bus signals. Refer to the block diagram below for the following discussion of a single TU-12 demultiplexer block. The remaining 20 blocks operate in an identical manner but with different timing signals.

Figure 3. LXT6251A Block Diagram


3.2.1 Receive Alarms

There are two alarms associated with the Telecom bus interface.

3.2.1.1 Parity Alarm

The receive telecom bus data integrity is monitored with a single odd parity bit. The parity is calculated over the DTBDATA bus only. The mapper checks the parity for errors every 500mS multiframe and indicates an alarm in “[GLOB_INTS—Global Interrupt Source \(00CH\)](#)” on page 60 if there are more than 16 errors within the 500mS time window. The interrupt is maskable in “[INT_CONF—Interrupt Configuration Register \(00BH\)](#)” on page 59.

3.2.1.2 Loss of Multiframe

A loss of multiframe alarm is detected if the DTBH4EN signal is always low. The alarm status and interrupt is indicated in “[GLOB_INTS—Global Interrupt Source \(00CH\)](#)” on page 60.

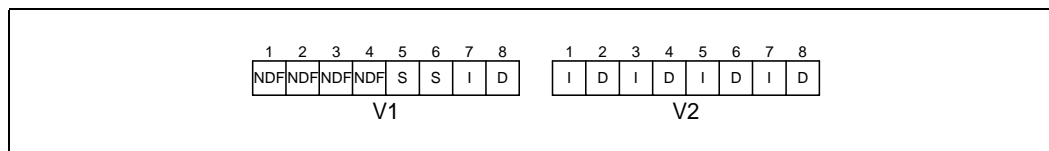
Consequent Actions:

- An LOM alarm will cause the SF alarm bit on the SAP bus to be high for all 21 tributaries. The SF alarm is used to indicate errors that should cause a VC path protection event. The SAP bus is described in detail in “[Serial/Remote Alarm Processing Port](#)” on page 40.

3.3 High Order Path Adaptation

Within each of the 21 TU-12 demapper blocks, the telecom bus data bytes first enter the higher order path adaptation (HPA) block for TU-12 pointer interpretation. The TU-12 pointer is contained in the V1 and V2 bytes shown below. The 8 bits of V2 and the 2 LSB bits of V1, shown as I and D bits, represent a binary number that represents the number of TU-12 bytes between the V5 POH byte and V2. The SS bits identify Tributary type, and the remaining 4 bits represent a New Data Flag (NDF). Based on the incoming J0J1, Payload, and H4 timing signals, the V1 and V2 bytes are located and interpreted. The pointer interpreter state machine follows the state diagram provided in the Appendix of ITU-T G.783. The variable N in that specification, which specifies the number of invalid pointers required to enter the Loss of Pointer state, is set to eight (8) in the LXT6251A. When a valid pointer is found (a valid pointer defined as being between the values 0 and 139), the pointer processing block will synchronize the TU timing block and remove the Loss of Pointer (LOP) alarm.

Figure 4. V1/V2 Pointer Diagram



After achieving a normal pointer state, the processor will continually monitor V1 and V2 for the following events:

- Positive Justification from the inversion of the I bits (3 of 5 majority decision)
- Negative Justification from the inversion of the D bits (3 of 5 majority decision)
- New pointer value from 3 new valid values in a row
- New pointer value from single NDF indication (if in Normal or AIS state only)
- All 1's condition on the V1/V2 bytes
- Invalid pointer values occurring 8 times in a row to trigger a LOP alarm
- Reception of NDF indication 8 times in a row to trigger a LOP alarm

3.3.1 Alarms and Status

3.3.1.1 TU-AIS

If 3 consecutive TU pointers in the all 1's (AIS) state are detected, the TU-AIS status bit in “TRIB_STA—Tributary Status (x3-x2H)” on page 63 is set. It is cleared when either the LOP or Normal states are entered. Whenever the TU-AIS status changes the TU-AIS interrupt bit in “TRIB_INT—Tributary Interrupt (x1-x0H)” on page 61 is set.

Consequent Actions:

- An RDI Indication will be sent to the transmitter via the SAP interface. The RDI indication will be set on the transmitted V5 byte unless the XmtLptRdiEn bit in “ERRI_CONF—Error Insert Configuration (xDH)” on page 58 is set to 0
- Outgoing E1 data on DTDx will be forced to AIS with derived 2.048MHz clock on DTCx

3.3.1.2 TU Loss of Pointer (LOP)

If an invalid pointer state is detected in the TU pointer, the TU-LOP status bit in “TRIB_STA—Tributary Status (x3-x2H)” on page 63 is set. An invalid pointer state is entered from either the normal or AIS pointer state after 8 consecutive invalid pointer values or 8 consecutive NDF pointers are detected. It is exited when either the LOP or Normal states are entered at which time the TU-LOP status bit in “TRIB_STA—Tributary Status (x3-x2H)” on page 63 is cleared. Whenever the TU-LOP status changes the TU-LOP interrupt bit in “TRIB_INT—Tributary Interrupt (x1-x0H)” on page 61 is set.

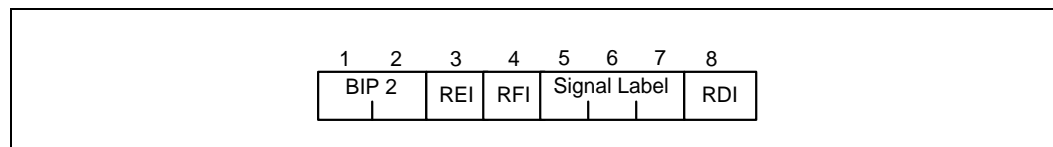
Consequent Actions:

- An RDI alarm will be sent to the transmitter via the SAP interface. The RDI alarm will be set in the transmitted V5 byte unless the XmtLptRdiEn bit in “ERRI_CONF—Error Insert Configuration (xDH)” on page 58 is set to 0
- Outgoing E1 data on DTDx will be forced to AIS with derived 2.048 MHz clock on DTCx.

3.4 Low Order Path Termination

After the TU Timing control has been updated by the pointer interpreter, the received data is processed by the lower order path termination (LPT) block which terminates the POH bytes of each VC-12, and records all information extractable from the POH for processing by the microprocessor. For the V5 byte this includes counting BIP-2 and REI errors and monitoring the RDI, RFI and signal label bits. For the J2 Path Trace byte this includes monitoring the Path trace identification and CRC-7 alarms, and for the K4 byte this includes monitoring enhanced RDI information. All alarm indications and counts are available via the microprocessor interface, with the RDI, REI, VC-AIS, and BIP errors additionally fed to the Serial alarm port (SAP) for real-time tributary alarm indication and remote alarm processing.

Figure 5. V5 Byte



3.4.1 V5 Processing

3.4.1.1 BIP-2 Errors (V5, bits 1,2)

The LPT block continually calculates the BIP-2 value by generating a two-bit parity, starting with V5. After receiving the 140 bytes in a multiframe, the calculated value is compared with the first two bits of the next V5 and if a mismatch between the calculated and received BIP-2 is detected a BIP-2 error interrupt is generated in “TRIB_INT—Tributary Interrupt (x1-x0H)” on page 61. BIP-2 mismatches are also counted with results available in “BIP2_ERRCNT—BIP2 Error Counter (x7-x6H)” on page 63. The BIP2 counters can be configured from “GLOB_CONF—Global Configuration (000H)” on page 55 to count either two possible counts per multiframe (bit count) or one possible count per multiframe (block count). The counter will count to a maximum of 4095, which exceeds the maximum number of bit alarms in one second and the maximum number of block errors in two seconds. If the counter overflows, an Overflow interrupt is generated in “TRIB_INT—Tributary Interrupt (x1-x0H)” on page 61 and the count recycles to zero.

To read the BIP counter registers, the microprocessor must first perform a write (any value) to either (x6H,x7H), then wait at least three cycles of DTBYCK (0.5uS in STM-0) before reading the two registers. The write action latches the counter value into the two registers, and clears the counter to zero.

Consequent Actions:

- REI indication will be sent to the transmitter via the SAP interface. The REI indication will be set on the transmitted V5 byte unless the XmtLptReiEn bit in “ERRI_CONF—Error Insert Configuration (xDH)” on page 58 is set to 0.

3.4.1.2 REI Detection (V5, bit 3)

The LPT block continually monitors the value of the REI bit and sets the REI interrupt bit in “TRIB_INT—Tributary Interrupt (x1-x0H)” on page 61 whenever it is found to be ‘1’ (an event).

These events are also counted with results available in “REI_CNT—Remote Error Indication (REI) Counter (x9-x8H)” on page 64. The counter will count to a maximum of 2047, which is more than the maximum number of REI alarms within one second. If the counter overflows, an Overflow interrupt is generated in “TRIB_INT—Tributary Interrupt (x1-x0H)” on page 61 and the count recycles to zero.

To read the REI counter registers, the microprocessor must first perform a write (any value) to either register (x8H, x9H), then wait at least three cycles of DTBYCK (0.5uS in STM-0) before reading the two registers. The write action latches the counter values into the two registers, and clears the counter to zero.

Consequent Actions: none

3.4.1.3 RFI Detection (V5, bit 4)

The LPT block continually monitors the value of the RFI bit and updates the RFI status bit in “TRIB_STA—Tributary Status (x3-x2H)” on page 63 with its detected value (there is no filtering or hysteresis on this bit). Whenever the RFI status bit changes the RFI interrupt bit in “TRIB_INT—Tributary Interrupt (x1-x0H)” on page 61 is set.

Consequent Actions: none

3.4.1.4 Signal Label Mismatch (V5, bits 5-7)

A signal label mismatch (SLM) status bit will be set in “TRIB_STA—Tributary Status (x3-x2H)” on page 63 if the signal label does not match a valid pattern that can be processed by this chip for five multiframes. Valid label values are 000 (Unequipped), 001 (Equipped, non-specific), and 010 (Equipped, asynchronous). It is cleared when the signal label equals a valid pattern for five multiframes.

Whenever the SLM status bit changes the SLM interrupt bit in “TRIB_INT—Tributary Interrupt (x1-x0H)” on page 61 is set.

Consequent Actions:

- Outgoing E1 data on DTDx will be forced to AIS with derived 2.048MHz clock on DTCx

3.4.1.5 Unequipped Detection (V5, bits 5-7)

The Unequipped (UNEQP) status bit will be set in “TRIB_STA—Tributary Status (x3–x2H)” on page 63 if a ‘000’ is detected in the signal label for five consecutive multiframes. It is cleared when the signal label equals a pattern other than ‘000’ for five consecutive multiframes.

Whenever the UNEQP status bit changes the UNEQP interrupt bit in “TRIB_INT—Tributary Interrupt (x1–x0H)” on page 61 is set.

Consequent Actions:

- If the global Unequipped configuration is not set to Supervisory, an RDI Indication will be sent to the transmitter via the SAP interface. The RDI indication will be set on the transmitted V5 byte unless the XmtLptRdiEn bit in “ERRI_CONF—Error Insert Configuration (xDH)” on page 58 is set to 0. No indication is sent in Supervisory mode.
- Outgoing E1 data on DTDx will be forced to AIS with derived 2.048MHz clock on DTCx

3.4.1.6 VC-AIS Detection (V5, bits 5-7)

If the signal label is detected as ‘111’ in any one multiframe, a VC-AIS alarm will be indicated on the SAP bus. There is no internal alarm or interrupt associated with this alarm, and no hysteresis filtering. If the SAP bus is used to control protection switching at the TU-12 level, it is recommended that hysteresis filtering be added to this alarm in the external circuit.

VC-AIS is treated like a signal label mismatch. Thus, consequent actions follow SLM actions.

Consequent Actions:

- A VC-AIS/SF Indication will be output on the SAP interface.

3.4.1.7 RDI Detection (V5, bit 8)

The LPT block continually monitors the value of the RDI bit and updates the RDI status bit in “TRIB_STA—Tributary Status (x3–x2H)” on page 63 with its detected value (after five consecutive frames). Whenever the RDI status bit changes the RDI interrupt bit in “TRIB_INT—Tributary Interrupt (x1–x0H)” on page 61 is set.

Consequent Actions: none

3.4.2 J2 Processing

J2 Trace Identifier processing is supported on a per tributary basis for both transmit and receive paths. Within the receive section of each tributary, the RxJ2Access bit in “TRIB_INTE—Tributary Interrupt Enable (x5–x4H)” on page 62 controls the support for J2 processing. When RxJ2Access is a ‘1’, both the J2 Path Label Mismatch and the CRC-7 error detection alarms are completely masked. In this state the microprocessor is also able to access the J2 RAM cell of the tributary. This is the default state after a power-up condition. When RxJ2Access is ‘0’, the two alarms are enabled, and the microprocessor cannot access the J2 RAM.

3.4.2.1 J2 Memory Access

The J2 RAM for each tributary is indirectly accessible by the microprocessor. That is, there is a single data port to access the data, while the address is internally generated and automatically incremented as the J2 RAM byte is read or written. The following procedure should be followed to correctly program the J2 RAM.

- Ensure that RxJ2Access is set to '1' in [“TRIB_INTE—Tributary Interrupt Enable \(x5–x4H\)” on page 62](#).
- Write (any value) to J2_MRST-- J2 Memory reset_(008H) page 50. This resets the global counter used to generate the RAM address. This step is only required once if multiple tributaries are being programmed.
- Write the 16 bytes of the J2 word consecutively to [“J2_ESDATA—J2 Expected String Data \(xCH\)” on page 58](#). Each toggle of the write (or read) will increment the internal counter in DMA fashion.

If write verification is desired, the microprocessor can now read 16 bytes in DMA fashion. The internal address counter resets to 0 after the 16 writes.

Once the RAM is filled and verified, the RxJ2Access bit can be set to '0' to enable the alarms.

Note that all 16 bytes should be written to the RAM by the microprocessor. The CRC-7 byte is not needed in the receiver RAM (the received CRC-7 byte is compared with a calculated value only), however the microprocessor must write some value on the first write to align the remaining 15 words in the RAM.

During normal operation with J2 support, the RxJ2Access bit should be set to '0', allowing the alarms associated with J2 to be generated. As data is received, each J2 byte is analyzed until the CRC-7 byte is found, which is distinguished from the other 15 bytes by having a 1 in the most significant bit. The CRC-7 byte is stored, then the following 15 bytes are used to calculate a CRC-7 value and compared with successive locations in the RAM. The CRC-7 byte is never compared with the contents of the J2 RAM.

Two alarms can be generated: the Trace Identifier Mismatch (TIM) and the CRC-7 mismatch (CRC7).

3.4.2.2 CRC-7 Error

The chip calculates the CRC-7 value over the 15 bytes of the received J2 string. This value will be compared with the received CRC-7 byte. If the calculated and received CRC-7 bytes do not match, the J2 CRC-7 error (CRC7Err) status bit is set in [“TRIB_STA—Tributary Status \(x3–x2H\)” on page 63](#). If the calculated and received CRC-7 bytes do match, the CRC7Err status bit is cleared.

Whenever the CRC7Err status bit changes the CRC7Err interrupt bit in [“TRIB_INT—Tributary Interrupt \(x1–x0H\)” on page 61](#) is set.

Consequent Actions: none

3.4.2.3 Trace Identifier Mismatch

The chip compares the received J2 string with the one stored in memory. If the calculated CRC-7 matches that of the received value, but there are errors in the comparison of the remaining 15 bytes, the TIM status bit is set in “TRIB_STA—Tributary Status (x3-x2H)” on page 63. There is no filtering of this alarm, since the CRC-7 match will indicate the J2 word has been received without error. The TIM status bit is cleared when the J2 string is received without errors.

Whenever the TIM status bit changes the TIM interrupt bit in “TRIB_INT—Tributary Interrupt (x1-x0H)” on page 61 is set.

Consequent Actions:

- An RDI Indication will be sent to the transmitter via the SAP interface
- Outgoing E1 data toward the PDH network will be forced to AIS with derived 2.048MHz clock

3.4.3 N2 Processing

N2 processing is not implemented at this time.

3.4.4 K4 Processing

The K4 byte contains a protection function and an Enhanced RDI (ERDI) function. The LXT6251A supports the ERDI function. No alarms or interrupts will be generated based only on the K4 ERDI information. The V5 RDI bit generates the alarms.

3.4.4.1 Enhanced RDI

Upon detection of a V5 RDI alarm, “K4_STA—K4 Status (xAH)” on page 64 can be accessed to determine the nature of the RDI alarm, assuming the trail termination source supports the K4 ERDI processing. The following defects are supported in the ERDI

Table 4. Enhanced RDI Interpretation

K4, bit 5	K4, bit 6	K4, bit 7	Alarm
0	X	X	No Alarm
1	0	0	Non-specific RDI alarm
1	1	1	Non-specific RDI alarm
1	0	1	TU-AIS, TU-LOP
1	1	0	TIM, UNEQ
NOTE: The bit numbers above reference a byte whose least significant bit is bit 8.			

3.4.5 Summary of Alarms causing E1 AIS

A number of alarms cause the LXT6251A to generate an all 1’s AIS signal at the E1 output port. The following list summarizes those alarm and the conditions.

3.4.5.1 TU-AIS Alarm

V1/V2 = FFh for 8 consecutive multiframes

3.4.5.2 TU-LOP Alarm

V1/V2 invalid for 8 consecutive multiframes

3.4.5.3 Signal Label Mismatch

Signal Label invalid for 5 consecutive multiframes. A VC-AIS is also considered as an SLM.

3.4.5.4 Unequipped Alarm

Signal Label set to '000' for 5 consecutive multiframes (either supervisory or non-supervisory mode)

3.4.5.5 J2 Path Label Mismatch

16 byte J2 string has correct CRC-7 but does not match expected value.

The AIS consequent action from these alarms cannot be disabled with the exception of the J2 mismatch, which can be disabled via the use of the RxJ2Access bit. A Loss of multiframe should also cause an E1 AIS condition, however there is no direct action taken by the device to generate the AIS, the incoming Telecom bus data should already be in AIS.

3.5 Low Order Path Adaptation

After processing by the Path Overhead Terminator, the data is passed to the lower order path adaptation (LPA) block. First, the three C1C2 bits are processed and a majority decision made as to the value of the two stuffing indicator bits. A majority of 1's for Cx indicates the associated Sx bit is data, while majority 0's indicates the Sx bit is stuff and should be ignored. This is then used along with other timing inputs to extract the E1 payload data.

The data at this point is still parallel and therefore needs to be converted to serial and a relatively smooth 2.048MHz clock generated. The degapper circuit performs these functions.

3.5.1 Desynchronizer

The LXT6251A implements a bit leaking function to reduce the multiplexing jitter that is created during both the E1 to VC-12 stuffing process and SDH pointer movements at both the AU and TU level. The input to the degapper is the byte parallel clock, byte data, TU timing information, and indications of pointer movement from the TU level. The degapper block first interprets the stuffing indicators and extracts the proper data, then attempts to smooth the clock, anticipating gaps created by the frame, TU pointer movements, and stuffing. The output of the degapper directly feeds to output pins (DTCx/DTDX) and consists of a relatively smooth E1 clock (and NRZ data) in which the large gaps from pointer movements have been distributed over a period of time. In order for the E1 output to conform to G.783 residual jitter requirements, an external jitter attenuation circuit is required, such as that available in Intel's octal digital interface, the LXT6282 or Intel's LXT318 Line Interface with Jitter Attenuator.

The external jitter attenuator must meet the following specifications or the final output jitter cannot be guaranteed to meet ITU G.783:

- Loop Bandwidth of 3 Hz or lower
- An elastic buffer of at least 32 bits
- First or second order loop. Second order is recommended for best performance

4.0 Transmit Section, Terminal Mode

At the MTDx/MTCx input pins, the Mapper expects to receive asynchronous E1 signals in the form of NRZ data and clock. The mapper also requires the Telecom Bus timing signals MTBJ0J1EN, MTBPAYEN, MTBH4EN, and MTBTUGEN (STM-1 only) to drive the internal timing machine. Refer to [“Telecom Bus Interface” on page 35](#) for details on these timing signals.

The E1 signal must be valid and within frequency tolerance. Should there be a Loss of Signal alarm on an E1 input to the line interface circuits prior to the LXT6251A, it is the responsibility of the LIU or other external element to generate a valid E1 clock and AIS signal. The LXT6251A does not support a method to generate a mapped E1 AIS signal.

4.1 Low Order Path Adaptation

The E1 data and clock pairs immediately enter the first-in first-out memory within the lower order path adaptation (LPA) block. The LPA block receives timing information from the master timing control block to identify the frame positions of the Information (I) bytes, the stuffing indicators C1C2, and the stuffing bits S1 and S2. This timing, along with the depth of the FIFO is used to determine the stuffing decisions for each multiframe. The data out of the FIFO is converted to parallel bytes at each I byte position, and the appropriate stuffing indicators and stuffing bits added during the appropriate time slots. The output of the LPA block thus consists of a C12 container, which includes I bytes, R bytes, and stuffing indicator bytes also containing four O bits. The LXT6251A sets both the R bytes and the O bits to ‘0’.

4.2 Low Order Path Termination

Next the LPT function adds the path overhead bytes V5, J2, N2, and K4. The following descriptions detail the POH bytes and the supported bits within each byte.

4.2.1 V5 Processing

4.2.1.1 BIP-2

As the LPT block is generating the VC-12, a 2 bit Bit Interleave Parity (BIP-2) value is being calculated on all the bytes. At the end of the multiframe, the BIP-2 value is inserted into the following V5 byte (see Figure 4).

To aid the system designer in the testing phase, the LXT6251A includes a BIP error generator that is enabled by setting the BipInv bit in [“ERRI_CONF—Error Insert Configuration \(xDH\)” on page 58](#). The default value is ‘0’, and the BIP value is not affected. When set to ‘1’, the calculated BIP value will be inverted on every V5 byte, simulating a degraded VC-12 for a receiver.

4.2.1.2 REI Bit

The Remote Error Indication bit is updated every multiframe by monitoring the receive side status data on the Remote Alarm Port (RAP). The RAP port is further described in [“Serial/Remote Alarm Processing Port” on page 40](#). If the corresponding receive side TU-12 tributary detects BIP-2 errors, the RAP port will indicate to the transmit LPT block that the REI bit should be set to ‘1’.

Two bits in “ERRI_CONF—Error Insert Configuration (xDH)” on page 58 can modify the setting of the REI bit. First, the XmtLptReiEn bit can be set to ‘0’ to disable the automatic response to the RAP data. By default this bit is set to ‘1’. Second, the XmtLptRdiFrc can be set to ‘1’ to force the REI bit to be set to ‘1’ as long as this register bit is set. By default this bit is set to ‘0’.

4.2.1.3 RFI Bit

The Remote Failure Indication bit as of yet has no standard definition that would allow automatic generation with the LXT6251A. Therefore, the RFI bit can only be set by the microprocessor via the RFISet bit in “SIGLA_SET—Signal Label Setting (xEH)” on page 57.

4.2.1.4 Signal Label

The transmitted signal label is set to the value contained in the three SigLabelSet bits in “SIGLA_SET—Signal Label Setting (xEH)” on page 57. By default, the value is set to ‘010’ which indicates the VC-12 is mapped asynchronously. This value can be set to ‘001’ for equipped non-specific, or to ‘000’ to indicate the channel is unequipped.

Setting the SigLabelSet bits to ‘000’ indicates that a TU tributary is unused. By doing so, the chip will generate an unequipped VC-12 signal. If the UNEQMode bit in “GLOB_CONF—Global Configuration (000H)” on page 55 is set to ‘0’, the result will be a VC-12 with all bytes set to ‘0’ except the V5 BIP-2. If UNEQMode is set to ‘1’, indicating Supervisory Unequipped mode, the resulting unequipped signal will additionally contain a valid J2, valid REI and RDI bits within the V5 byte, and N2 set to 00h.

It is important to set the Signal Label to a valid value. An invalid value will be detected in a receiver as a Signal Label mismatch alarm with a consequent action of generating an AIS signal at the output E1 port.

4.2.1.5 RDI Bit

The RDI bit is updated every multiframe by monitoring the receive side status data on the Remote Alarm Port (RAP). The RAP port is further described in “Serial/Remote Alarm Processing Port” on page 40. If the corresponding receive side TU-12 tributary detects defects consisting of TU-AIS, TU-LOP, J2 TIM, or UNEQ, the RAP port will indicate to the transmit LPT block that the RDI bit should be set to ‘1’. There are two bits in “ERRI_CONF—Error Insert Configuration (xDH)” on page 58 that can modify the setting of the RDI bit. First, the XmtLptRdiEn bit can be set to ‘0’ to disable the automatic response to the RAP data. By default this bit is set to ‘1’. Second, the XmtLptRdiFrc can be set to ‘1’ to force the RDI bit to be set to ‘1’ as long as this register bit is set. By default this bit is set to ‘0’.

4.2.2 J2 Processing

J2 Trace Identifier processing support can be enabled on a tributary per tributary basis for the transmit path. Within the transmit section of each tributary, the XmtJ2Access bit in “ERRI_CONF—Error Insert Configuration (xDH)” on page 58 controls the support for J2 processing. When XmtJ2Access is a ‘1’, the power up default state, J2 transmission is disabled, and the value ‘00h’ (Unequipped mode) or ‘01’h (Supervisory Unequipped mode) is sent on every J2 byte. Additionally, in this state the microprocessor is able to read and write to the J2 RAM cell of the tributary. When XmtJ2Access is ‘0’, the value contained in the J2 RAM is transmitted, and the microprocessor is not able to access the J2 RAM.

4.2.2.1 J2 Memory Access

The J2 RAM for each tributary is indirectly accessible by the microprocessor. That is, there is a single data port to access the data, while the address is internally generated and automatically incremented as the J2 RAM byte is read or written. The following procedure should be followed to correctly program the J2 RAM.

- Ensure that XmtJ2Access is set to '1' in “ERRI_CONF—Error Insert Configuration (xDH)” on page 58.
- Write (any value) to J2_MRST-- J2 Memory reset_(008H) page 50. This resets the global counter used to generate the RAM address. This step is only required once if multiple tributaries are being programmed.
- Write the 16 bytes of the J2 word consecutively to “J2_TSDATA—J2 Transmit String Data (xFH)” on page 58. Each toggle of the write (or read) will increment the internal counter in DMA fashion
- If write verification is desired, the microprocessor can now read 16 bytes in DMA fashion. The internal address counter resets to 0 after the 16 writes.
- Once the RAM is filled and verified, the XmtJ2Access bit can be set to '0' to enable the transmit J2 word.

All 16 bytes are written to the RAM by the microprocessor. This places a requirement on the microprocessor that it must calculate the CRC-7 byte on the 15 byte Path Trace ID and write the calculated CRC-7 byte in the first position of the J2 RAM.

4.2.3 K4 Processing

The chip supports generation of the enhanced RDI function if the TxK4En configuration bit is set in “GLOB_CONF—Global Configuration (000H)” on page 55. All other bits in the K4 byte will be set to '0'. The alarm status received on the RAP port will drive the K4 byte as follows:

Table 5. Enhanced RDI Generation

K4, bit 5	K4, bit 6	K4, bit 7	Alarm
0	0	0	No Alarm or TxK4En not set
1	0	1	TU-AIS, TU-LOP
1	1	0	TIM, UNEQ
1	1	1	Forced RDI Alarm
NOTE: The bit numbers above reference a byte whose least significant bit is bit 8			

The forced RDI condition is set by setting the XmtLptRdiFrc bit in “ERRI_CONF—Error Insert Configuration (xDH)” on page 58 to '1'.

4.2.4 N2 Processing

N2 processing is not implemented at this time. The transmitted value for the N2 byte is '00000000'.

4.3 High Order Path Adaptation

After low order path termination, the completed 35 byte by 4 multiframe VC-12 data enters the HPA block. At this stage, the four pointer bytes V1-V4 are added to complete the 36 byte by 4 multiframe TU-12. Since there is no mechanism that would require pointer processing, the V1 and V2 bytes are statically set with a pointer value of 16, the New Data Flag set to the normal value of '0110' and the SS bits set to 01, identifying the payload as E1 traffic. The values of V3 and V4 are set to '00'h.

With all 21 tributaries generated up to the TU-12 level, the final stage of the HPA block formats the data into the appropriate higher order path container. In STM-0, the output is a 86 byte by 9 column C3 container, consisting of seven interleaved TUG-2 structures and the two columns of fixed stuff at columns 30 and 59. In STM-1, the output is an 86 byte by 9 column TUG-3 structure consisting of seven interleaved TUG-2 structures and the two columns of fixed stuff at columns 1 and 2. The TUG-3 data is output onto the MTBDATA bus when MTBTUGEN is a '1'. When the MTBTUGEN is '0', the output is in tri-state, allowing other LXT6251A devices to share the MTBDATA bus. For configurations where each LXT6251A is installed on separate cards interconnected via a backplane, the MTBDOE pin can be used to drive the enable pin of an external tri-state driver. The signal is high whenever the MTBDATA bus contains valid data.

The final output also includes an odd parity bit on the MTBPAR pin calculated over the output MTBDATA byte.

5.0 Add/Drop Configuration

The LXT6251A can be configured to operate as an Add/Drop multiplexer by setting the OpMode bit in “GLOB_CONF—Global Configuration (000H)” on page 55 to ‘1’. This causes a number of internal configurations to change from the terminal mode:

- All Telecom bus data received on the DTBDATA bus is made available to the transmit section (Pass through mode)
- The PTSOH pin controls the transparent pass-through of the higher order path and section data received on the Telecom Bus.
- “TADD_CONF—Transmit Add Configuration (003–001H)” on page 56 control the transparent pass through of each of the 21 TU tributaries accessible by the device.
- The Port Mapping function is enabled allowing each tributary mapping/demapping circuit to operate on any TU time slot within the STM-0 data or the active TUG-3 within STM-1. The result of this function is that each E1 data port (DTCx/DTDX and MTCx/MTDX pairs) can be assigned any TU time slot. More information on the Port Mapping function can be found in “Port Mapping Configuration” on page 34.

The block diagram shown in Figure 6 highlights the data and timing flow in the Add/Drop configuration. It is a requirement in the ADM configuration that the DTBYCK and MTBYCK are the same clock, sourced, for example, from the LXT6051 DTBYCK pin.

5.1 ADM Receive

The receive section of the LXT6251A operates essentially the same in ADM mode as it does in terminal mode. The key difference is the Port Mapping function mentioned above. Details of the Port Mapping function can be found in “Port Mapping Configuration” on page 34. As in terminal mode, the LXT6251A expects at the Telecom Bus input to receive C-3 or C-4 payload data along with the Telecom Bus signals DTBJ0J1EN, DTBPAYEN, DTBTUGEN and DTBH4EN timing signals to synchronize the receive timing generator to the data. From the Telecom bus input out to the E1 port output, the tributaries behave as in terminal mode; all tributaries are processed and all alarms are enabled, unless masked by the appropriate IRQ Mask Registers. To minimize unnecessary alarm information, it is recommended that the alarms from those channels that are passed through be completely masked unless required for monitoring purposes. The final output of the receiver will be E1 data.

5.2 ADM Transmit

Most functions of the transmit section operate the same in ADM mode as in Terminal mode. There are a few important differences however. First, in ADM mode, the timing of the transmitter is controlled by the receive telecom bus signals DTBJ0J1EN, DTBPAYEN, DTBTUGEN and DTBH4EN. The transmit telecom bus timing signals MTBJ0J1EN, MTBPAYEN, and MTBH4EN timing signals become outputs which drive the OHT device (i.e. the receive timing information is passed through to the transmit side). Second, an Add Enable function is provided in “TADD_CONF—Transmit Add Configuration (003–001H)” on page 56. These registers control the source of each TU time slot data output on the MTBDATA bus. The bits in these three registers control the Add Enable status of each TU time slot. If set to ‘0’, the time slot data is taken from the

received DTBDATA input, if set to '1', the TU time slot data is added from an E1 input port; which port is determined by the Port Mapping registers. Finally, as with the receive section, the Port Mapping function is enabled.

It is possible to enable all 21 channels in the Add/Drop mode and use the device in a terminal configuration. One consequence of this configuration is that both transmit and receive sections operate with the same clock and timing references.

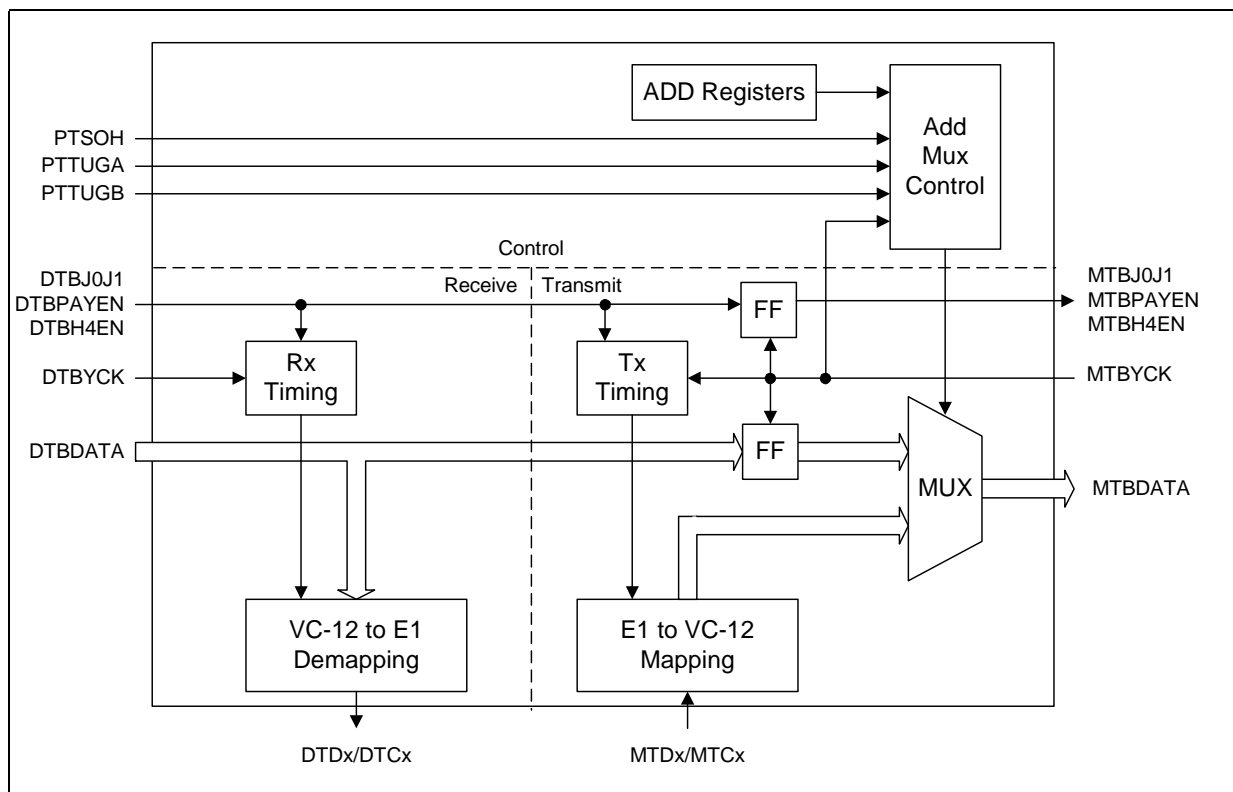
5.2.1 Data Pass-Through

In the Add/Drop configuration for STM-1, it is necessary to control the pass through of the higher order overhead bytes and the non-dropped TUG-3 payloads. The LXT6251A uses three external pins for this control: PTSOH, PTTUGA and PTTUGB.

5.2.1.1 PTSOH

The PTSOH pin controls the pass-through of the SOH and HPOH bytes along with the Telecom bus timing signals. Connecting this pin high will cause the nine columns of the STM-1 SOH, the single column of VC-4 HPOH and the two VC-4 fixed stuff columns and the timing signals MTBJ0J1, MTBPAY, and MTBH4EN to be output on the MTBDATA bus. If PTSOH is tied low, none of the above mentioned bytes are output: MTBDATA is tri-stated during the corresponding time slots and timing signal pins are held in tri-state. This pin should be tied low in STM-0 mode as well as in the STM-1 terminal configuration.

Figure 6. Add/Drop Configuration Data Flow



5.2.1.2 PTTUGx

The PTTUGA and PTTUGB pins are used only in STM-1 mode to control the pass through of the other TUG-3 payloads not being processed by the device. The need for this function can arise if an ADM site is configured to access data in only one TUG-3 payload, thereby requiring only one LXT6251A. The LXT6251A will process the TUG-3 that corresponds with the TUG enable signal connected to its input pin DTBTUGEN. The other two TUG-3 payloads can be passed through by connecting the remaining two DTBTUGEN signals from the OHT to the PTTUGA and PTTUGB pins. Whenever either of these pins is high, the data on the receive Telecom bus is passed through to the transmit Telecom Bus. For example, if the ADM site contains two LXT6251A mappers processing TUG-3 #1 and TUG-3 #3, then one of the mappers can be configured to pass through the TUG-3 #2 payload by connecting the OHT DTBTUGEN2 signal to the PTTUGA pin and connecting the PTTUGB pin to ground. The second mapper chip must have these two pins connected to ground. The different configurations are shown schematically in Figure 6. The functional timing diagram in Figure 9 provides examples of PTTUGA and PTTUGB.

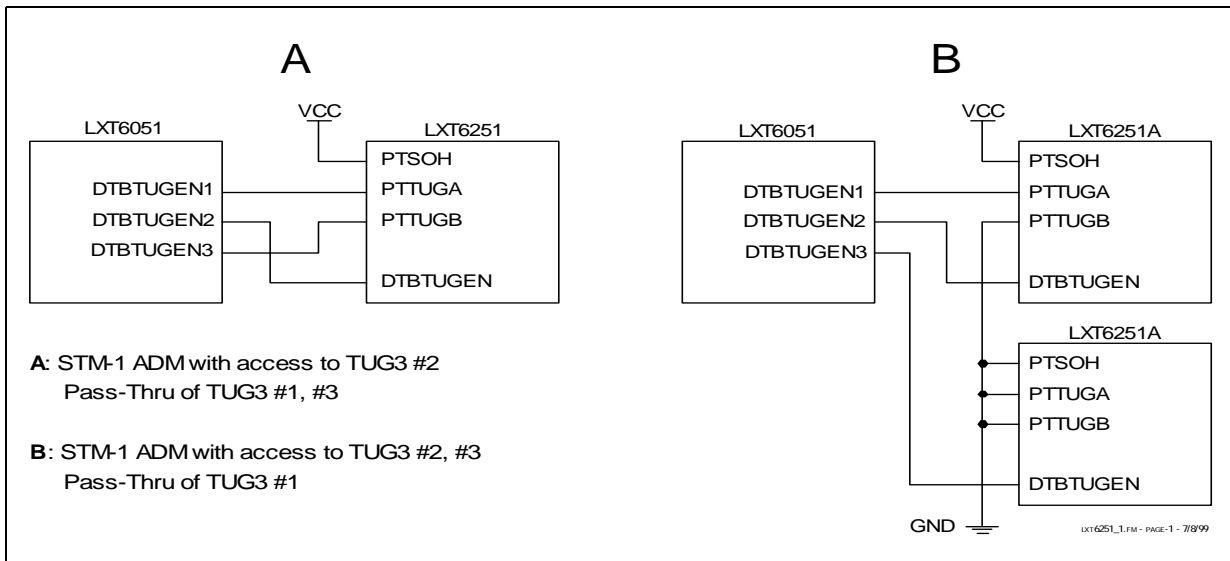
5.2.2 MTBDATA Drive Enable

Table 6 on page 32 shows the drive of the MTBDATA bus in all configurations. The first column gives the configuration, while the remaining four columns represent the four different data types that can be output on this bus. For example, the STM-1 ADM multiplexer with PTSOH tied to ground will drive the bus when MTBTUGEN is active, and will be in tri-state during the SOH, HPOH (and two bytes of VC-3/VC-4 fixed stuff), and the other two TUG-3 payloads. It is recommended that PTTUGA/B signals be active only on the device with PTSOH set high.

Table 6. Multiplex Telecom Bus Drive Matrix

Configuration	Section Overhead	POH and VC Fixed Stuff	PTTUGA/B = '1'	MTBTUGEN = '1'
STM-1 ADM, PTSOH = '1'	Data	Data	Data	Data
STM-1 ADM, PTSOH = '0'	Hi-Z	Hi-Z	Hi-Z	Data
STM-1 Term	Hi-Z	Hi-Z	Hi-Z	Data
STM-0 ADM	Data	Data	N/A	Data
STM-0 Term	Data	Data	N/A	Data

Figure 7. ADM Multi-chip Configuration



6.0 Application Information

6.1 Port Mapping Configuration

To allow for the design of a cost-reduced ADM mapper module, the LXT6251A supports a programmable E1 port mapping feature that allows each E1 I/O port to be assigned to any tributary time slot. The cost-reduced module may contain only four or eight E1 line interface circuits, but the use of the Port Mapping would allow access to any TU-12 tributary within a TUG-3 or STM-0 payload at an ADM site.

There is a 5 bit Port Mapping register per tributary circuit that is used to configure the time slot on which the circuit operates. Each of the 21 circuits has associated with it a set of alarm and control registers (address range $x0H$ through xFH) and the E1 I/O ports MTD(T)/MTC(T) and DTB(T)/DTC(T), where T ranges from 1 to 21. By configuring the port mapping register to a timeslot, all processing of the assigned TU-12 is performed by the hardware circuit associated with the port mapping register. That is, when the Port Mapping function is used, both the register address and the physical E1 port (both Tx and Rx) will operate on the selected TU-12 time slot.

Table 7 contains the default register values and the ITU specified Time Slot numbering for the 21 tributaries. In the STM-1 configuration, the input DTBTUGEN control pin determines the TUG-3 number (K). The default associations map port 1 to the first TU-12 time slot (1,1) and linearly progress to port 21 with TU-12 slot 21 (7,3).

When configuring the port mapping registers, care must be taken to keep the value in each register unique. If port 1 is assigned TS (2,1), then no other port should be assigned to this timeslot. Failure to ensure this could result in an unstable system. It is also suggested that the multiplexer Telecom bus be placed in tri-state (the TBTristate bit in the Global Configuration register) whenever the Port Mapping registers are changed.

Table 7. E1 Port Time Slot Assignment

Tributary Circuit (Port)	Register Address	Default Value	Default Time Slot	TU-12 Address (L, M)
1	161h	1	1	(1, 1)
2	162h	2	2	(2, 1)
3	163h	3	3	(3, 1)
4	164h	4	4	(4, 1)
5	165h	5	5	(5, 1)
6	166h	6	6	(6, 1)
7	167h	7	7	(7, 1)
8	168h	8	8	(1, 2)
9	169h	9	9	(2, 2)
10	16Ah	10	10	(3, 2)
11	16Bh	11	11	(4, 2)
12	16Ch	12	12	(5, 2)
13	16Dh	13	13	(6, 2)
14	16Eh	14	14	(7, 2)

Table 7. E1 Port Time Slot Assignment (Continued)

Tributary Circuit (Port)	Register Address	Default Value	Default Time Slot	TU-12 Address (L, M)
15	16Fh	15	15	(1, 3)
16	170h	16	16	(2, 3)
17	171h	17	17	(3, 3)
18	172h	18	18	(4, 3)
19	173h	19	19	(5, 3)
20	174h	20	20	(6, 3)
21	175h	21	21	(7, 3)

6.2 Telecom Bus Interface

The LXT6251A uses an industry standard Telecom Bus to interface with other SDH products, including LXT6051. The standard is based on the original work of the IEEE P1396 project that never made it to final approval. Intel has enhanced the bus to be compatible with other standard SDH products on the market.

6.2.1 Multiplexer Telecom Bus, Terminal Mode

In terminal mode, the multiplexer side Telecom Bus operates in a contra-directional mode, meaning the Mapper receives the timing signals and generates the Data synchronized to the timing signals but delayed by one half clock cycle. Functional Timing diagrams are shown in Figure 7 and Figure 8.

MTBYCK	Input Telecom Bus byte clock at 6.48 MHz for STM0 or 19.44 MHz for STM1.
MTBDATA	Output Byte parallel Data. In STM-0, the data consists of the 21 TU-12 signals in a 7 by TUG-2 format plus the 2 fixed stuff columns of a C3 container at positions 30 and 59. The data bus is also driven during all other SOH and HPOH bytes, however, the data during these times is not valid. In STM-1, the data consists of a single TUG-3 payload controlled by MTBTUGEN. The bus is in tri-state for all other bytes (SOH, HPOH, fixed stuff)
MTBPAR	Output parity bit calculated on each output MTBDATA byte. This is an odd parity calculation.
MTBJ0J1EN	Input Frame Position indicator, active high during both the J0 and J1 bytes. The J0 byte is identified when the MTBPAYEN is low, J1 when MTBPAYEN is high. Optionally the MultiFrmSel configuration bit in “GLOB_CONF—Global Configuration (000H)” on page 55 can be set to ‘1’, which adds a multiframe indication (byte H4=00 for TU-12 V1 byte location) by detecting a two-byte wide J1 pulse every fourth frame. Note the H4 indication can be active even when MTBPAYEN is Low.
MTBPAYEN	Input Payload Enable. A high on this input enables the driving of the MTBDATA bus with the VC-3 or VC-4 payload. A low indicates the location of the SOH bytes and the AU Pointers bytes.
MTBH4EN	Input indicates the multiframe start position. This signal must be active high during the J1 byte following the multiframe when the H4 byte equals

'00'. This signal need not be present if the multiframe indication exists in MTBJ0J1EN.

MTBTUGEN Input used in STM-1 only. A high enables the MTBDATA bus to be driven with the TUG-3 being output by the device. This signal must also be High during the VC-4 HPOH byte, regardless of the TUG-3 it is enabling. In STM-0, this signal should be tied high.

Note: Note on Telecom Bus Timing Reference: All Telecom Bus timing signals (MTBH4EN, MTBPAYEN, MTBJ0EN and MTBTUGEN) are sampled on the falling edge of the MTBYCK clock, and the output data (MTBPAR and MTBDATA) are clocked out of the device on the falling edge of this clock. See Telecom bus timings in Figure 7 and Figure 8.

6.2.2 Multiplexer Telecom Bus, ADM Mode

In the Add/Drop configuration, the Telecom Bus operates in a co-directional mode, meaning that both the timing signals and the data are generated by the Mapper. The enable signals are coincident with the associated data on the bus.

MTBYCK	Input, identical to the Terminal mode
MTBDATA	Output, at a minimum this data bus contains the 7 by TUG-2 (STM-0) or TUG-3 (STM-1) data. Depending on the pass-through configuration, MTBDATA could contain SOH, HPOH, and other TUG-3 data (STM-1). Refer to Table 6.
MTBPAR	Output, active whenever MTBDATA is active.
MTBJ0J1EN	Output, this is directly the DTBJ0J1EN delayed by 3 MTBYCK clock periods.
MTBPAYEN	Output, this is directly the DTBPAYEN delayed by 3 MTBYCK clock periods.
MTBH4EN	Output, this is directly the DTBH4EN delayed by 3 MTBYCK clock periods
MTBTUGEN	Not used in ADM mode

Note: Note on Telecom Bus Timing Reference: All Telecom Bus timing signals (MTBH4EN, MTBPAYEN, MTBJ0EN and MTBTUGEN) and data (MTBPAR and MTBDATA) are clocked out of the device on the rising edge of this clock. See Telecom bus timings in Figure 7 and Figure 8.

6.2.3 MTBDATA Output Enable

The configuration bit TBTristate within “GLOB_CONF—Global Configuration (000H)” on [page 55](#) is used to force the multiplexer telecom bus into tri-state during configuration of the chip. It exists for those configurations in STM-1 where multiple chips drive the bus. At power up, the bit defaults to ‘1’ disabling the MTBDATA and MTBPAR signals while initial configuration is performed. After all devices that drive the MTBDATA/MTBPAR bus are configured, each device can then be enabled by setting the bit to ‘0’. Should a configuration change take place, for example re-configuring an ADM site, all devices might be set into tri-state during the configuration operation if no specific care is to be given to the propagation order.

6.2.4 Demultiplexer Telecom Bus

In both terminal and ADM configurations, the demultiplexer side Telecom Bus operates in a co-directional mode, meaning that both the timing signals and the data are inputs to the LXT6251A. The enable signals are coincident with the associated data on the bus.

DTBYCK	Input Telecom Bus byte clock at 6.48 MHz for STM0 or 19.44 MHz for STM1
DTBDATA	Input byte wide Data. In STM-0, the data must consist of the 21 TU-12 signals in a 7 by TUG-2 format with the 2 fixed stuff columns at positions 30 and 59. The HPOH and SOH data on the bus is ignored, except as required for ADM pass-through. In STM-1, the data must consist of a valid TUG-3 payload active when DTBTUGEN is high. Other TUG-3, HPOH, and SOH data is ignored, except as required for ADM pass-through.
DTBPAR	Input Parity bit calculated on each DTBDATA byte. This is an odd parity calculation.
DTBJ0J1EN	Input Frame Position indicator, active high during both the J0 and J1 bytes. The J0 byte is identified when the DTBPAYEN is low, J1 when DTBPAYEN is high. Optionally the MultiFrmSel configuration bit in “GLOB_CONF—Global Configuration (000H)” on page 55 can be set to ‘1’, which adds a multiframe indication (byte H4=00 for TU-12 V1 byte location) by detecting a two-byte wide J1 pulse every fourth frame. Note the H4 indication can be active even when DTBPAYEN is Low.
DTBPAYEN	Input Payload Enable. A high on this input indicates that the DTBDATA bus is being driven with the VC-3 or VC-4 payload. A low indicates the location of the SOH bytes and the AU Pointer bytes.
DTBH4EN	Input indicates the multiframe start position. This signal must be active high during the J1 byte following the multiframe when the H4 byte equals ‘00’. This signal need not be present if the multiframe indication exists in DTBJ0J1EN.
DTBTUGEN	Input used in STM-1 only. A high indicates that the DTBDATA bus is being driven with the TUG-3 that is to be processed by the device. This signal must also be High during the VC-4 HPOH byte, regardless of the TUG-3 it is enabling. In STM-0, this signal should be tied High.

Note: Note on Telecom Bus Timing Reference: All Telecom Bus timing signals (DTBH4EN, DTBPAYEN, DTBJ0EN and DTBTUGEN), and the output data (DTBPAR and DTBDATA) are sampled on the falling edge of the DTBYCK clock. See Telecom bus timings in Figure 7 and Figure 8.

6.2.5 Telecom Bus Timing

The following diagrams show the relation of timing reference and data signals on the Telecom bus. In summary, if the timing reference signals (DTBJ0J1, DTBPAYEN) and the data are sourced from the same device (co-directional timing), the data byte (i.e., J1) will be coincident with the J1 indicator. If the timing reference signals are sourced from a device that expects to receive data (contra-directional timing), then the data will be received one half clock cycle later.

Figure 8. STM-0 Telecom Bus Timing

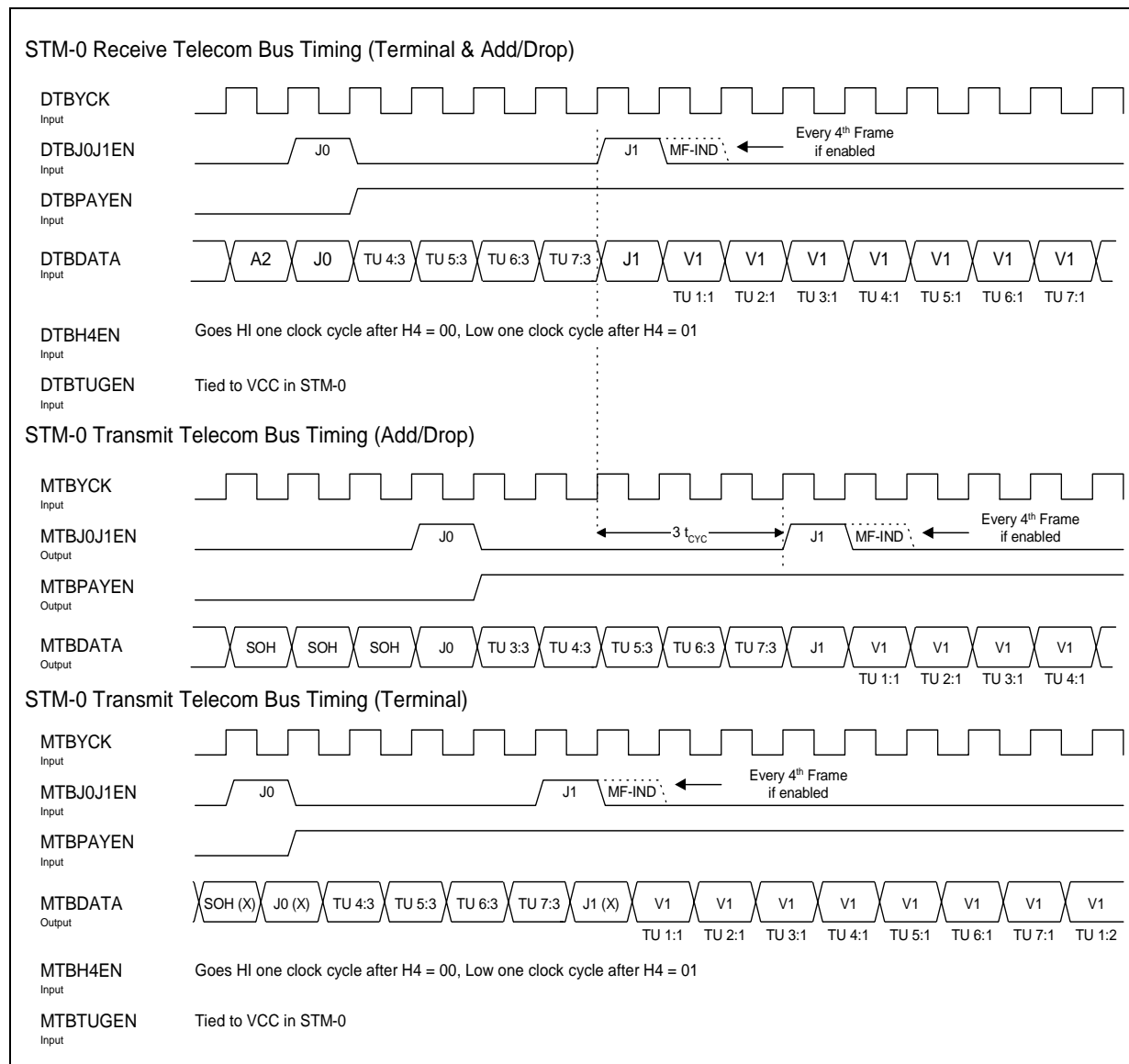


Figure 9. Terminal STM-1 Telecom Bus Timing (

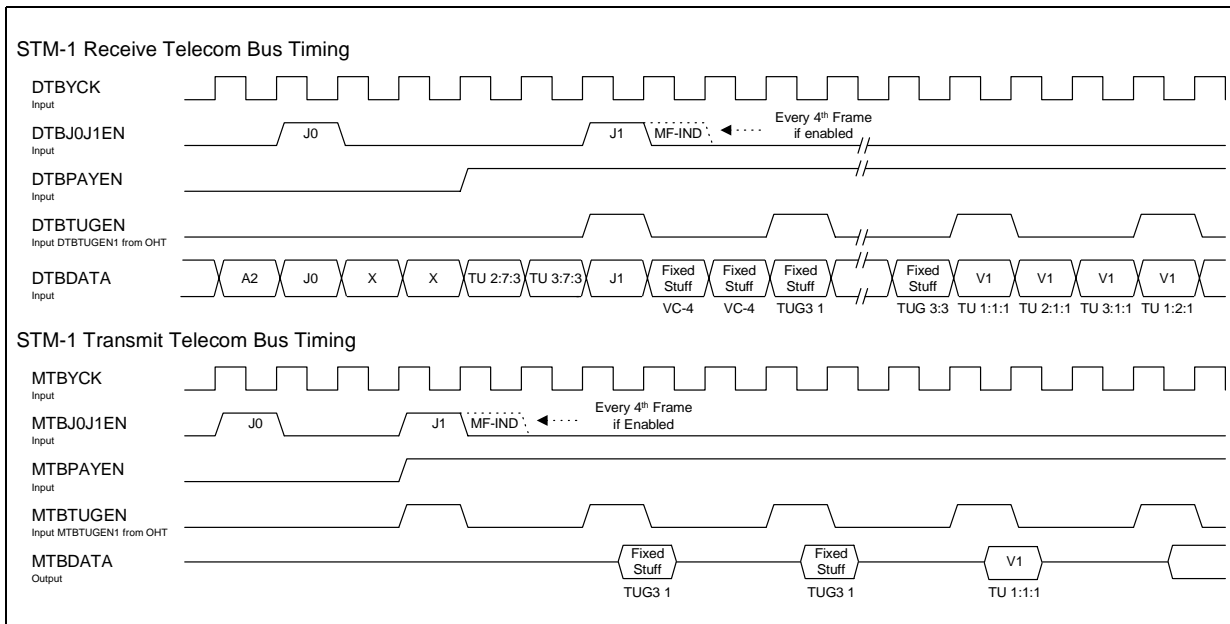


Figure 10. ADM STM-1 Telecom Bus Timing w/ PTSOH=1

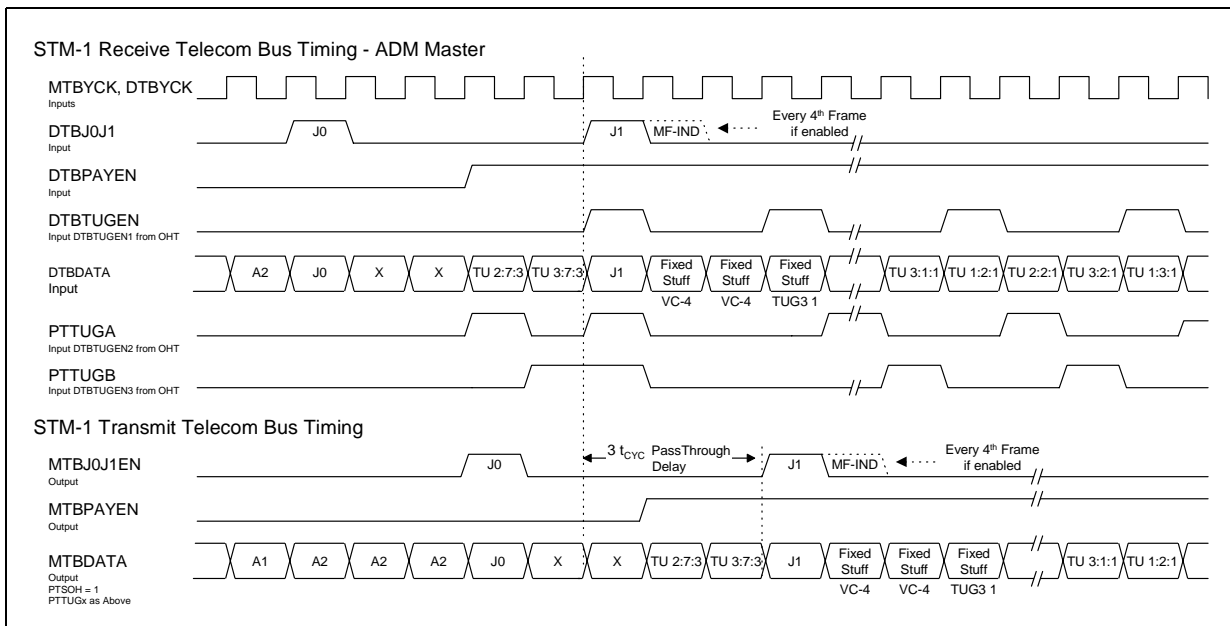
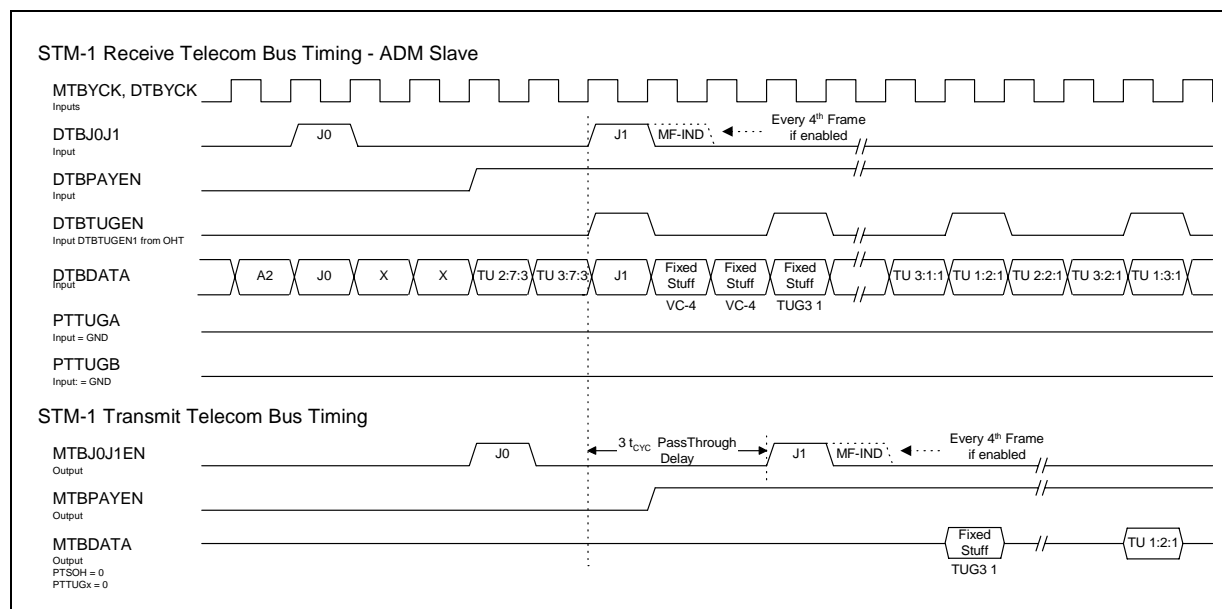


Figure 11. ADM STM-1 Telecom Bus Timing w/ PTSOH = 0



6.3 Serial/Remote Alarm Processing Port

There are six pins on the chip dedicated to remote alarm processing, three for the receive section to output the alarm data (SAP), and three to input the data into the transmit section (RAP). In a Terminal configuration, the output SAP pins should be connected to the input RAP pins. In the ADM configuration, an LXT6251A processes data in one direction only, therefore the SAP port is used to transfer the REI/RDI and other feedback alarm information between the East traffic and West traffic mappers. The configurations for connecting the SAP Bus are shown in Figure 11.

The SAP Bus consists of three signals: clock, frame signal, and the alarm data. The following Alarm data is provided in a framed format on the SAPDATA signal (refer to Figure 4 for V5 bit assignment):

REI	REI indication (from BIP-2 error), Drives TX V5 REI bit on Tx
RDI-1	Connectivity Defect (UNEQ, TIM), Drives TX V5 RDI bit, K4 ERDI on Tx. Note the UNEQ alarm is not active in Supervisory Unequipped configuration
RDI-2	Server Defect (TU-LOP, TU-AIS), Drives TX V5 RDI bit, K4 ERDI on Tx
SF	Signal Fail alarm. A one bit alarm that is active when the receiver detects either type of RDI alarm, VC-AIS, or H4 Loss of multiframe.

The SF bit is ignored on the Tx RAP bus input. It is provided exclusively for a fast tributary alarm indication and can be used by using a small external circuit to control VC-12 protection switching. The frame format for the SAP Bus is shown in Figure 13.

Figure 12. SAP Bus Connections for Terminal & ADM

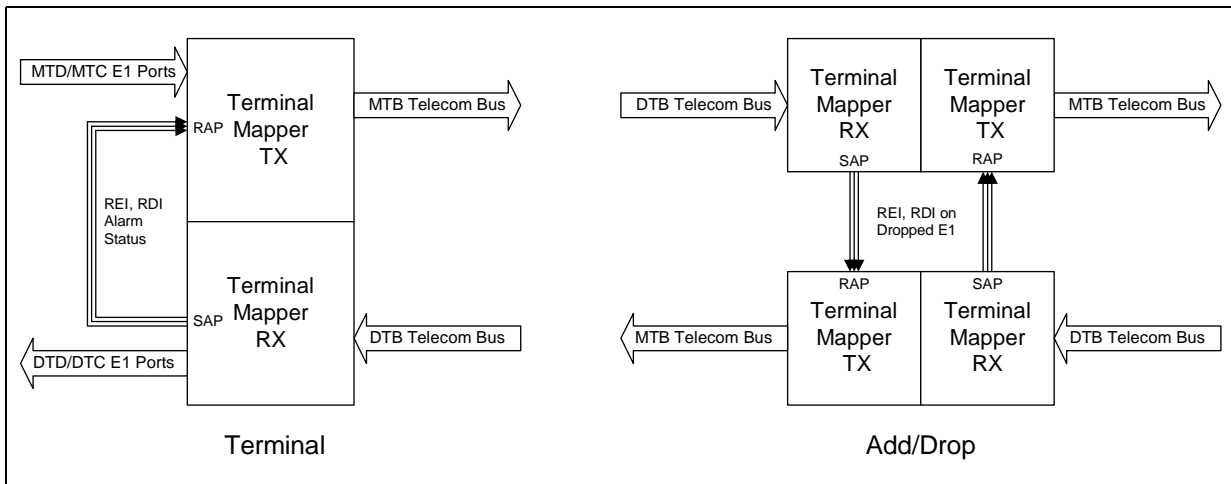
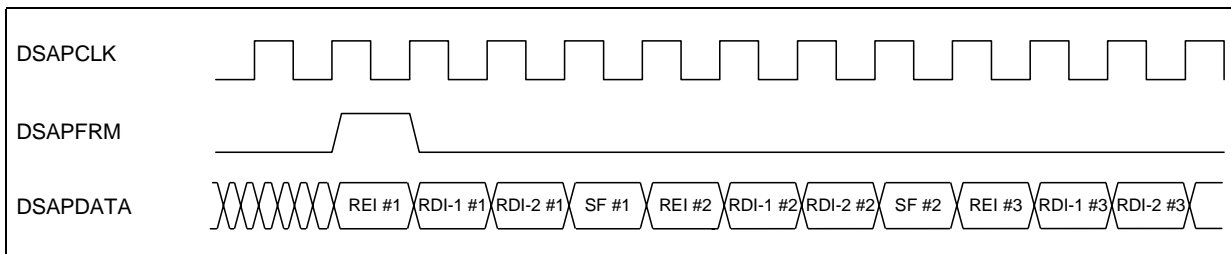


Figure 13. SAP Bus Frame Format



7.0 Test Specifications

Note: Minimum and maximum values in tables 9 through 11 represent the performance specifications of the LXT6251A and are guaranteed by test unless otherwise noted. Minimum and maximum values in tables 12 through 27 and figures 32 through 45 represent the performance specifications of the LXT6251A and are guaranteed by design and are not subject to production testing.

Note: All timing parameters assume that the outputs have a 50 pF load unless otherwise noted.

Table 8. Absolute Maximum Ratings

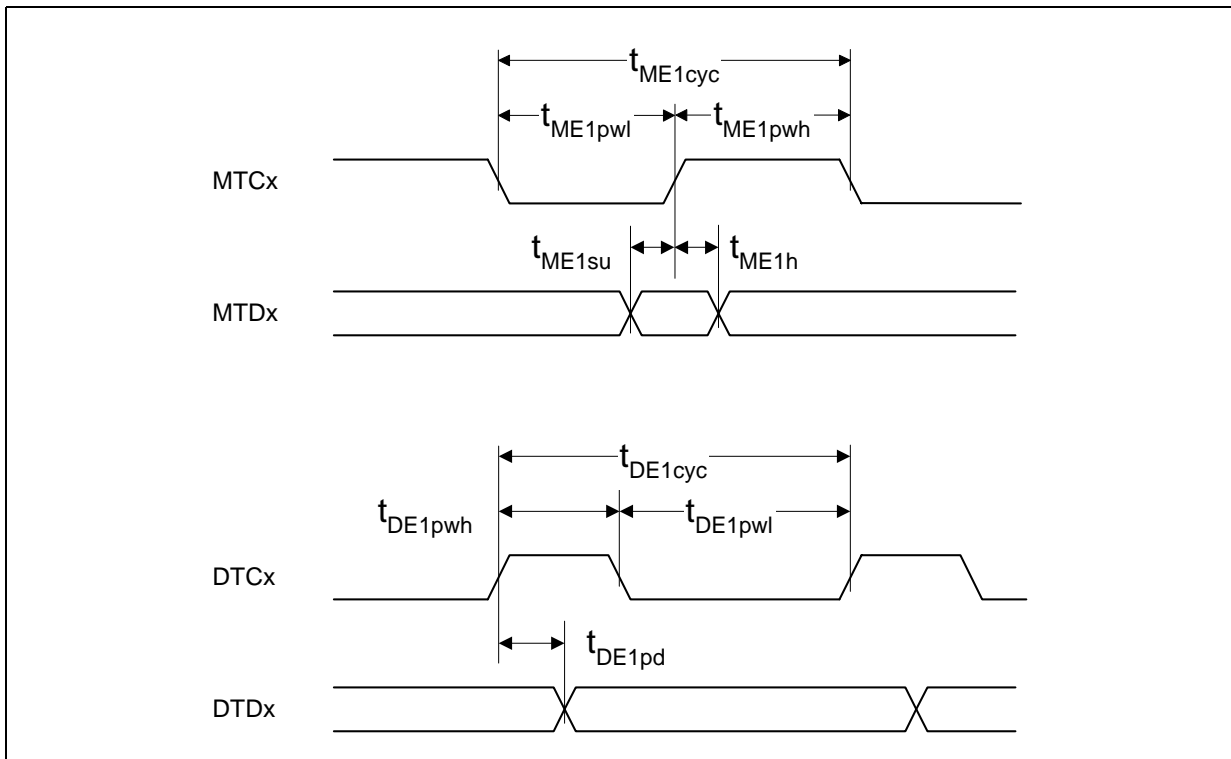
Parameter	Symbol	Min	Max	Unit
Supply Voltage	VCC		6.0	V
DC Voltage on any pin ¹	VIN	-2.0	+7.0	V
Ambient operating temperature	TOP	-40	+85	C
Storage temperature range	TST	-65	+150	C
1. Minimum voltage is -0.6V dc which may undershoot to -2.0 V for pulses of less than 20 ns				
CAUTION: Exceeding these values may cause permanent damage.				
CAUTION: Functional operation under these conditions is not implied				
CAUTION: Exposure to maximum rating conditions for extended periods may affect device reliability				

Table 9. Operating Conditions

Parameter	Symbol	Min	Typ ¹	Max	Unit
Recommended Operating Temperature	TOP	-40	-	+85	C
Supply Voltage - I/O Ring	VCC5	4.75	5	5.25	V
Supply Voltage - Core	VCC3	3.15	3.3	3.45	V
Supply Current - I/O Ring ³	IDD5	-	15	25	mA
Supply Current - Core ³	IDD3		200	250	mA
1. Typical values are at 25C and nominal voltage and are provided for design aid only; not guaranteed nor subject to production testing					
2. Voltages with respect to ground unless otherwise specified					
3. STM-1 Terminal mode, PRBS data on all tributaries, outputs loaded, not subject to production testing					

Table 10. 5 V Digital I/O Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
TTL Input Low Voltage	VIL			0.8	V	
TTL Input High Voltage	VIH	2.0			V	
TTL Switching Threshold	VT		1.4		V	VCC=5.0V, 25C
Input Leakage High	I _{IH}			10	uA	VIN-VCC=5.5V
Output Low Voltage	VOL		0.2	0.4	V	VCC=4.5V
Output High Voltage	VOH	0.7xVCC	4.2			VCC=4.5V
Output Leakage (no pull up)	IOZ	-10		10	uA	VIN=VDD=5.5V
1. All values applicable over recommended Voltage and Temperature operating range unless otherwise noted						

Figure 14. Tributary Timing

Table 11. Tributary Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
MTCx Input E1 Clock pulse width low	t_{ME1PWL}	$TM + 3$ ¹			ns
MTCx Input E1 Clock pulse width high	t_{ME1PWH}	$TM + 5$ ¹			ns
MTCx Input E1 Clock cycle time	t_{ME1CYC}		488		ns
MTDx setup time to MTCx rising edge	t_{ME1SU}	4			ns
MTDx hold time from MTCx rising edge	t_{ME1H}	2			ns
DTCx output clock pulse width low	t_{DE1pwl}	$2(1+2S)TD - 5$ ^{2,3}	$2(1+2S)TD$ ^{2,3}	$5(1+2S)TD + 2$ ^{2,3}	ns
DTCx output clock pulse width high	t_{DE1pwh}	$(1+2S)TD - 2$ ^{2,3}	$(1+2S)TD$ ^{2,3}	$(1+2S)TD + 5$ ^{2,3}	ns
DTCx output E1 Clock cycle time	t_{DE1CYC}	$3(1+2S)TD$ ^{2,3}		$6(1+2S)TD$ ^{2,3}	ns
DTDx delay from DTCx rising edge	t_{DE1pd}			9	ns

1. TM is the clock period of MTBYCK
 2. TD is the clock period of DTBYCK
 3. S is '0' for STM0 application and '1' for STM1 application.

Figure 15. Receive Telecom Bus Timing

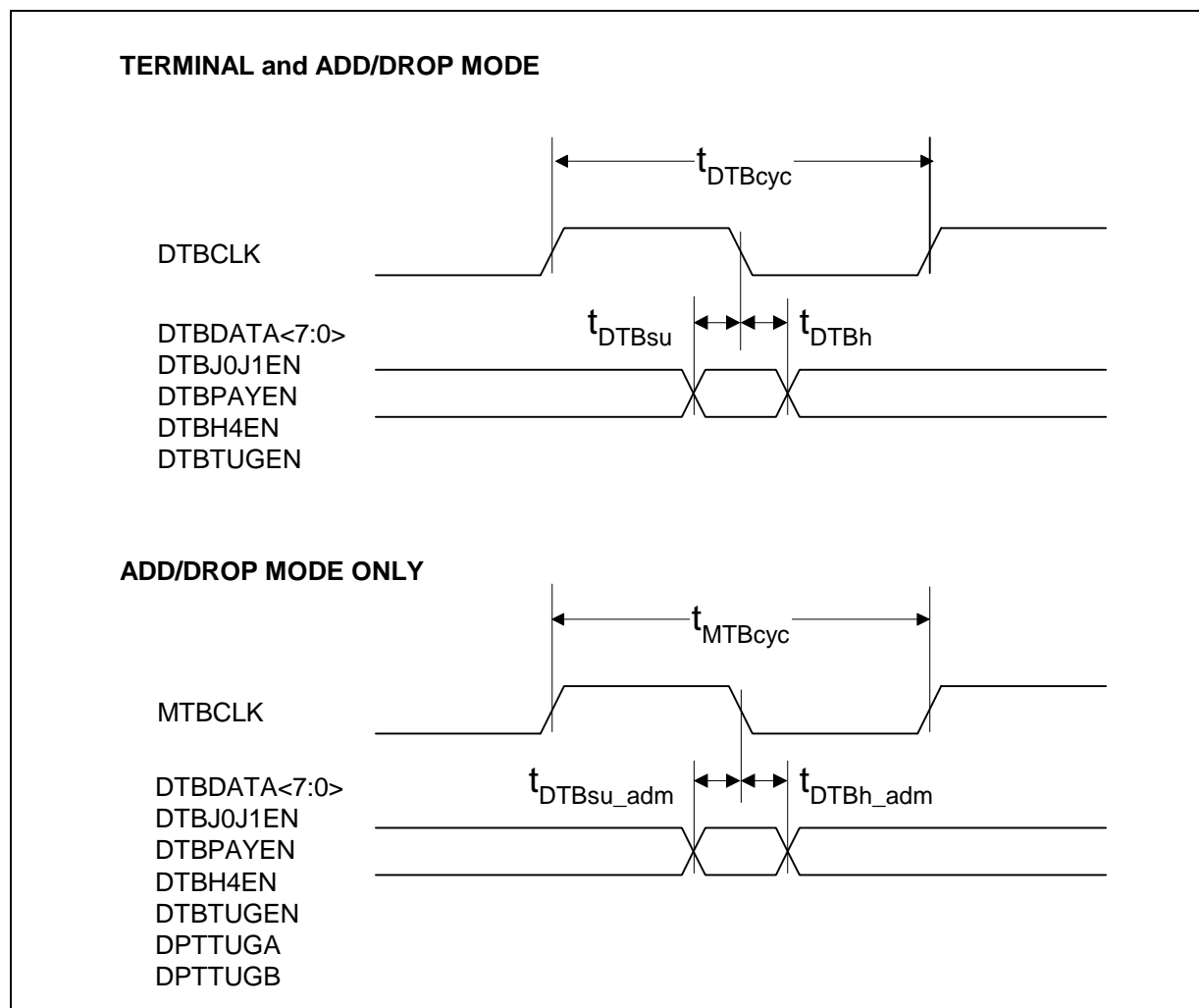
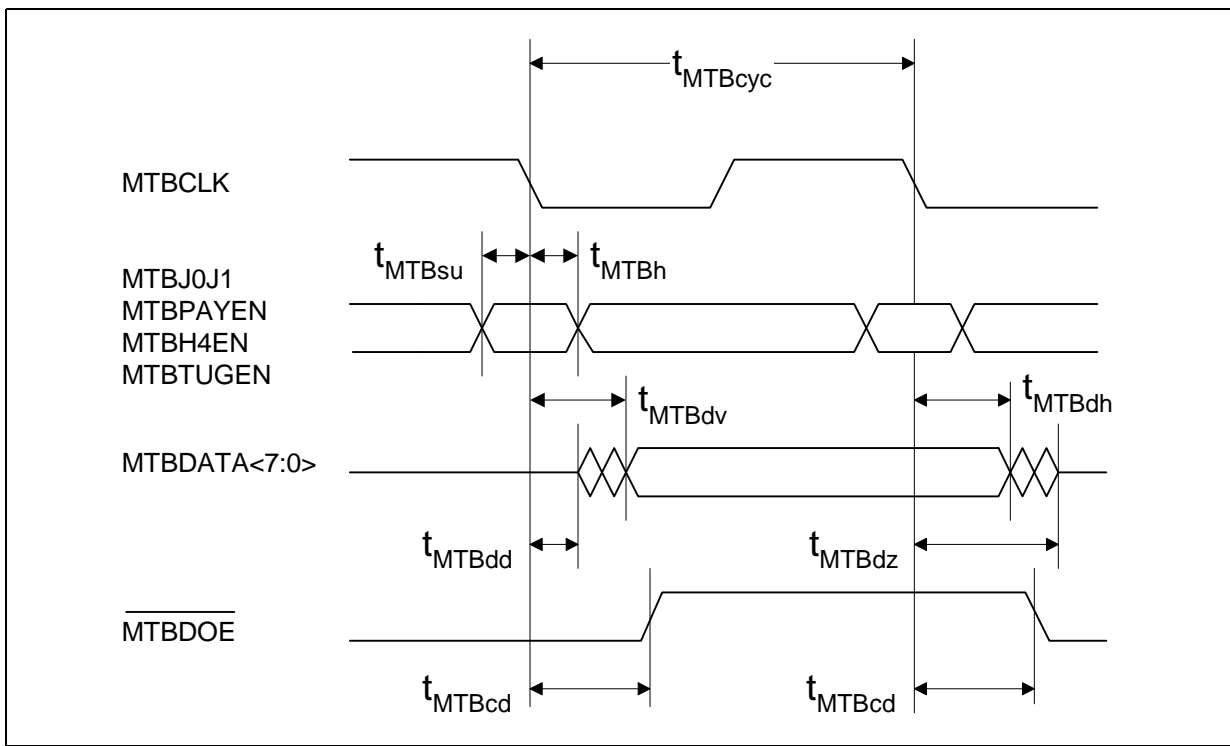


Table 12. Receive Telecom Bus Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
DTBCLK Input clock cycle time	tDTBcyc		6.48/19.44		MHz
MTBCLK Input clock cycle time	tMTBcyc		6.48/19.64		MHz
Any telecom bus input setup time to DTBCLK falling edge	tDTBsu	3	-	-	ns
Any telecom bus input hold time after DTBCLK falling edge	tDTBh	5	-	-	ns
Any telecom bus input setup time to MTBCLK falling edge	tDTBsu_adm	4	-	-	ns
Any telecom bus input hold time after MTBCLK falling edge	tDTBh_adm	3	-	-	ns

Figure 16. Transmit Telecom Bus Timing - Terminal

Table 13. Transmit Telecom Bus Timing - Terminal Parameters

Parameter	Symbol	Min	Typ	Max	Unit
MTBCLK Input clock cycle time	t_{MTBcyc}		6.48/19.44		MHz
Any telecom bus timing input setup time to MTBCLK falling edge	t_{MTBsu}	1	-	-	ns
Any telecom bus timing input hold time after MTBCLK falling edge	t_{MTBh}	3	-	-	ns
MTBCLK falling edge to MTBDATA bus driven (STM1 only)	t_{MTBdd}	9	-	-	ns
MTBCLK falling edge to MTBDATA valid	t_{MTBdv}		-	24	ns
MTBDATA hold time after MTBCLK falling edge	t_{MTBdh}	-	-	7	ns
MTBCLK falling edge to MTBDATA bus Hi-Z (STM1 only)	t_{MTBdz}	-	-	19	ns
\overline{MTBDOE} output delay from MTBCLK falling edge	t_{MTBcd}	9	-	28	ns

Figure 17. Transmit Telecom Bus Timing - ADM Parameters

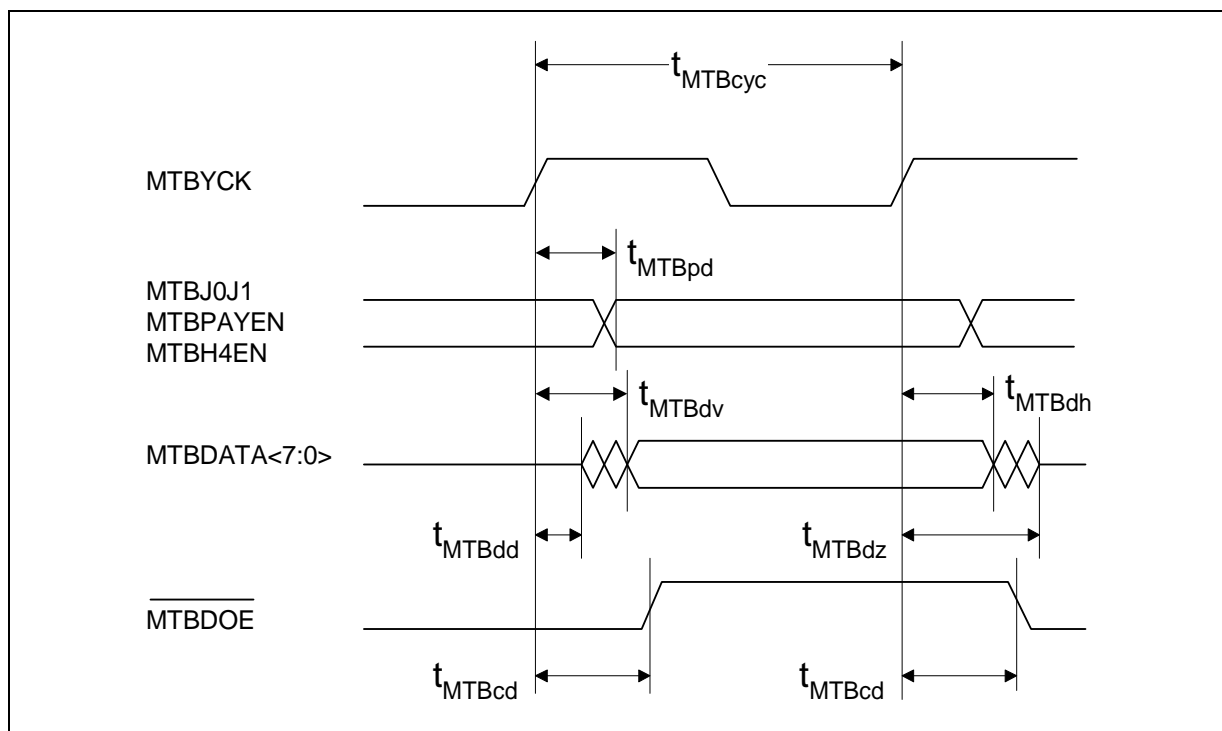
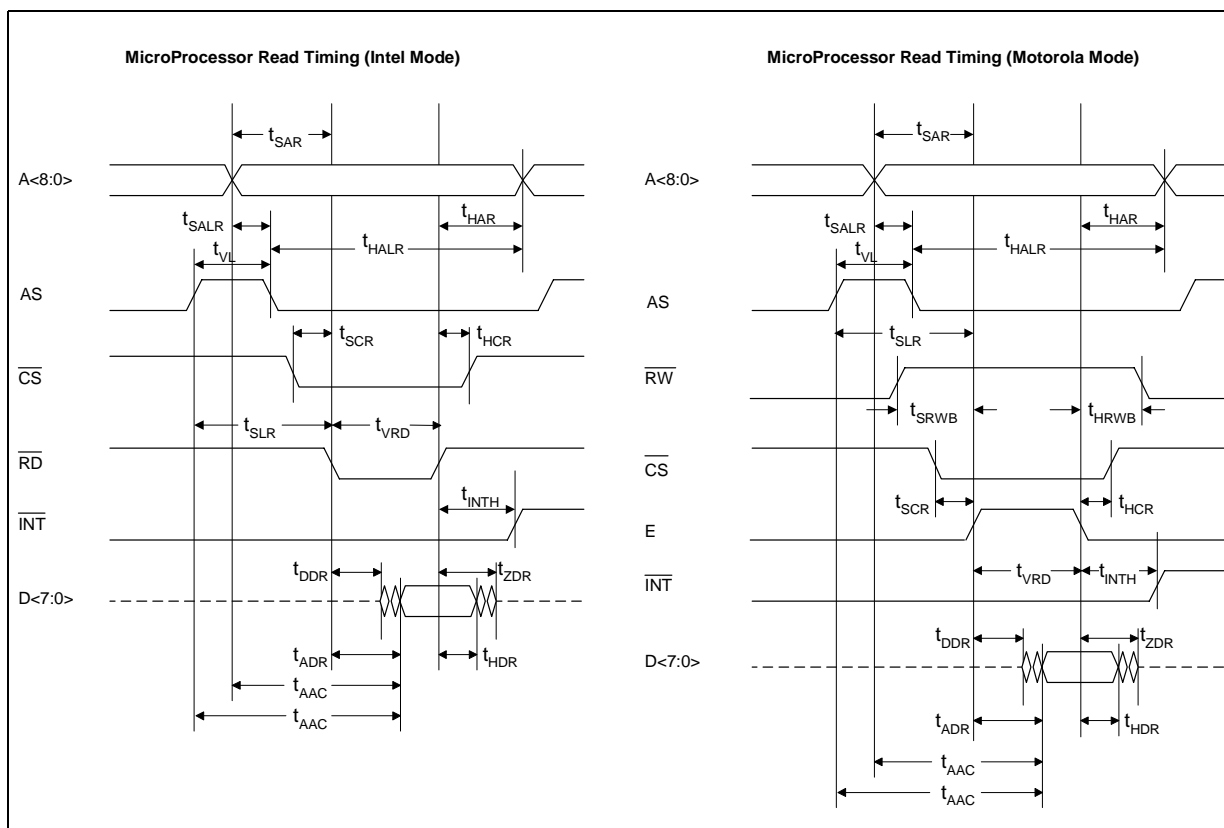


Table 14. Transmit Telecom Bus Timing - ADM Parameters

Parameter	Symbol	Min	Typ	Max	Unit
MTBCLK Input clock cycle time	t_{MTBcyc}		6.48/19.44		MHz
Any telecom bus timing output delay from MTBCLK rising edge	t_{MTBpd}	8	-	24	ns
MTBCLK rising edge to MTBDATA bus driven (STM1 only)	t_{MTBdd}	10	-	-	ns
MTBCLK rising edge to MTBDATA valid	t_{MTBdv}		-	23	ns
MTBDATA hold time after MTBCLK falling edge	t_{MTBdh}	-	-	8	ns
MTBCLK rising edge to MTBDATA bus Hi-Z (STM1 only)	t_{MTBdz}	-	-	22	ns
MTBDOE output delay from MTBCLK rising edge	t_{MTBcd}	8	-	24	ns

Figure 18. Microprocessor Data Read Timing

Table 15. Microprocessor Data Read Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
A<8:0> setup time to active read	t_{SAR}	10	-	-	ns
A<8:0> hold time from inactive read	t_{HAR}^1	2	-	-	ns
A<8:0> setup time to latch	t_{SALR}^2	1	-	-	ns
A<8:0> hold time from latch	t_{HALR}^2	3	-	-	ns
Valid latch pulse width	t_{VL}^2	1.5	-	-	ns
AS rising edge to active read setup	t_{SLR}^2	11	-	-	ns
\overline{RW} setup to active read	t_{SRWB}	3	-	-	ns
\overline{RW} hold from inactive read	t_{HRWB}	2	-	-	ns
\overline{CS} setup to active read	t_{SCR}	2	-	-	ns
\overline{CS} hold from inactive read	t_{HCR}	2	-	-	ns
D<7:0> access time from valid address (or AS whichever comes last for muxed AD bus)	t_{AAC}	-	-	51	ns

1. For non multiplexed Address and Data bus (AS tied high)
 2. For multiplexed Address and Data bus (AS used as address latch enable)
 3. T is the minimum cycle time of either MTBYCK or DTBYCK (typically 51.44 ns for STM1, 154.32 ns for STM0)
 4. Consecutive reads from the on-chip RAM ("expected" and "transmitted" J2 strings) must be separated by more than $4 \cdot T$

Table 15. Microprocessor Data Read Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
D<7:0> bus driven from active read	t_{DDR}	6	-	-	ns
D<7:0> access time from active read	t_{ADR}	-	-	17	ns
D<7:0> hold from inactive read	t_{HDR}	5	-	-	ns
D<7:0> High impedance from inactive read	t_{ZDR}	-	-	16	ns
Valid read pulse width	t_{VRD}^3	T+2	-	-	ns
Inactive read to inactive INT (due to reset on read feature)	t_{INTH}	3*T + 2	-	4*T + 36	ns

1. For non multiplexed Address and Data bus (AS tied high)
 2. For multiplexed Address and Data bus (AS used as address latch enable)
 3. T is the minimum cycle time of either MTBYCK or DTBYCK (typically 51.44 ns for STM1, 154.32 ns for STM0)
 4. Consecutive reads from the on-chip RAM ("expected" and "transmitted" J2 strings) must be separated by more than 4*T

Figure 19. Microprocessor Data Write Timing

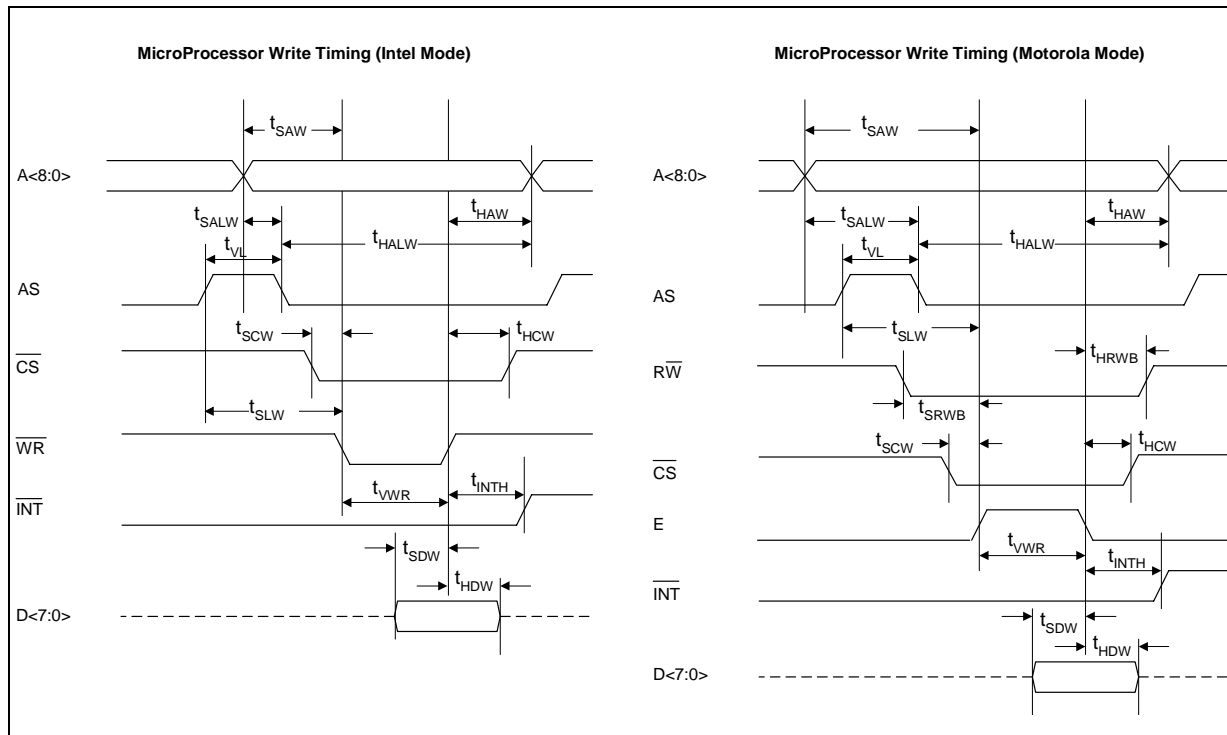


Table 16. Microprocessor Data Write Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
A<8:0> setup time to active write	t_{SAW}	8	-	-	ns
A<8:0> hold time from inactive write	t_{HAW}^1	3	-	-	ns
A<8:0> setup time to latch	t_{SALW}^2	1	-	-	ns
A<8:0> hold time from latch	t_{HALW}^2	3	-	-	ns
Valid latch pulse width	t_{VL}^2	1.5	-	-	ns
AS rising edge to active write setup	t_{SLW}^2	10	-	-	ns
\overline{RW} setup to active write	t_{SRWB}	3	-	-	ns
\overline{RW} hold from inactive write	t_{HRWB}	2	-	-	ns
\overline{CS} setup to active write	t_{SCW}	2	-	-	ns
\overline{CS} hold from inactive write	t_{HCW}	2	-	-	ns
D<7:0> setup to inactive write	t_{SDW}	9	-	-	ns
D<7:0> hold from inactive write	t_{HDW}	6	-	-	ns
Valid write pulse width	t_{VWR}^3	T+2	-	-	ns
Inactive write to inactive INT (due to interrupt masking)	t_{INTH}	12	-	36	ns
1. For non multiplexed Address and Data bus (AS tied high) 2. For multiplexed Address and Data bus (AS used as address latch enable) 3. T is the minimum cycle time of either MTBYCK or DTBYCK (typically 51.44 ns for STM1, 154.32 ns for STM0) 4. There must be more than 4*T between the rising edge of a write to a BIP or REI error counter and the falling edge of the read to a BIP or REI error counter 5. Consecutive writes to the on-chip RAM ("expected" and "transmitted" J2 strings) must be separated by more than 4*T					

8.0 Microprocessor Interface & Register Definitions

8.1 Microprocessor Interface

The LXT6251A incorporates an asynchronous microprocessor interface. A microprocessor can be connected to the LXT6251A for reading and writing data via the microprocessor interface pins.

The microprocessor interface is a generic asynchronous interface, including an address bus (A<8:0>), data bus (DATA<7:0>) and control pins ($\overline{\text{WR}}/\text{RW}$, $\overline{\text{RD}}/\text{E}$, $\overline{\text{CS}}$, and AS). The MCUTYPE input pin configures the type of microprocessor interface to be used – Intel or Motorola. There is also an $\overline{\text{INT}}$ output pin that indicates alarm conditions to the microprocessor.

8.1.1 Intel Interface

The Intel interface is indicated by driving the MCUTYPE input pin Low. In this mode the $\overline{\text{WR}}/\text{RW}$ input pin is used as a write-bar ($\overline{\text{WR}}$) and the $\overline{\text{RD}}/\text{E}$ input pin as read-bar ($\overline{\text{RD}}$).

A read cycle is indicated to the LXT6251A by the microprocessor forcing a Low on the $\overline{\text{RD}}$ pin with the $\overline{\text{WR}}$ pin held High.

A write cycle is indicated to the LXT6251A by the microprocessor forcing a Low on the $\overline{\text{WR}}$ pin with the RD pin held High.

Both cycles require the CSB pin to be Low and the microprocessor to drive the A<8:0> address pins. In the case of the write cycle, the microprocessor is also required to drive the DATA<7:0> data pins. In the case of the read cycle, the LXT6251A drives the DATA<7:0> data pins.

When a multiplexed data/address bus is used, the falling edge of the AS input latches the address provided on A<8:0>. If the address and data are not multiplexed the AS pin should be tied High.

Timing diagrams for the Intel interface can be found in [Figure 18](#) and [Figure 19](#) starting on [page 47](#).

8.1.2 Motorola Interface

The Motorola interface is indicated by driving the MCUTYPE input pin High. In this mode the $\overline{\text{WR}}/\text{RW}$ input pin is used as a read/write-bar ($\overline{\text{RW}}$) and the $\overline{\text{RD}}/\text{E}$ input pin as enable clock (E).

A read cycle is indicated to the LXT6251A by the microprocessor forcing a High on the $\overline{\text{RW}}$ pin.

A write cycle is indicated to the LXT6251A by the microprocessor forcing a Low on the $\overline{\text{RW}}$ pin.

Both cycles are initiated by a Low on the E input. The E input is connected to the E output from the Motorola microprocessor and is typically a 50% duty cycle waveform with a frequency derived from the microprocessor clock.

Both cycles require the $\overline{\text{CS}}$ pin to be Low and the microprocessor to drive the A<8:0> address pins. In the case of the write cycle, the microprocessor is also required to drive the DATA<7:0> data pins. In the case of the read cycle, the LXT6251A drives the DATA<7:0> data pins.

When a multiplexed data/address bus is used, the falling edge of the AS input latches the address provided on A<8:0>. If the address and data are not multiplexed the AS pin should be tied High.

Timing diagrams for the Intel interface can be found in [Figure 18](#) and [Figure 19](#) starting on page [page 47](#).

8.2 Interrupt Handling

There are 21 tributaries that are each capable of generating 13 alarms. Any one of these alarms (if enabled) can cause the device interrupt pin to become active.

Each tributary has three registers associated with it:

- Interrupt source: These registers identify the source of the interrupt(s).
- Alarm status: These registers provide the current status of alarm monitoring hardware processes.
- Interrupt Enable: These registers enable interrupt sources to affect the state of the $\overline{\text{INT}}$ pin.

8.2.1 Interrupt Sources

There are three types of interrupt sources:

- Status alarm changes: Any time a status alarm changes state, an interrupt bit is set. For example, the LXT6251A monitors the incoming V5 RDI bit. A hardware process monitors this bit for changes and sets bit 3 in “TRIB_INT—Tributary Interrupt (x1-x0H)” on [page 61](#) when the change persists for 5 frames.
- Event Alarms: Any time a momentary event alarm occurs, an interrupt bit is set. For example, the LXT6251A monitors the incoming V5 byte for a change in its REI bit from a ‘0’ to a ‘1’. Such an event will SET bit 5 in interrupt register x0H.
- Counter overflows: The LXT6251A monitors the incoming V5 to see if its REI bit is set. Each multiframe with the REI bit set causes an REI counter to be incremented. If the counter overflows, bit 4 of interrupt register x0H is set.

8.2.1.1 Interrupt Identification

There are four registers used to identify the source of an interrupt. The Global Interrupt Source register provides three bits to identify tributaries 1-8, 9-14, or 15-21. After the group is determined, there are three associated Tributary ID registers to indicate the tributary which caused the alarm.

8.2.2 Interrupt Enables

In order for an interrupt source to affect the state of the $\overline{\text{INT}}$ output pin, its associated interrupt enable bit must be set. The setting (whether it is 0 or 1) of the interrupt enables does not affect the updating of the interrupt, status, overhead byte or counter registers.

Assuming the interrupt enable for a particular interrupt source is SET and the interrupt source is active, the $\overline{\text{INT}}$ output pin will be activated.

For example, when a tributary incurs a Signal Label Mismatch (SLM), if the interrupt is enabled, the `SlmAlm` bit in the interrupt register will be set causing the device interrupt pin to become active. The microprocessor would then read the tributary interrupt registers `00DH–00FH` to identify the tributary in alarm. Next the tributary IRQ registers `x0H` & `x1H` would be read to identify the alarm. Finally, the status register `x2H` or `x3H` is read to determine the current alarm state.

A read of the status register is usually the event that causes the interrupt bits to be cleared (active bits in registers `x0H` & `x1H`). However, for Non-persistent events and counter overflow alarms a read of the interrupt register (`x0H` or `x1H`) is all that is required. In fact, the primary difference between each of interrupt types is the way their respective interrupt bits are *cleared*.

8.2.3 Interrupt Clearing

- Status Alarm interrupt sources have their interrupt bits cleared when their status register is read. For example, the interrupt due to a change in the incoming V5 RDI (bit 3 of interrupt register `x0H`) is cleared when status register `x2H` is read. All of these alarm types have associated status bits.
- Event alarm interrupt sources have their interrupt bits cleared when their interrupt register is read. For example, the interrupt due to a change in the incoming V5 REI (bit 5 of interrupt register `x0H`) from a '0' to a '1' is cleared when register `x0H` is read. None of these alarm types have associated status bits.
- Interrupt sources due to counter overflows have their interrupt bits cleared when their interrupt register is read. See below for description of counter access.

8.2.4 UpdateEn Configuration Bit

The LXT6251A provides an `UpDateEn` signal within “[INT_CONF—Interrupt Configuration Register \(00BH\)](#)” on page 59 to help avoid the problem with an asynchronous microprocessor interface with respect to the system data clock. With an asynchronous interface, it is possible, though very rare, that a status register change could fail to set its associated interrupt register because of the finite time taken to clear the interrupt registers after a status read. The time is three byte clock cycles which is enough to provide a small window after each status read when alarms detected will not cause an interrupt. This situation as described may be acceptable and will exist when the `UpDateEn` bit is set to '0'.

If the `UpdateEn` signal is set to '1', this problem is avoided by freezing both the status and interrupt registers whenever any interrupt bit within a register is set.

We encourage programmers to set the `UpdateEn` bit to '1' during the interrupt service routine to avoid missing alarm information. The `UpdateEn` bit can be set to '0' after the routine has completed.

8.3 Register Address Map

The registers within the LXT6251A provide access for configuration, alarm monitoring and control of the chip. [Table 17](#) shows the LXT6251A register address map. The registers are listed by ascending address in the table.

Nine address bits are used to access the LXT6251A register (512 byte address space). Global registers occupy memory space from 000H to 00FH, and from 160H and above. Registers pertaining to the individual TU tributaries are accessed from memory locations 010H through 15FH. The upper 5 address bits identify the tributary (1-21) and the lower 4 address bits identify the register for a particular tributary. All tributary configuration, status and interrupt registers are identified within this 4 bit address space. The nomenclature used when referring to tributary addresses is provided in the *Register Notations and Definitions* section.

8.3.1 Counter Access

There are two performance counters associated with each receive tributary. Both counters contain at least 11 bits of data and therefore are accessed by reading two adjacent 8 bit register addresses. Counters are accessed by first buffering their contents and then reading the buffer. Each counter value is buffered by writing to either register of the counter, then reading both counter addresses after a wait of at least three clock cycles of the byte clock (6.48 MHz or 19.44 MHz).

For example, to read tributary 21's Low Order Path REI counter in STM-0, a write to register 159H (15 is a hex value = 21 in decimal) is required. After 0.5uS (3 STM-0 clock cycles), the contents of the buffer can now be read by reading registers 158H & 159H (in either order).

8.3.2 Register Notations and Definitions

The following notations and definitions are used in the register descriptions.

RO	Read Only. Unless otherwise stated in the register description, writes have no affect
WO	Write Only. Reads return undefined values.
R/W	Read/Write. A register (or bit) with this attribute can be read and written.
Reserved Bits	Some of the registers contain <i>reserved</i> bits. Software must deal correctly with reserved fields. For reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. In some cases, software must program reserved bit positions to a particular value. This value is defined in the individual bit descriptions.

Default	When the LXT6251A is reset, it sets its registers to predetermined default states. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of software to properly determine the operating parameters, and optional system features that are applicable, and to program the LXT6251A registers accordingly.
Default = X	Undefined
Tributary Register Addressing	The first nibble of the tributary register address (address bits <3:0>) represents a specific register in a given tributary. The upper 5 bits of the address (bits <8:4>) identify the tributary and is represented by the letter 'x'. For example, xCH refers to the CH register in tributary x. The x is the Tributary identifier with valid values of 1H to 15H (1 to 21 decimal). Thus, 14AH refers to tributary 20's K4 Status Register.

Table 17. Register Address Map

Address	Mnemonic	Register Name	Type	Page #
Global Configuration Registers				
000H	GLOB_CONF	Global Configuration	R/W	page 55
001–003H	TADD_CONF	Transmit Address Configuration	R/W	page 56
008H	J2_MRST	J2 Memory Reset	WO	page 57
005–009H	—	Reserved	—	
00AH	CHIP_ID	Chip Identification	RO	page 59
00BH	INT_CONF	Interrupt Configuration	R/W	page 59
00CH	GLOB_INTS	Global Interrupt Source	RO	page 60
00D–00FH	TRIB_ISRC	Tributary Interrupt Source Identification	RO	page 60
TU Tributary Registers (x=1–15H and represents each of the 21 tributary register sets)				
x0–x1H	TRIB_INT	Tributary Interrupt	RO	page 61
x2–x3H	TRIB_STA	Tributary Status	RO	page 63
x4–x5H	TRIB_INTE	Tributary Interrupt Enable	R/W	page 62
x6–x7H	BIP2_ERRCNT	BIP2 Error Counter	RO	page 63
x8–x9H	REI_CNT	Remote Error Indication Counter	RO	page 64
xAH	K4_STA	K4 Status	RO	page 64
xBH	V5_STA	V5 Status	RO	page 64
xCH	J2_ESDATA	J2 Expected String Data	R/W	page 58
xDH	ERRI_CONF	Error Insert Configuration	R/W	page 58
xEH	SIGLA_SET	Signal Label Set	R/W	page 57
xFH	J2_TSDATA	J2 Transmit String Data	R/W	page 58

Table 17. Register Address Map

Address	Mnemonic	Register Name	Type	Page #
Global Configuration Registers				
160H	—	Reserved	—	
161–175H	TU_TS_CONF	TU Time Slot Configuration (21 registers representing Port 1 to Port 21)	R/W	page 57
176–1FFH	—	Reserved	—	

8.4 Configuration Registers

The registers described in this section are related to global configuration. The global address space includes 000H through 00FH, as well as 161H through 175H.

8.4.1 GLOB_CONF—Global Configuration (000H)

This register configures the high level operational characteristics of the chip.

Bit	Name	Label	Type	Default
7	Reserved			
6	TxK4En	This signal enables the use of the K4 Enhanced RDI in the transmit direction. 0 = Force K4 ERDI to 0 1 = Drive K4 ERDI with input RAP alarm signals.	R/W	0
5	MultiFrmSel	Selects the multiframe indicator used. 0 = Use DTBH4EN and MTBH4EN signals 1 = Use DTBJOJ1EN and MTBJOJ1EN signals (OHT must be configured likewise).	R/W	0
4	TBTristate	This signal defaults to '1', forcing the Transmit side Telecom bus timing signal pins to tri-state. This bit should be set to '0' <i>after</i> both this chip and other chips sharing the telecom bus are configured to avoid any device from trashing the bus before configuration is complete. 0 = Telecom Bus outputs enabled 1 = Telecom Bus outputs in Tri-state	R/W	1
3	BIPMode	Sets the BIP Error counting mode for all receive tributary LPT blocks. 0 = Block Error Counting 1 = BIP Error Counting	R/W	0

Bit	Name	Label	Type	Default
2	UNEQMode	Sets the form of the unequipped signal generated by all transmit tributary LUG blocks, as defined in G707, section 6.2.4.2. 0 = Unequipped 1 = Supervisory Unequipped	R/W	0
1	OpMode	Master configuration for the entire chip's operation, either Terminal or ADM. 0 = Terminal Configuration 1 = Add/Drop Configuration	R/W	0
0	StmMode	Selects the speed of operation and the Telecom bus I/O format. This is a read-only register; the value is set by pin 32. 0 = STM-0, 7 by TUG-2 output 1 = STM-1, TUG-3 output	R	X

8.4.2 TADD_CONF—Transmit Add Configuration (003–001H)

003H=Bits<23:16>, 002H=Bits<15:8>, 001H=Bits<7:0> (Byte access only)

This set of registers configures the transmit side added tributary channels in an Add/Drop mode configuration (register 000H bit 1, set to '1'). All bits in these registers that are set to '1' will add tributary data from the E1 input source, all bits set to '0' will pass through the tributary data received on the Telecom bus.

This register is ignored if the chip is configured as a terminal.

Bit	Name	Description	Type	Default
23:21	Reserved			
20	Trib21 (7,3)	1 = Add; 0 = Pass through.	R/W	0
19	Trib20 (6,3)	1 = Add; 0 = Pass through.	R/W	0
18	Trib19 (5,3)	1 = Add; 0 = Pass through.	R/W	0
17	Trib18 (4,3)	1 = Add; 0 = Pass through.	R/W	0
16	Trib17 (3,3)	1 = Add; 0 = Pass through.	R/W	0
15	Trib16 (2,3)	1 = Add; 0 = Pass through.	R/W	0
14	Trib15 (1,3)	1 = Add; 0 = Pass through.	R/W	0
13	Trib14 (7,2)	1 = Add; 0 = Pass through.	R/W	0
12	Trib13 (6,2)	1 = Add; 0 = Pass through.	R/W	0
11	Trib12 (5,2)	1 = Add; 0 = Pass through.	R/W	0
10	Trib11 (4,2)	1 = Add; 0 = Pass through.	R/W	0
9	Trib10 (3,2)	1 = Add; 0 = Pass through.	R/W	0
8	Trib9 (2,2)	1 = Add; 0 = Pass through.	R/W	0
7	Trib8 (1,2)	1 = Add; 0 = Pass through.	R/W	0
6	Trib7 (7,1)	1 = Add; 0 = Pass through.	R/W	0
5	Trib6 (6,1)	1 = Add; 0 = Pass through.	R/W	0
4	Trib5 (5,1)	1 = Add; 0 = Pass through.	R/W	0
3	Trib4 (4,1)	1 = Add; 0 = Pass through.	R/W	0

Bit	Name	Description	Type	Default
2	Trib3 (3,1)	1 = Add; 0 = Pass through.	R/W	0
1	Trib2 (2,1)	1 = Add; 0 = Pass through.	R/W	0
0	Trib1 (1,1)	1 = Add; 0 = Pass through.	R/W	0

8.4.3 TU_TS_CONF—TU Time Slot Configuration (161–175H)

21 Registers; 161H (Port 1) through 175H (Port 21)

These registers set the TU Time slot for each of the 21 Transmit and Receive I/O ports. The register should only be used in the Add/Drop configuration.

Bit	Name	Description	Type	Default
7:5	Reserved	Unused		
4:0	TimeSlot	Selects which TU Timeslot is associated with Port X. Valid value range is 1 through 21. The default value corresponds to the port number. For example, register 168h (configuration for port 8) is associated with TU 8 by default and so its default value will be '01000'. Refer to "Port Mapping Configuration" for a discussion about these 21 registers and a table of the default values.	R/W	*

8.4.4 SIGLA_SET—Signal Label Setting (xEH)

$x=1-15H$

This register sets the signal label value in outgoing V5 byte. The register also sets the RFI bit.

Bit	Name	Label	Type	Default
7:5	Reserved	Unused		
4	RFISet	Set the value of V5 RFI bit in V5.	R/W	0
3:1	SigLabelSet	Set the values of the three Signal Label bits in V5. The only valid values that indicate modes supported by the chip are 000, 001 and 010. Setting the channel to Unequipped will cause the mapper to generate an unequipped VC-12 toward the SDH network. The type of unequipped signal is controlled from the Global Configuration register.	R/W	010
0	Reserved	Unused		

8.4.5 J2_MRST—J2 Memory Reset (008H)

This register is provided as a protection measure when accessing the J2 memories. During configuration of a tributary's J2 memory, a global pointer is used to step through the internal memory locations. This pointer is incremented with each write to the address of the string data. Writing to this register location resets this pointer to ensure the proper alignment of the microprocessor and the internal memory. It will take four system clock cycles (6.48MHz/19.44MHz) for the reset to complete. Under normal use, the 16 reads or writes necessary to access a J2 word will reset this global pointer back to 0 for the next tributary.

Bit	Name	Description	Type	Default
7:0	J2MemReset	No specific value. A write resets the memory pointer.	WO	00H

8.4.6 J2_ESDATA—J2 Expected String Data (xCH)

$x=1-15H$

This register is used to access the J2 memory for this receive channel. Successive reads or writes to this register will increment a global counter that increments the address 0 through 15. A write to global register 004H resets this counter to 0. This is not needed if all 16 bytes are always read or written to J2 memory.

Bit	Name	Description	Type	Default
7:0	ExpcJ2StrgData	Bits <7:0> correspond to data <7:0>, respectively.	R/W	00H

8.4.7 J2_TSDATA—J2 Transmit String Data (xFH)

$x=1-15H$

This register is used to access the J2 memory for this transmit channel. Successive reads or writes to this register will increment a global counter that increments the address 0 through 15. A write to global register 004H resets this counter to 0. This is not needed if all 16 bytes are always read or written to J2 memory.

Bit	Name	Description	Type	Default
7:0	XmtJ2StrgData	Bits <7:0> correspond to data <7:0>, respectively.	R/W	00H

8.4.8 ERRI_CONF—Error Insert Configuration (xDH)

$x=1-15H$

Configures normal operation diagnostic functionality. These registers should be set to their default configuration unless the unit is in diagnostic mode and is not transmitting valid traffic.

Bit	Name	Description	Type	Default
7	Reserved			
6	XmtJ2Access	1 = Allows the microprocessor to access the transmit J2 RAM via register xFH. Sixteen consecutive writes to xFH will fill the RAM. The address is internally incremented after each write. A write to register 004H resets this global address counter. Also forces the J2 output byte to 00H when globally configured for standard unequipped, or 01H for supervisory unequipped. 0 = Disable	R/W	1
5	XmtHpaAisFrc	Force TU-AIS generation towards SDH network. 1 = Force 0 = Disable	R/W	0

Bit	Name	Description	Type	Default
4	XmtLptRdiEn	Enable/Disable automatic hardware updates of V5 RDI bit. Used when the microprocessor needs direct control of RDI. 1 = Enable 0 = Disable	R/W	1
3	XmtLptRdiFrc	Force active status of V5 RDI. Also causes K4 ERDI bits to be set to '111'. 1 = Force 0 = Disable	R/W	0
2	XmtLptReiEn	Enable/Disable automatic hardware updates of V5 REI bit. Used when the microprocessor needs direct control of REI. 1 = Enable 0 = Disable	R/W	1
1	XmtLptReiFrc	Force active status of V5 REI. 1 = Force 0 = Disable	R/W	0
0	InvBip	Enable/Disable the insertion of BIP-2 bit errors. Used to test receiver functions downstream. When set, both BIP values are inverted from their calculated value. 1 = Enable 0 = Disable	R/W	0

8.4.9 INT_CONF—Interrupt Configuration Register (00BH)

Bit	Name	Description	Type	Default
7:4	Reserved	Unused		
3	UpdateEn	Controls the tributary Status register update mechanism. When set to '1', an interrupt in the IRQ register associated with the status register will freeze both registers until the status register has been read. A '0' allows updates to the status registers every multiframe. 0 = Always update status every multiframe 1 = Disable status update if interrupt alarm	R/W	0
2	LOMIntEn	When set to '1', allows a LOM alarm to activate the $\overline{\text{INT}}$ pin. 0 = Disable $\overline{\text{INT}}$ output pin dependency 1 = Enable $\overline{\text{INT}}$ output pin dependency	R/W	0
1	TBParIntEn	When set to '1', allows a parity error detected on the receive telecom bus to activate the $\overline{\text{INT}}$ pin. 0 = Disable $\overline{\text{INT}}$ output pin dependency 1 = Enable $\overline{\text{INT}}$ output pin dependency	R/W	0
0	MasIntEn	Master Interrupt Enable; disables the $\overline{\text{INT}}$ output from chip. 0 = Disable 1 = Enable	R/W	0

8.4.10 CHIP_ID—Chip Identification Number (00AH)

This register is read-only and is used to identify the version of the Chip.

Bit	Name	Description	Type	Default
7:0	ChipID	Chip Identification < 7:0>	RO	

8.5 Interrupt Registers

8.5.1 GLOB_INTS—Global Interrupt Source (00CH)

The Tributary Alarm Group identifies the tributary group that is in alarm. The microprocessor will require two reads (this and the Tributary ID interrupt register) to determine which tributary is in alarm. Global alarms not associated with tributaries are also in this register.

Bit	Name	Description	Type	Default
7:6	Reserved	Unused		X,X
5	LOMSt	1 = Indicates the H4 multiframe indicator has been lost. The alarm is set when the DTBH4EN signal is constant '0'.	RO	0
4	LOMInt	1 = Indicates the interrupt has been generated by the LOM alarm. The interrupt bit is reset when the register is read.	RO	0
3	TBParInt	1 = indicates a mismatch between the received DTBPAR parity bit and the calculated parity on the DTBDATA byte. The mismatch must occur 15 times in one multiframe for the alarm to be set. The alarm will be reset when the register is read.	RO	0
2	TribGrp3	1 = Indicates Tributaries 17-21 are source of interrupt.	RO	0
1	TribGrp2	1 = Indicates Tributaries 9-16 are source of interrupt	RO	0
0	TribGrp1	1 = Indicates Tributaries 1-8 are source of interrupt	RO	0

8.5.2 TRIB_ISRC—Tributary Interrupt Source Identification (00F–00DH)

00FH=Bits<23:16>, 00EH=Bits<15:8>, 00DH=Bits<7:0> (Byte access only)

This 24-bit register indicate which tributary (or tributaries) has active interrupts. A '1' indicates tributary has an active interrupt.

Bit	Name	Description	Type	Default
23:21	Reserved	Unused		
20	Trib21	1 = Tributary has alarm.	R	
19	Trib20	1 = Tributary has alarm.	R	
18	Trib19	1 = Tributary has alarm.	R	
17	Trib18	1 = Tributary has alarm.	R	
16	Trib17	1 = Tributary has alarm.	R	
15	Trib16	1 = Tributary has alarm.	R	
14	Trib15	1 = Tributary has alarm.	R	
13	Trib14	1 = Tributary has alarm.	R	
12	Trib13	1 = Tributary has alarm.	R	

Bit	Name	Description	Type	Default
11	Trib12	1 = Tributary has alarm.	R	
10	Trib11	1 = Tributary has alarm.	R	
9	Trib10	1 = Tributary has alarm.	R	
8	Trib9	1 = Tributary has alarm.	R	
7	Trib8	1 = Tributary has alarm.	R	
6	Trib7	1 = Tributary has alarm.	R	
5	Trib6	1 = Tributary has alarm.	R	
4	Trib5	1 = Tributary has alarm.	R	
3	Trib4	1 = Tributary has alarm.	R	
2	Trib3	1 = Tributary has alarm.	R	
1	Trib2	1 = Tributary has alarm.	R	
0	Trib1	1 = Tributary has alarm.	R	

8.5.3 TRIB_INT—Tributary Interrupt (x1–x0H)

$x=1-15H$; $x1H=Bits<15:8>$, $x0H=Bits<7:0>$ (Byte access only)

Each tributary has a set of these registers that identify the interrupt source for the tributary. For those alarms that are persistent (i.e. they can be active longer than a multiframe), there are associated status registers in “[TRIB_STA—Tributary Status \(x3–x2H\)](#)” on page 63 which follow the same bit pattern.

These registers are normally updated every multiframe. However if the UpDateEn bit is set to ‘1’ in “[INT_CONF—Interrupt Configuration Register \(00BH\)](#)” on page 59 they will be frozen until the associated status register is read.

Bit	Name	Description	Type	Default
15:13	Reserved	Unused		
12	TuNDF	This alarm indicates the HPA section has received an NDF flag in the V1 pointer.	R	X
11	Tim	This alarm indicates a J2 Trace MisMatch alarm. It is asserted IF the received vs. calculated CRC-7 match (no J2 bit errors), but the received J2 word does not match that stored in RAM. The CRC-7 byte in RAM is not used in the comparison.	R	X
10	Crc7Err	This alarm indicates a bit error has been detected in the J2 word. The alarm is asserted when the received CRC-7 byte does not match the one calculated on the received data. Detection of this alarm will mask the TIM alarm.	R	X
9	TuLop	This alarm indicates the demapper has detected a Loss of Pointer alarm.	R	X
8	TuAis	This alarm indicates the demapper has detected the pointer value is in an AIS condition.	R	X
7	Bip2	This alarm indicates that a BIP error has been detected.	R	X
6	Bip2OvrFlw	This alarm indicates the BIP counter has overflowed. The counter will rollover to 0 and continue counting.	R	X
5	Rei	This alarm indicates the V5 REI bit was set to ‘1’.	R	X

Bit	Name	Description	Type	Default
4	ReiOvrFlw	This alarm indicates the REI counter has overflowed. The counter will rollover to 0 and continue counting.	R	X
3	Rdi	This alarm indicates the V5 RDI bit was set to '1' for five consecutive multiframes.	R	X
2	Rfi	This alarm indicates the V5 RFI bit was set to '1'.	R	X
1	Slm	This alarm indicates that a Signal Label Mismatch has occurred. This alarm is asserted if the Signal Label is detected to be a value other than '000' (Uneq), '001' (Equip, non specific), or '010' (Equip, async) for five consecutive frames. Removal of the alarm also requires five consecutive frames.	R	X
0	UnEqp	This alarm indicates that the Signal Label in V5 is detected as '000' for five consecutive frames. Removal of the alarm also requires five consecutive frames.	R	X

8.5.4 TRIB_INTE—Tributary Interrupt Enable (x5–x4H)

$x=1-15H$; $x5H=Bits<15:8>$, $x4H=Bits<7:0>$ (Byte access only)

Each tributary has a set of these registers that can be used to enable an interrupt source for a particular tributary. The Reset default is not enabled ('0').

Bit	Name	Description	Type	Default
15:14	Reserved	Unused		
13	RxJ2Access	1 = Allows the microprocessor to control access to the expected J2 RAM via register xCH. Sixteen consecutive writes to xCH will fill the RAM. The address is internally incremented after each write. A write to register 004h will reset this global counter. Also disables both the TIM and CRC7 alarm associated with J2 so no alarms or RDI feedback is generated during configuration of the expected J2 string.	R/W	1
12	TuNDFIntEn	1 = Enable 0 = Disable	R/W	0
11	TimIntEn	1 = Enable 0 = Disable	R/W	0
10	Crc7ErrIntEn	1 = Enable 0 = Disable	R/W	0
9	TuLopIntEn	1 = Enable 0 = Disable	R/W	0
8	TuAisIntEn	1 = Enable 0 = Disable	R/W	0
7	Bip2IntEn	1 = Enable 0 = Disable	R/W	0
6	Bip2OvrFlwIntEn	1 = Enable 0 = Disable	R/W	0
5	ReiIntEn	1 = Enable 0 = Disable	R/W	0
4	ReiOvrFlwIntEn	1 = Enable 0 = Disable	R/W	0

Bit	Name	Description	Type	Default
3	RdiIntEn	1 = Enable 0 = Disable	R/W	0
2	RfiIntEn	1 = Enable 0 = Disable	R/W	0
1	SlmIntEn	1 = Enable 0 = Disable	R/W	0
0	UnEqIntEn	1 = Enable 0 = Disable	R/W	0

8.6 Status and Control Registers

8.6.1 TRIB_STA—Tributary Status (x3–x2H)

$x=1-15H$; $x3H=Bits<15:8>$, $x2H=Bits<7:0>$ (Byte access only)

Each tributary has a set of these registers giving the present status of each alarm source for a particular tributary. The Rdi, Rfi, Slm & UnEq bits in interrupt register $x0H$ are cleared when $x2H$ is read. The TIM, TimCrc7, TuLop & TuAis bits in $x1H$ are cleared when $x3H$ is read. These registers mirror the interrupt registers but do not contain status of non-persistent alarm events such as the BIP-2 error event.

These registers are normally updated every multiframe. However if the UpDateEn bit is set to '1' in "INT_CONF—Interrupt Configuration Register (00BH)" on page 59 they will be frozen until the register is read.

Bit	Name	Description	Type	Default
15:12	Reserved	Unused		
11	TimSt		RO	X
10	Crc7ErrSt		RO	X
9	TuLopSt		RO	X
8	TuAisSt		RO	X
7:4	Reserved	Unused		
3	RdiSt		RO	X
2	RfiSt		RO	X
1	SlmSt		RO	X
0	UnEqSt		RO	X

8.6.2 BIP2_ERRCNT—BIP2 Error Counter (x7–x6H)

$x=1-15H$; $x7H=Bits<15:8>$, $x6H=Bits<7:0>$ (Byte access only)

This counter increments each time a BIP error event in the Low Order Path section is detected. To access the count, the microprocessor must provide a Write command to the MSB address bit of register x6H at least 3 byte clock periods (0.5us in STM-0) before the two Read commands. The Write command clears the counter after buffering it.

Bit	Name	Description	Type	Default
15:12	Reserved	Unused		
11:0	BipCnt	Bits<11:8> are the most significant byte of the BIP error event counter. Bits<7:0> are the least significant bits.	RO	X

8.6.3 REI_CNT—Remote Error Indication (REI) Counter (x9–x8H)

$x=1-15H$; $x9H=Bits<15:8>$, $x8H=Bits<7:0>$ (Byte access only)

This counter increments each frame in which the receive V5 REI bit is set. To access the count, the microprocessor must provide a Write command to the MSB address bit of register x9H at least three byte clock periods (0.5us in STM-0) before the two Read commands. The Write command clears the counter after buffering it.

Bit	Name	Description	Type	Default
15:11	Reserved	Unused		
10:0	LptReiCnt	Bits<10:8> are the most significant bits of the Low Order Path OverHead REI error event counter. Bits<7:0> are the least significant bits.	RO	X

8.6.4 K4_STA—K4 Status (xAH)

$x=1-15H$

The K4 byte provides an Enhanced RDI that can be retrieved via a read of this register. This register is updated only if there is a change in the V5 RDI bit and the tributary source supports K4 ERDI.

Bit	Name	Description	Type	Default
7:4	Reserved		RO	0
3:1	Enhanced RDI	K4 ERDI bits.	RO	X
0	Reserved		RO	0

8.6.5 V5_STA—V5 Status Register (xBH)

$x=1-15H$

The V5 status register is provided for raw access to the received V5 byte (see Figure 4). There is no alarm or INT generation directly associated with this register. The value in this register changes every multiframe (500uS).

Bit	Name	Description	Type	Default
7:6	BIP2	V5 BIP-2 bits	RO	X
5	REI	V5 REI bit	RO	X
4	RFI	V5 RFI bit	RO	X
3:1	SigLabel	V5 Signal Label bits	RO	X
0	RDI	V5 RDI bit	RO	X

9.0 Testability Modes

The LXT6251A 21E1 Mapper/Demapper provides a method for enhancing testability: IEEE1149.1 Boundary Scan (JTAG) is used for testing of the interconnect.

9.1 IEEE 1149.1 Boundary Scan Description

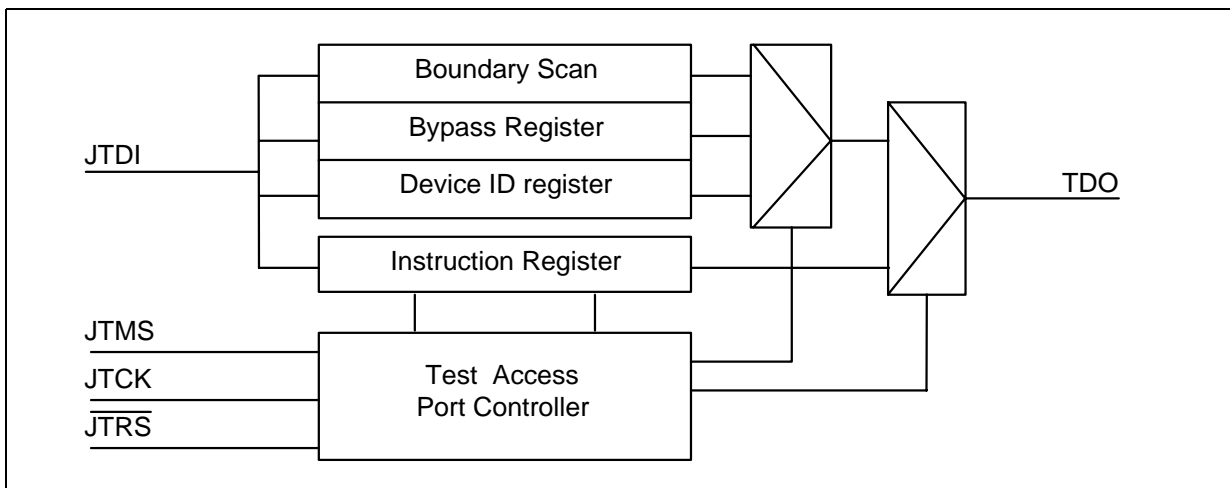
The boundary scan circuitry allows the user to test the interconnection between the LXT6251A and the circuit board.

The boundary scan port consists of 5 pins as shown in [Table 18](#). The heart of the scan circuitry is the Test Access Port controller (TAP). The TAP controller is a 16 state machine that controls the function of the boundary scan circuitry. Inputs of the TAP controller are the Test Mode Select (JTMS) and the Test Clock (JTCK) signals.

Data and instructions are shifted into the LXT6251A through the Test Data In pin (JTDI). Data and instructions are shifted out through the Test Data Out pin (JTDO). The asynchronous reset pin (JTRS) resets the boundary scan circuitry.

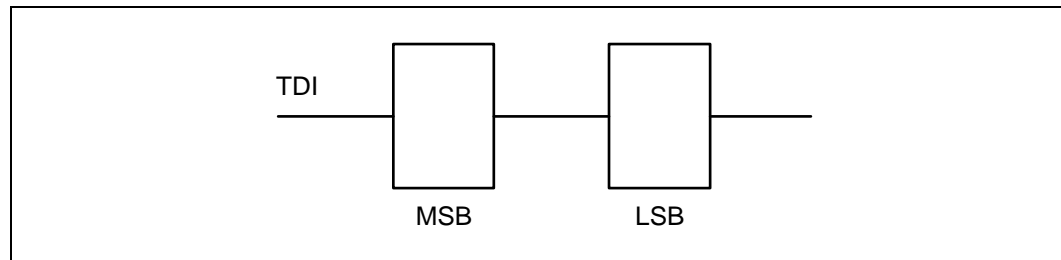
Table 18. JTAG Pin Description

Pin #	Name	I/O	Function
152	JTMS_P	I	Test Mode Select: Determines state of TAP Controller. Pull up 48k
153	JTCK_P	I	Test Clock: Clock for all boundary scan circuitry
151	JTRS_P	I	Test Reset: Active low asynchronous signal that causes the TAP controller to reset. Pull down 35k
150	JTDI_P	I	Test Data In: Input signal used to shift in instructions and data. Pull up 48k
149	JTDO_P	O	Test data Out: Output signal used to shift out instructions and data.

Figure 20. Test Access Port


9.1.1 Instruction Register and Definitions

The LXT6251A supports the following instructions IEEE1149.1: EXTEST, SAMPLE/PRELOAD, BYPASS and IDCODE. Instructions are shifted into the instruction register during the SHIFT-IR state, and become active upon exiting the UPDATE-IR state. The instruction register definition is shown in the following figure.

Figure 21. Instruction Register


9.1.1.1 EXTEST ('b00)

This instruction allows the testing of circuitry external to the package, typically the board interconnect, to be tested. While the instruction is active, the boundary scan register is connected between TDI and TDO, for any data shifts. Boundary scan cells at the output pins are used to apply test stimuli, while those at input pins capture test results. Signals present on input pins are loaded into the BSR inputs cells on the rising edge of JTCK during CAPTURE-DR state. BSR contents are shifted one bit location on each rising edge of JTCK during the SHIFT-DR state. BSR output cell contents appear at output pins on the falling edge of JTCK during the UPDATE-IR state.

One test cycle is:

1. A test stimuli pattern is shifted into the BSR during SHIFT-DR state.
2. This pattern is applied to output pins during the UPDATE-DR state.
3. The response is loaded into the input BSR cells during the CAPTURE-DR state.

4. The results are shifted out and next test stimuli shifted into the BSR.

9.1.1.2 SAMPLE/PRELOAD ('b01)

This instruction allows a snapshot of the normal operation of the LXT6251A. The boundary scan register is connected between the TDI and TDO for any data shifts while this instruction is active. All BSR cells capture data present at their inputs on the rising edge of JTCK during the CAPTURE-DR state. No action is taken during the UPDATE-DR state.

9.1.1.3 BYPASS ('b11)

This instruction allows a device to be effectively removed from the scan chain, by inserting a one-bit shift register stage between TDI and TDO during data shifts. When the instruction is active, the test logic has no impact upon the system logic performing its system function. When selected, the shift-register is set to a logic zero on the rising edge of the JTCK during the CAPTURE-DR state.

9.1.1.4 IDCODE ('b10)

This instruction allows the reading of component types via the scan chain. During this instruction, the 32-bit Device Identification Register (ID-Register) is placed between TDI and TDO. The ID Register captures a fixed value of ('h 1186B0FD) on the rising edge of JTCK during the CAPTURE-DR state. The Device Identification Register contains the following information: Manufacturer ID: 'd126; Design Part Number: 'd 6251; Design Version Number: 'd1.

9.1.2 Boundary Scan Register

The Boundary Scan Register is a 165 bit shift register, made of four styles of shift-register cells with two sub-types. According to the Boundary Scan Description Language (BSDL):

JTAG_BSRINBOTH,
JTAG_BSROUTBOTH and
JTAG_BSRCTL are designated TYPE2, JTAG_BSRINCLKOBS is designated TYPE1.

Description

- Length: 165 BSR cells
- JTCK_P Jtag Test Clock
- JTDI_P Jtag Test Data Input
- JTDO_C Jtag Test Data Output Control enable
- JTDO_P Jtag Test Data Output
- JTMS_P Jtag Test Mode Select
- JTRS_P Jtag Test Reset

Figure 22. Boundary Scan Cells

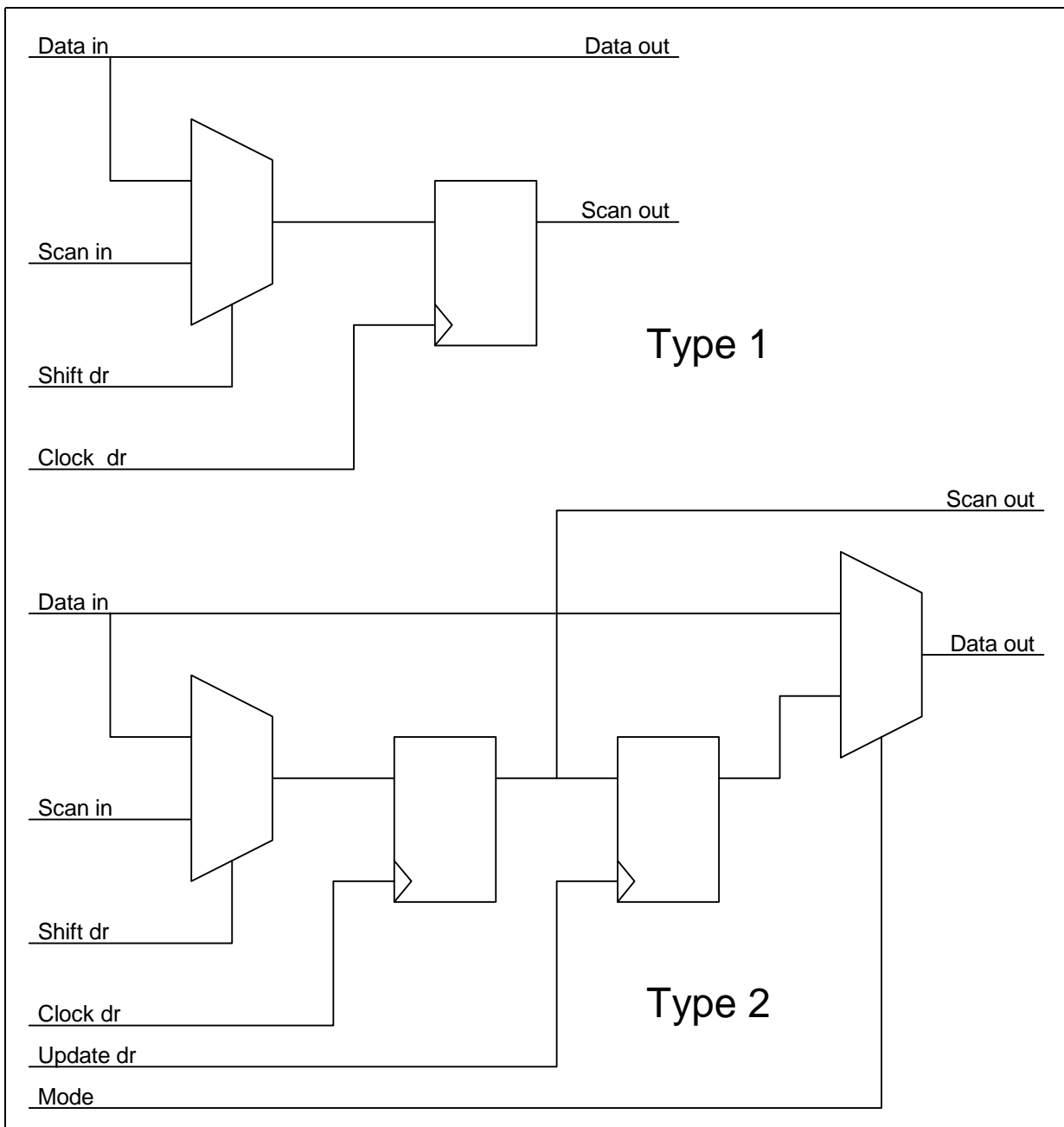


Table 19. JTAG Scan Chain

PIN Name	Type	Numbering in Scan chain	Type of BSR Cell	Associated Control enable
OEN	Data	1	JTAG_BSRINBOTH	
OEN_c	Enable	2	JTAG_BSRCTL	
SCANEN	Data	3	JTAG_BSRINBOTH	
DtbDATA<7>	Data	4	JTAG_BSRINBOTH	
DtbDATA<6>	Data	5	JTAG_BSRINBOTH	
DtbDATA<5>	Data	6	JTAG_BSRINBOTH	
DtbDATA<4>	Data	7	JTAG_BSRINBOTH	
DtbDATA<3>	Data	8	JTAG_BSRINBOTH	
DtbDATA<2>	Data	9	JTAG_BSRINBOTH	
DtbDATA<1>	Data	10	JTAG_BSRINBOTH	
DtbDATA<0>	Data	11	JTAG_BSRINBOTH	
DtbPAR	Data	12	JTAG_BSRINBOTH	
DtbYck	Clock	13	JTAG_BSRINCLKOBS	
DtbJ0J1en	Data	14	JTAG_BSRINBOTH	
DtbTUGen	Data	15	JTAG_BSRINBOTH	
PTTUGA	Data	16	JTAG_BSRINBOTH	
PTTUGB	Data	17	JTAG_BSRINBOTH	
PTSOH	Data	18	JTAG_BSRINBOTH	
DtbPAYEN	Data	19	JTAG_BSRINBOTH	
DtbH4en	Data	20	JTAG_BSRINBOTH	
MtbH4en/I	Data	21	JTAG_BSRINBOTH	
MtbH4en/O	Data	22	JTAG_BSROUTBOTH	MtbTime_c
MtbPAYEN/I	Data	23	JTAG_BSRINBOTH	
MtbPAYEN/O	Data	24	JTAG_BSROUTBOTH	MtbTime_c
MtbTUGen	Data	25	JTAG_BSRINBOTH	
MtbJ0J1en/I	Data	26	JTAG_BSRINBOTH	
MtbJ0J1en/O	Data	27	JTAG_BSROUTBOTH	MtbTime_c
MtbTime_c	Enable	28	JTAG_BSRCTL	
MtbYck	Clock	29	JTAG_BSRINCLKOBS	
MtbPAR	Data	30	JTAG_BSROUTBOTH	MtbDATA_c
MtbDATA<0>	Data	31	JTAG_BSROUTBOTH	MtbDATA_c
MtbDATA<1>	Data	32	JTAG_BSROUTBOTH	MtbDATA_c
MtbDATA<2>	Data	33	JTAG_BSROUTBOTH	MtbDATA_c
MtbDATA<3>	Data	34	JTAG_BSROUTBOTH	MtbDATA_c
MtbDATA<4>	Data	35	JTAG_BSROUTBOTH	MtbDATA_c
MtbDATA<5>	Data	36	JTAG_BSROUTBOTH	MtbDATA_c

Table 19. JTAG Scan Chain (Continued)

PIN Name	Type	Numbering in Scan chain	Type of BSR Cell	Associated Control enable
MtbDATA<6>	Data	37	JTAG_BSRROUTBOTH	MtbDATA_c
MtbDATA<7>	Data	38	JTAG_BSRROUTBOTH	MtbDATA_c
MtbDATA_c	Enable	39	JTAG_BSRCTL	
MtbDOE	Data	40	JTAG_BSRROUTBOTH	OEN_C
DATA/I<7>	Data	41	JTAG_BSRINBOTH	
DATA/O<7>	Data	42	JTAG_BSRROUTBOTH	D_c
DATA/I<6>	Data	43	JTAG_BSRINBOTH	
DATA/O<6>	Data	44	JTAG_BSRROUTBOTH	D_c
DATA/I<5>	Data	45	JTAG_BSRINBOTH	
DATA/O<5>	Data	46	JTAG_BSRROUTBOTH	D_c
DATA/I<4>	Data	47	JTAG_BSRINBOTH	
DATA/O<4>	Data	48	JTAG_BSRROUTBOTH	D_c
DATA/I<3>	Data	49	JTAG_BSRINBOTH	
DATA/O<3>	Data	50	JTAG_BSRROUTBOTH	D_c
DATA/I<2>	Data	51	JTAG_BSRINBOTH	
DATA/O<2>	Data	52	JTAG_BSRROUTBOTH	D_c
DATA/I<1>	Data	53	JTAG_BSRINBOTH	
DATA/O<1>	Data	54	JTAG_BSRROUTBOTH	D_c
DATA/I<0>	Data	55	JTAG_BSRINBOTH	
DATA/O<0>	Data	56	JTAG_BSRROUTBOTH	D_c
D_c	Enable	57	JTAG_BSRCTL	
A<8>	Data	58	JTAG_BSRINBOTH	
A<7>	Data	59	JTAG_BSRINBOTH	
A<6>	Data	60	JTAG_BSRINBOTH	
A<5>	Data	61	JTAG_BSRINBOTH	
A<4>	Data	62	JTAG_BSRINBOTH	
A<3>	Data	63	JTAG_BSRINBOTH	
A<2>	Data	64	JTAG_BSRINBOTH	
A<1>	Data	65	JTAG_BSRINBOTH	
A<0>	Data	66	JTAG_BSRINBOTH	
CSB	Data	67	JTAG_BSRINBOTH	
AS	Data	68	JTAG_BSRINBOTH	
WR/RW	Clock	69	JTAG_BSRINCLKOBS	
RD/E	Data	70	JTAG_BSRINBOTH	
INT	Data	71	JTAG_BSRROUTBOTH	OEN_c
MCUTYPE	Data	72	JTAG_BSRINBOTH	
STMMODE	Data	73	JTAG_BSRINBOTH	

Table 19. JTAG Scan Chain (Continued)

PIN Name	Type	Numbering in Scan chain	Type of BSR Cell	Associated Control enable
RST	Data	74	JTAG_BSRINBOTH	
MRAPDATA	Data	75	JTAG_BSRINBOTH	
MRAPCLK	Data	76	JTAG_BSRINBOTH	
MRAPFRM	Data	77	JTAG_BSRINBOTH	
DSAPFRM	Data	78	JTAG_BSROUTBOTH	OEN_c
DSAPCLK	Data	79	JTAG_BSROUTBOTH	OEN_c
DSAPDATA	Data	80	JTAG_BSROUTBOTH	OEN_c
DTC0	Data	81	JTAG_BSROUTBOTH	OEN_c
DTD0	Data	82	JTAG_BSROUTBOTH	OEN_c
MTD0	Data	83	JTAG_BSRINBOTH	
MTC0	Data	84	JTAG_BSRINBOTH	
MTC1	Data	85	JTAG_BSRINBOTH	
MTD1	Data	86	JTAG_BSRINBOTH	
DTD1	Data	87	JTAG_BSROUTBOTH	OEN_c
DTC1	Data	88	JTAG_BSROUTBOTH	OEN_c
DTC2	Data	89	JTAG_BSROUTBOTH	OEN_c
DTD2	Data	90	JTAG_BSROUTBOTH	OEN_c
MTD2	Data	91	JTAG_BSRINBOTH	
MTC2	Data	92	JTAG_BSRINBOTH	
MTC3	Data	93	JTAG_BSRINBOTH	
MTD3	Data	94	JTAG_BSRINBOTH	
DTD3	Data	95	JTAG_BSROUTBOTH	OEN_c
DTC3	Data	96	JTAG_BSROUTBOTH	OEN_c
DTC4	Data	97	JTAG_BSROUTBOTH	OEN_c
DTD4	Data	98	JTAG_BSROUTBOTH	OEN_c
MTD4	Data	99	JTAG_BSRINBOTH	
MTC4	Data	100	JTAG_BSRINBOTH	
MTC5	Data	101	JTAG_BSRINBOTH	
MTD5	Data	102	JTAG_BSRINBOTH	
DTD5	Data	103	JTAG_BSROUTBOTH	OEN_c
DTC5	Data	104	JTAG_BSROUTBOTH	OEN_c
DTC6	Data	105	JTAG_BSROUTBOTH	OEN_c
DTD6	Data	106	JTAG_BSROUTBOTH	OEN_c
MTD6	Data	107	JTAG_BSRINBOTH	
MTC6	Data	108	JTAG_BSRINBOTH	
MTC7	Data	109	JTAG_BSRINBOTH	
MTD7	Data	110	JTAG_BSRINBOTH	

Table 19. JTAG Scan Chain (Continued)

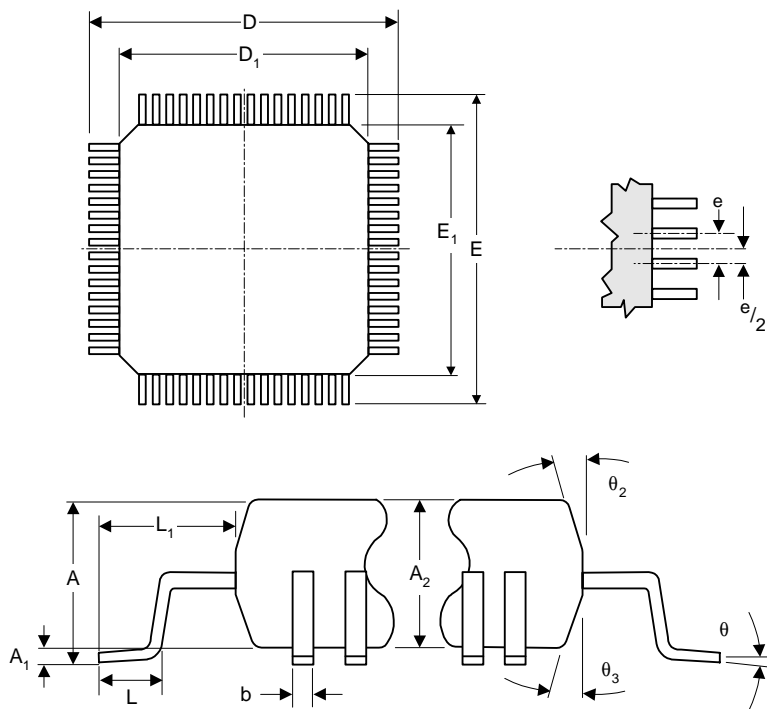
PIN Name	Type	Numbering in Scan chain	Type of BSR Cell	Associated Control enable
DTD7	Data	111	JTAG_BSROUTBOTH	OEN_c
DTC7	Data	112	JTAG_BSROUTBOTH	OEN_c
DTC8	Data	113	JTAG_BSROUTBOTH	OEN_c
DTD8	Data	114	JTAG_BSROUTBOTH	OEN_c
MTD8	Data	115	JTAG_BSRINBOTH	
MTC8	Data	116	JTAG_BSRINBOTH	
MTC9	Data	117	JTAG_BSRINBOTH	
MTD9	Data	118	JTAG_BSRINBOTH	
DTD9	Data	119	JTAG_BSROUTBOTH	OEN_c
DTC9	Data	120	JTAG_BSROUTBOTH	OEN_c
DTC10	Data	121	JTAG_BSROUTBOTH	OEN_c
DTD10	Data	122	JTAG_BSROUTBOTH	OEN_c
MTD10	Data	123	JTAG_BSRINBOTH	
MTC10	Data	124	JTAG_BSRINBOTH	
MTC11	Data	125	JTAG_BSRINBOTH	
MTD11	Data	126	JTAG_BSRINBOTH	
DTD11	Data	127	JTAG_BSROUTBOTH	OEN_c
DTC11	Data	128	JTAG_BSROUTBOTH	OEN_c
DTC12	Data	129	JTAG_BSROUTBOTH	OEN_c
DTD12	Data	130	JTAG_BSROUTBOTH	OEN_c
MTD12	Data	131	JTAG_BSRINBOTH	
MTC12	Data	132	JTAG_BSRINBOTH	
MTC13	Data	133	JTAG_BSRINBOTH	
MTD13	Data	134	JTAG_BSRINBOTH	
DTD13	Data	135	JTAG_BSROUTBOTH	OEN_c
DTC13	Data	136	JTAG_BSROUTBOTH	OEN_c
DTC14	Data	137	JTAG_BSROUTBOTH	OEN_c
DTD14	Data	138	JTAG_BSROUTBOTH	OEN_c
MTD14	Data	139	JTAG_BSRINBOTH	
MTC14	Data	140	JTAG_BSRINBOTH	
MTC15	Data	141	JTAG_BSRINBOTH	
MTD15	Data	142	JTAG_BSRINBOTH	
DTD15	Data	143	JTAG_BSROUTBOTH	OEN_c
DTC15	Data	144	JTAG_BSROUTBOTH	OEN_c
DTC16	Data	145	JTAG_BSROUTBOTH	OEN_c
DTD16	Data	146	JTAG_BSROUTBOTH	OEN_c
MTD16	Data	147	JTAG_BSRINBOTH	

Table 19. JTAG Scan Chain (Continued)

PIN Name	Type	Numbering in Scan chain	Type of BSR Cell	Associated Control enable
MTC16	Data	148	JTAG_BSRINBOTH	
MTC17	Data	149	JTAG_BSRINBOTH	
MTD17	Data	150	JTAG_BSRINBOTH	
DTD17	Data	151	JTAG_BSRROUTBOTH	OEN_c
DTC17	Data	152	JTAG_BSRROUTBOTH	OEN_c
DTC18	Data	153	JTAG_BSRROUTBOTH	OEN_c
DTD18	Data	154	JTAG_BSRROUTBOTH	OEN_c
MTD18	Data	155	JTAG_BSRINBOTH	
MTC18	Data	156	JTAG_BSRINBOTH	
MTC19	Data	157	JTAG_BSRINBOTH	
MTD19	Data	158	JTAG_BSRINBOTH	
DTD19	Data	159	JTAG_BSRROUTBOTH	OEN_c
DTC19	Data	160	JTAG_BSRROUTBOTH	OEN_c
DTC20	Data	161	JTAG_BSRROUTBOTH	OEN_c
DTD20	Data	162	JTAG_BSRROUTBOTH	OEN_c
MTD20	Data	163	JTAG_BSRINBOTH	
MTC20	Data	164	JTAG_BSRINBOTH	
SCANTEST	Data	165	JTAG_BSRINBOTH	

10.0 Package Specification

- Part Number LXT6251A
- 208-pin Plastic Quad Flat Pack
- Extended Temperature Range (-40, +85°C)



Dim	Millimeters	
	Min	Max
A	-	4.10
A1	0.05	-
A2	3.20	3.60
b	0.17	0.27
D	30.60 BSC.	
D ₁	28.00 BSC.	
E	30.60 BSC.	
E ₁	28.00 BSC.	
e	.50 BSC.	
L	0.50	0.75
L ₁	1.30 REF	
q	0°	7°
θ ₂	5°	16°
θ ₃	5°	16°

11.0 Glossary

AIS	Alarm Indication Signal
AUG	Administrative Unit Group
RDI	Remote Defect Indication
REI	Remote Error Indication
RFI	Remote Fail Indication
FIFO	First in/First Out Memory
MSOH	Multiplexer Section Overhead
NRZ	Non-Return to Zero
POH	Path Overhead
RSOH	Regenerator Section Overhead
SDH	Synchronous Digital Hierarchy
SPE	Synchronous Payload Envelope
SONET	Synchronous Optical NETWORK
STM	Synchronous Transport Module
STM-RR	Synchronous Transport Module for Radio Relay
STS	Synchronous Transport Signal
TUG	Tributary Unit Group
VC	Virtual Container