M74LS373P

OCTAL D-TYPE TRANSPARENT LATCHS WITH 3-STATE OUTPUTS

DESCRIPTION

The M74LS373P is a semiconductor integrated circuit containing 8 D-type latch circuits with 3-state output and is provided with an output controlling input and an enable input common to all circuits.

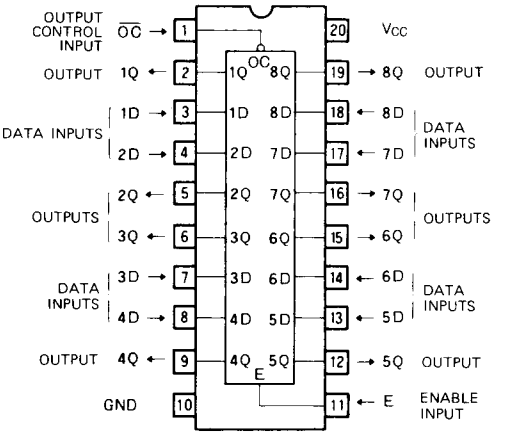
FEATURES

- 3-state, high fan-out output
- Since pnp transistor input is used in output control and enable inputs, the input load factor is small
- The enable input has high noise margin (Hysterisis = 400mV typical)
- Package density is high with 8 circuits in one package
- Provided with output control and enable inputs which are common to all 8 circuits.
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

FUNCTIONAL DESCRIPTION

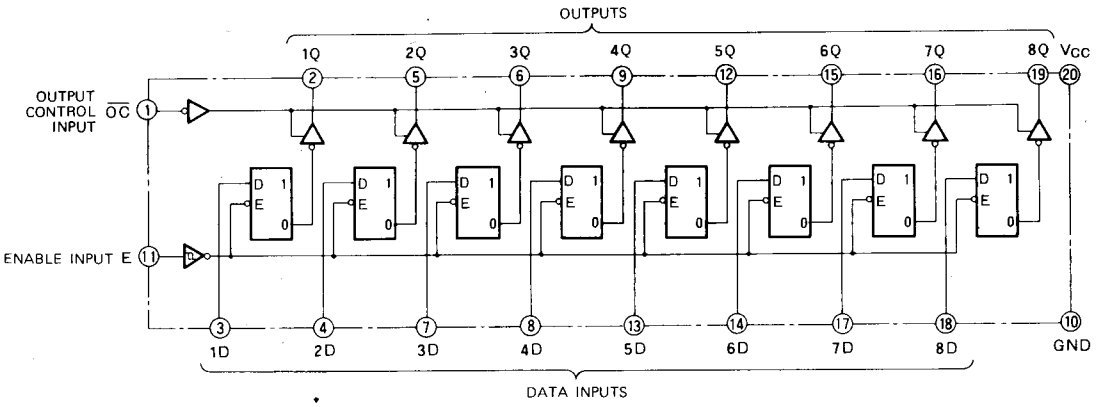
Since the 8 D-type latches use pnp transistor input for the output control input $\overline{OC}$ and enable input E, which are common to all 8 circuits, the input load factor is small. With a hysteretis of 400mV (typical) specially given to the input circuit E, noise margin is high.

When E is high, the information from the data input D appears in the output Q.

When the D signal changes, the signal that appears in Q also changes. When E changes from high to low, the status of D immediately before the change is latched. While E is low, the status of Q does not change even if the D is changed.

When $\overline{OC}$ is high, 1Q – 8Q are all put in the high-impedance state irrespective of other input signals. Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bi-directional bus driver. For application, see M74LS374P.

BLOCK DIAGRAM



OCTAL D-TYPE TRANSPARENT LATCHS WITH 3-STATE OUTPUTS

FUNCTION TABLE (Note 1)

$\overline{OC}$	E	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q^0
H	X	X	Z

Note 1: Q^0 : level of Q before the indicated steady-state input conditions were established
Z : high-impedance
X : irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	Off-state	−0.5 ~ +7	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geq 2.4V$	0		−2.6	mA
I_{OL}	Low-level output current	$V_{OL} \leq 0.4V$	0		12	mA
		$V_{OL} \leq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ*	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage	E					0.75	V
		D, $\overline{OC}$					0.8	
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $I_{OH}=-2.6mA$		2.4	3.1		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$	$I_{OL}=12$ mA		0.25	0.4	V
				$I_{OL}=24$ mA		0.35	0.5	V
I_{OZH}	Off-state high-level output current		$V_{CC}=5.25V$, $V_I=2V$, $V_O=2.7V$				20	μA
I_{OZL}	Off-state low-level output current		$V_{CC}=5.25V$, $V_I=2V$, $V_O=0.4V$				−20	μA
I_{IH}	High-level input current		$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
			$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current		$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)		$V_{CC}=5.25V$, $V_O=0V$		−30		−130	mA
I_{CCZ}	Supply current, all outputs off		$V_{CC}=5.25V$ (Note 3)			24	40	mA

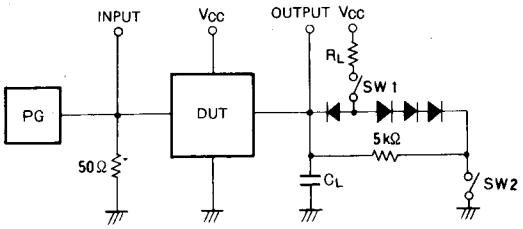
* : All typical values are at V_{CC} = 5V, Ta = 25°C.
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.
3: I_{CCZ} is measured with $\overline{OC}$ input at 4.5V.

OCTAL D-TYPE TRANSPARENT LATCHS WITH 3-STATE OUTPUTS

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input 1D~8D to output 1Q~8Q	C_L=45pF (Note 4)		9	18	ns
t_{PHL}				11	18	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input E to output 1Q~8Q			14	30	ns
t_{PHL}				13	30	ns
t_{PZH}	Output enable time to high-level	R_L=667Ω, C_L=45pF (Note 4)		13	28	ns
t_{PZL}	Output enable time to low-level	R_L=667Ω, C_L=45pF (Note 4)		14	36	ns
t_{PHZ}	Output disable time from high-level	R_L=667Ω, C_L= 5pF (Note 4)		16	20	ns
t_{PLZ}	Output disable time from low-level	R_L=667Ω, C_L= 5pF (Note 4)		8	25	ns

Note 4: Measurme Measurement circuit



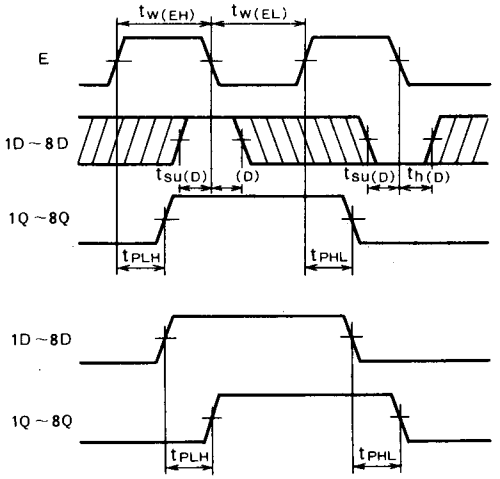
Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

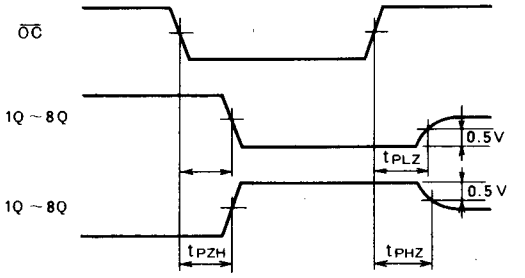
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
V_P = 3V_{P-P}, Z_O = 50Ω
(2) All diodes are switching diodes ($t_{rr} \leqq$ 4ns)
(3) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(EH)}$	Enable input E high pulse width		15	11		ns
$t_{W(EL)}$	Enable input E low pulse width		15	10		ns
t_{SU}	Setup time 1D~8D to E		5	−2		ns
t_h	Hold time 1D~8D to E		20	7		ns

TIMING DIAGRAM (Reference level = 1.3V)





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

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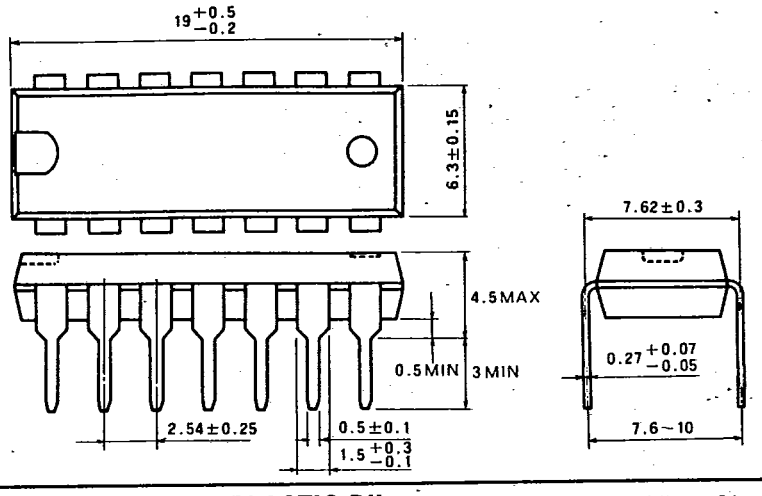
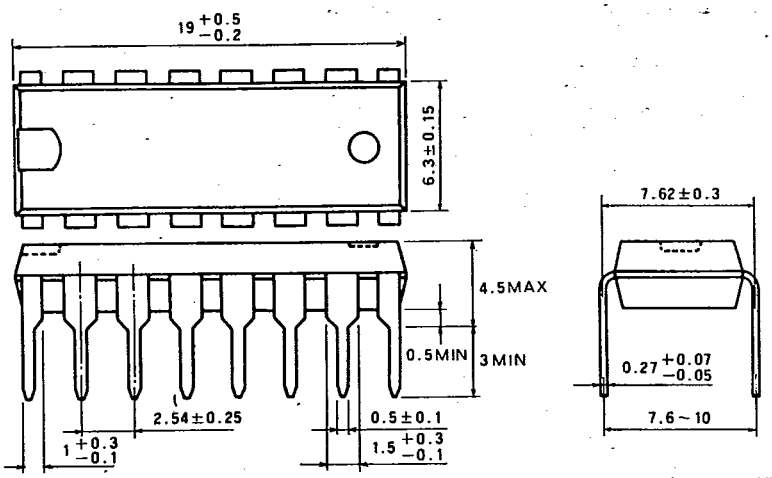
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm