NEC
NEC Electronics U.S.A. Inc.
Microcomputer Division

μPB406/406-1/406-2
μPB426/426-1/426-2
1024 WORD BY 4-BIT
4096-BIT BIPOLAR TTL PROM

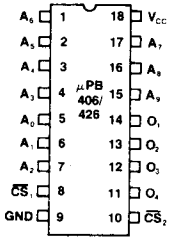
Description

The μPB406 and μPB426 are high-speed, electrically programmable, fully decoded 4096-bit TTL read-only memories. On-chip address decoding, two chip-enable inputs and open-collector/three-state outputs allow easy expansion of memory capacity. The μPB406 and μPB426 are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

Features

- ☐ 1024 word x 4 bit organization (fully decoded)
- ☐ TTL interface
- ☐ Fast Read Access Time: 50 ns max. (μPB406-2, μPB426-2)
- ☐ Power consumption: 500 mW typ.
- ☐ Two Chip Select inputs for memory expansion
- ☐ Open-collector output (μPB406)
  Three-state outputs (μPB426)
- ☐ Ceramic and plastic 18-lead dual in-line packages
- ☐ Fast programming time: 200 μs/bit typ.
- ☐ Compatible with: 7642/7643, 6352/6353 types and equivalent devices (as a ROM)
- ☐ A.I.M. (Avalanche Induced Migration), Shorted-junction technology

Pin Configuration



Pin Names

A_0-A_9	Address Inputs
O_1-O_4	Data Outputs
$\overline{CS}_1$, $\overline{CS}_2$	Chip Selects
V_{CC}	Power (+5V)
GND	Ground

Operation

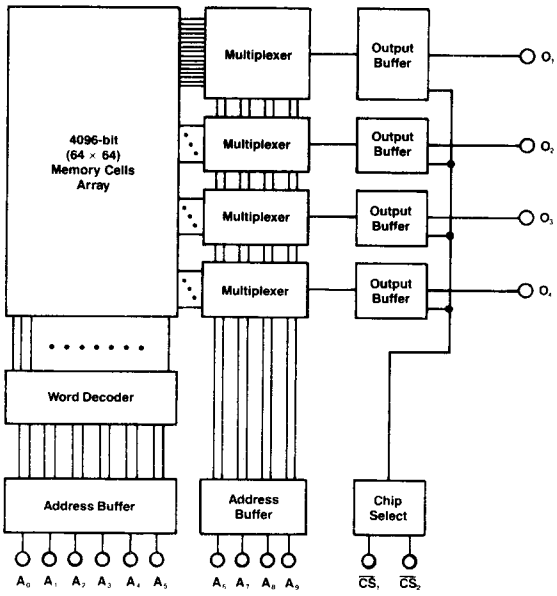
Programming

A logic one can be permanently programmed into a selected bit location by using a programmer. First, the desired word is selected by the ten address inputs in TTL levels. Either or both of the two chip select inputs must be at a logic one (high). Secondly, a train of high-current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then stopped.

Reading

To read the memory, both of the two chip select inputs should be held at logic zero (low). The outputs then correspond to the data programmed in the selected words. When either or both of the two chip select inputs are at logic one (high), all the outputs will be high (floating).

Block Diagram



Absolute Maximum Ratings*

T_a = 25° C	
Operating Temperature	−25°C to +75°C
Storage Temperature	−65°C to +150°C
All Output Voltages	−0.5 to +5.5 Volts
All Input Voltages	−0.5 to +5.5 Volts
Supply Voltage V_{CC}	−0.5 to +7.0 Volts
Output Currents	50 mA

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

μPB406/426

DC Characteristics

T_a = 0°C to +75°C, V_{CC} = 4.50V to 5.50V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Input High Current	I_{IL}			40	μA	V_I = 5.5V, V_{CC} = 5.5 V
Input Low Current	$-I_{IL}$			0.5	mA	V_I = 0.4V, V_{CC} = 5.5V
Output Low Voltage	V_{OL}			0.45	V	I_O = 16 mA, V_{CC} = 4.5V
Output Leakage Current	I_{OFF1}			40	μA	V_O = 5.5V, V_{CC} = 5.5V
Output Leakage Current	$-I_{OFF2}$			40	μA	V_O = 0.4V, V_{CC} = 5.5V
Input Clamp Voltage	$-V_{IC}$			1.3	V	I_I = −18 mA, V_{CC} = 4.5V
Power Supply Current	I_{CC}		100	150	mA	All Inputs Grounded
Output High Voltage①	V_{OH}	2.4			V	I_O = − 2.4 mA
Output Short Circuit Current①	$-I_{SC}$	15		60	mA	V_O = 0V

NOTE:
① Applicable to μPB426 only.

Capacitance

T_a = 25°C, f = 1 MHz, V_{CC} = 5.0V, V_{IN} = 2.5V

Characteristics	Symbol	Min.	Max.	Unit
Input Capacitance	C_{IN}		8	pF
Output Capacitance	C_{OUT}		10	pF

AC Characteristics

T_a = 0°C to +75°C, V_{CC} = 4.50V to 5.50V

Parameter	Symbol	μPB406 μPB426 Min.	Max.	μPB406-1 μPB426-1 Min.	Max.	μPB406-2 μPB426-2 Min.	Max.	Unit	Test Conditions
Address Access Time	t_{AA}		70		60		50	ns	
Chip Select Access Time	t_{ACS}		45		40		30	ns	① ② ③ ④
Chip Select Disable Time	t_{DCS}		45		40		30	ns	

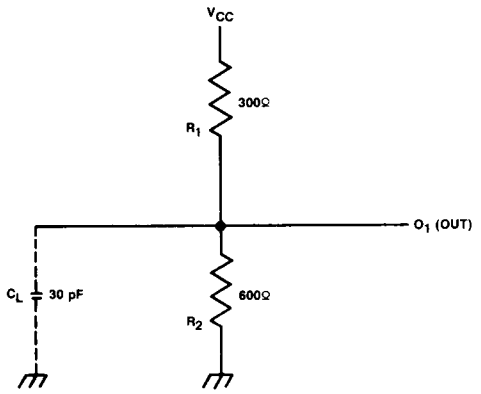


Figure 1

Notes:
① Output Load: See Figure 1.
② Input Waveform: 0.0V for low level and 3.0V for high level, less than 10 ns for both rise and fall times.
③ Measurement References: 1.5V for both inputs and outputs.
④ C_L in Figure 1 includes jig and probe stray capacitances.

Programming Specification

You must rigorously observe this specification in order to program the μPB406 and μPB426 correctly. NEC will not accept responsibility for any device found to be defective if it was not programmed according to this specification.

A typical programming operation is performed by sensing, programming, and sensing again to find out if the word to be programmed has reached the desired state. Either or both of the two chip enable inputs must be at a logic one (high).

Sensing is accomplished by forcing a 20 mA current into the selected location via the output. The sense measurement ensures that the voltage required to force this 20 mA current is less than the reference voltage. If this condition is satisfied, then that bit location is in the logic one (high) state.

Programming is accomplished by forcing a 200 mA current into the selected bit via the output. The current pulse is applied for 7.5 μs and then the location is sensed before a second programming current pulse is applied. This process continues until the selected bit is altered to the one state. You can tell that a bit is programmed when two successive sense readings, 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied, and the sense current is terminated.

Characteristic	Limit	Unit	Notes
Ambient Temperature	25 ± 5	°C	
Programming pulse			
Amplitude	200 ± 5%	mA	
Clamp voltage	28 + 0% − 2%	V	
Ramp rate (both in rise and in fall)	70 max.	V/μs	
Pulse width	7.5 ± 5%	μs	15V point/ 150Ω load.
Duty cycle	70% min.		
Sense current			
Amplitude	20 ± 0.5	mA	
Clamp voltage	28 + 0% − 2%	V	
Ramp rate	70 max.	V/μs	15V point/ 150Ω load.
Sense current interruption before and after address change	10 min.	μs	
Programming V_{CC}	5.0 + 5% − 0%	V	
Maximum sensed voltage for programmed one	7.0 ± 0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 min.	μs	

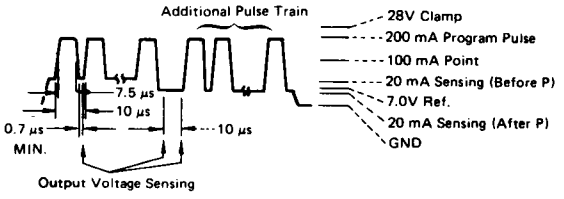
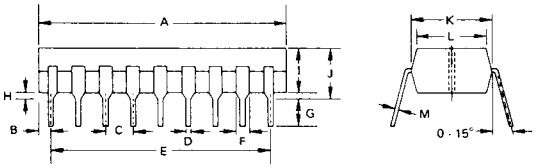


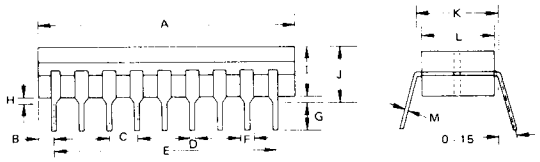
Figure 2 – Typical Output Voltage Waveform

Package Outlines

μPB406/426C PLASTIC



μPB406/426D CERDIP



Plastic

Item	Millimeters	Inches
A	23.2 Max.	0.91 Max.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 Min.	0.1 Min.
H	0.5 Min.	0.02 Min.
I	4.6 Max.	0.18 Max.
J	5.1 Max.	0.2 Max.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

Cerdip

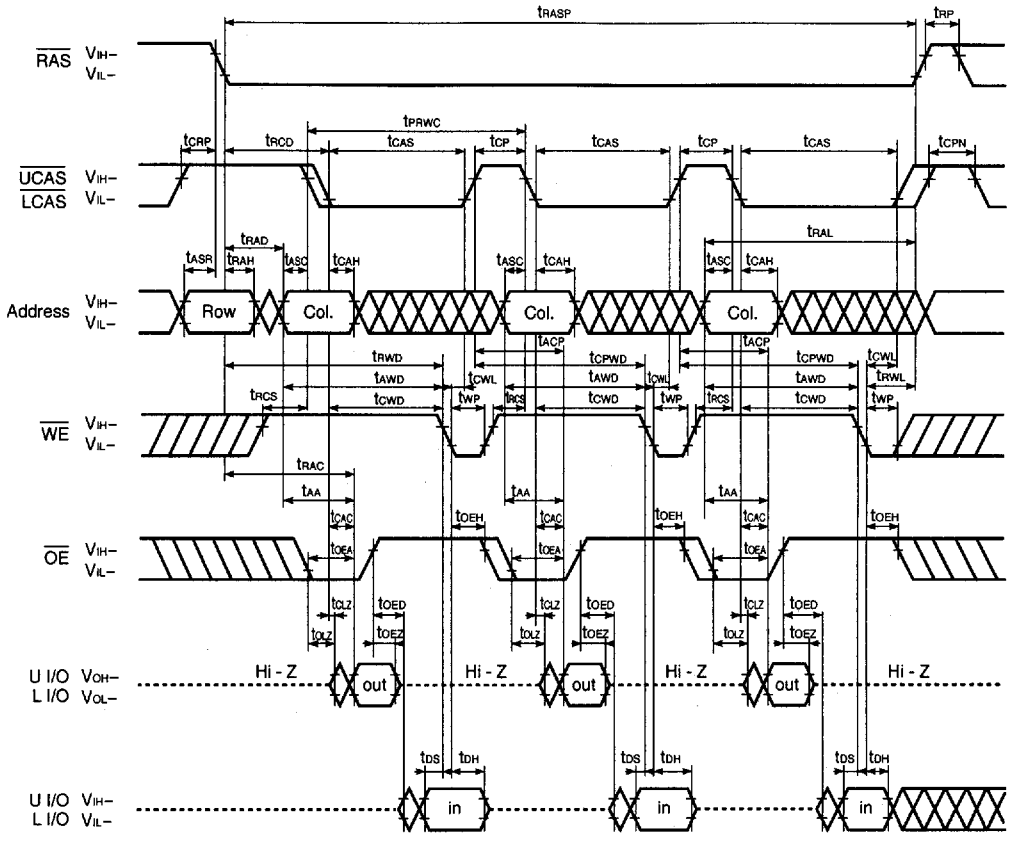
Item	Millimeters	Inches
A	23.2 Max.	0.91 Max.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 Min.	0.1 Min.
H	0.5 Min.	0.02 Min.
I	4.6 Max.	0.18 Max.
J	5.1 Max.	0.2 Max.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

4

Qualified Programming Equipment

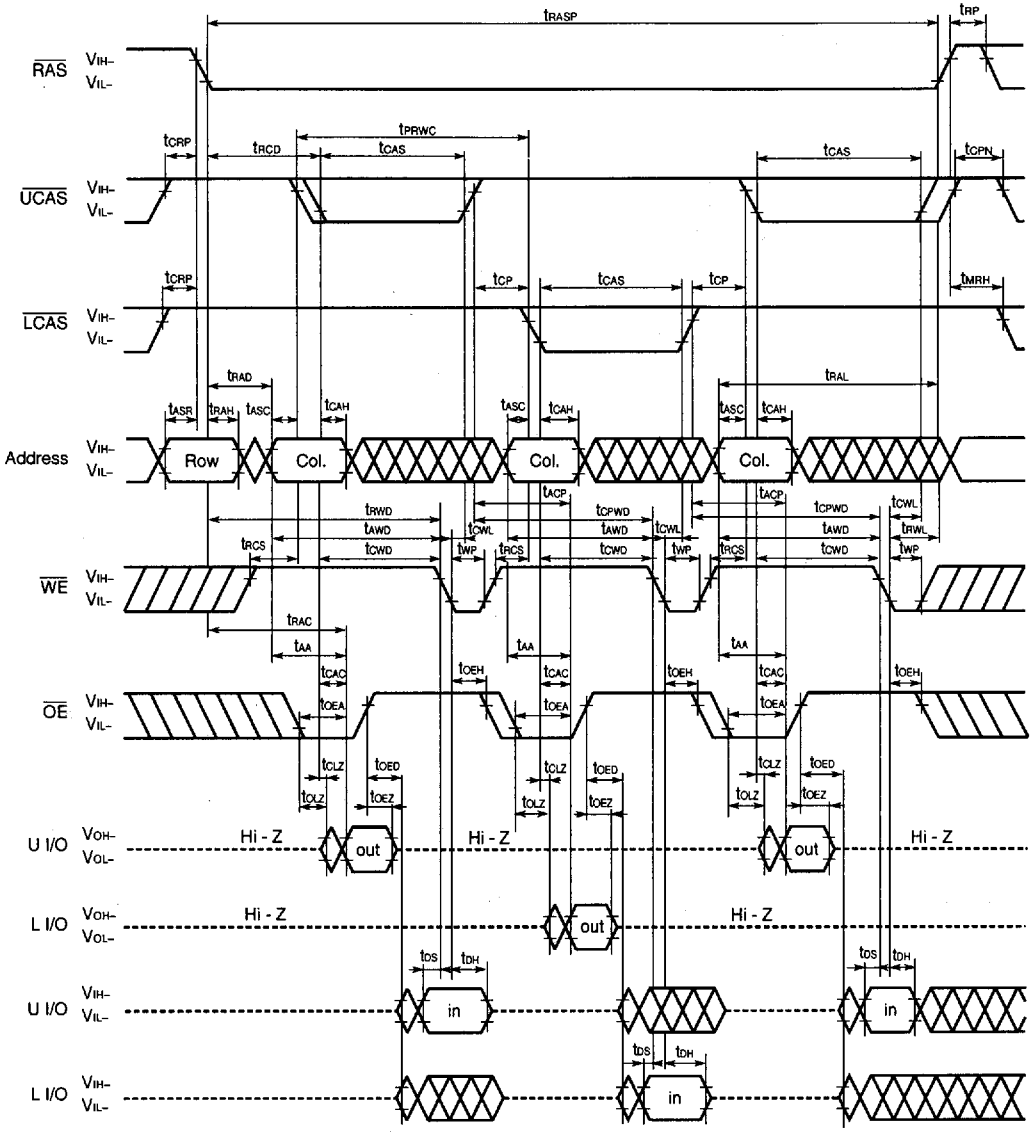
Approved Manufacturer	Model No.	Personality Module	Socket Adaptors
Data I/O Issaquah, WA	5, 7, 9, 17, 19	919-1555	715-1305-5
Minato Electronics Tokyo, Japan	1802	μPB4XX	SA-18/B426
Takeda Riken Tokyo, Japan	TR-429 B	PZ 3834	WZ3256-78
Tokyo Data Tokyo, Japan	PECKER-O	UN-711F	AD-7115

Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

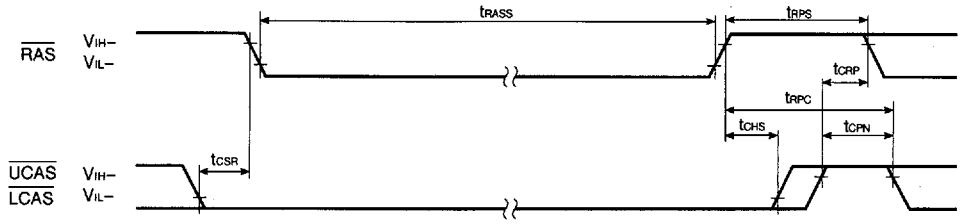
Fast Page Mode Byte Read Modify Write Cycle



Remarks 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S18160)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

μPD42S18160: 1,024 times within a 16 ms interval

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

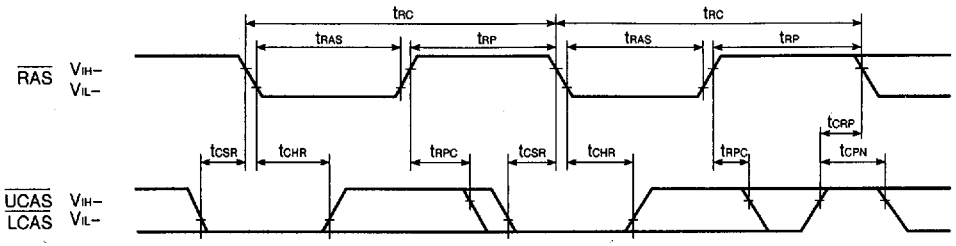
μPD42S18160: 1,024 times within a 16 ms interval

(3) If $t_{RASS\ (MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100\ \mu s$), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If $10\ \mu s < t_{RAS} < 100\ \mu s$, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles as follows should be met.

μPD42S18160: 1,024 times within a 128 ms interval

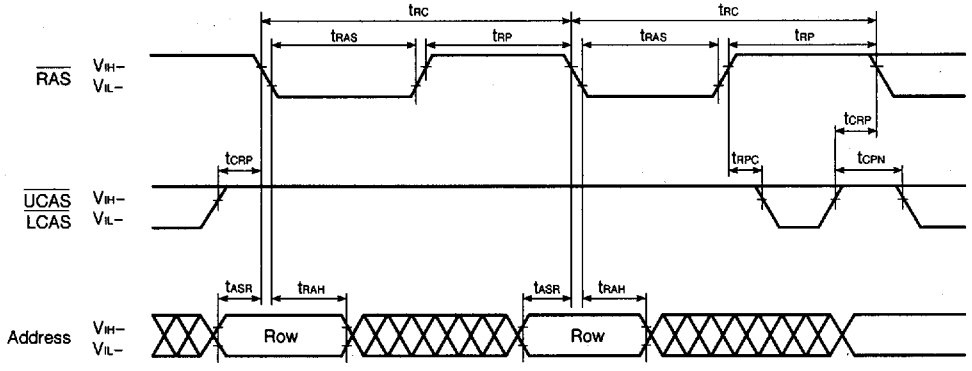
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle



Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)