

HT9305/6 Series 5-Memory Tone/Pulse Dialer

Features

Patent Number: 64097, 86474, 113235(R.O.C.), 5424740(U.S.A.)

- Universal specification
- Operating voltage: 2.0V~5.5V
- Low standby current
- Low memory retention current: $0.1 \mu A$ (Typ.)
- Tone/pulse switchable
- Interface with LCD driver
- 32 digits for redialing
- 32 digits for the SA memory dialing
- One-key redialing
- Pause and $P \rightarrow T$ key for PBX
- 4×5 keyboard matrix
- 3.58MHz crystal or ceramic resonator

General Description

The HT9305/6 series tone/pulse dialers are CMOS LSIs for telecommunication systems. They are designed to meet various dialing specifications through resistor option matrix.

The HT9305/6 series tone/pulse dialers are offered in four different versions. They are HT9305x/HT9306x normal version; HT9305xL/HT9305xL

- Hand-free control
- Hold-line control
- Pause, $P \rightarrow T$ can be saved for redialing
- Lock function
- Keytone function
- Resistor options:
 - M/B ratio

1

- Flash function and flash time(86ms~600ms)
- Pause and $P{\rightarrow}T$ duration
- Pulse number
- Keyboard operated IDD lock function
- Key board form

lock version, with keyboard-operated IDD lock function; HT9305xT keytone version; and HT9305xLT/HT9305xIT keytone/lock function version. The four versions also supply the following functions: Hold-line, Hand-free and LCD dialing number display interface, all of which are suitable for feature phone applications.



Selection Table

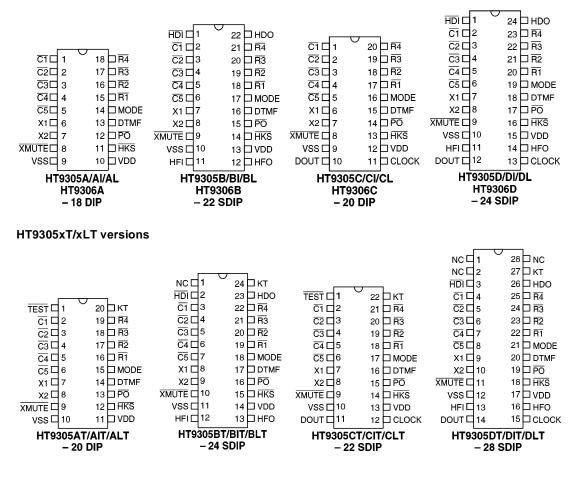
Function	Keytone	Lock Function	Hold- Line	Hand- Free	LCD Interface	Min. Flash Time	Package
HT9305x	(Norma	al version)					
HT9305A	<u> </u>	_	_	_	_		18 DIP
НТ9305В	_	_	1	√	_		22 SDIP
HT9305C	_	_	_	_	\checkmark	98 ms	20 DIP
HT9305D	_	_	\checkmark	\checkmark	\checkmark		24 SDIP
HT9305xl	(Mecha	nical Lock versior	י ו)				
HT9305AI	_		_	_	_		18 DIP
HT9305BI	_	Lock 0	\checkmark	\checkmark	_		22 SDIP
HT9305CI	_	Lock 0, 9 Lock All	_	_	\checkmark	98 ms	20 DIP
HT9305DI	-		\checkmark	\checkmark	\checkmark		24 SDIP
HT9305xL	(Mecha	nical and Keyboa	rd Operate	ed Lock ve	ersion)		
HT9305AL	_	Lock 0	_		_		18 DIP
HT9305BL	—	Lock 0, 9 Lock All	\checkmark	\checkmark	-	09 mg	22 SDIP
HT9305CL	—	Keyboard-	_	_	\checkmark	98 ms	20 DIP
HT9305DL	_	Operated lock	\checkmark	\checkmark	\checkmark		24 SDIP
HT9305xT	(Norma	I version with Key	rtone)				
HT9305AT	\checkmark	—	—	—	_		20 DIP
HT9305BT	\checkmark	-	\checkmark	\checkmark	_	98 ms	24 SDIP
HT9305CT	\checkmark		_	_	\checkmark	30 113	22 SDIP
HT9305DT	\checkmark	_	\checkmark	\checkmark	\checkmark		28 SDIP
HT9305xIT	(Mecha	nical Lock with Ke	eytone ver	sion)			
HT9305AIT	7		_	_	_		20 DIP
HT9305BIT	7	Lock 0 Lock 0, 9	\checkmark	\checkmark	_	98 ms	24 SDIP
HT9305CIT	7	Lock All	_	_	\checkmark	30 113	22 SDIP
HT9305DIT	7		\checkmark	\checkmark	\checkmark		28 SDIP
HT9305xLT	(Mecha	nical and Keyboa	rd Operate	ed Lock wit	th Keytone	version)	
HT9305ALT	7	Lock 0					20 DIP
HT9305BLT	7	Lock 0, 9 Lock All	\checkmark	\checkmark		98 ms	24 SDIP
HT9305CLT	~	Keyboard-			\checkmark	00 113	22 SDIP
HT9305DLT	7	Operated lock	\checkmark	\checkmark	\checkmark		28 SDIP
HT9306x	(Norma	al version)					
HT9306A	—				-		18 DIP
НТ9306В	_		\checkmark	\checkmark		86 ms	22 SDIP
HT9306C					\checkmark	00 118	20 DIP
HT9306D			\checkmark	\checkmark	\checkmark		24 SDIP

21st Jan '98



Pin Assignment

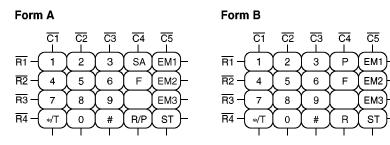
HT9305x/xL, HT9306x version



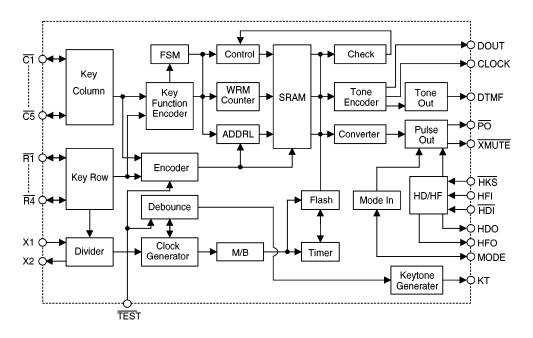
21st Jan '98



Keyboard Information



Block Diagram



4



Pin Description

Pin Name	I/O	Internal Connection	Description
$\frac{\overline{C1}}{\overline{R1}} \sim \frac{\overline{C5}}{\overline{R4}}$	I/O	CMOS IN/OUT	These pins form a 4×5 keyboard matrix which can perform keyboard input detection and dialing specification setting functions. When on-hook (\overline{HKS} =high) all the pins are set high. While off-hook the column group ($\overline{C1}$ - $\overline{C5}$) remains low and the row group ($\overline{R1}$ - $\overline{R4}$) is set high for key input detection. An inexpensive single contact 4×5 keyboard can be used as an input device. Pressing a key connects a single column to a single row, and actuates the system oscillator that results in a dialing signal output. If more than two keys are pressed at the same time, no response occurs. The key-in debounce time is 20ms. Refer to the keyboard information for keyboard arrangement and to the functional description for dialing specification selection.
X1	I	OSCILLATOR	The system oscillator consists of an inverter, a bias resistor and the necessary load capacitor on chip. Connecting a standard 3.579545MHz crystal or ceramic resonator to the X1 and X2 terminals can implement the oscillator function. The
X2	0		oscillator is turned off in the standby mode, and is actuated whenever a keyboard entry is detected.
XMUTE	0	NMOS OUT	$\overline{\text{XMUTE}}$ is an NMOS open drain structure pulled to VSS during dialing signal transmission. Otherwise, it is an open circuit. $\overline{\text{XMUTE}}$ is used to mute the speech circuit when transmitting the dial signal.
HKS	I	CMOS IN	This pin is used to monitor the status of the hook-switch and its combination with HFI/HDI can control the PO pin output to make or break the line. HKS=VDD: On-hook state (PO=low). Except for HFI/HDI (hand-free/hold-line control input), other functions are all disabled. HKS=VSS: Off-hook state (PO=high). The chip is in the standby mode and ready to receive the key input.
TEST	Ι	CMOS IN	This is a test pin. It should be connected to VDD when in normal operation.
PO	O CMOS OUT		This pin is a CMOS output structure, which by receiving the \overline{HKS} and HFO/HDO signals, control the dialer to connect or disconnect the telephone line. \overline{PO} outputs a low to break line when \overline{HKS} is high (on-hook) and HFO/HDO is low. \overline{PO} outputs a high to make line when \overline{HKS} is low (off-hook) or HFO is high or HDO is high. During the off-hook state, this pin also outputs the dialing pulse train in pulse mode dialing. While in the tone mode, this pin is always high.

5



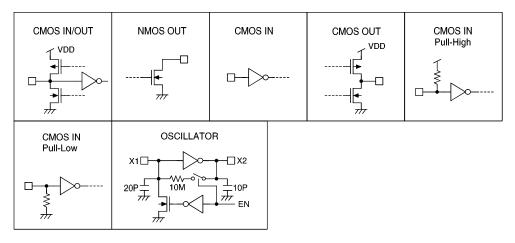
Pin Name	I/O	Internal Connection	Description
MODE	I/O	CMOS IN/OUT	This is a three-state input/output pin, used for dialing mode selection, either Tone mode or Pulse mode, 10pps/20pps MODE=VDD: Pulse mode, 10pps MODE=OPEN: Pulse mode, 20pps MODE=VSS: Tone mode During pulse mode dialing, switching this pin to the tone mode changes the subsequent digit entry to tone mode. When the chips are in tone mode, switching to pulse mode will also be recognized.
DTMF	0	CMOS OUT	This pin is active only when the chip transmits tone dialing signals. Otherwise, it always outputs a low. The pin outputs tone signals to drive the external transmitter amplifier circuit. The load resistor should not be less than $5k\Omega$.
HDI	I	CMOS IN Pull-High	This pin is a schmitt trigger input structure. Active low. Applying a negative going pulse to this pin can toggle the HDO output once. An external RC network is recommended for input debouncing. The pull-high resistance is $200k\Omega$ typ.
HDO	ο	CMOS OUT	The HDO is a CMOS output structure. Its output is toggle- controlled by a negative transition on \overline{HDI} . When HDO is toggled high, \overline{PO} keeps high to hold the line. The hold function can be released by setting HFO high or by an on-off hook operation or by another \overline{HDI} input. The HDO pin can directly drive the HT3810 series melody generator to produce a hold- line background melody. Refer to the functional description for the hold-line function.
КТ	0	CMOS OUT	Keytone output pin. It outputs a 1.2kHz tone carrier when any key is pressed in the pulse mode or when the function keys are pressed in the tone mode.
HFI	I	CMOS IN Pull-Low	This pin is a schmitt trigger input structure. Active high. Applying a positive going pulse to HFI can toggle the HFO once and hence control the hand-free function. The pull-low resistance of HFI is $200 k\Omega$ typ. An external RC network is recommended for input debouncing.
HFO	0	CMOS OUT	The HFO is a CMOS output structure. Its output is toggle- controlled by a positive transition on HFI pin. When HFO is high, the hand-free function is enabled and PO outputs a high to connect the line. The hand-free function can be released by setting HDO high or by an on-off-hook operation or by another HFI input. Refer to the functional description for the hand-free functional operation.

6



Pin Name	I/O	Internal Connection	Description
DOUT	0	NMOS OUT	NMOS open drain output pin. It outputs the BCD code of the dialing digits to the LCD driver chip (HT16XX series) or μ C for dialing number display. Refer to the functional description for the detailed timing.
CLOCK	0	NMOS OUT	NMOS open drain output. When dialing, it outputs a series of pulse trains for DOUT data synchronization. DOUT data is valid at the falling edge of the clock.
VDD	Ι	_	Positive power supply, 2.0V~5.5V for normal operation
VSS	Ι	_	Negative power supply

Approximate internal connection circuits



Absolute Maximum Ratings*

Supply Voltage0.3V to 6V	
Storage Temperature50°C to 125°C	

Input Voltage	Vss-0.3 to V _{DD} +0.3V
Operating Temperature	–20°C to 75°C

*Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7



Electrical Characteristics

(Fosc=3.5795MHz, Ta=25°C)

Sumbal	Donomatan	Parameter Test Conditions		onditions	M:	T ****	Mor	T Int
Symbol	rarameter	VDD	Conditions		Min.	Тур.	Max.	Unit
VDD	Operating Voltage	_		_	2		5.5	V
I _{DD}	Operating Current	2.5V	Pulse Tone	Off-hook Keypad entry No load		0.2 0.6	1 2	mA mA
I _{STB}	Standby Current	1V	On-ho No ent	ok, no load try	_		1	μΑ
VR	Memory Retention Voltage	_		_	1		5.5	V
I _R	Memory Retention Current	1V	On-ho	ok	_	0.1	0.2	μA
VIL	Input Low Voltage	_		_	Vss		$0.2V_{DD}$	V
V _{IH}	Input High Voltage			_	0.8V _{DD}	_	V _{DD}	V
Ixmo	XMUTE Leakage Current		Vxmu No ent	TE=12V try	_		1	μΑ
IOLXM	XMUTE Sink Current	2.5V	VXMU	<u>re</u> =0.5V	1		_	mA
IHKS	HKS Pin Input Current	2.5V	V _{HKS} =	2.5V	—		0.1	μA
R _{HFI}	HFI Pull-Low Resistance	2.5V	V _{HFI} =	2.5V	_	200	_	kΩ
RHDI	HDI Pull-High Resistance	2.5V	V _{HDI} =	0V	—	200	—	kΩ
I _{OH1}	Keypad Pin Source Current	2.5V	V _{OH} =0)V	-4		-40	μA
IOL1	Keypad Pin Sink Current	2.5V	Vol=2	2.5V	200	400	_	μΑ
I _{OH2}	HFO Pin Source Current	2.5V	V _{OH} =2	2V	-1		_	mA
IOL2	HFO Pin Sink Current	2.5V	Vol=0	0.5V	1		_	mA
I _{OH3}	HDO Pin Source Current	2.5V	V _{OH} =2	2V	-1	_	—	mA
IOL3	HDO Pin Sink Current	2.5V	Vol=0	0.5V	1	_	—	mA
T _{FP}	Pause Time After Flash		Contro	ol key	_	0.2	_	s
IFF			Digit l	key	_	1	_	3
T _{RP}	One-key Redialing Pause Time	—	One-key redialing		—	1	—	S
T _{DB}	Key-in Debounce Time		_			20		ms
T _{BRK}	Break Time for One-key Redialing	_	One-key redialing		—	1.2	_	s
T _{KT}	Keytone Duration		_		34		ms	
F _{KTC}	Keytone Frequency			_	1.2		kHz	
Fosc	System Frequency		Crysta	al=3.5795MHz	3.5759	3.5795	3.5831	MHz

21st Jan '98



Symbol	Denometer		Test Conditions	Min	Tron	Max.	Two More	
Symbol	Parameter	VDD	Conditions	Min.	Тур.	max.	Unit	
I _{POH}	PO Output Source Current	2.5V	V _{OH} =2V	-0.2	_		mA	
IPOL	PO Output Sink Current	2.5V	V _{OL} =0.5V	0.2	0.6		mA	
PR	Pulse Rate	_	$\begin{array}{c} MODE \ pin \ is \ connected \\ to \ V_{DD} \end{array}$	_	10		pps	
			MODE pin is opened	_	20			
M/B	Make/Break Ratio		A resistor is linked between $\overline{R2}$ and $\overline{C1}$	_	33:66		%	
IVI/D	Make/Break Ratio	_	No resistor is linked between $\overline{R2}$ and $\overline{C1}$	_	40:60	70		
т	Due disit neuse Time		M/B ratio=40:60	_	40 (10pps) 20 (20pps)			
T _{PDP}	Pre-digit-pause Time	_	M/B ratio=33:66	_	33 (10pps) 17 (20pps)		ms	
T	Later Batter There		Pulse rate=10pps	_	800	_		
T _{IDP}	Inter-digit-pause Time	_	Pulse rate=20pps	_	500	_	ms	
T	Pulse Make Duration		A resistor is linked between $\overline{R2}$ and $\overline{C1}$	_	33 (10pps) 17 (20pps)			
T _M	ruise make Duration		No resistor is linked between $\overline{R2}$ and $\overline{C1}$	_	40 (10pps) 20 (20pps)		ms	
т_	Pulse Break Duration		A resistor is linked between $\overline{R2}$ and $\overline{C1}$	_	66 (10pps) 33 (20pps)			
TB	Pulse Break Duration		No resistor is linked between $\overline{R2}$ and $\overline{C1}$	_	60 (10pps) 30 (20pps)		ms	

Pulse Mode Electrical Characteristics

(Fosc=3.5795MHz, Ta=25°C)

21st Jan '98



Tone Mode Electrical Characteristics

(Fosc=3.5795MHz, Ta=25°C)

General	bol Parameter		Test Conditions		T	Man	Unit	
Symbol	Parameter	V _{DD}	Conditions	Min.	Тур.	Max.	Unit	
VTDC	DTMF Output DC Level	—	—	$0.45 V_{DD}$	—	$0.7 V_{DD}$	v	
I _{TOL}	DTMF Sink Current	2.5V	V _{DTMF} =0.5V	0.1	_		mA	
VTAC	DTMF Output AC Level	—	Row group, $R_L=5k\Omega$	0.12	0.155	0.18	Vrms	
RL	DTMF Output Load	2.5V	THD≤–23dB	5	—	_	kΩ	
Acr	Column Pre-emphasis	2.5V	Row group=0dB	1	2	3	dB	
THD	Tone Signal Distortion	2.5V	$R_L=5k\Omega$	_	-30	-23	dB	
T _{TMIN}	Minimum Tone Duration	—	Auto-redial	_	82.5	_	ms	
T _{ITPM}	Minimum Inter-tone Pause		Auto-redial	_	85.5	_	ms	

THD (Distortion) (dB) = $20 \log (\sqrt{V1^2 + V2^2 + ... + Vn^2} / \sqrt{Vi^2 + Vh^2})$ Vi, Vh: Row group and column group signals V1, V2, ... Vn: Harmonic signals (BW=300Hz~3500Hz)

Functional Description

Keyboard matrix

 $\overline{C1}$ - $\overline{C5}$ and $\overline{R1}$ - $\overline{R4}$ form a keyboard matrix. Together with a standard 4×5 keyboard, the keyboard matrix is used for dialing entries. In addition, the keyboard matrix provides resistor option for different dialing specification selections. The keyboard arrangement for each of the HT9305/6 series are shown in the **Keyboard Information**.

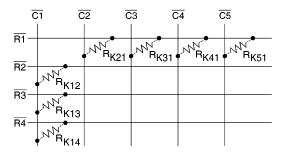
Tone frequen	су
---------------------	----

Tone	Output Fre	% Error	
Name	Specified Actual		% EITOP
R1	697	699	+0.29%
R2	770	766	-0.52%
R3	852	847	-0.59%
R4	941	948	+0.74%
C1	1209	1215	+0.50%
$\overline{C2}$	1336	1332	-0.30%
C3	1477	1472	-0.34%

Note: % Error does not contain the crystal frequency drift

Dialing specification selection

Various dialing specifications can be selected by adding resistors across keyboard matrix pins, . The allowable option resistor connections are shown below.



10



All the resistors are $330k\Omega$. The resistor option functions and the default specifications (without option resistors) are listed below.

Option Resistor	Option Function	Default (No Resistor)
R _{K12}	Make/Break Ratio Selection	40:60
R _{K13}	Flash Function	Flash= control
R _{K14}	and Flash Time Selection	function Flash time= 600ms
R _{K21}	Pause & P→T Duration Selection	$T_{P}=3.6s$ $T_{P\rightarrow T}=3.6s$
R _{K31}	Pulse Number	N or Keyboard
R _{K41}	Selection or IDD Lock Selection	operated lock
R _{K51}	Keypad Form	FormA

M/B ratio selection table

R _{K12}	M/B Ratio (%)
No	40:60
Yes	33.3:66.6

Flash function/time (duration) selection table

• HT9305x/xT

R _{K13}	R _{K14}	Flash Function	Flash Time (T _F)
No	No	Control	600ms
No	Yes	Digit	600ms
Yes	No	Digit	98ms
Yes	Yes	Digit	300ms

• HT9305xL/xLT

R _{K13}	R _{K14}	Flash Function	Flash Time (T _F)
No	No	Control	600ms
No	Yes	Control	600ms
Yes	No	Control	98ms
Yes	Yes	Control	300ms

11

• HT9306x

R _{K13}	R _{K14}	Flash Function	Flash Time (T _F)
No	No	Control	600ms
No	Yes	Digit	600ms
Yes	No	Digit	86ms
Yes	Yes	Digit	300ms

Pause and $P \rightarrow T$ duration selection table

R _{K21}	T _P (sec)	$T_{P ightarrow T}$ (sec)
No	3.6	3.6
Yes	2	1

Pulse number selection table

• This table shows the pulse number selections for HT9305x/HT9306x and HT9305xT. The table for HT9305xL and HT9305xLT is used to select IDD lock function.

R _{K31}	R K41	Pulse Number
No	No	Ν
No	Yes	N+1
Yes	No	10-N
Yes	Yes	—



Pulse number table

Keypad	Output Pulse Number			
Digit Key	Normal N Zealand (10-N)		Sweden/ Denmark (N+1)	
1	1	9	2	
2	2	8	3	
3	3	7	4	
4	4	6	5	
5	5	5	6	
6	6	4	7	
7	7	3	8	
8	8	2	9	
9	9	1	10	
0	10	10	1	
*/T	$P {\rightarrow} T$	$P \rightarrow T$	$P \rightarrow T$	
#	Ignored	Ignored	Ignored	

The keyboard arrangement selection table

R K51	Keypad Form			
No	Form A (see keyboard information)			
Yes	Form B (see keyboard information)			

Hand-free function operation

- Hand-free function execution When HFO is low, a rising edge triggers the HFI, enabling the Hand-free function (HFO becomes high).
- Reset Hand-free function
- When HFO is high, the Hand-free function is enabled and can be reset by:

- Off-hook
- Applying a rising edge to HFI
- Changing the HDO pin from low to high

• Hand-free function table

Current State		Input			Next	State	
HKS	HFO	HDO	HDI	HFI	HKS	HFO	HDO
Н	L	X	Н	L	An	L	An
Н	L	Х	Н	₫	An	Н	L
Н	н	X	Н	_	An	L	An
Н	X	L	Н	L	L	L	L
\mathbf{L}	L	X	Н	L	An	L	An
\mathbf{L}	L	X	н	∮	An	Н	L
\mathbf{L}	н	L	Н	_	An	L	An
\mathbf{L}	X	X	Н	L	Н	An	An
Х	х	L	T	L	An	L	Н

H: Logic HIGH	X: Don't care	🛉 : Rising edge
L: Logic LOW	An: Unchanged	🔪 : Falling edge

Hold-line function operation

• Hold-line function execution

When HDO is low, a falling edge triggers the $\overline{\text{HDI}}$, asserting the Hold-line function (HDO becomes high). The $\overline{\text{XMUTE}}$ remains low when HDO is high.

• Reset Hold-line function

When HDO is high, the Hold-line function is enabled and can be reset by:

- Off-hook
- Applying a falling edge to HDI
- Changing the HFO pin from low to high

12



• Hold-line function table

Current State			Input		Next	State	
HKS	HDO	HFO	HFI	HDI	HKS	HDO	HFO
н	L	х	L	н	An	L	An
н	L	х	L	ł	An	Н	L
н	н	\mathbf{L}	L	ł	An	L	An
н	х	х	L	Н	L	L	L
L	L	х	L	н	An	L	An
L	L	х	\mathbf{L}	₹	An	Н	\mathbf{L}
L	Н	\mathbf{L}	\mathbf{L}	₹	An	L	An
L	х	х	\mathbf{L}	н	н	An	An
x	х	\mathbf{L}	_ _	н	An	L	н
H: Logic HIGH X: Don't care L: Logic LOW An: Unchanged ↓: Falling edge							

DOUT BCD code

When dialing, the corresponding 4-bit BCD codes are serially presented on DOUT from MSB to LSB. The data of DOUT is valid at the falling edge of the CLOCK pin. The following table lists the BCD codes corresponding to the keyboard input.

Key-In	ey-In BCD Code Key-In		BCD Code
1	0001	8	1000
2	0010	9	1001
3	0011	0	1010
4	0100	*/T	1101
5	0101	#	1100
6	0110	F	1011
7	0111	Р	1110

LOCK function

The function aims to detect locked dialing number to prevent a long distance call. The dialing output of the chip is disabled if the first input key after on-off-hook is the locked number when the lock function is enabled. The lock function selection is listed on the table. This function is implemented on both the HT9305xL/HT9305xI and HT9305xLT/HT9305xIT. The HT9305x/HT9306x and HT9305xT do not support this function.

R K31	R K41	Function
No	No	Keyboard operated IDD lock (not supported for HT9305xI & HT9305xIT)
No	Yes	Lock 0
Yes	No	Lock 0, 9
Yes	Yes	All keys are locked

Key definition

• 0,1,2,3,4,5,6,7,8,9 keys

These are dialing number input keys for both the pulse mode and the tone mode operations.

• */T

This key executes the $P{\rightarrow}T$ function and waits a $T_{P{\rightarrow}T}$ duration in the pulse mode. On the other hand, the */T key executes the * function in the tone mode.

• #

This is a dialing signal key for the tone mode only, no response in the pulse mode.

• SA

Pressing this key can save the preceding dialing telephone numbers. The saved number is redialed if it is pressed again. SA will also redial the saved number if it is the first key pressed at the off-hook state. During the dialing signal transmission, the SA key is inhibited.

The flash key can be selected as a digit or as a control key by the option resistors $R_{K13} \& R_{K14}$. Pressing the flash key will force the PO pin to be "low" for the T_F duration and is then followed by T_{FP} (sec). T_F can also be selected by R_{K13} , R_{K14} .

• P

Pause key. The execution of this key pauses the output for the T_P duration. T_P can be selected by $R_{K21}.$

Redial key. Executes redialing as well as onekey redial function.

[•] F

[•] R



• ST

Store key. The execution of this key can actuate the store memory function with (or without) dialing output and it can store lock numbers with personal code in IDD lock operation. During the dialing signal transmission, the ST key is inhibited.

• R/P

Redial and pause function key. If it is pressed

Keyboard operation

The following operations are described under an on-off- hook or on-hook with the hand-free active condition.

Normal dialing

 Pulse mode 	– Tone mode
(a) without */T	(a) without */T
Keyboard input: D1 D2 Dn	Keyboard input: D1 D2 Dn
Dialing output: D1 D2 Dn	Dialing output: D1 D2 Dn
RM: D1 D2 Dn	RM: D1 D2 Dn
SAM: Unchanged	SAM: Unchanged
(b) with */T	(b) with */T
Keyboard input: D1 D2 Dn */T Dn+1	Keyboard input: D1 D2 Dn */T Dn+1
Dm	Dm
Dialing output: Q1 D2 Dn Tp→r Dn+1 Dm	Dialing output: D1 D2 Dn * Dn+1 Dm
Pulse Tone	RM: D1 D2 Dn * Dn+1 Dm
RM: D1 D2 Dn */T Dn+1 Dm	SAM: Unchanged
SAM: Unchanged	

Note: The maximum capacity of the RM memory is 32 digits. When more than 32 digits are entered, the signal is transmitted but the redial function is inhibited.

Redial

- Pulse mode	- Tone mode
(a) without */T	(a) without */T
RM content: D1 D2 Dn	RM content: D1 D2 Dn
Keyboard input: $[R]$ or R/P]	Keyboard input: [R or R/P]
Dialing output: D1 D2 Dn	Dialing output: D1 D2 Dn
RM: Unchanged	RM: Unchanged
SAM: Unchanged	SAM: Unchanged
(b) with */T	(b) with */T
RM content: D1 D2 Dn */T Dn+1 Dm	RM content: D1 D2 Dn */T Dn+1 Dm
Keyboard input: [R or R/P]	Keyboard input: [R or R/P]
Dialing output: ℚ1 D2 Dn Tp→⊤ ℚn+1 Dm	Dialing output: D1 D2 Dn * Dn+1 Dm
Pulse Tone	RM: Unchanged
RM: Unchanged	SAM: Unchanged
SAM: Unchanged	Ň

14

21st Jan '98

as the first key after off-hook, this key executes the redial function. Otherwise, it works as the pause key.

• EM1~EM3

One-touch memory dialing key. For speedcalling convenience, they provide memory dialing in either pulse or tone mode.



One-key redial

```
- Pulse mode

Tone mode

  (a) without */T
     Keyboard input: D1 D2 ... Dn R
     Dialing output: D1 D2 ... Dn TBRK TRP
                   D1 D2 ... Dn
     RM: D1 D2 ... Dn
     SAM: Unchanged
  (b) with */T
     Keyboard input: D1 D2 ... Dn */T Dn+1 ...
                    Dm R
     Dialing output: D_1 D_2 \dots D_n T_{P \to T} D_{n+1} \dots D_m
                       Pulse
                                          Tone
                    TBRK TRP D1 D2 ... Dn TP→T
                                 Pulse
                    Dņ+1 ... Dm
                       Tone
     RM: D1 D2 ... Dn */T Dn+1 ... Dm
     SAM: Unchanged
```

```
(a) without */T
Keyboard input: D1 D2 ... Dn R
Dialing output: D1 D2 ... Dn TBRK TRP D1 D2 ... Dn
RM: D1 D2 ... Dn
SAM: Unchanged
(b) with */T
Keyboard input: D1 D2 ... Dn * Dn+1 ... Dm
Dialing output: D1 D2 ... Dn * Dn+1 ... Dm
TBRK TRP D1 D2 ... Dn * Dn+1 ... Dm
RM: D1 D2 ... Dn * Dn+1 ... Dm
RM: D1 D2 ... Dn * Dn+1 ... Dm
SAM: Unchanged
```

Note: If the dialing number exceeds 32 digits, redialing is inhibited and $\overline{PO}=VDD$

```
• SA copy
```

```
- Pulse mode
                                                   - Tone mode
  (a) without */T
                                                     (a) without */T
     Keyboard input: D1 D2 ... Dn SA
                                                        Keyboard input: D1 D2 ... Dn SA
     Dialing output: D1 D2 ... Dn
                                                        Dialing output: D1 D2 ... Dn
     RM: D1 D2 ... Dn
                                                        RM: D1 D2 ... Dn
     SAM: D1 D2 ... Dn
                                                        SAM: D1 D2 ... Dn
                                                     (b) with */T
  (b) with */T
                                                        Keyboard input: D1 D2 ... Dn */T Dn+1 ...
     Keyboard input: D1 D2 ... Dn */T Dn+1 ...
                   Dm SA
                                                                       Dm SA
     Dialing output: D1 D2 ... Dn TP→T Dn+1 ... Dm
                                                         Dialing output: D1 D2 ... Dn * Dn+1 ... Dm
                       Pulse
                                         Tone
                                                         RM: D1 D2 ... Dn * Dn+1 ... Dm
     RM: D1 D2 ... Dn */T Dn+1 ... Dm
                                                         SAM: D1 D2 ... Dn * Dn+1 ... Dm
     SAM: D1 D2 ... Dn */T Dn+1 ... Dm
```

Note: The maximum capacity of the RM memory is 32 digits. When more than 32 digits plus the "SA" key are entered, the SAVE function will not be executed, and all the existing data in the save memory will not be changed.

15



• SA dialing

Pulse mode

(a) without */T
SAM content: D1 D2 ... Dn
Keyboard input: SA
Dialing output: D1 D2 ... Dn
RM: Unchanged
SAM: Unchanged
(b) with */T
SAM content: D1 D2 ... Dn */T Dn+1 ... Dm
Keyboard input: SA
Dialing output: D1 D2 ... Dn TP→T Dn+1 ... Dm
Fulse
RM: Unchanged
SAM: Unchanged

- Flash
 - Flash as a digital key

 (a) The intervenient key
 Keyboard input:
 D1D2 ... Dn F Dn+1 ...
 Dm

 Dialing output: D1 D2 ... Dn TF TFP Dn+1 ...
 Dm
 RM: D1 D2 ... Dn
 SAM: Unchanged
 (b) The first key
 Keyboard input: F D1D2 ... Dn
 Dialing output: TF TFP D1 D2 ... Dn
 RM: Unchanged
 SAM: Unchanged
 SAM: Unchanged

Tone mode

(a) without */T
SAM content: D1 D2 ... Dn
Keyboard input: SA
Dialing output: D1 D2 ... Dn
RM: Unchanged
SAM: Unchanged

(b) with */T

SAM content: D1 D2 ... Dn * Dn+1 ... Dm
Keyboard input: SA
Dialing output: D1 D2 ... Dn * Dn+1 ... Dm
RM: Unchanged
SAM: Unchanged
SAM: Unchanged

Flash as a control key
 Keyboard input: D1D2 ... Dn F Dn+1 ...
 Dm
 Dialing output: D1 D2 ... Dn TF TFP Dn+1 ...
 Dm
 RM: Dn+1 ... Dm
 SAM: Unchanged

Note: TF: break a flash time

Pause

Keyboard input: D1 D2 ... Dn [P or R/P] Dn+1 ... Dm Dialing output: D1 D2 ... Dn TP Dn+1 ... Dm RM: D1 D2 ... Dn P Dn+1 ... Dm SAM: Unchanged

16



Memory store

 Memory store without dialing output Keyboard input: <u>ST</u>[D1][D2]...[Dn][ST]<u>EMa</u> Dialing output: D1 D2 ... Dn RM: D1 D2 ... Dn SAM: Unchanged Memory store with dialing output
 Keyboard input: D1 D2 ... Dn ST ST EMa
 Dialing output: D1 D2 ... Dn
 RM: D1 D2 ... Dn
 SAM: Unchanged

Note: If the dialing number exceeds 32 digits, the memory store is inhibited. However, if the dialing number is not more than 32 digits the memory will store a max. of 16 digits. EMa=EM1~EM3

Memory dialing

EMa content: D1 D2 ... Dn Keyboard input: EMa Dialing output: D1 D2 ... Dn RM: D1 D2 ... Dn SAM: Unchanged

Note: EMa=EM1~EM3

Chain dialing

EM1 content: D1 D2 ... Dn EM2 content: Dn+1 ... Dm Keyboard input: D1 D2 D3 EM1 EM2 Dialing output: D1 D2 ... D3 D1 D2 ... Dn Dn+1 ... Dm EM1: Unchanged EM2: Unchanged RM: D1 D2 ... Dn SAM: Unchanged

Note: The maximum capacity of the RM memory is 32 digits. When the dialing number is over 32 digits, the redialing is inhibited and PO=VDD

17

Note:

RM: Redial memory SAM: Save dialing memory D1 D2 ... Dn: 0~9 Dn+1 ... Dm: 0~9, *, #



• IDD lock operation by the keyboard (2 lock numbers, 3 digits/number at maximum)

- Personal/Lock No.1/Lock No.2 input operation

(a) Personal code doesn't exist Stores Personal Code: ST D1 D2 D3 ST * 0 Stores Lock No.1: ST D4 D5 D6 ST * 1 Stores Lock No.2: ST D7 D8 D9 ST * 2 (b) Personal code exist Changes Personal Code: ST D1 D2 D3 ST # ST D4 D5 D6 ST * 0 (Old personal code) (New personal code) Changes Lock No.1: ST D1 D2 D3 ST # ST D4 D5 D6 ST * 1 (Personal code) (Lock No.1) Changes Lock No.2: ST D1 D2 D3 ST # ST D7 D8 D9 ST * 2 (Personal code) (Lock No.2) Changes Personal Code, Lock No.1 and Lock No.2 at one time ST D1 D2 D3 ST # ST D4 D5 D6 ST * 0 (continued) (Old personal code) (New personal code) ST D7 D8 D9 ST * 1 ST D10 D11 D12 ST * 2 (Lock No.1) (Lock No.2)

Personal/Lock No.1/Lock No.2 cancel operation

Cancels Personal code: ST D1 D2 D3 ST # ST # 0 Cancels Lock No.1: ST D1 D2 D3 ST # ST # 1 Cancels Lock No.2: ST D1 D2 D3 ST # ST # 2

 Temporary release both of the lock numbers (Lock No.1, Lock No.2): ST D1 D2 D3 ST # Dm Dm+1 Dm+2 DI ... Dn (Personal code)

18

Note: D1~D12 = 0~9 Dm Dm+1 Dm+2 = 0~9 DI ... Dn = 0~9, *, #

Note:

RM: Redial memory SAM: Save dialing memory D1 D2 ... Dn: 0~9 Dn+1 ... Dm: 0~9, *, # Dm+1 ... DI: 0~9, *, # Dl+1 ... DK: 0~9, *, #



High Impedance

Timing Diagrams

Normal dialing

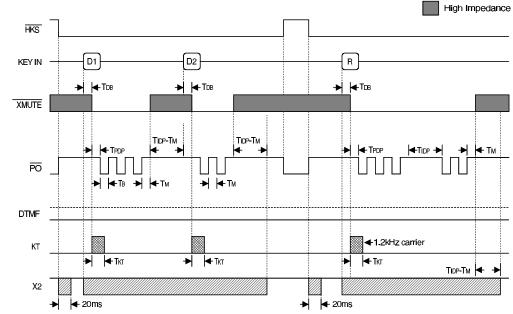
• Pulse mode

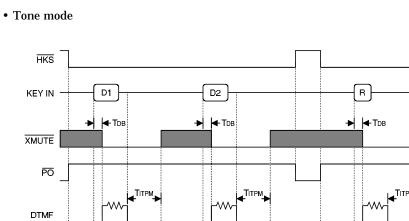
KΤ

X2

+

 20ms



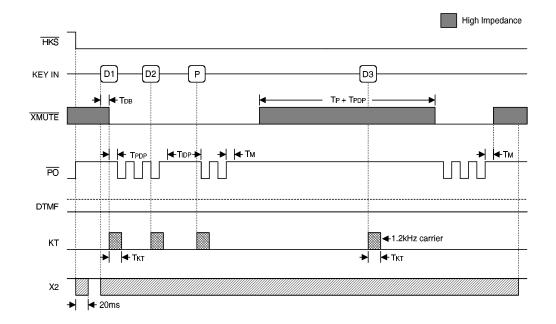


19

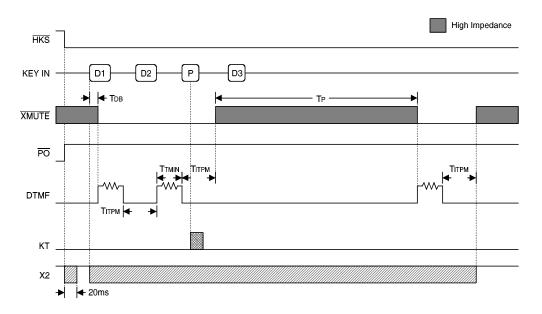


Dialing with pause key

• Pulse mode



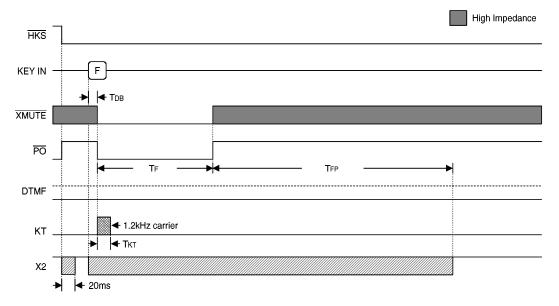
• Tone mode



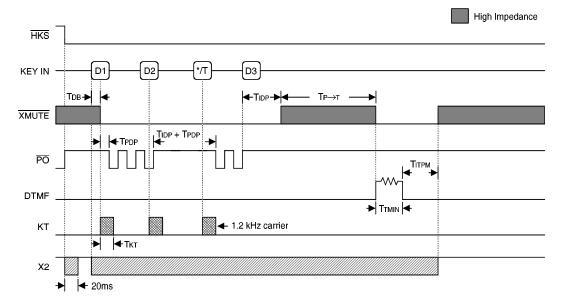
20



Flash key operation



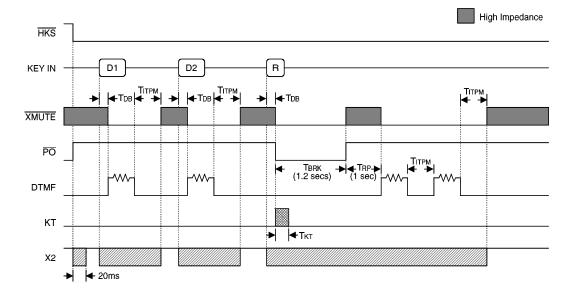


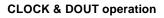


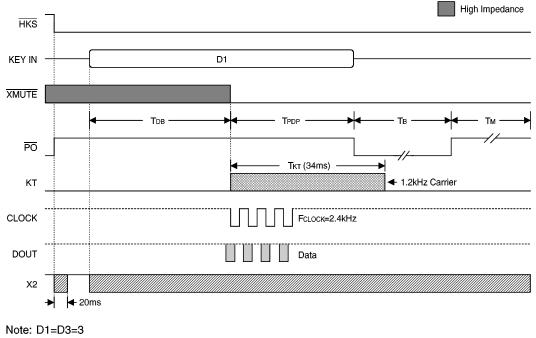
21



One key redial operation

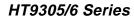






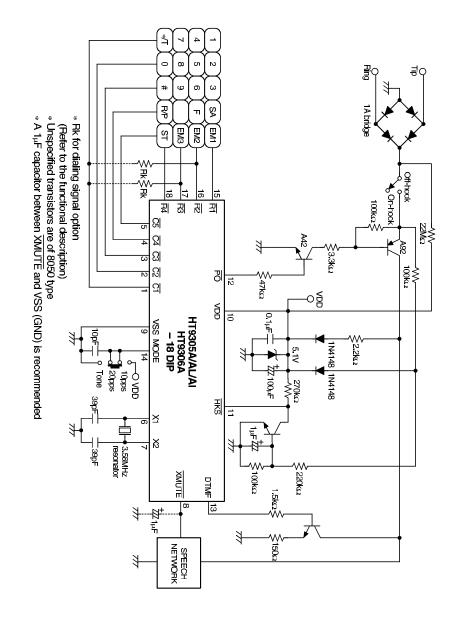
22

D2=2



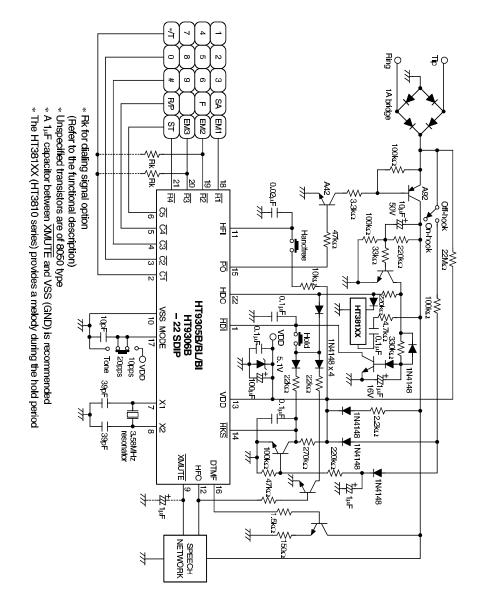


Application circuit 1



21st Jan '98

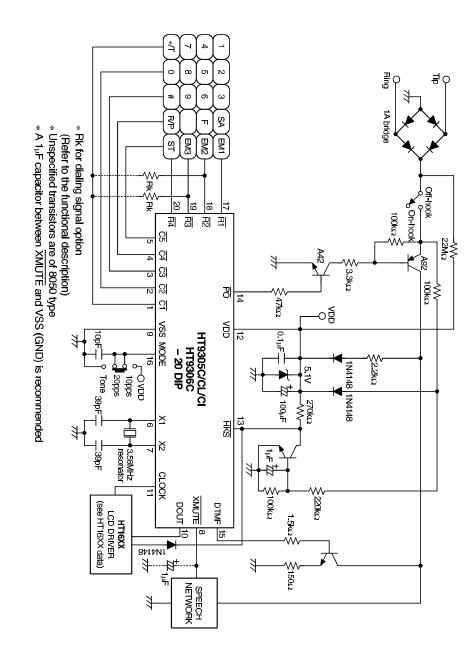




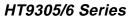
21st Jan '98



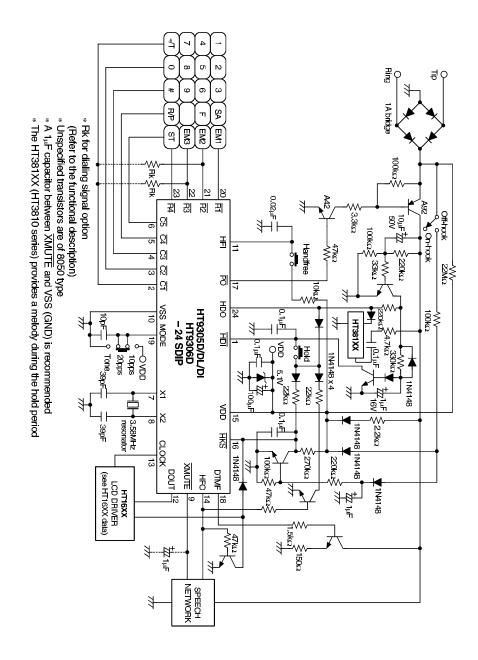




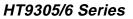
21st Jan '98



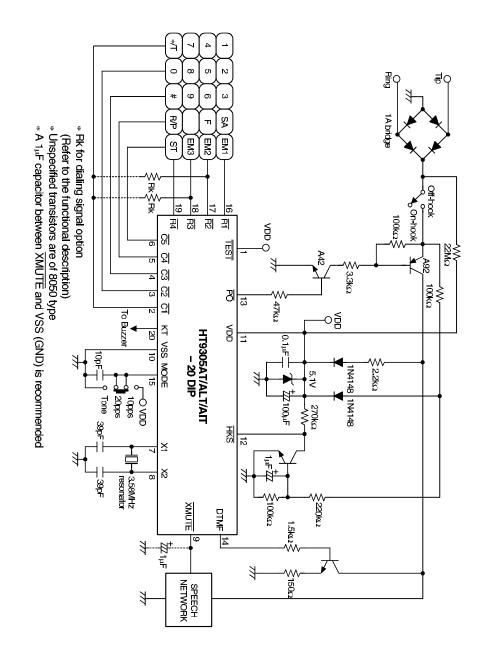




21st Jan '98

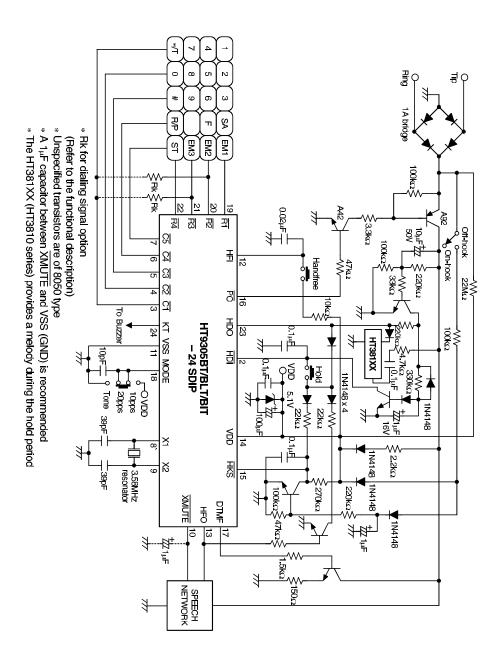




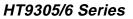


21st Jan '98

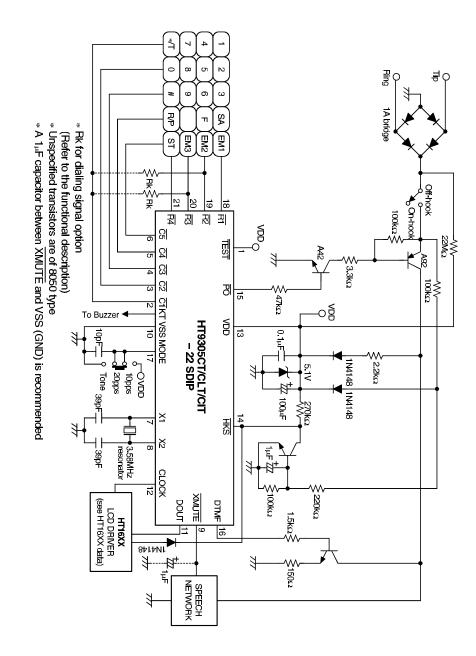




28

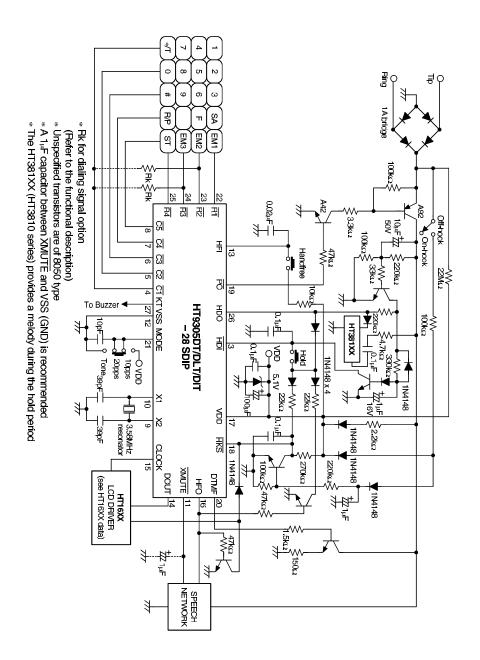






21st Jan '98





30