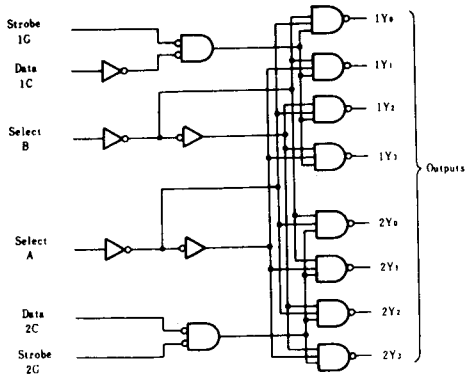
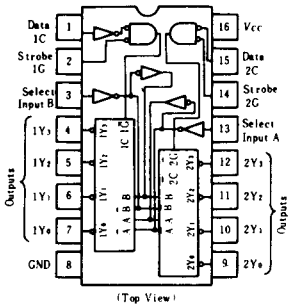
HD74LS155 ●Dual 2-line-to-4-line Decoders/Demultiplexers

This circuit features dual 1-line-to-4-line demultiplexer with individual strobes and common binary-address input. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating.

■BLOCK DIAGRAM



■PIN ARRANGEMENT



■FUNCTION TABLE

●2-line-to-4-line Decoder/1-line-to-4-line Demultiplexer

Inputs				Outputs			
Select		Strobe	Data				
B	A	1G	1C	$1Y_0$	$1Y_1$	$1Y_2$	$1Y_3$
×	×	H	×	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
×	×	×	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data				
B	A	2G	2C	$2Y_0$	$2Y_1$	$2Y_2$	$2Y_3$
×	×	H	×	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
×	×	×	H	H	H	H	H

●3-line-to-8-line Decoder/1-line-to-8-line Demultiplexer

Inputs				Outputs							
Select			Strobe Data	0	1	2	3	4	5	6	7
C	B	A	G	$2Y_0$	$2Y_1$	$2Y_2$	$2Y_3$	$1Y_0$	$1Y_1$	$1Y_2$	$1Y_3$
×	×	×	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

Notes) 1. C; input 1C and 2C connected together
2. G; inputs 1G and 2G connected together
3. H; high level, L; low level, X; irrelevant

HITACHI

Hitachi America Ltd. • 2210 O'Toole Ave. • San Jose, CA 95131 • (408) 435-8300

■ELECTRICAL CHARACTERISTICS ($Ta=-20\sim+75°C$)

Item	Symbol	Test Conditions		min	typ*	max	Unit
Input voltage	V_{IH}			2.0	–	–	V
	V_{IL}			–	–	0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	–	–	V
	V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$	–	–	0.4	V
			$I_{OL}=8mA$	–	–	0.5	
Input current	I_I	$V_{CC}=5.25V$, $V_I=7V$		–	–	0.1	mA
	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		–	–	20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		–	–	−0.4	mA
Short-circuit output current	I_{OS}	$V_{CC}=5.25V$		−5	–	−42	mA
Supply current**	I_{CC}	$V_{CC}=5.25V$		–	6.1	10	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		–	–	−1.5	V

* $V_{CC}=5V$, $Ta=25°C$

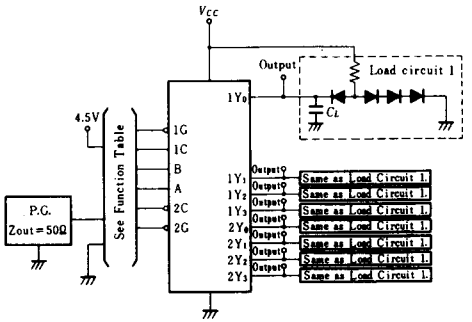
** I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5V, and 2C, 1G, and 2G inputs grounded.

■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

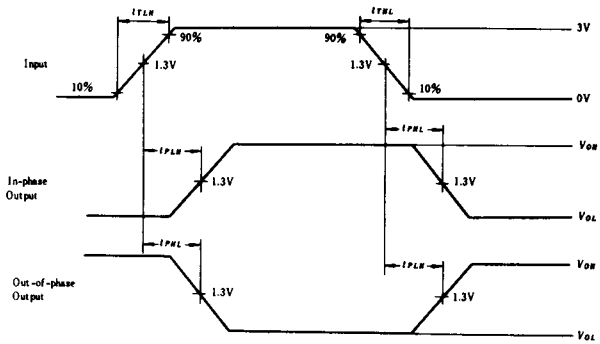
Item	Inputs	Output	Levels of logic	Test Conditions	min	typ	max	Unit
t_{PLH}	A, B, 2C	Y	2	$C_L=15pF$, $R_L=2k\Omega$	–	10	15	ns
t_{PHL}	1G or 2G				–	19	30	ns
t_{PLH}	A or B	Y	3		–	17	26	ns
t_{PHL}					–	19	30	ns
t_{PLH}	1C	Y	3		–	18	27	ns
t_{PHL}					–	18	27	ns

■TESTING METHOD

1) Test Circuit



Waveform



Notes) 1. Input pulse; $t_{TLH}\leqq 15ns$, $t_{THL}\leqq 6ns$, $PRR=1MHz$, duty cycle=50%
2. C_L includes probe and jig capacitance.
3. All diodes are 1S2074 Ⓗ.

PACKAGING INFORMATIONS

T-90-20

Factory orders for circuits described in this databook should include a three-part type number as explained in the following example.

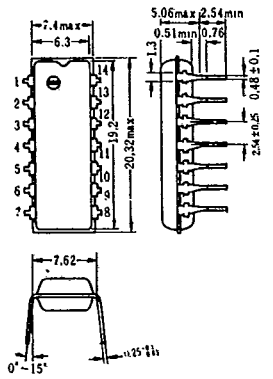
HD 74LS00 P

- Package ; Plastic DIP ; letters P
  Cerdip ; non-letters
- Circuit description
- Prefix : HD ; Hitachi Digital IC

■Plastic DIP

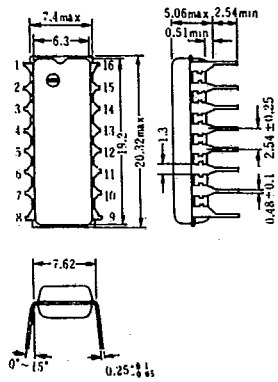
●14 Pin

DP-14



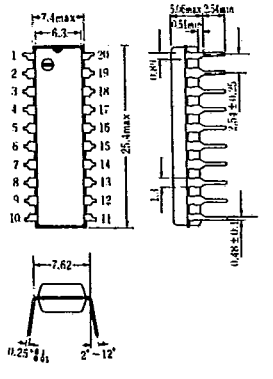
●16 Pin

DP-16



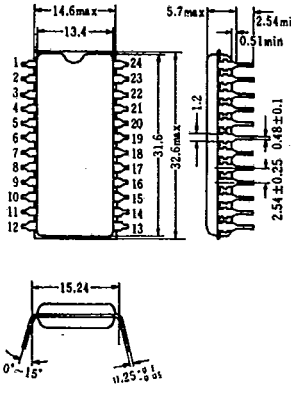
●20 Pin

DP-20



●24 Pin

DP-24



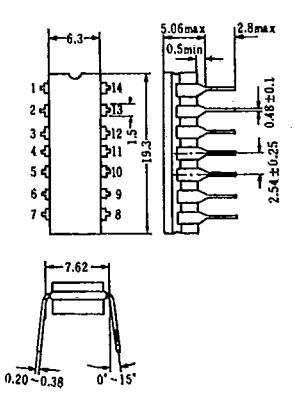
Hitachi America Ltd. • 2210 O'Toole Ave. • San Jose, CA 95131 • (408) 435-8300

PACKAGING INFORMATIONS

■Cerdip

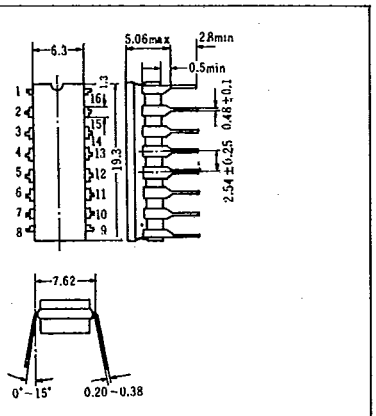
●14 Pin

DG-14



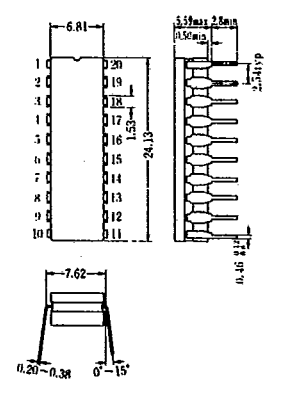
●16 Pin

DG-16



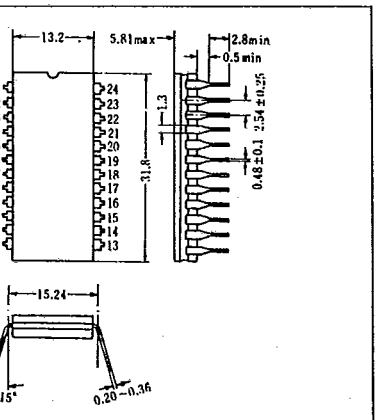
●20 Pin

DG-20



●24 Pin

DG-24



HITACHI
Hitachi America Ltd. • 2210 O'Toole Ave. • San Jose, CA 95131 • (408) 435-8300