T-46-23-08

CY7C171
CY7C172

CYPRESS SEMICONDUCTOR

4096 x 4 Static R/W RAM Separate I/O

Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed
  — t_{AA} = 25 ns
- Transparent Write (7C171)
- Low active power
  — 385 mW
- Low standby power
  — 83 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C171 and CY7C172 are high-performance CMOS static RAMs organized as 4096 by 4 bits with separate I/O. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 77% when deselected.

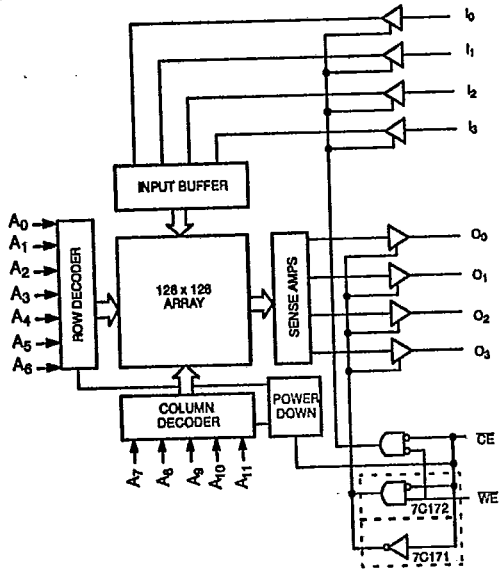
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four data output pins (O_0 through O_3).

The output pins stay in high-impedance state when write enable ($\overline{WE}$) is LOW (7C171 only), or chip enable ($\overline{CE}$) is HIGH.

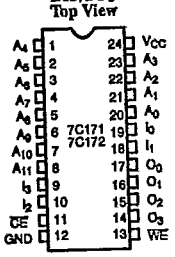
A die coat is used to insure alpha immunity.

Logic Block Diagram

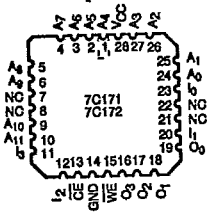


Pin Configurations

DIP/SOJ
Top View



LCC
Top View



Selection Guide

		7C171–25 7C172–25	7C171–35 7C172–35	7C171–45 7C172–45
Maximum Access Time (ns)		25	35	45
Maximum Operating Current (mA)	Commercial	90	90	70
	Military		90	70

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

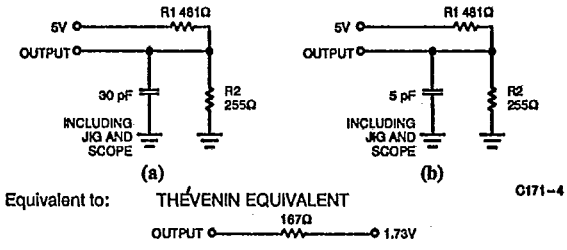
Parameters	Description	Test Conditions		7C171−25 7C172−25 Min.	7C171−25 7C172−25 Max.	7C171−35 7C172−35 Min.	7C171−35 7C172−35 Max.	7C171−45 7C172−45 Min.	7C171−45 7C172−45 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−50	+50	−50	+50	−50	+50	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		90		90		70	mA
			Mil		90		90		70	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Com'l		20		20		15	mA
			Mil		40		20		20	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V	Com'l		15		15		15	mA
			Mil		40		20		20	mA

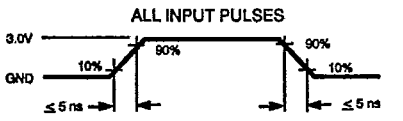
Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters

AC Test Loads and Waveforms





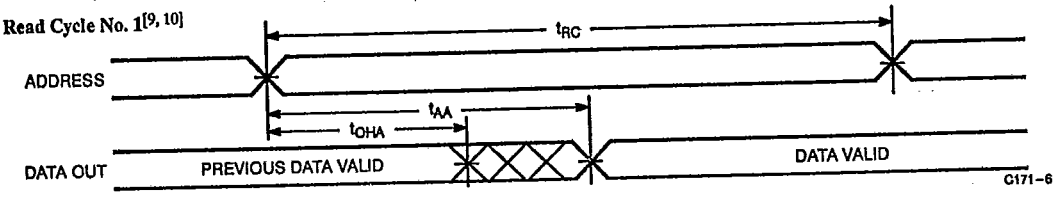
Switching Characteristics Over the Operating Range[2, 5]

Parameters	Description	7C171–25 7C172–25		7C171–35 7C172–35		7C171–45 7C172–45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		10		20		20	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		25		25		30	ns
t_{RCS}	Read Command Set-Up	0		0		0		ns
t_{RCH}	Read Command Hold	0		0		0		ns
WRITE CYCLE[8]								
t_{WC}	Write Cycle Time	25		35		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	25		30		35		ns
t_{AW}	Address Set-Up to Write End	20		30		35		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		30		ns
t_{SD}	Data Set-Up to Write End	10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		3		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6] (7C172)	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7] (7C172)		10		5		20	ns
t_{AWE}	$\overline{WE}$ LOW to Data Valid (7C171)		25		30		35	ns
t_{ADV}	Data Valid to Output Valid (7C171)		25		30		35	ns

Notes:
5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
7. t_{HZCE} and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CE}$ = V_{IL}.

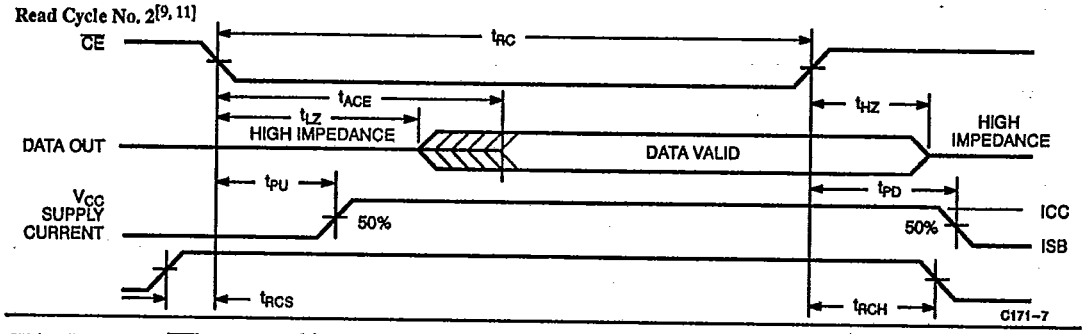
Switching Waveforms

Read Cycle No. 1[9, 10]

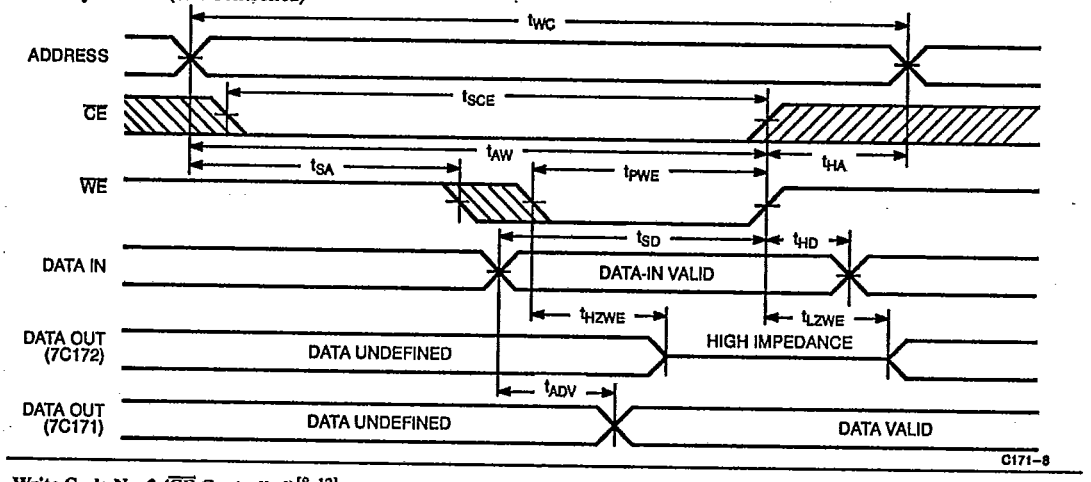


Switching Waveforms

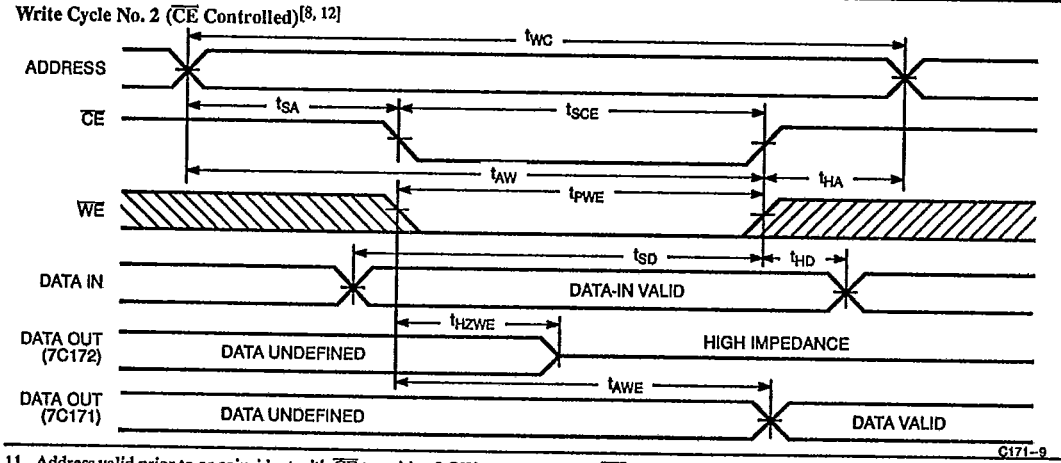
Read Cycle No. 2[9, 11]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[8]



Write Cycle No. 2 ($\overline{CE}$ Controlled)[8, 12]

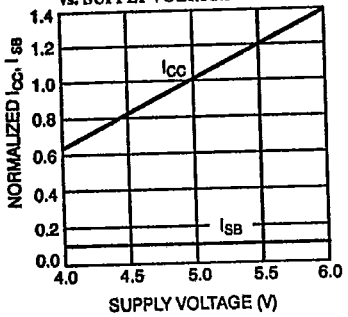


11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

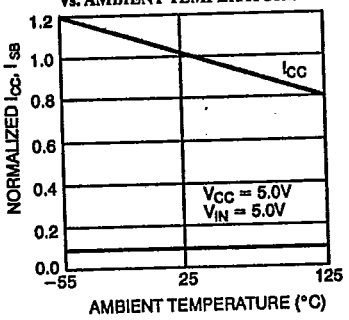
12. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state (7C172).

Typical DC and AC Characteristics

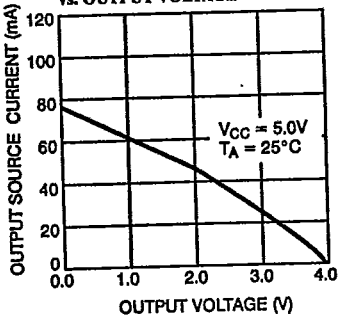
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



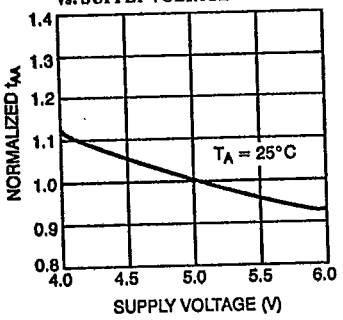
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



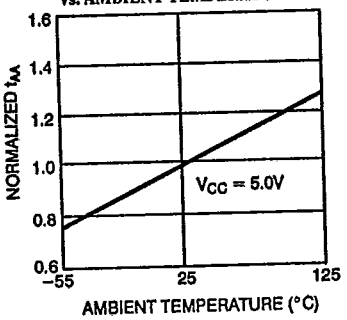
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



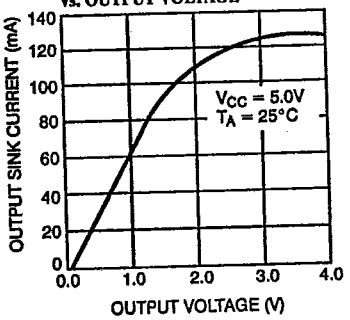
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



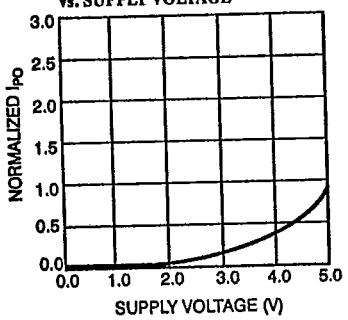
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



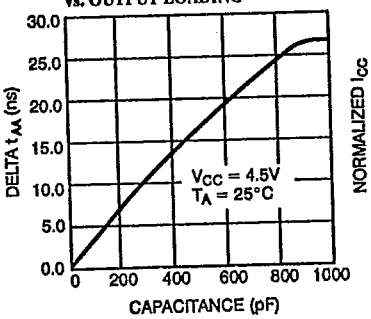
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



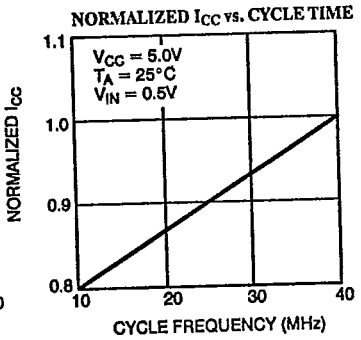
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C171–25PC	P13	Commercial
	CY7C171–25DC	D14	
	CY7C171–25LC	L64	
	CY7C171–25VC	V13	
35	CY7C171–35PC	P13	Commercial
	CY7C171–35DC	D14	
	CY7C171–35LC	L64	
	CY7C171–35VC	V13	
	CY7C171–35DMB	D14	Military
	CY7C171–35LMB	L64	
45	CY7C171–45PC	P13	Commercial
	CY7C171–45DC	D14	
	CY7C171–45LC	L64	
	CY7C171–45VC	V13	
	CY7C171–45DMB	D14	Military
	CY7C171–45LMB	L64	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C172–25PC	P13	Commercial
	CY7C172–25DC	D14	
	CY7C172–25LC	L64	
	CY7C172–25VC	V13	
35	CY7C172–35PC	P13	Commercial
	CY7C172–35DC	D14	
	CY7C172–35LC	L64	
	CY7C172–35VC	V13	
	CY7C172–35DMB	D14	Military
	CY7C172–35LMB	L64	
45	CY7C172–45PC	P13	Commercial
	CY7C172–45DC	D14	
	CY7C172–45LC	L64	
	CY7C172–45VC	V13	
	CY7C172–45DMB	D14	Military
	CY7C172–45LMB	L64	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{RCS}	7, 8, 9, 10, 11
t_{RCH}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{AWE}[13]	7, 8, 9, 10, 11
t_{ADV}[13]	7, 8, 9, 10, 11

Note:
13. 7C171 only.

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