Am29841/Am29843

High Performance Bus Interface Latches

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High speed parallel latches**
  - Noninverting transparent t_{PD} = 5.25 ns typ
  - Inverting transparent t_{PD} = 6.0 ns typ
- **Buffered common latch enable, clear and preset input**
- **Three-state outputs glitch free during power-up and down**
- **Outputs have Schottky clamp to ground**
- **48 mA Commercial I_{OL}**
- **Low input/output capacitance**
  - 6 pF inputs (typical)
  - 8 pF outputs (typical)
- **I_{OH} specified 2.0 V and 2.4 V**
- **24-pin 0.3" space saving package**
- **Fully TTL compatible inputs and outputs**
- **IMOX™ high performance IMplanted OXide isolated process**

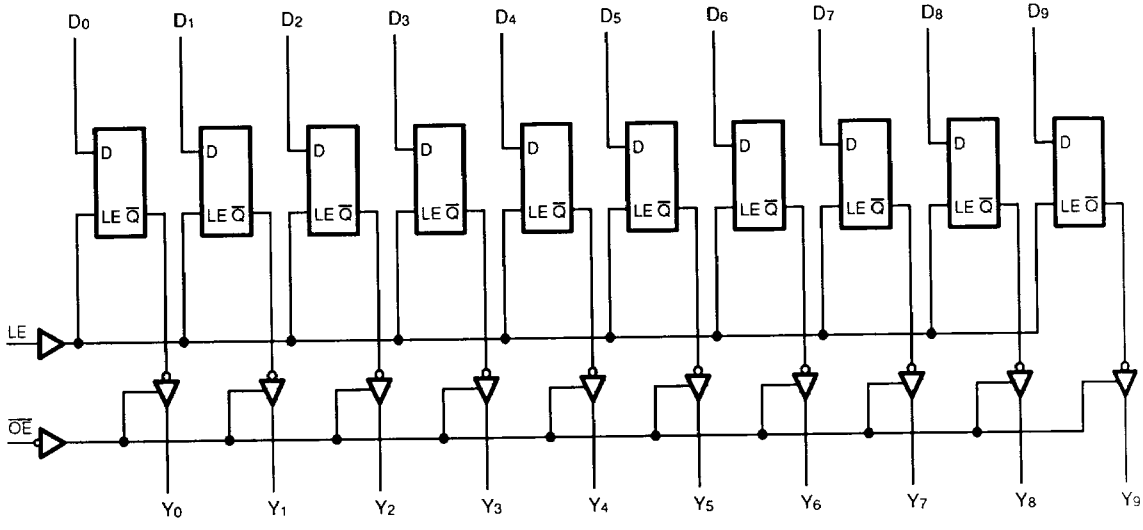
GENERAL DESCRIPTION

The Am29841/843 bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The Am29841 is a buffered, 10-bit wide version of the popular '373 function. The Am29843 is a 9-bit wide buffered latch with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high performance systems.

All of the Am29800 high performance interface family is designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

BLOCK DIAGRAMS

Am29841



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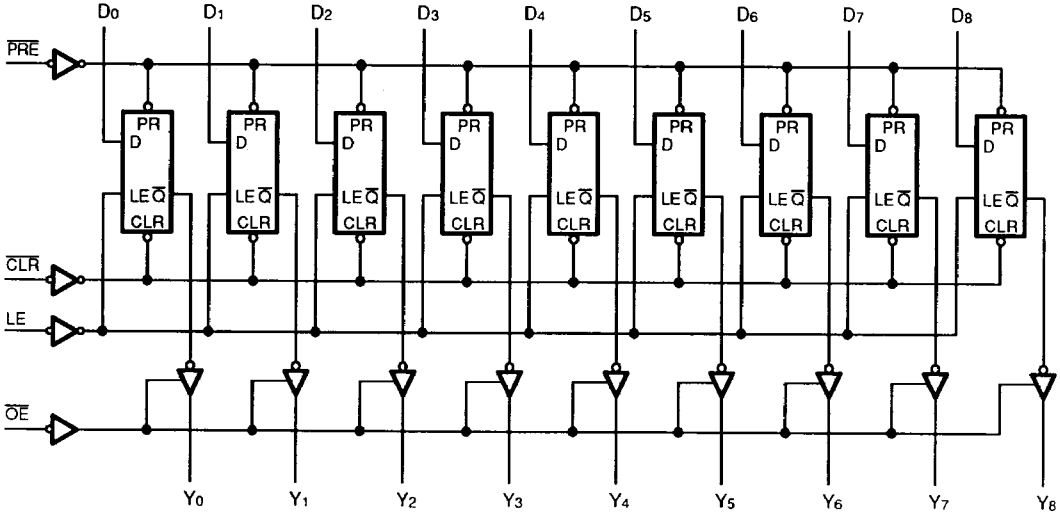
Publication# 01972 Rev. D Amendment/0
Issue Date: December 1990

BLOCK DIAGRAMS (Continued)
Am29843



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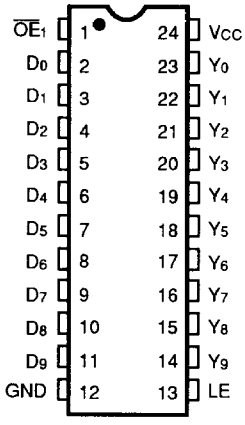
CONNECTION DIAGRAMS
Top View

Am29841

DIP



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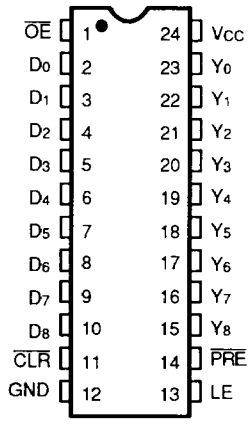
Am29843

DIP



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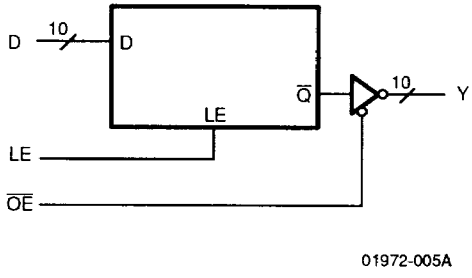
LOGIC SYMBOLS

Am29841
10-Bit Latch



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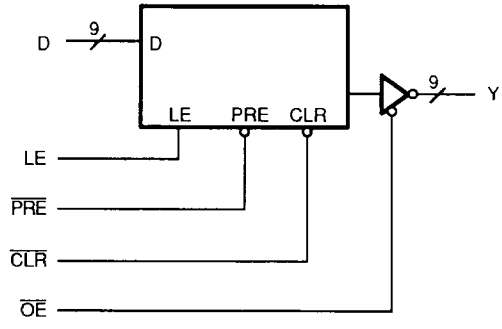
Am29843
9-Bit Latch



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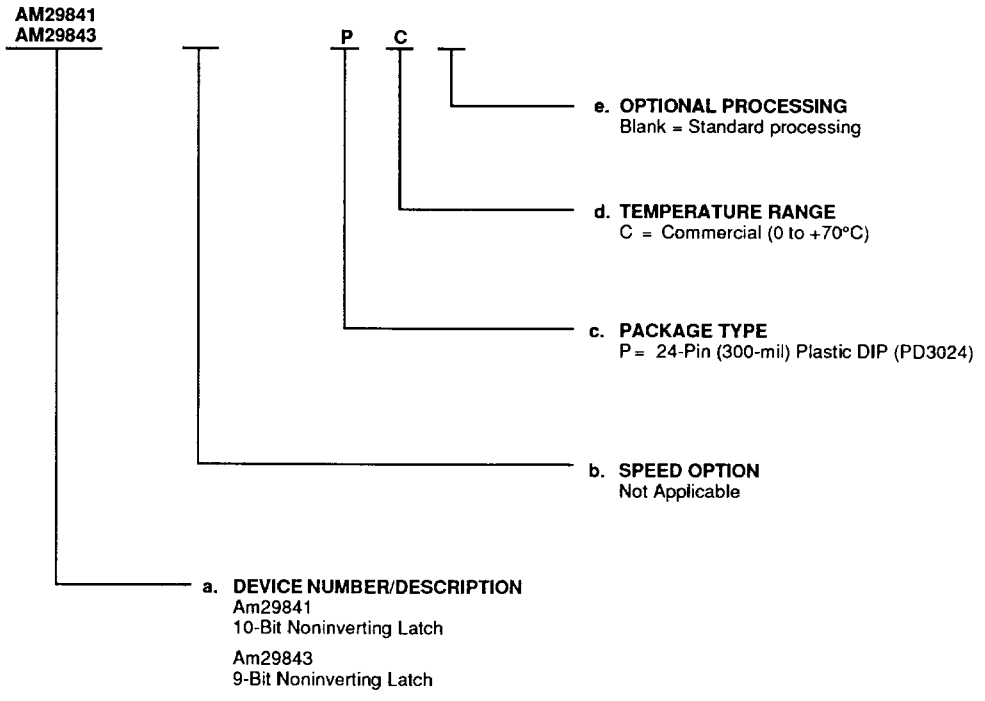
ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29841	PC
AM29843	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

$\overline{CLR}$

When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.

D_i

The latch data inputs.

LE

The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.

Y_i

The 3-state latch outputs.

$\overline{OE}$

The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs Y_i are in the high-impedance (off) state.

$\overline{PRE}$

Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.

FUNCTION TABLES

Am29841

Inputs			Internal	Outputs	
$\overline{OE}$	LE	D_i	$\overline{Q}_i$	Y_i	Function
H	X	X	X	Z	Hi–Z
H	H	L	H	Z	Hi–Z
H	H	H	L	Z	Hi–Z
H	L	X	NC	Z	Latched (Hi-Z)
L	H	L	H	L	Transparent
L	H	H	L	H	Transparent
L	L	X	NC	NC	Latched

Am29843

Inputs					Internal	Outputs	
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_i	$\overline{Q}_i$	Y_i	Function
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	L	H	Z	Hi-Z
H	H	H	H	H	L	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	L	H	L	Transparent
H	H	L	H	H	L	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	L	H	Preset
L	H	L	X	X	H	L	Clear
L	L	L	X	X	L	H	Preset
L	H	H	L	X	L	Z	Latched (Hi-Z)
H	L	H	L	X	L	Z	Latched (Hi-Z)

H = HIGH
L = LOW
X = Don't Care
NC = No Change
Z = High Impedance

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +5.5 V
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	100 mA
DC Input Current	−30 mA to +5.0 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0°C to +70°C
Supply Voltage (V_{CC})	5.0 V ± 10% 4.5 V to 5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V	I_{OH} = −15 mA	2.4		V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = −24 mA	2.0		
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48 mA		0.5	V
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0		V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	V
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA			−1.2	V
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = 0.4 V			−1.0	mA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V			50	µA
I_I	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V			1.0	mA
I_{OZ}	Output Off-State (Hi-Z)	V_{CC} = 5.5 V	V_O = 0.4 V		−50	µA
	Output Current		V_O = 2.4 V		50	
I_{SC}	Output Short Circuit Current (Note 1)	V_{CC} = 5.5 V		−75	−250	mA
I_{CC}	Supply Current	V_{CC} = 5.5 V	Over Temperature Range		120	mA
		Outputs Open	+70°C		110	

Note:

1. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0 V)

Parameter Symbol	Parameter Description		Test Conditions (Note 1)	Min.	Typ.	Max.	Unit
t_{PLH}	Data (D_i) to Output Y_i (LE = HIGH)		C_L = 50 pF	3.5	5.7	8	ns
t_{PHL}				3.5	6.2	8	ns
t_{PLH}			C_L = 300 pF		10	13	ns
t_{PHL}					10	13	ns
t_S	Data to LE Setup Time		C_L = 50 pF	2.0	–0.2		ns
t_H	Data to LE Hold Time			2.5	0.7		ns
t_{PLH}	Latch Enable (LE) to Y_i		C_L = 50 pF		8	10.5	ns
t_{PHL}					7.5	10	ns
t_{PLH}			C_L = 300 pF			15	ns
t_{PHL}						15	ns
t_{PLH}	Propagation Delay, Preset to Y_i		C_L = 50 pF		6.5	9	ns
t_S	Preset Recovery ($\overline{PRE}$ ↓) Time				7.3	12	ns
t_{PHL}	Propagation Delay, Clear to Y_i				15	18	ns
t_S	Clear Recovery ($\overline{CLR}$ ↓) Time				7.8	12	ns
t_{PWH}	LE Pulse Width	HIGH	C_L = 50 pF	4	2.5		ns
t_{PWL}	Preset Pulse Width	LOW		5			ns
t_{PWL}	Clear Pulse Width	LOW		6			ns
t_{ZH}	Output Enable Time $\overline{OE}$ ↓ to Y_i		C_L = 300 pF			17	ns
t_{ZL}						21	ns
t_{ZH}			C_L = 50 pF		7.3	12	ns
t_{ZL}					9.7	12	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ↑ to Y_i		C_L = 50 pF		10.4	14	ns
t_{LZ}					4.7	11	ns
t_{HZ}			C_L = 5 pF (Note 2)		3.4	8	ns
t_{LZ}					3.8	8	ns

Notes:

1. See test circuit and waveforms (Chapter 2).
2. Not tested.

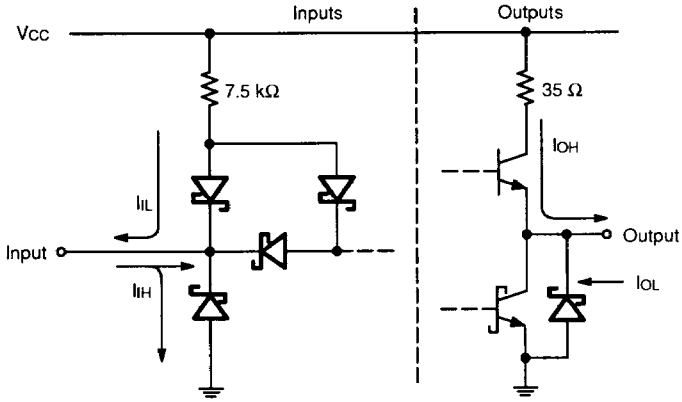
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description		Test Conditions (Note 1)	Min.	Max.	Unit
t_{PLH}	Data (D_i) to Output Y_i (LE = HIGH)		C_L = 50 pF	3.5	9.5	ns
t_{PHL}				3.5	9.5	ns
t_{PLH}			C_L = 300 pF		12.5	ns
t_{PHL}					13	ns
t_S	Data to LE Setup Time		C_L = 50 pF	2.5		ns
t_H	Data to LE Hold Time			2.5		ns
t_{PLH}	Latch Enable (LE) to Y_i		C_L = 50 pF		12	ns
t_{PHL}					12	ns
t_{PLH}			C_L = 300 pF		16	ns
t_{PHL}					16	ns
t_{PLH}	Propagation Delay, Preset to Y_i		C_L = 50 pF		12	ns
t_S	Preset Recovery ($\overline{PRE}$ ↓) Time				14	ns
t_{PHL}	Propagation Delay, Clear to Y_i				21	ns
t_S	Clear Recovery ($\overline{CLR}$ ↓) Time				14	ns
t_{PWH}	LE Pulse Width	HIGH	C_L = 50 pF	6		ns
t_{PWL}	Preset Pulse Width	LOW		8		ns
t_{PWL}	Clear Pulse Width	LOW		8		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ↓ to Y_i		C_L = 300 pF		20	ns
t_{ZL}					23	ns
t_{ZH}			C_L = 50 pF		14	ns
t_{ZL}					14	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ↑ to Y_i		C_L = 50 pF		15	ns
t_{LZ}					12	ns
t_{HZ}			C_L = 5 pF		9	ns
t_{LZ}					9	ns

Note:

1. See test circuit and waveforms (Chapter 2).

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



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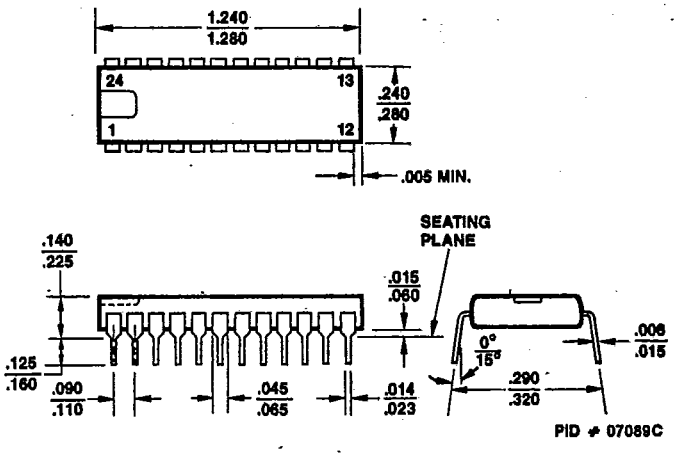
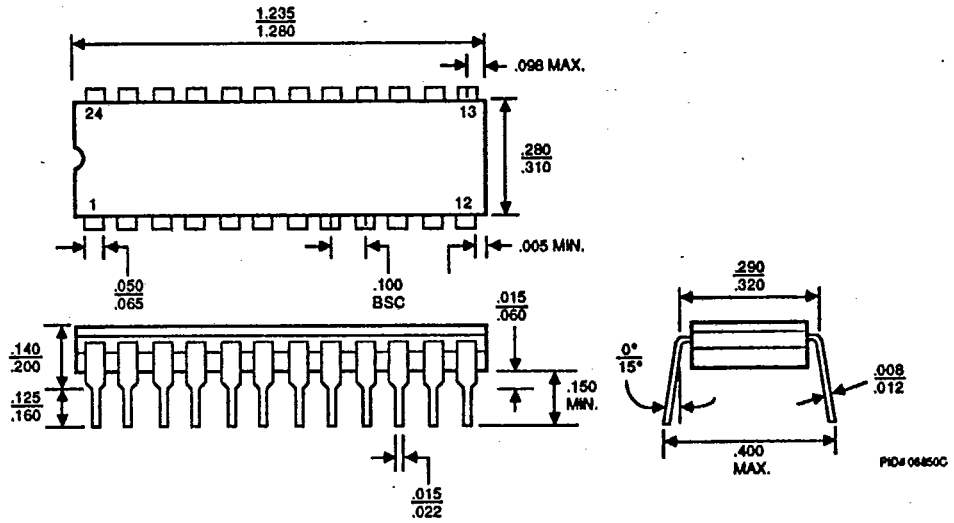
PACKAGE OUTLINES*

T-90-20

PD3024



CD3024

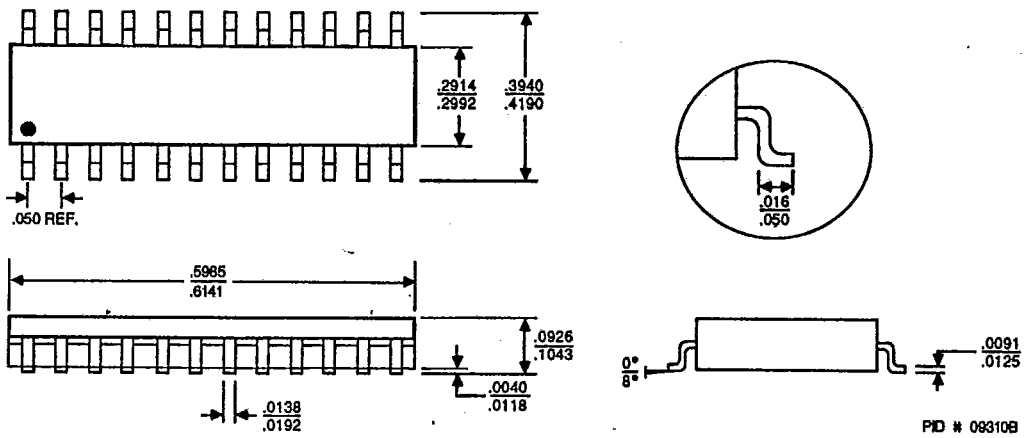


*For reference only.

PACKAGE OUTLINES (Cont'd.)

T-90-20

SO 024



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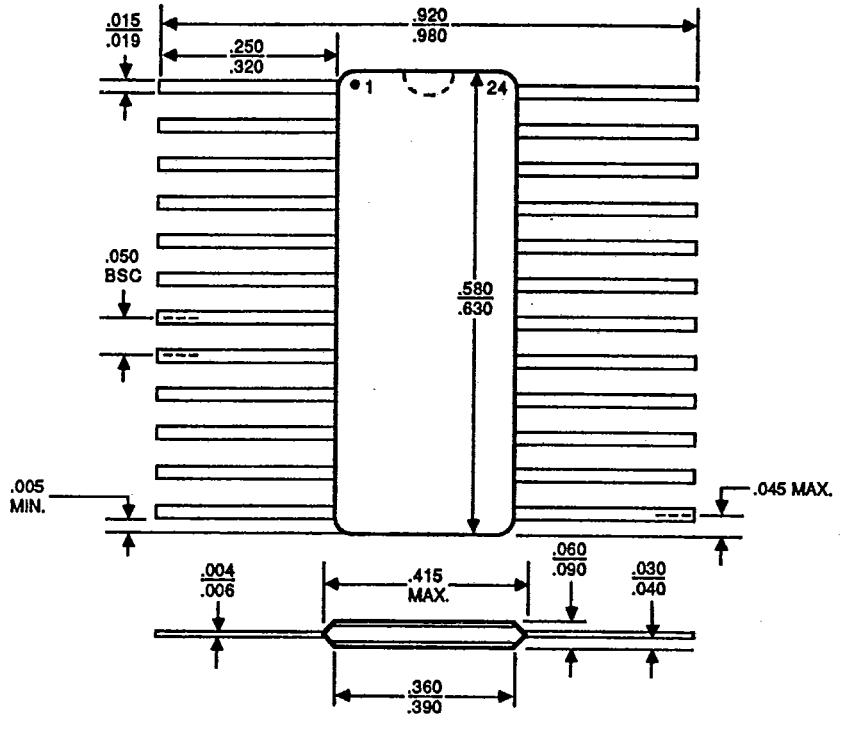
CFM024



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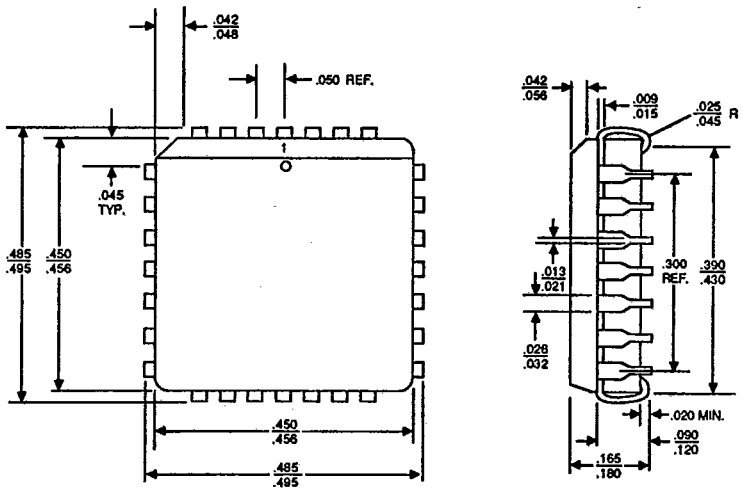
PACKAGE OUTLINES (Cont'd.)

T-90-20

PL 028



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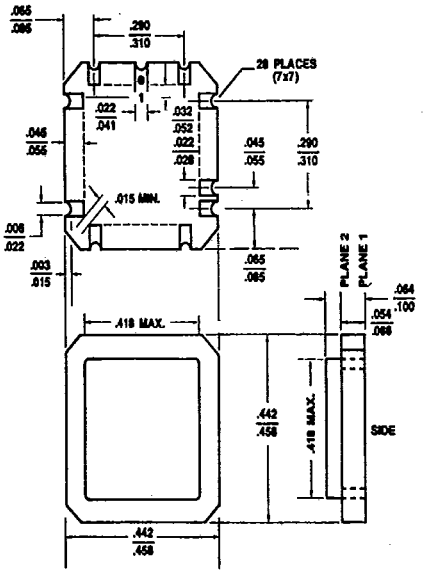

PID # 06595D

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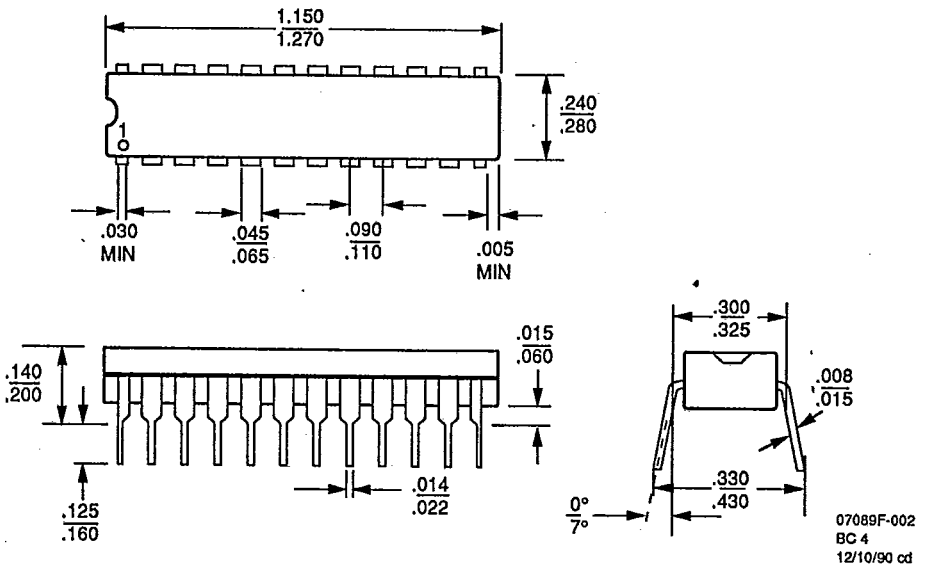
T-90-20

PD3024
24-Pin 300-mil Plastic SKINNYDIP



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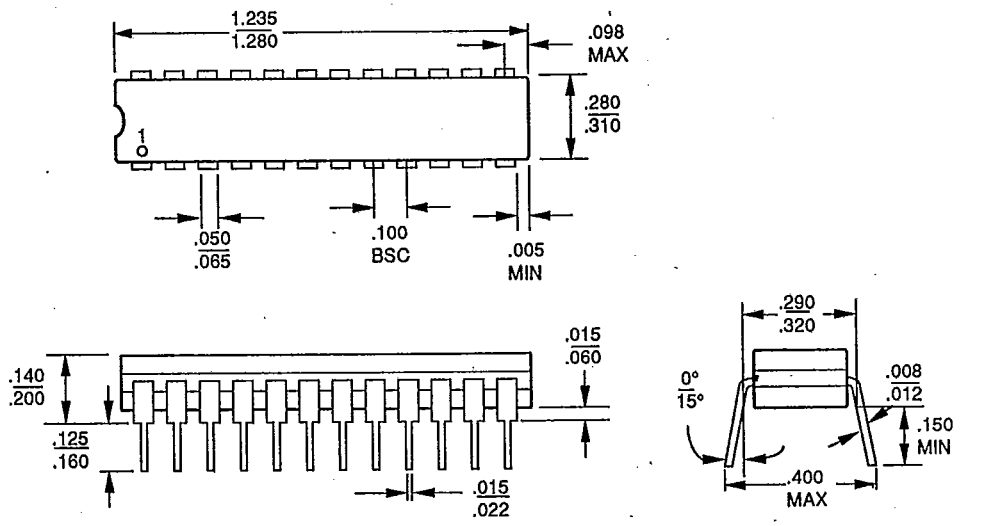
BC 4
12/10/90 cd

Note:
For reference only. All dimensions measured in inches. BSC is an ANSI standard for Basic Space Centering.

CD3024
24-Pin 300-mil Ceramic SKINNYDIP



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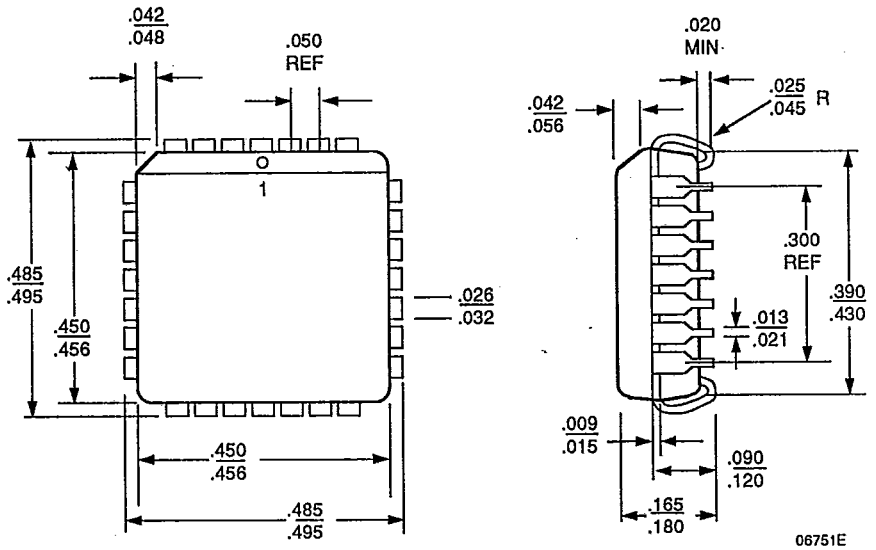
PL 028
28-Pin Plastic Leaded Chip Carrier



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SO 024
24-Pin Plastic Small Outline Package

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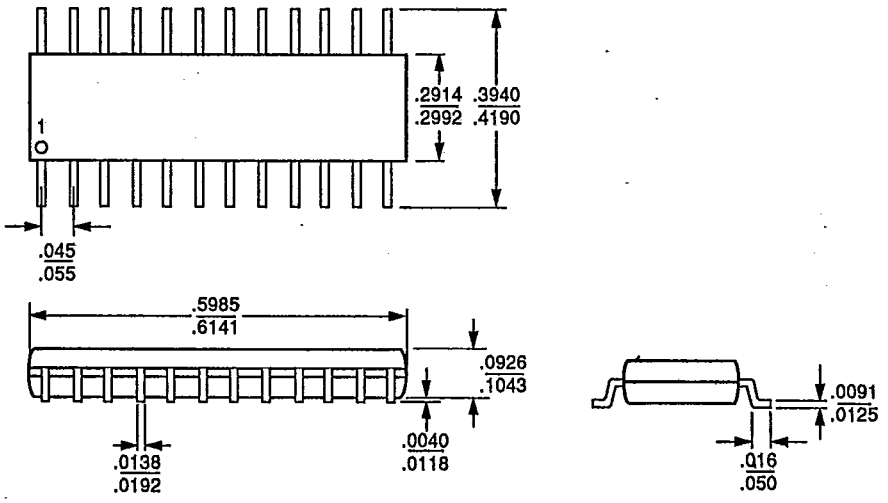

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