CLOCK GENERATOR AND DRIVER FOR 8080A PROCESSORS

DESCRIPTION

The μPB8224 is a single chip clock generator and driver for 8080A processors. The clock frequency is determined by a user specified crystal and is capable of meeting the timing requirements of the entire 8080A family of processors. MOS and TTL level clock outputs are generated.

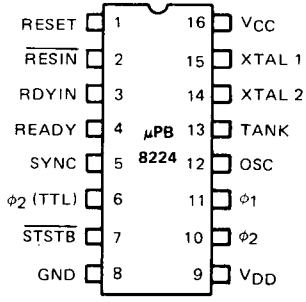
Additional logic circuitry of the μPB8224 provides signals for power-up reset, an advance status strobe and properly synchronizes the ready signal to the processor. This greatly reduces the number of chips needed for 8080A systems.

The μPB8224 is fabricated using NEC's Schottky bipolar process.

FEATURES

- Crystal Controlled Clocks
- Oscillator Output for External Timing
- MOS Level Clocks for 8080A Processor
- TTL Level Clock for DMA Activities
- Power-up Reset for 8080A Processor
- Ready Synchronization
- Advanced Status Strobe
- Reduces System Package Count
- Available in 16-pin Cerdip and Plastic Packages

PIN CONFIGURATION



PIN NAMES

$\overline{RESIN}$	Reset Input
RESET	Reset Output
RDYIN	Ready Input
READY	Ready Output
SYNC	Sync Input
$\overline{STSTB}$	Status STB Output
φ1	Processor Clocks
φ2	
XTAL 1	Crystal Connections
XTAL 2	
TANK	Used With Overtone Crystal
OSC	Oscillator Output
φ2 (TTL)	φ2 CLK (TTL Level)
V_{CC}	+5V
V_{DD}	+12V
GND	0V

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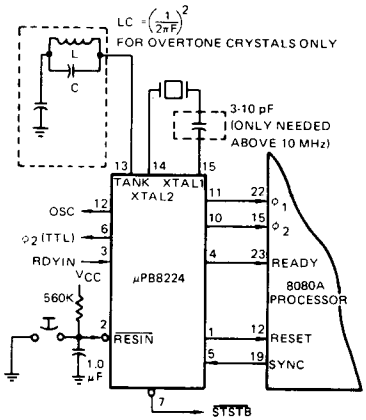
Clock Generator

The clock generator circuitry consists of a crystal controlled oscillator and a divide-by-nine counter. The crystal frequency is a function of the 8080A processor speed and is basically nine times the processor frequency, i.e.:

$$\text{Crystal frequency} = \frac{9}{t_{CY}}$$

where t_{CY} is the 8080A processor clock period.

A series resonant fundamental mode crystal is normally used and is connected across input pins XTAL1 and XTAL2. If an overtone mode crystal is used, an additional LC network, AC coupled to ground, must be connected to the TANK input of the μPB8224 as shown in the following figure.



The formula for the LC network is:

$$LC = \left(\frac{1}{2\pi F}\right)^2$$

where F is the desired frequency of oscillation.

The output of the oscillator is input to the divide-by-nine counter. It is also buffered and brought out on the OSC pin, allowing this stable, crystal controlled source to be used for derivation of other system timing signals. The divide-by-nine counter generates the two non-overlapping processor clocks, ϕ_1 and ϕ_2, which are buffered and at MOS levels, a TTL level ϕ_2 and internal timing signals.

The ϕ_1 and ϕ_2 high level outputs are generated in a 2-5-2 digital pattern, with ϕ_1 being high for two oscillator periods, ϕ_2 being high for five oscillator periods, and then neither being high for two oscillator periods. The TTL level ϕ_2,ϕ_2 (TTL), is normally used for DMA activities by gating the external device onto the 8080A bus once a Hold Acknowledge (HLDA) has been issued.

Additional Logic

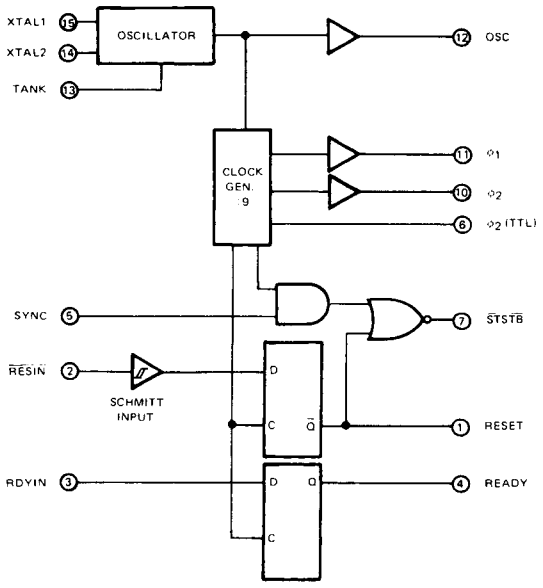
In addition to the clock generator circuitry, the μPB8224 contains additional logic to aid the system designer in the proper timing of several interface signals.

The $\overline{\text{STSTB}}$ signal indicates, at the earliest possible moment, when the status signals output from the 8080A processor are stable on the data bus. $\overline{\text{STSTB}}$ is designed to connect directly to the μPB8228 System Controller and automatically resets the μPB8228 during power-on Reset.

The $\overline{\text{RESIN}}$ input to the μPB8224 is used to automatically generate a RESET signal to the 8080A during power initialization. The slow rise of the power supply voltage in an external RC network is sensed by an internal Schmitt Trigger. The output of the Schmitt Trigger is gated to generate an 8080A compatible RESET. An active low manual switch may also be attached to the RC circuit for manual system reset.

The RDYIN input to the μPB8224 accepts an asynchronous "wait request" and generates a READY output to the 8080A that is fully synchronized to meet the 8080A timing requirements.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
All Output Voltages (TTL) . . . . . −0.5 to +7 Volts
All Output Voltages (MOS) . . . . . −0.5 to +13.5 Volts
All Input Voltages . . . . . −1.0 to +7 Volts
Supply Voltage V_{CC} . . . . . −0.5 to +7 Volts
Supply Voltage V_{DD} . . . . . −0.5 to +13.5 Volts
Output Currents . . . . . 100 mA

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a 0°C to +70°C; V_{CC} = +5V ±5%; V_{DD} = +12V ±5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Current Loading	I_F			−0.25	mA	V_F = 0.45V
Input Leakage Current	I_R			10	μA	V_R = 5.25V
Input Forward Clamp Voltage	V_C			−1.0	V	I_C = −5 mA
Input "Low" Voltage	V_{IL}			0.8	V	V_{CC} = 5.0V
Input "High" Voltage	V_{IH}	2.6			V	Reset Input
		2.0				All Other Inputs
RESIN Input Hysteresis	V_{IH}-V_{IL}	0.25			V	V_{CC} = 5.0V
Output "Low" Voltage	V_{OL}			0.45	V	(Φ_1, Φ_2), Ready, Reset, STSTB
						I_{OL} = 2.5 mA
				0.45	V	All Other Inputs
						I_{OL} = 15 mA
Output "High" Voltage	V_{OH}					
Φ_1, Φ_2		9.4			V	I_{OH} = −100 μA
READY, RESET		3.6			V	I_{OH} = −100 μA
All Other Outputs		2.4			V	I_{OH} = −1 mA
Output Short Circuit Current (All Low Voltage Outputs Only)	I_{SC} ①	−10		−60	mA	V_O = 0V, V_{CC} = 5.0V
Power Supply Current	I_{CC}			115	mA	
Power Supply Current	I_{DD}			12	mA	

Note: ① Caution, Φ_1 and Φ_2 output drivers do not have short circuit protection

CAPACITANCE①

T_a = 25°C; f = 1 MHz; V_{CC} = 5V; V_{DD} = 12V; V_{BIAS} = 2.5V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			8	pF	

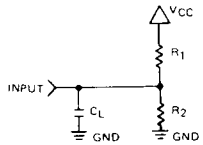
Note: ① This parameter is not 100% tested.

AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ±5%; V_{DD} = +12V ±5%

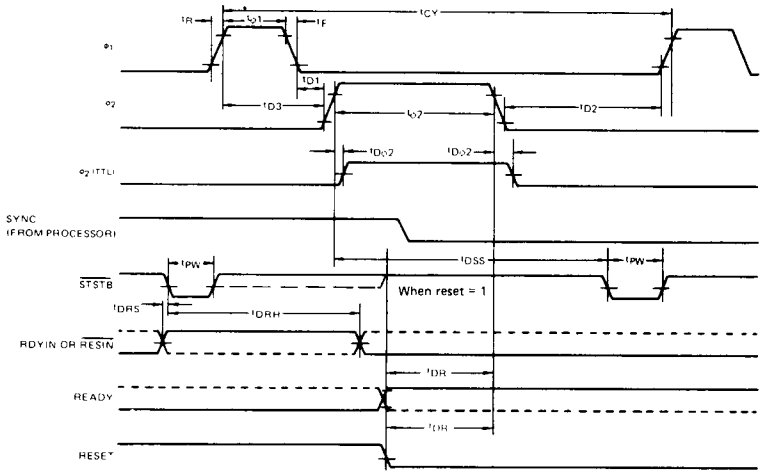
PARAMETER	SYMBOL	LIMITS ①			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
ϕ_1 Pulse Width	$t_{\phi 1}$	$\frac{2t_{CY}}{9}$ −20 ns			ns	C_L = 20 pF to 50 pF
ϕ_2 Pulse Width	$t_{\phi 2}$	$\frac{5t_{CY}}{9}$ −35 ns				
ϕ_1 to ϕ_2 Delay	t_{D1}	0				
ϕ_2 to ϕ_1 Delay	t_{D2}	$\frac{2t_{CY}}{9}$ −14 ns				
ϕ_1 to ϕ_2 Delay	t_{D3}	$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9}$ +20 ns		
ϕ_1 and ϕ_2 Rise Time	t_R			20		
ϕ_1 and ϕ_2 Fall Time	t_F			20		
ϕ_2 to ϕ_2 (TTL) Delay	$t_{D\phi 2}$	−5		+15	ns	ϕ_2 TTL, CL = 30 pF R_1 = 300Ω R_2 = 600Ω
ϕ_2 to $\overline{STSTB}$ Delay	t_{DSS}	$\frac{6t_{CY}}{9}$ −30 ns		$\frac{6t_{CY}}{9}$	ns	$\overline{STSTB}$, CL = 15 pF R_1 = 2K R_2 = 4K
$\overline{STSTB}$ Pulse Width	t_{PW}	$\frac{t_{CY}}{9}$ −15 ns			ns	
RDYIN Setup Time to $\overline{STSTB}$	t_{DRS}	50 ns − $\frac{4t_{CY}}{9}$				
RDYIN Hold Time After $\overline{STSB}$	t_{DRH}	$\frac{4t_{CY}}{9}$				
READY or RESET to ϕ_2 Delay	t_{DR}	$\frac{4t_{CY}}{9}$ −25 ns			ns	Ready and Reset CL = 10 pF R_1 = 2K R_2 = 4K
Crystal Frequency	f_{CLK}		$\frac{9}{t_{CY}}$		MHz	
Maximum Oscillating Frequency	f_{MAX}			27	MHz	

Note ① t_{CY} represents the processor clock period



TEST CIRCUIT

TIMING WAVEFORMS



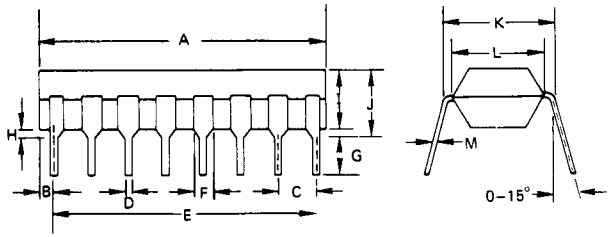
Voltage Measurement Points: ϕ_1, ϕ_2 Logic "0" = 1.0V, Logic "1" = 8.0V.
All other signals measured at 1.5V.

CRYSTAL REQUIREMENTS

Tolerance	0.005% at 0°C–70°C
Resonance	Series (Fundamental) ①
Load Capacitance	20-35 pF
Equivalent Resistance	75-20 ohms
Power Dissipation (Min)	4 mW

Note: ① With tank circuit use 3rd overtone mode.

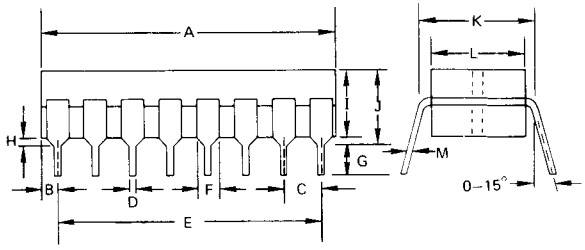
PACKAGE OUTLINE μPB8224C



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX	0.76 MAX
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.02 MIN
I	4.05 MAX	0.16 MAX
J	4.55 MAX	0.18 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

μPB8224D



(CERDIP)

ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.8	0.27
M	$0.25^{+0.10}_{-0.05}$	$0.0098^{+0.0039}_{-0.0019}$

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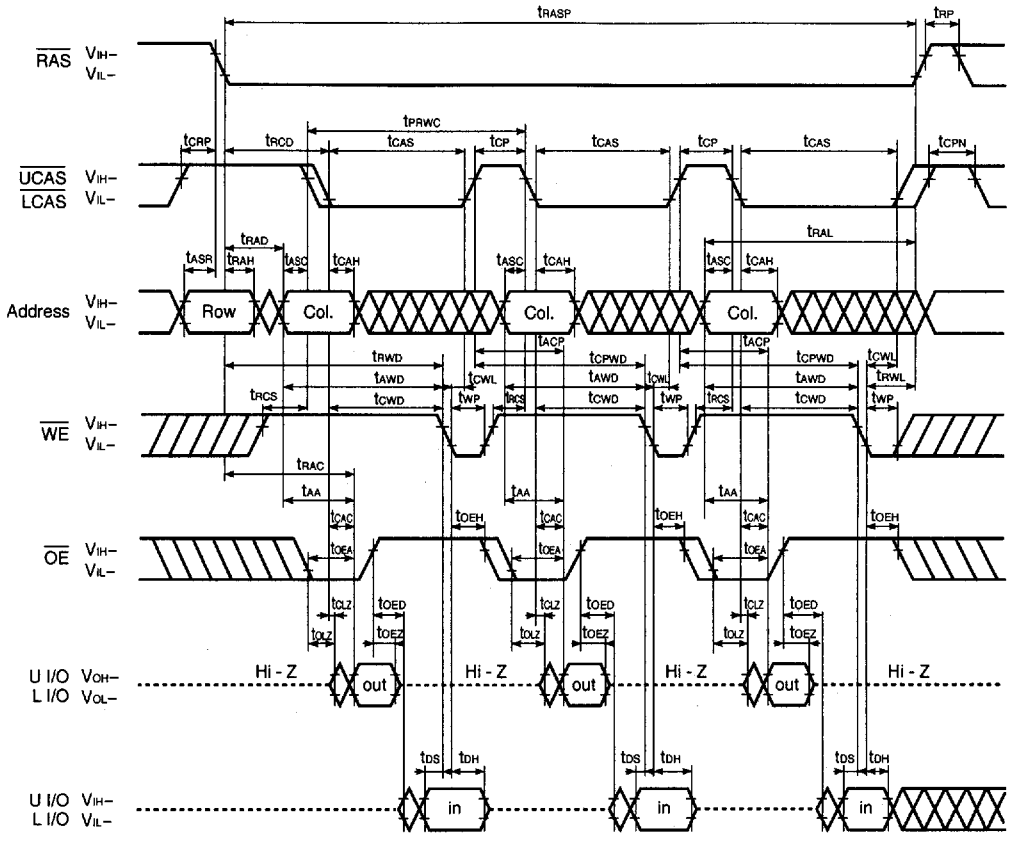
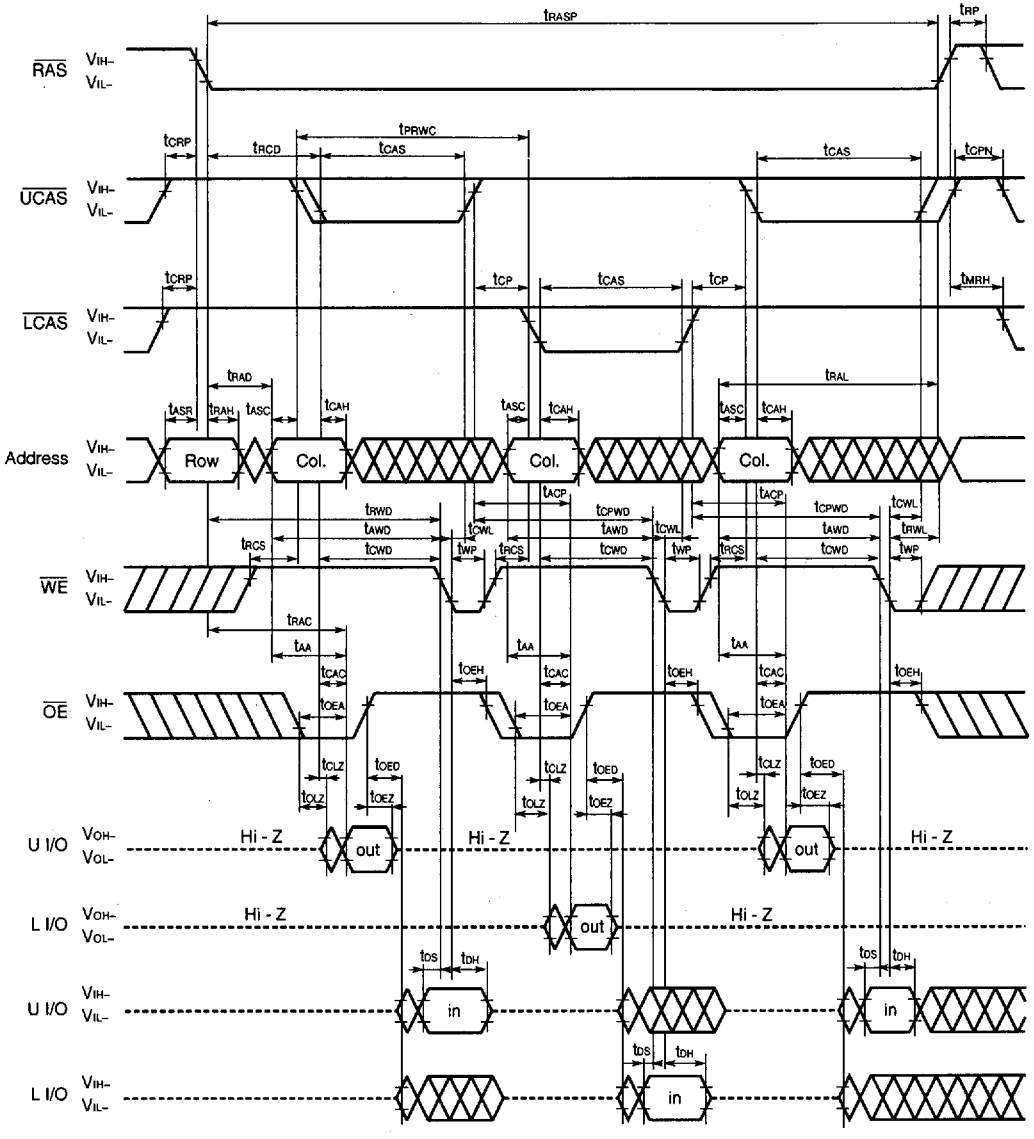
Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

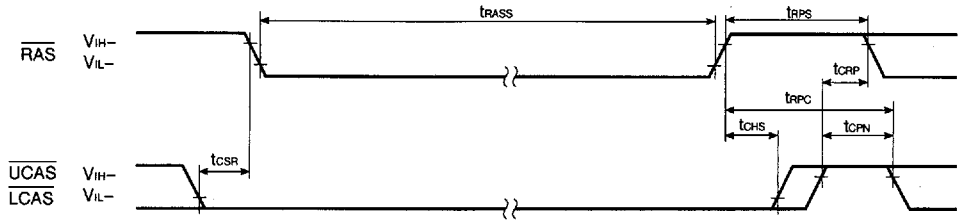
Fast Page Mode Byte Read Modify Write Cycle



Remarks 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S18160)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

μPD42S18160: 1,024 times within a 16 ms interval

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

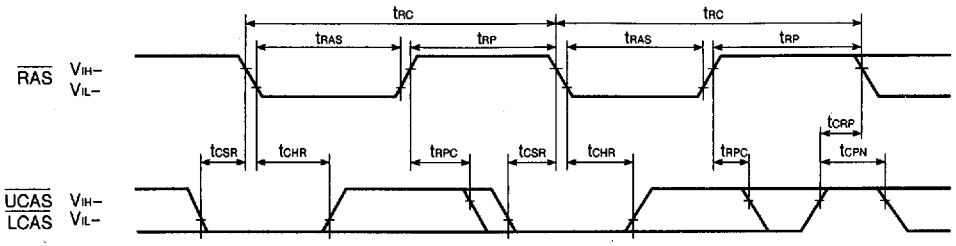
μPD42S18160: 1,024 times within a 16 ms interval

(3) If $t_{RASS\ (MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100\ \mu s$), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If $10\ \mu s < t_{RAS} < 100\ \mu s$, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles as follows should be met.

μPD42S18160: 1,024 times within a 128 ms interval

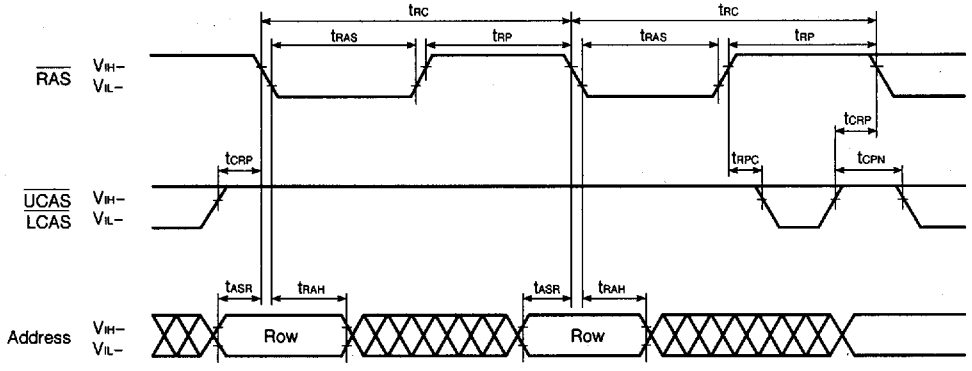
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle



Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)