T-75-07-15

PBM 3911
Voice-switched Speakerphone Circuit

Description

The PBM 3911 is a CMOS integrated circuit, designed for voice switched speakerphone systems. The circuit incorporates complementary digitally controlled attenuators for the necessary half duplex behavior, microphone and receive amplifiers, transmit and receive level detectors and an advanced background noise reduction system. A 4-bit analogue-to-digital converter implements a voltage controlled volume-setting. The background noise reduction system uses a DC converted noise signal to increase the microphone threshold, ensuring proper operation of the voice switch even in a noisy environment. The same signal is used to attenuate the microphone channel, thereby suppressing the background noise.

A three-state Disable / Enable / Mic. mute input provides a privacy function combined with a disable function, facilitating co-operation with µ-processors etc.

Key Features

- Input amplifiers in both channels.
- Incorporates all necessary level detection circuitry.
- Digitally controlled ramping of the attenuators giving a howling free, constant and linear response with no switch over clicks.
- A/D-converter providing a linear volume control.
- 50 dB attenuation range in each channel.
- Easy and independent trimming of parameters, using few external components.
- Low power CMOS (I_{DD}< 2 mA).
- 24-pin plastic skinny-DIP package (300 mil wide).

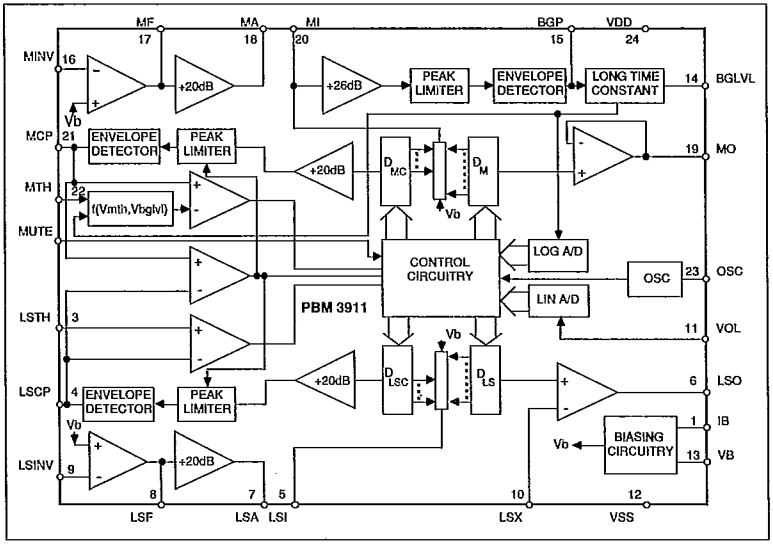
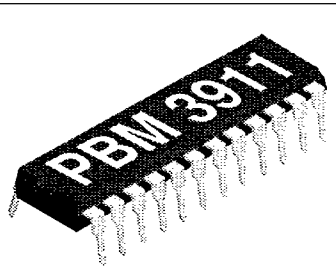


Figure 1. Block diagram.



24-pin plastic DIP

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PBM 3911

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Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	6.0	V
Storage temperature	T_{Stg}	-55	+125	°C
Operating ambient temperature	T_{Amb}	-15	+70	°C
Voltage on any pin (Note 1)	V_{In}	V_{ss} -0.3	V_{DD} +0.3	V
DC-current MO and LSO	I_{DC}		10	mA

Electrical Characteristics

At T_{Amb} = +25 °C using test circuit of fig. 3 unless otherwise noted.

Parameter		Ref. fig.	Conditions	Min	Typ	Max	Unit
Attenuators DM, DLS, DMC, DLSC							
Maximum input voltage	V_{In}		V_{DD} = 5V, R_{Bias} = 120 kohm				
			THD < 2% (DM, DLS), R_L = 10 kohm		3.0		V_{PP}
Note 2			V_{DD} = 3.5 V, R_{Bias} = 120 kohm				
			THD < 2% (DM, DLS), R_L = 10 kohm		1.5		V_{PP}
Input impedance, (Note 2), R_{MI}, R_{LSI}				30			kohm
Range of attenuation, (Table 1)			V_{VOLI} = 0V				
DM, DLS					0-50		dB
DMC, DLSC					0-25		dB
Nominal attenuation	DM		0 dB setting				
	DLS		R_L = 10 kohm	0	0.1	0.3	dB
Total harmonic distortion	DM		V_{DD} = 3.0 V, I_{Bias} = 16 µA				
	DLS		V_{In} = 1.0 V_{pp}, R_L = 10 kohm			2	%
Output impedance	Z_{MO}		I_{Bias} = > 16 µA		1		ohm
	Z_{LSO}		f_{In} = 1 kHz		10		ohm
Output noise voltage at M0 Psophometric wheighted relative to 1V_{rms}	V_{Psoph}				-90	-80	dB
Microphone/receive amplifier							
Equivalent input offset voltage	V_{OS}					20	mV
Input leakage current	I_{MINV}					5	nA
	I_{LSINV}					5	nA
Open loop voltage gain	G_{MF}		RF = ∞		80		dB
	G_{LSF}		I_{Bias} = 16 µA		80		dB
	G_{MA}		RF=R_{inv}-2 kohm=20 kohm		20		dB
	G_{LSA}		I_{Bias} = 16µA		20		dB
Gain Bandwidth product	GB_{MF}			2	4.5		MHz
	GB_{LSF}		f_{In}= 1 kHz, RF = ∞, I_{Bias}= 16µA	2	4.5		MHz
-3dB Bandwidth	BW_{MA}		AV= (0+20) dB		0.2		MHz
	BW_{LSA}		RF=R_{inv}- 2kohm, I_{Bias}=16µA		0.2		MHz
Output impedance	Z_{MF}		I_{Bias} > 10µA		2		kohm
	Z_{LSF}		f_{In}=1 kHz		2		kohm
	Z_{MA}				10		ohm
	Z_{LSA}				10		ohm
Total harmonic distortion	V_{MA}		AV= 20dB+20dB			2	%
	V_{LSA}		f_{In}= 1 kHz, V_{pp}= 3.0 V			2	%
			I_{Bias}= 16µA, R_L=R_{In}=40kohm				
Equivalent input noise voltage	V_{OS}		Psophometric weighted relative to 1 V_{rms}	-100		-94	dBV
Power supply rejection ratio	P_{SRR}		f=25kHz		-65		dB

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Parameter		Ref. fig.	Conditions	Min	Typ	Max	Unit
Speaker amplifier							
Open loop voltage gain	G_{LSO}		I_{Bias}=16µA, R_{LSO}=10kohm		80		dB
Gain bandwidth product	BW_{LSO}		f_{in}=1kHz		180		kHz
Output current	I_{LSO}		V_{DD}=5.0V, V_{LSO}=4.5V_{pp}		1		mA
Input leakage current	I_{LSX}					5	nA
Peakdetector output accuracy	V_{MCP}					1.0	dB
	V_{LSCP}					1.0	dB
Offset error	V_{MCP}					10	mV
	V_{LSCP}					10	mV
Settling time	t_{MCP}		C_{MCP}=C_{LSCP}=10nF			1	ms
	t_{LSCP}		f_{in}=1kHz, f_{Osc}=25kHz			1	ms
Equivalent pulldown resistor	R_{MCP}		f_{Osc}=25kHz		10		Mohm
	R_{LSCP}				10		Mohm
Peak limit voltage	V_{MCP}		V_{MCP}>V_{LSCP}		10•V_{MTH}		V
			V_{MCP}<V_{LSCP}		12•V_{MTH}		V
	V_{LSCP}		V_{LSCP}>V_{MCP}		10•V_{MTH}		V
			V_{LSCP}<V_{MCP}		12•V_{MTH}		V
Comparator inputs	**MTH, LSTH**						
Input offset voltage	V_{MTH}					10	mV
	V_{LSTH}					10	mV
Input resistance			f_{Osc}=25kHz				
	R_{MTH}				10		Mohm
	R_{LSTH}				10		Mohm
Input capacitance						20	pF
	C_{MTH}						
	C_{LSTH}					20	pF
Peak detector output BCP							
Offset error voltage	V_{BGP}					10	mV
Settling time	t_{Set}		C_{BCP}=10nF, f_{in}=1kHz, f_{Osc}=25kHz			1	ms
Equivalent pulldown resistor	R_{BGP}		f_{Osc}=25kHz		12		Mohm
Peak limit voltage	V_{BGP}				4•V_{MTH}		V
Background noise level detector							
Input offset voltage	V_{BGPVL}					10	mV
Reset time	t_{Res}		C_{BGPVL}=470nF		100		ms
Equivalent pulldown resistor	R_{BGP}		f_{Osc}=25kHz		12		Mohm
Disable / Enable / Mic. mute							
Disable voltage	V_{Dis}		V_{DD}=3.0V	V_{DD}-0.5			V
Disable current	I_{Dis}					10	µA
Enable voltage	V_{EN}			+1.2		V_{DD}-1.2	V
Enable current	I_{EN}				1		µA
Microphone mute voltage	V_{Mute}					V_{SS}+0.5	V
Microphone mute current	I_{Mute}			-10			µA
Disable voltage	V_{Dis}		V_{DD}=5.0V	V_{DD}-0.5			V
Disable current	I_{Dis}					30	µA
Enable voltage	V_{En}			+2		V_{DD}-2	V
Enable current	I_{En}					1	µA
Microphone mute voltage	V_{Mute}					V_{SS}+0.5	V
Microphone mute current	I_{Mute}			-30			µA
Input capacitance	C_{In}					20	pF

Parameter		Ref. fig.	Conditions	Min	Typ	Max	Unit
Clock oscillator							
Oscillator frequency	f_{Osc}		R_{CL}=470kohm C_{CI}=220pF, V_{DD}=3.0-5.5V	23.7	25	26.5	kHz
Temperture coefficient						±10	ppm/ °C
Volume control, V_{VOLI}							
Control range					0-22.6		dB
Volume voltage	V_{Voli}		0dB	0		0.01 •V_{DD}	
			-22.6 dB		0.5 •V_{DD}		
Equivalent Input resistance	R_{In}		f_{Osc}=25kHz		50		Mohm
Input capacitance	C_{In}					20	pF
Power supply							
Recommended supply voltage	V_{DD}			3.0		5.5	V
DC supply current	I_{DD}		V_{DD}=5V, R_{Bias}=220kohm, R_{LSO}=100kohm		1.9	2.5	mA
			V_{DD}=3V, R_{Bias}=120kohm, R_{LCSO}=100kohm		0.9		mA
			V_{Dis}=V_{DD}-0.5V		0.5		mA

Notes:

1. Should never exceed 6.0 Volts.
2. The input MI and LSI are internally biased to V_{DD} / 2 and should therfore be AC-coupled.

Pin Descriptions

Refer to figure 2.

DIP	Symbol	Description
1	IB	The resistance between this input and ground (V_{SS}) determines the bias currents for the internal amplifiers. A bias resistance of 220 kohm is recommended at V_{DD}=5V.
2	Disable/ ENABLE/ MUTE	Three-state input for mute/secrecy and disable function. Mic. mute is accomplished by tieing the pin to V_{SS} whereas the disable function is achieved by forcing the input to V_{DD}.
3	LSTH	To determine the receive openening sensitivity. Use a resistive voltage divider (R_{total} > 1 Mohm) between V_{DD} and V_B to set the DC-level in the range of 10 to 250 mV (Vb as reference voltage).
4	LSCP	Output of the receive level detector. A capacitor at this pin determines the decay time of the envelope detector. Typical capacitor values of 3.3 to 15 nF corresponds to decay times in the order of 50 to 300 milliseconds.
5	LSI	Input to the receive attenuators DIs and DIsc. Input impedance is typically 65 kohm. The pin is internally biased to Vb and should therefore be AC-coupled.
6	LSO	Speaker amplifier/buffer output (from the receive attenuator).
7	LSA	Output of the 2nd receive amplfier. Output impedance is approximately 10 ohms.
8	LSF	Output of the gain setting receive amplifier and input to the following fix gain (Av=10) amplifier.
9	LSINV	Inverting input of the gain setting receive amplifier.
10	LSX	Inverting input of the speaker amplifier/buffer.
11	VOL	Volume control input. A DC-voltage on this pin of V_{DD} / 2 corresponds to minimum volume (attenuation 22.6 dB) when the receive channel is open. 0 V input corresponds to maximum volume (0 dB attenuation). Careful design due to very high input impedance.
12	V_{SS}	The most negative supply voltage on the chip.
13	VB	This V_{DD} / 2 output, completed with a filter capacitor, serves as the analouge ground for the input amplifiers. It also provides a reference voltage for the receive and transmit threshold settings. Since the output impedance is in the order of 10 kohm, it is of great importance not to load the input with current consuming circuitry.
14	BGLVL	A capacitor (typ 470 nF) on this pin determines the long time constant for the background noise level detector.
15	BGP	Output of the envelope detector in the background level detector. A capacitor on the pin determines the decay time. For typical capacitor values, see the LSCP pin.

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16	MINV	Inverting input of the gain setting microphone amplifier.
17	MF	Output of the gain setting microphone amplifier and input to the following fix gain (Av=10) amplifier.
18	MA	Output of the 2nd microphone amplifier. The output impedance is approx 10 ohms.
19	MO	Transmit attenuator output. Output impdance is approx 1 ohm.
20	MI	Input to the transmit attenuators Dm and Dmc. Input impedance is typically 65 kohm. The pin is internally biased to Vb and should therefore be AC-coupled.
21	MCP	Output of the transmit level detector. A capacitor at this pin determines the decay time of the envelope detector. For typical capacitor values see the LSCP pin.
22	MTH	Determines the transmit opening sensitivity. Use the same resistive voltage divider as for LSTH. This pin also determines the activation voltage of three peak limiters.
23	OSC	A 1 Mohm resistor to V_{DD} and a capacitor of 100 pF to V_{SS} sets the oscillator frequency to 25 kHz (nominal). The oscillator pin can as well be driven from an external clock.
24	V_{DD}	The most positive supply voltage on the chip.

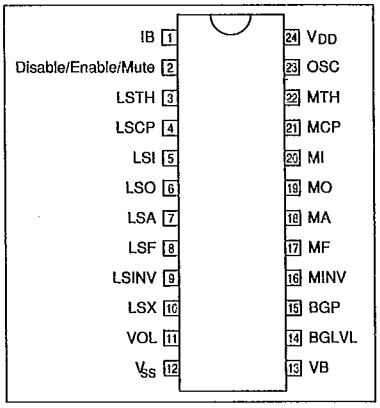

Figure 2. Pin configuration.

Functional Description

Microphone and receive amplifiers

The microphone and receive amplifier blocks are identical. Each block is divided into two stages. In stage one, the total gain and filter response is specified by external components, while stage two provides a fix gain of 20 dB (10 V / V). The hysteresis (control margin) between the two channels can be controlled over a selected frequency range thanks to the flexibility of stage one.

The available output swing from the second stage is approximately one (1) volt from each power - rail (V_{DD}-2 V). This is quite sufficient with respect to necessary opening sensitivities and possible offset - induced errors in the level detectors and the comparator logic.

Attenuators and control logic

The primary task of the two main attenuators, Dm and Dls, is to realize the half duplex, behaviour, necessary for a hands-free speakerphone. The AC-coupled signals from the microphone and receive amplifiers are here, in a complementary manner, controlled from the control logic via a 5-bit data-bus. The control logic receives information from six sources:

1. The transmit comparator.
2. The receive comparator.
3. The idle comparator.
4. The data-bus from the A/D-converter in the volume control.
5. The logarithmic A/D-converter in the background level circuitry.
6. The clock-generator, which besides the ordinary clocking of the digital logic, also determines the switching times.

Three steady states exists:

a) idle

b) transmit

c) receive

Both channels have an attenuation of 0 dB when open, 50 dB when closed and approximately 25 dB when in the idle state. See table 1. Depending on the information from the above stated six sources, the control logic selects both the appropriate destination (the attenuator that is to be adjusted) and the ramping time (correct number of clock-pulses). The timing is set by the oscillator-frequency, which is programmable from the external RC-network. The nominal switching times (f_{Osc}=25 kHz) are shown in figure 5. The attack time from active to active state is approximately 20 ms (10 ms from the idle state). There is an inhibition period of 60 ms after an indication to open the receive channel. This feature eliminates different kind of erroneous turnover indications, most notably when a person from the far end sets the circuits into transmit mode as a result of the room echo.

This "hysteresis-in-time" also removes (very) short sound transients from the room and hence develops a feeling of a consistent behaviour. If no signal is detected at the MCP and LSCP inputs, the attenuators slowly (650 ms) ramp back to the idle state.

The two control attenuators Dmc and Dlsc provide a two attenuated signals for the transmit and receive level detector respectively. The maximum attenuation of 25 dB and the attenuation in the idle state of 12.3 dB provide a proper combination of hysteresis (control margin) and sensitivity.

Volume control

The control logic sets the minimum attenuation level in the receive channels as per the information given by the A / D converted VOLI input. By also adjusting the transmit - attenuators (Dm and Dmc), the total main attenuation of 50 dB and the selected hysteresis (control margin) remain unaffected. The volume control covers a range down to approx 23 dB. See table 1.

Speaker amplifier and micorphone output buffer

The two main attenuators are followed by one output buffer each. These are used to drive the external amplifying circuitry. In the case of the receive-channel it may be a power amplifier. In line-powered applications, it is important to consider the current consumption. By using the LSX-input, i.e. the inverting input of the loudspeaker output buffer, it is possible to turn the buffer into an almost

complete power amplifier, ready to drive a 50 ohm loudspeaker element. An external push & pull stage added at the output (LSO) and a customary AC-coupled feedback-loop, to set the gain, completes the amplifier. See figure 6.

By using only the Rlso-resistor and tying the LSO-pin and the LSX-pin together, this open drain amplifier behaves as a buffer with a gain equal to 1. The resistor value is optimised with respect to the following circuitry and current consumption.

The maximum peak-to-peak voltage of the two buffers (the loudspeaker amplifier in a follower configuration; Av =1) is approximately equal to V_{DD} - 2V. With a gain greater than 4 in the speaker amplifier, the output range increases to V_{DD} - 0.2 V or with an external power stage according to figure 6. V_{DD} - 0.2 V - 2 • V_{BE} (of the two bipolar transistors).

Transmit and receive level detectors

The signals to the attenuators are AC-coupled to prevent possible offset-errros (generated in the input amplifiers) from entering the transmit and receive level detectors. After the control atttenuators the two signals are amplified another 20 dB's (10X) in offset cancelling amplifiers (SC-amplifiers). They are also level limited to increase the dynamic control range. The two limiters have a complementary hysterisis, preventing the circuit to switch due to side tone or an acoustic coupling.

The rise time of each envelope detector is determined by the external capacitor. (C_{MCP} or C_{LSCP}) and an internal resistor in the order of 50 kohm.

This charge time thereby reaches a couple of tenths of a millisecond. The decay time is in the same way determined by the external capacitor and as an internal resistor. The value of this resistor (in fact a switched capacitor) is dependent on the oscillator frequency according to the expression: R = 200 Mohm / f_{osc}, where the frequency is represented in kHz. Calculating with a capacitor of 4.7 nF and fosc = 25 kHz, gives a decay time of approximately 100 ms. Note the low value of the capacitor, giving a low leakage as well as a low price.

The limiters are made in a way that allows the decay time from a limited valute to be constant (2.5 • R internal • C_{MCP}) and independent of the chosen microphone threshold.

Transmit, receive and idle detection circuitry

A total of three comparators are used to detect the present operating status.

Two of the three comparators are used to compare each channel strength (at MCP and LSCP respectively) with their corresponding threshold value and one comparator is used to decide which, if anyone, of the channels is to be opened. The threshold inputs in conjunction with the control attenuators and the 10X - amplifiers in the envelope detectors, determine the sensitivity (to open) for each channel. Thanks to the 10X-amplifiers, the threshold voltage end up in the order of tenths of a millivolt and are therefore easily set by a resistive voltage divider between the V_{DD} -rail and the V_b-voltage.

Background Noise Reduction System

The noise level detection is done in two steps. The first step is an envelope-detection of the present microphone signal. Unlike in the transmit level detector this is done directly on the MI-input, making it possible to continously sense the true un-attenuated microphone signal. In a second step, a long time constant, accomplished by an internal switched capacitor and an external capacitor (C_{BGLVL}), suppresses the rapidly fluctuating speech and leaves a remaining DC-level corresponding to the back-ground noise level.

An introduction of 6 dB's "offset" in the background path (an extra amplification of 6 dB's) provides a smooth (and safe) transition between a background-affected microphone threshold and a threshold voltage selected from the MTH-input. This means that the microphone threshold due to the background noise, starts to increase the very moment the noise crosses half the MTH-voltage (or V_{MTH} - 6 dB), see figure 4.

The background level is limited to four microphone thresholds, i.e. V_{MTH} + 12 dB, in order to prevent a large threshold changes, which could cause problems in opening the microphone channel.

The attenuation function in the transmit path is realised by a logaritmic 2-bit "flash" analogue-to digitial converter. The digitized background level is treated exactly in the same manner as is the signal from the A/D converter in the volume control. The attenuation is regulated by the ratio 2.3:1, i.e. a 3.7 dB increase of the background noise level results in an 1.6 dB attenuated transmit signal. This ratio roughly corresponds to the automatic increases in the speech level made by a person in a noisy environment, which means an unaffected signal strength to the line. See figure 4 for the exact performance.

The reset time of the BG-level, using an external capacitor value of 470 nF, is in the order of 50 ms. The internal charging as well as the discharging switched capacitors gives the equivalent resistance of 200 Mohm / f_{osc} (exactly as in the transmit and receive level detectors). A 470 nF capacitor and an oscillator frequency of 25 kHz provides a rise time of about 10 s.

Microphone mute and enable facilities

The mute control, also known as the privacy button, disconnects the transmit channel, the transmit level detectors included. The disable control is used to disable the entire chip, with a few exceptions. All outputs except the LSO-output, i.e. the MA, LSA and MO outputs, are set into a high-impedance mode and the oscillator is turned off. Consequently the current consumption is drastically cut down by a factor of five.

The mute and disable and functions are, as can be seen in fig. 6, dedicated to one common pin. This three-state input is internally biased to half V_{DD} and sets therefore when unconnected the circuit into normal operation, i.e. neither muted nor disabled. The mute mode is obtained by tying the DISABLE / MIC.MUTE to V_{SS} and the disable mode is reached by forcing the input to V_{DD} . The privacy function is hence easily accomplished, for example by driving the input from an open drain output of a u-processor.

The V_B- Pin

V_B is the internal V_B-voltage separated by a 10 kohm resistor. The pin, connected to an external filter capacitor is used to attain a stable low-impedance signal ground for the two comparator thresholds MTH and LSTH. It is of great importance the voltage-divider has a high impedance (> 1 Mohm), partly to avoid affecting the voltage level (voltage drop along the 10 k resistor) but also in order not to spoil the (from V_{DD}-noise) filtered low impedance behaviour.

The I_B- pin

The bias input determines the bias current for the analogue circuit on the chip, such as the different operation amplifiers. This provides a possibility to choose the optimal power-consumption / performance ratio for every specific application. Standard values in the range of 100 kΩ to 300 kΩ are recommended.

Oscillator

As earlier mentioned, the timing of the circuit (the ramping times in the attenuators and the decay times in the envelope detectors) are set by the oscillator frequency. A 470 kohm resistor to V_{DD} and a 220 pF capacitor to V_{SS} on the OSC-pin selects a nominal frequency of 25 kHz. Disabling the circuit stops the oscillator and forces the oscillator pin to a high impedance condition.

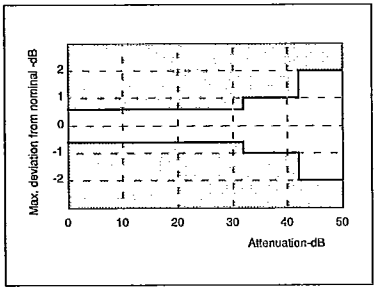

Figure 3. Attenuator accuracy vs. attenuation, MO and LSO outputs.

Nominal Attenuation Levels

Table 1. Relationship between the four attenuator settings.

	DM dB	DLS dB	DMC dB	DLSC dB	DLSC-DMC dB	DM-DLS dB
BG noise control range (when DM is open)	0.0	50.0	0.0	25.0		50.0
	1.6	48.4	0.0	25.0	25.0	
	3.2	46.8	1.7	23.3		50.0
	4.8	45.2	1.7	23.3	25.0	50.0
	6.5	43.5	3.3	21.7		50.0
	8.1	41.9	3.3	21.7	25.0	50.0
	9.7	40.3	5.0	20.0		50.0
	11.3	38.7	5.0	20.0	25.0	50.0
	12.9	37.1	6.7	18.3		50.0
	14.5	35.5	6.7	18.3	25.0	50.0
	16.1	33.9	8.3	16.7		50.0
	17.7	32.3	8.3	16.7	25.0	50.0
	19.4	30.6	10.0	15.0		50.0
	21.0	29.0	10.0	15.0	25.0	50.0
	22.6	27.4	11.7	13.3		50.0
Idle state	24.2	25.8	11.7	13.3	25.0	50.0
	25.8	24.2	13.3	11.7		50.0
	27.4	22.6	13.3	11.7	25.0	50.0
	29.0	21.0	15.0	10.0		50.0
	30.6	19.4	15.0	10.0	25.0	50.0
	32.3	17.7	16.7	8.3		50.0
Volume control range (when DLS is open)	33.9	16.1	16.7	8.3	25.0	50.0
	35.5	14.5	18.3	6.7		50.0
	37.1	12.9	18.3	6.7		50.0
	38.7	11.3	20.0	5.0		50.0
	40.3	9.7	20.0	5.0	25.0	50.0
	41.9	8.1	21.7	3.3		50.0
	43.5	6.5	21.7	3.3	25.0	50.0
	45.2	4.8	23.3	1.7		50.0
	46.8	3.2	23.3	1.7	25.0	50.0
	48.4	1.6	25.0	0.0		50.0
	50.0	0.0	25.0	0.0	25.0	50.0

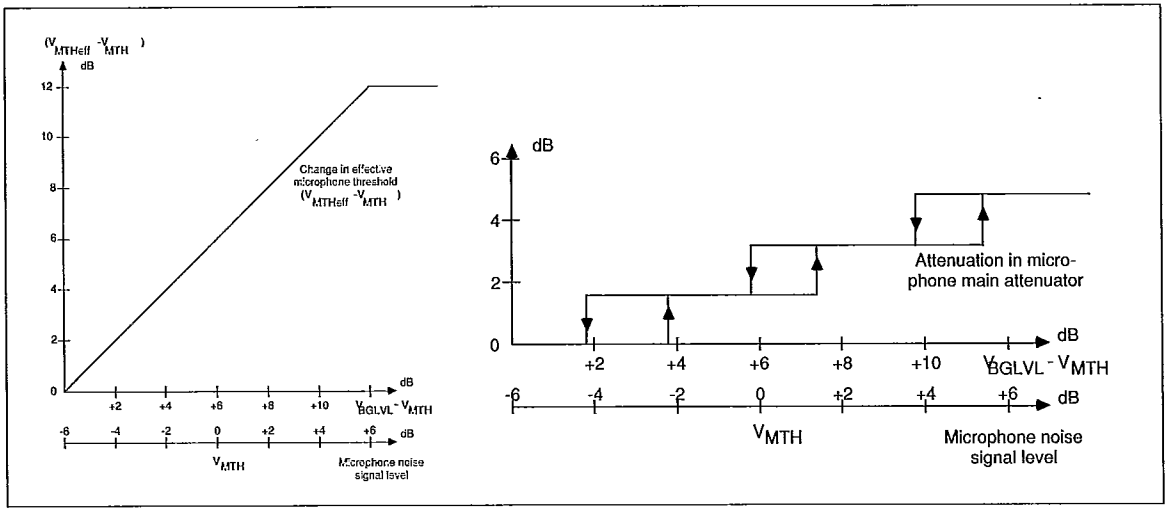

Figure 4. Background noise filter regulation, (left) effective opening voltage vs. noise level, (right) attenuation in transmit channel.

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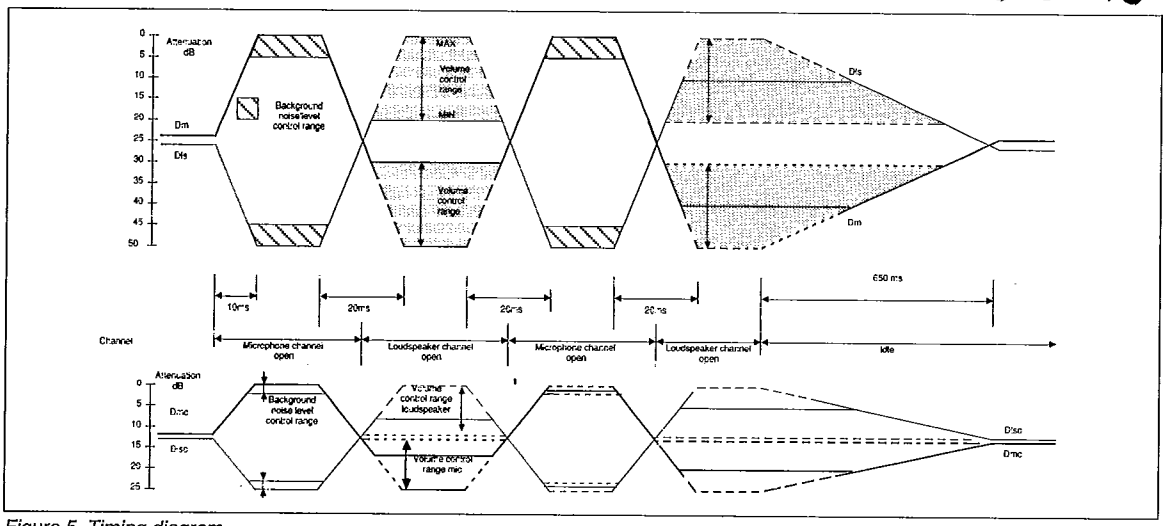

Figure 5. Timing diagram.

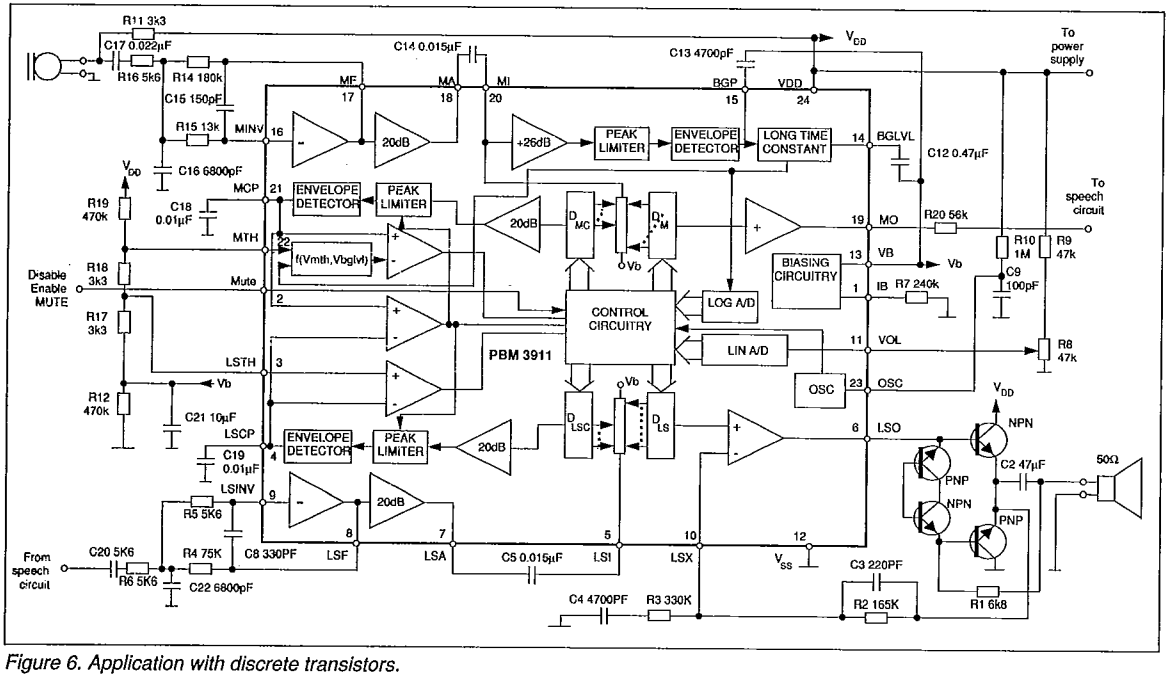

Figure 6. Application with discrete transistors.

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