T-46-23-05

CY2147

CYPRESS SEMICONDUCTOR

4096 x 1 Static R/W RAM

Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed
  - 35 ns
- Low active power
  - 690 mW (commercial)
  - 770 mW (military)
- Low standby power
  - 140 mW
- TTL-compatible imputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY2147 is a high-performance CMOS static RAM organized as 4096 by 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY2147 has an automatic power-down feature, reducing the power consumption by 80% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

The output pin stays in high-impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

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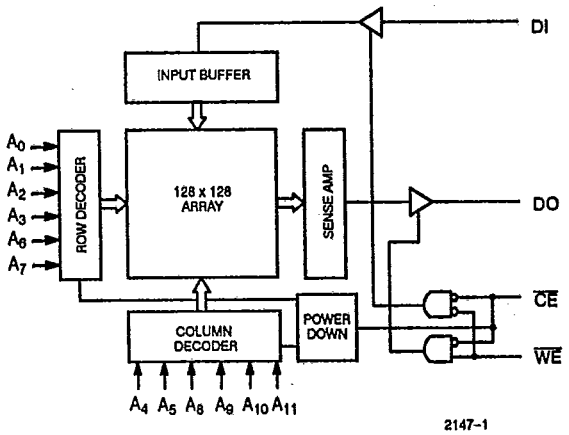
Logic Block Diagram



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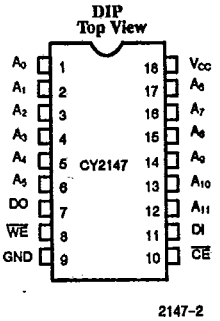
Pin Configuration



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Selection Guide (For higher performance and lower power, refer to CY7C147 data sheet.)

		2147-35	2147-45	2147-55
Maximum Access Time (ns)		35	45	55
Maximum Operating Current (mA)	Commerical	125	125	125
	Military		140	140
Maximum Standby Current (mA)	Commerical	25	25	25
	Military		25	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to + 150°C

Ambient Temperature with Power Applied ..... – 55°C to + 125°C

Supply Voltage to Ground Potential ..... – 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to + 7.0V

DC Input Voltage ..... – 3.0V to + 7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	– 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

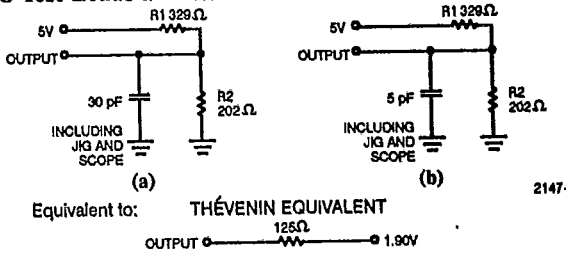
Parameters	Description	Test Conditions		2147 Min.	2147 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			–3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–50	+50	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			–350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		125	mA
			Mil		140	
I_{SB}	Automatic $\overline{CE}$ Power-Down Current[4]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Com'l		25	mA
			Mil		25	

Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		6	pF

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Duration of the short circuit should not exceed 30 seconds.
4. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



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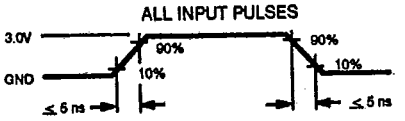

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Equivalent to: THÉVENIN EQUIVALENT

Switching Characteristics Over the Operating Range[2,6]

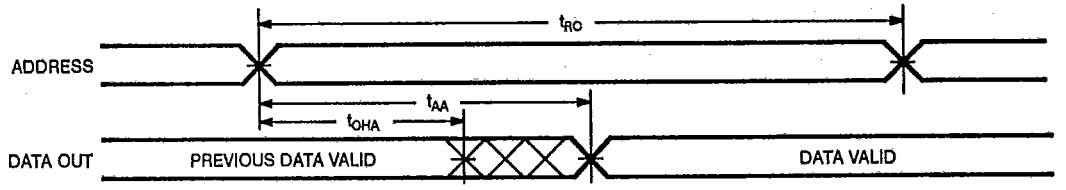
Parameters	Description	2147-35		2147-45		2147-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Output Hold from Address Change	5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		35		45		55	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		30		30		30	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		20		20		20	ns
WRITE CYCLE[9]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	35		45		45		ns
t_{AW}	Address Set-Up to Write End	35		45		45		ns
t_{HA}	Address Hold from Write End	0		0		10		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		25		ns
t_{SD}	Data Set-Up to Write End	20		25		25		ns
t_{HD}	Data Hold from Write End	10		10		10		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7]		20		25		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7, 8]	0		0		0		ns

Notes:

6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices.
8. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CE}$ = V_{IL}.
12. Address valid prior to or coincident with $\overline{CE}$ transition low.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

Read Cycle No. 1[10,11]



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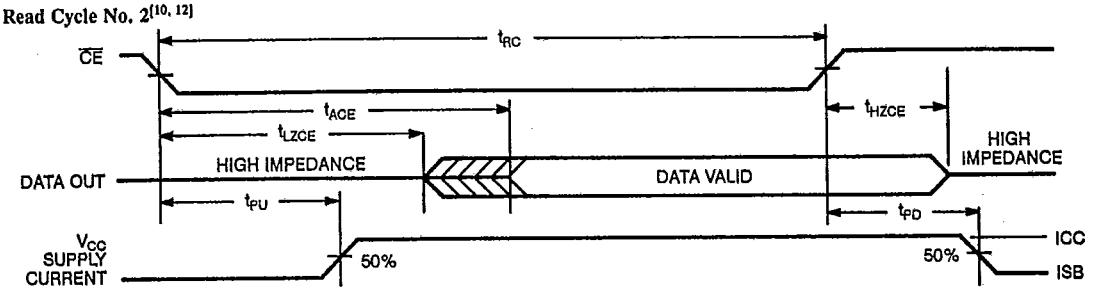
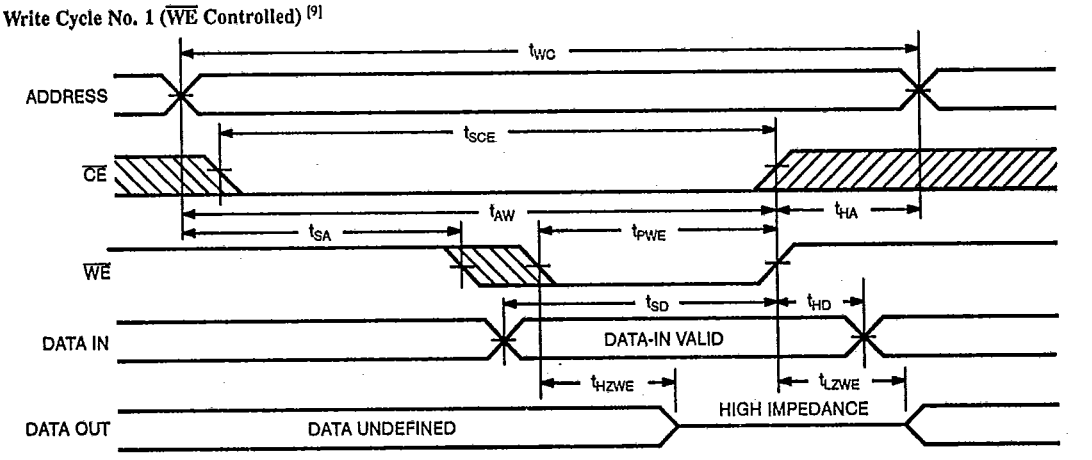
Switching Waveforms

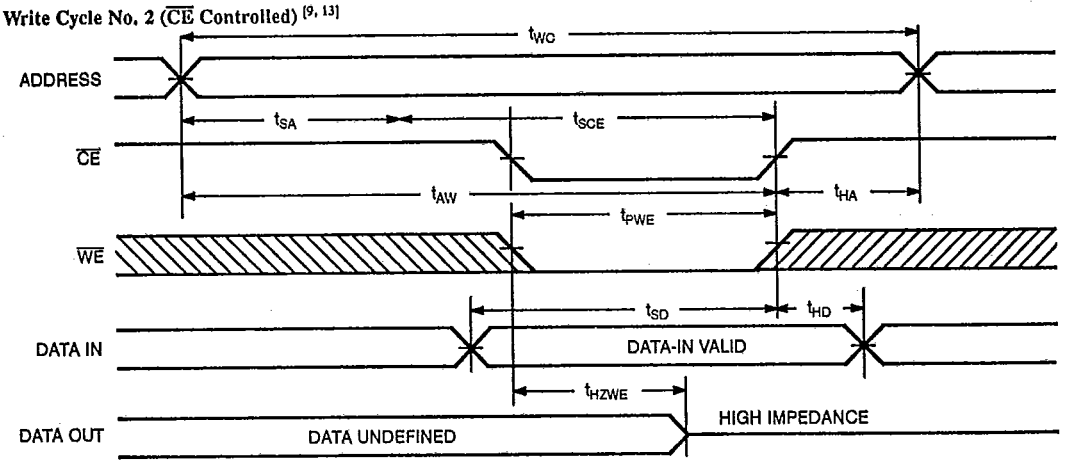
Read Cycle No. 2[10, 12]



Write Cycle No. 1 ($\overline{WE}$ Controlled) [9]



Write Cycle No. 2 ($\overline{CE}$ Controlled) [9, 13]



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C147-35PC	P3	Commercial
	CY7C147-35DC	D4	
45	CY7C147-45PC	P3	Commercial
	CY7C147-45DC	D4	
	CY7C147-45DMB	D4	Military
55	CY7C147-55PC	P3	Commercial
	CY7C147-55DC	D4	
	CY7C147-55DMB	D4	Military

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MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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