LXT312 / LXT315

Low Power T1 PCM Repeaters

General Description

The LXT312 and LXT315 are integrated repeater circuits for T1 carrier systems. The LXT312 is a dual repeater and the LXT315 is a single repeater. The LXT312 and LXT315 are designed to operate as regenerative repeaters for 1.544 Mbit/s data rate PCM lines. Each includes all circuits required for a regenerative repeater system including the equalization network, automatic line build-out (ALBO), and a state of the art analog/digital clock extraction network tuned by an external crystal.

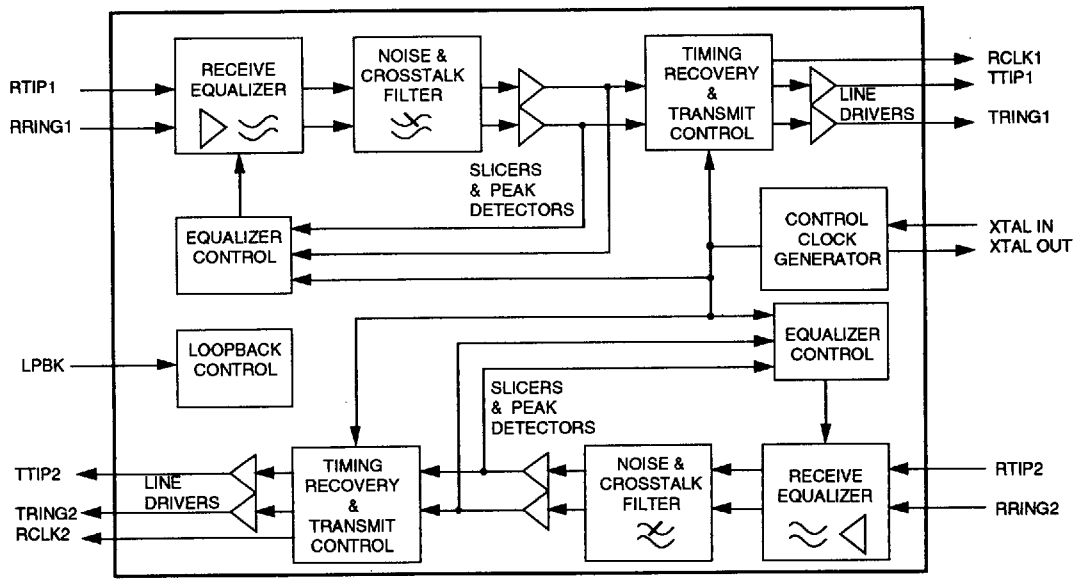
The key feature of the LXT312 family is that it requires only a crystal and a minimum of other components to complete a repeater design. Compared with traditional tuned coil-type repeaters, they offer significant savings in component and labor costs, along with reduced voltage drop/power consumption, and improved reliability. To ensure performance for all loop lengths, the LXT312 and LXT315 are 100% AC/DC tested using inputs generated by Level One's proprietary transmission line and network simulator.

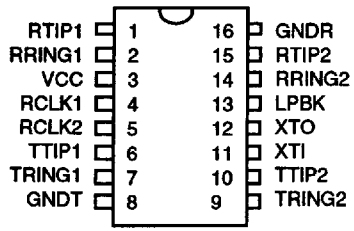
The LXT312 and LXT315 are advanced CMOS devices which require only a single +5V power supply.

Features

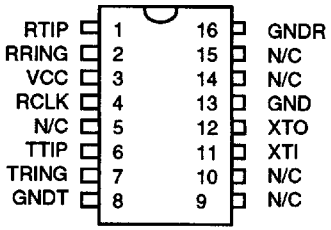
- Integrated repeater circuit on a single CMOS chip
- On-chip equalization network
- On-chip ALBO
- Low power consumption
- No tuning coil
- On-chip Loopback
- Recovered Clock Output
- 0 to 36 dB dynamic range
- -11 dB interference margin
- Compatible with CB113/TA24 specifications
- Single 5 V only CMOS technology
- Available in 16-pin ceramic DIP

Figure 1. LXT312 Block Diagram





LXT312



LXT315

Pin Descriptions

Pin #	Sym	I/O	Name	Description
1	RTIP1	I	Repeater Tip and	Tip and ring receive inputs for Channel 1.
2	RRING1	I	Ring Inputs	
4	RCLK1	O	Recovered Clock	Clock output recovered from Channel 1 receive input.
6	TTIP1	O	Repeater Tip and	Open drain output drivers for Channel 1.
7	TRING1	O	Ring Outputs	
11	XTI	I	Crystal Oscillator	Either a 6.176 MHz crystal must be connected across these two
12	XTO	O	Input and Output	pins, or a clock must be applied at XTI and XTO left floating.
3	VCC	I	Power Supply	Power supply input for all circuits. +5 V (±0.25 V)
8	GNDT	–	Transmit Ground	Ground return for transmit circuits.
16	GNDR	–	Receive Ground	Ground return for receive circuits.
9 [1]	TRING2	O	Repeater Side 2 Tip	On the LXT312 dual repeater, these are open drain output
10 [1]	TTIP2	O	and Ring Outputs	drivers for Channel 2.
14 [1]	RRING2	I	Repeater Side 2	On the LXT312 dual repeater these are tip and ring receive
15 [1]	RTIP2	I	Ring and Tip Inputs	inputs for Channel 2.
5 [1]	RCLK2	O	Recovered Clock	On the LXT312 dual repeater, this is the recovered clock output for Channel 2.
13 [2]	LPBK	I	Loopback Control	On the LXT312, this pin controls Loopback Selection. High = Loopback side 1 data to side 2. Low = No Loopback.

Notes:
1. On the LXT315 single repeater, these pins are not connected (N/C).
2. On the LXT315 single repeater, this pin must be connected to GND.

Absolute Maximum Ratings*

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

• Supply Voltage	V_{CC}	-0.3 V to 6 V
• Driver Voltage	V_{OH}	18 V
• Receiver Current	I_{CC}	100 mA
• Operating temperature	T_{OP}	-40 °C (min) to +85 °C (max)
• Storage temperature	T_{ST}	-65 °C (min) to +150 °C (max)

Recommended Operating Conditions (Voltages are with respect to ground unless otherwise specified.)

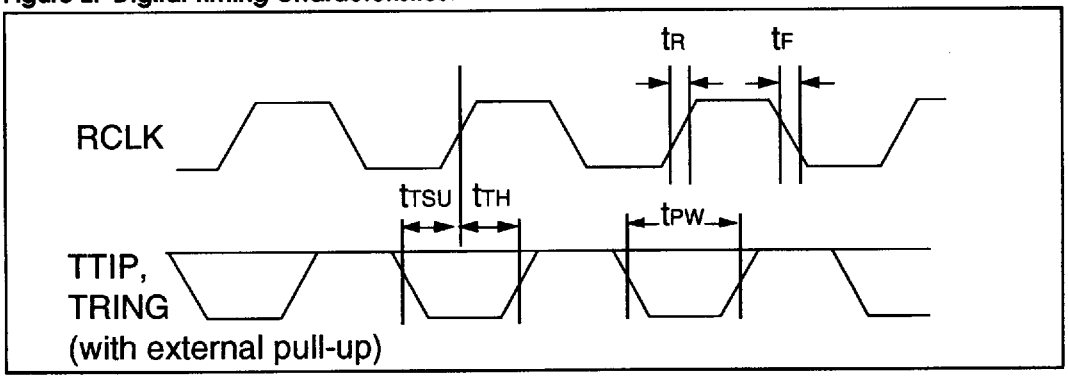
Parameter	Symbol	Min	Typ	Max	Units
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Operating temperature	T_{OP}	-40	–	85	°C

Electrical Characteristics (Ta = -40 to 85 °C, V_{CC} = 5V ±5%)

Parameter		Symbol	Min	Typ[1]	Max	Units
Interference Margin		SNR	-11	–	–	dB
Receiver Dynamic Range		–	-36	–	0	dB
Digital Outputs - Low	(I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
	(I_{OL} = 10 µA)	V_{OL}	–	0.2	–	V
Digital Outputs - High	(I_{OH} = 0.4 mA)	V_{OH}	2.4	–	–	V
	(I_{OH} < 10 µA)	V_{OH}	–	4.5	–	V
Digital Inputs - High		V_{IH}	2.0	–	–	V
Digital Inputs - Low		V_{IL}	–	–	0.8	V
Supply Current	All zeros	I_{CC}	–	15	22	mA
(from VCC supply)[2]	All ones	I_{CC}	–	–	23	mA
Driver Leakage Current (V_{DVR} = 18 V)		I_{LL}	–	–	100	µA
Driver Pulse Amplitude (Driver output I_o = 20 mA)		A_P	0.65	–	0.95	V
Driver Pulse Width		t_{PW}	299	324	349	ns
Driver Pulse Imbalance		–	–	–	15	ns
Rise and Fall Time (any digital output[2])		t_R / t_F	–	–	18	ns
Setup Time - TTIP/TRING to RCLK		t_{TSU}	90	–	–	ns
Hold Time - TTIP/TRING from RCLK		t_{TH}	90	–	–	ns

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Measured with $C_{LOAD} \leq 10$ pF, $R_{LOAD} > 100$ kΩ.

Figure 2: Digital Timing Characteristics



General Description

PCM signals are attenuated and dispersed in time as they travel down a transmission line. Repeaters are required to amplify, reshape, regenerate and retime the PCM signal, then retransmit it.

The LXT312 and LXT315 each contain all the circuits required to build a complete PCM repeater. The operational range of the repeaters is 0 to 36 dB of cable loss at 772 kHz (equal to 6300 feet of 22 gauge pulp-insulated cable between repeaters).

Functional Description

Receive Function

The signal is received through a 1 : 1 transformer at RTIP and RRING and equalized for up to 36 dB of cable loss. The receive equalizer uses a proprietary on-chip adaptive filter technique which is equivalent to a 3-port ALBO equalizer design. The monolithic structure of the filter and the absence of external components provide excellent ISI and dispersion elimination, and accurate data transfer over temperature.

Receiver noise immunity is optimized by a proprietary crosstalk elimination filter which eliminates the unneeded high frequency components of the received signal.

Timing Recovery Function

The equalized signal is full wave rectified and used to generate information for the timing recovery circuit. This circuit uses a mixed analog/digital technique to provide a low-jitter PLL similar to a tuned tank with excellent jitter tracking ability. But unlike a tuned tank, the free running frequency of the PLL clock is accurately controlled by the external reference crystal. No adjustment is required. Refer to Table 1 for crystal specifications.

Recovered clock signals are available on the RCLK pins for applications that require synchronization to the bit stream.

Transmit Function

Recovered data is resynchronized to the recovered clock signal by the timing recovery and transmit control section. The data is then retransmitted to the network via two open drain, high voltage transistors.

Loopback Function (LXT312 Only)

The LXT312 includes a loopback function for network diagnostics. With the LPBK pin low, the repeater operates in the normal mode. When the LPBK pin is pulled high, the data is looped back from side 1 to side 2.

Test Setups

Both the LXT312 and LXT315 are fully tested (100% AC and DC parameters) using inputs generated by Level One's proprietary transmission line and network simulator. Device testing includes receiver jitter tolerance, jitter transfer and interference margin, and receiver immunity to gaussian and 60 Hz noise. Specifications and bench test setups are shown in Figures 3 through 10.

Receiver Jitter Tolerance Testing

Receiver jitter tolerance meets the template shown in Figure 3, when operated at line losses from 0 to 36 dB. Figure 4 shows the setup used for jitter tolerance testing.

Table 1: LXT312/315 Crystal Specifications

Parameter	Specification
Frequency	6.176 MHz
Frequency [1]	± 50 ppm
Effective series resistance	40 Ω Maximum
Crystal cut	AT
Resonance	Parallel
Maximum drive level	2.0 mW
Mode of operation	Fundamental

[1] @ 25° C, C Load = 10 pF; and from -40° C to + 85° C (Ref 25° C reading)

Figure 3: Receiver Jitter Tolerance Template

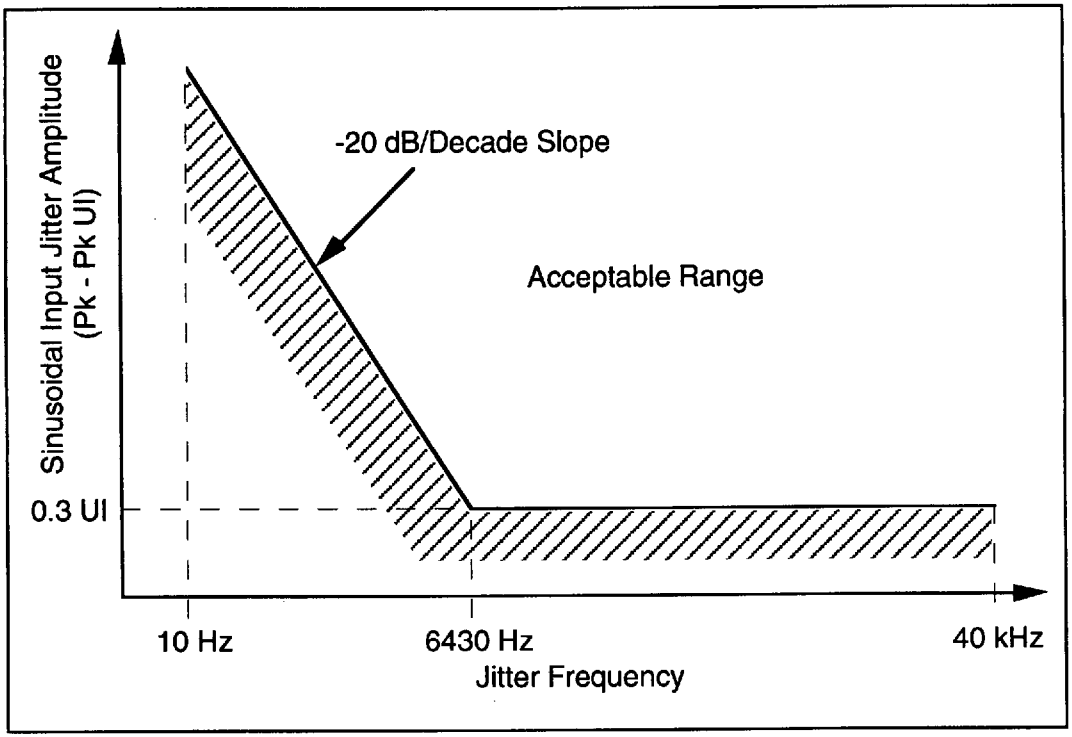
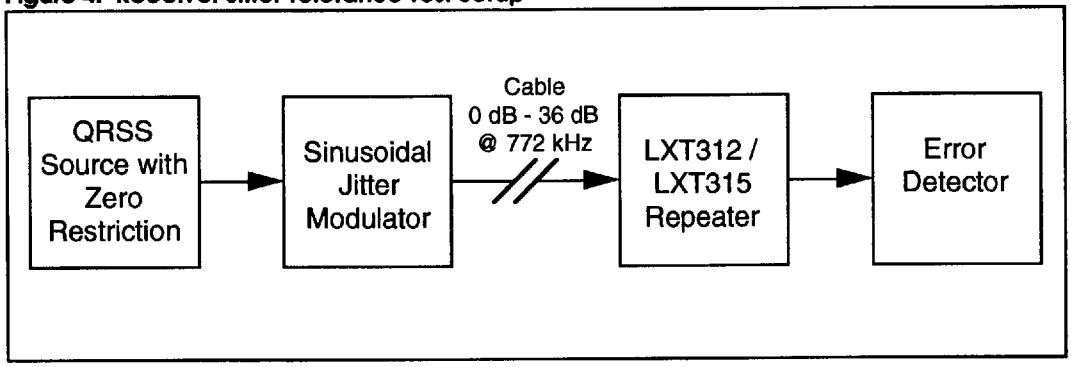


Figure 4: Receiver Jitter Tolerance Test Setup



Receiver Jitter Transfer Testing

Receive jitter transfer meets the template shown in Figure 5, when operated with line losses from 0 to 36 dB and input jitter amplitude of 0.15 UI peak-to-peak. Jitter gain at a given frequency is defined as the difference between intrinsic jitter and additive jitter at the measurement frequency, divided by the amplitude of the input jitter. Figure 6 shows the setup used for jitter transfer testing.

Interference Margin Testing

The LXT312 and LXT315 receiver noise interference margin is specified at a minimum of -11 dB for line losses from 0 dB to 36 dB. The test setup used to measure noise margin is shown in Figure 7.

Figure 5: Receiver Jitter Transfer Template

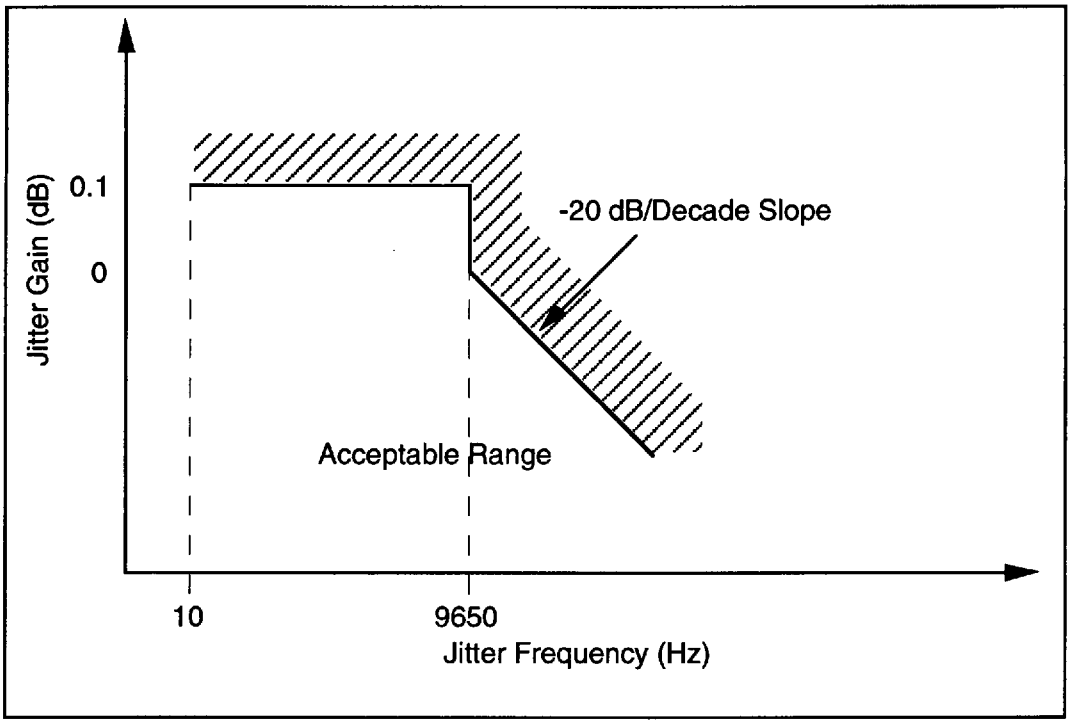
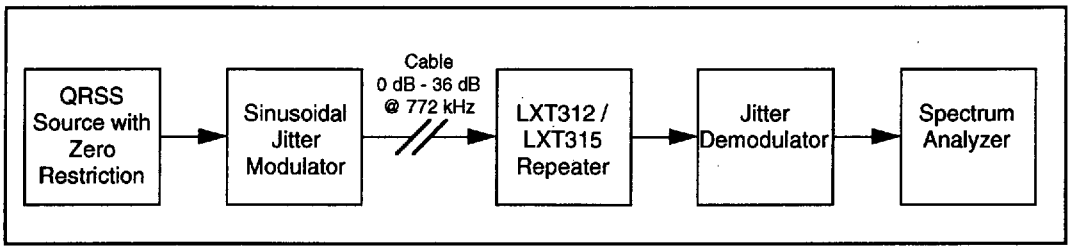


Figure 6: Receiver Jitter Transfer Test Setup



Gaussian Noise Immunity Testing

Receiver immunity to gaussian noise is specified at a maximum BER of 10^{-7} for a quasi-random T1 signal at 1.544 MHz (± 130 ppm). The receiver must be immune to noise power expressed as Np = - (L + 4.7) dBm, where L corresponds to the line loss and is valid for 0 - 36 dB.

Figure 8 shows the setup used to test gaussian noise immunity. The noise source is gaussian to at least 6 sigma and filtered to simulate expected noise in a binder group (per AT&T TA #24/CB113).

60 Hz Pulse Modulation Immunity Testing

Receiver immunity to 60 Hz pulse amplitude modulation is specified using the gaussian noise source described in the previous paragraph on gaussian noise immunity. Pulse amplitude modulation is specified between 10% and 30% of the nominal amplitude (see AT&T TA #24/CB113 for details on the modulation envelope). Figure 9 shows the setup used for testing receiver immunity to 60 Hz pulse amplitude modulation. The following figures reflect noise power for 10^{-7} BER at each modulation level, where L corresponds to the line loss and is valid for 0 - 35 dB:

Modulation Level	Noise Power
10%	Np = - (L + 5.7) dBm
20%	Np = - (L + 6.7) dBm
30%	Np = - (L + 8.7) dBm

2

Figure 7: Receiver Noise Interference Margin Test Setup

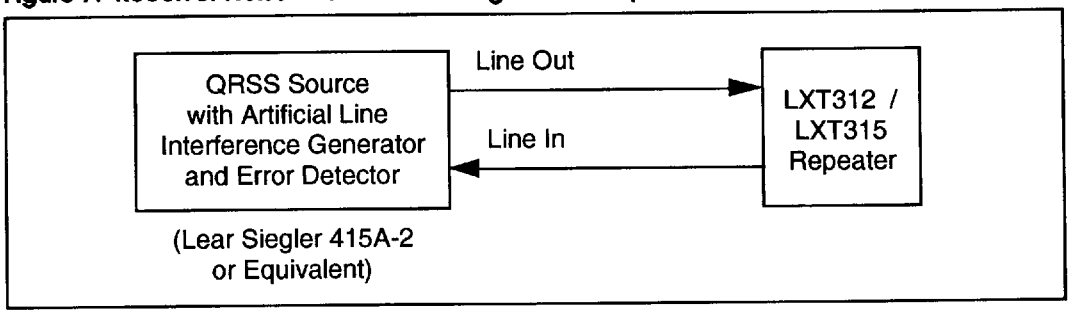
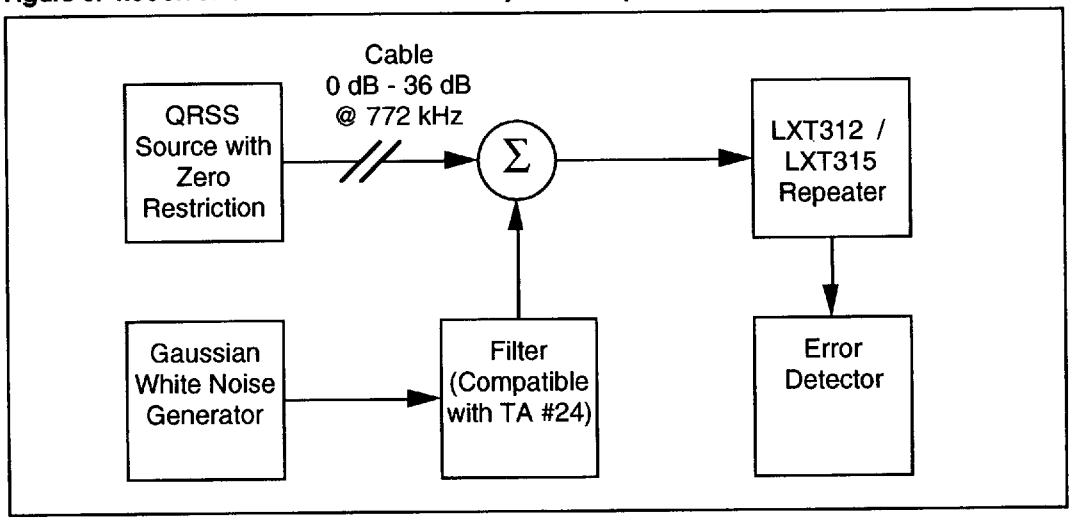


Figure 8: Receiver Gaussian Noise Immunity Test Setup



Receiver Timing Recovery Testing

Receiver timing recovery phase shift modulation for repetitive 8-bit patterns is specified at less than 0.07 UI. This is tested using any two out of 35 possible 8-bit patterns and measuring the change in output pulse timing from one pattern to the other (see AT&T TA #24 / CB113 for details on the patterns). Switching rate from one pattern to the other is specified at between 300 Hz and 500 Hz. The setup used to test receiver timing recovery phase shift modulation is shown in Figure 10.

Figure 9: Receiver 60 Hz Pulse Amplitude Modulation Immunity Test Setup

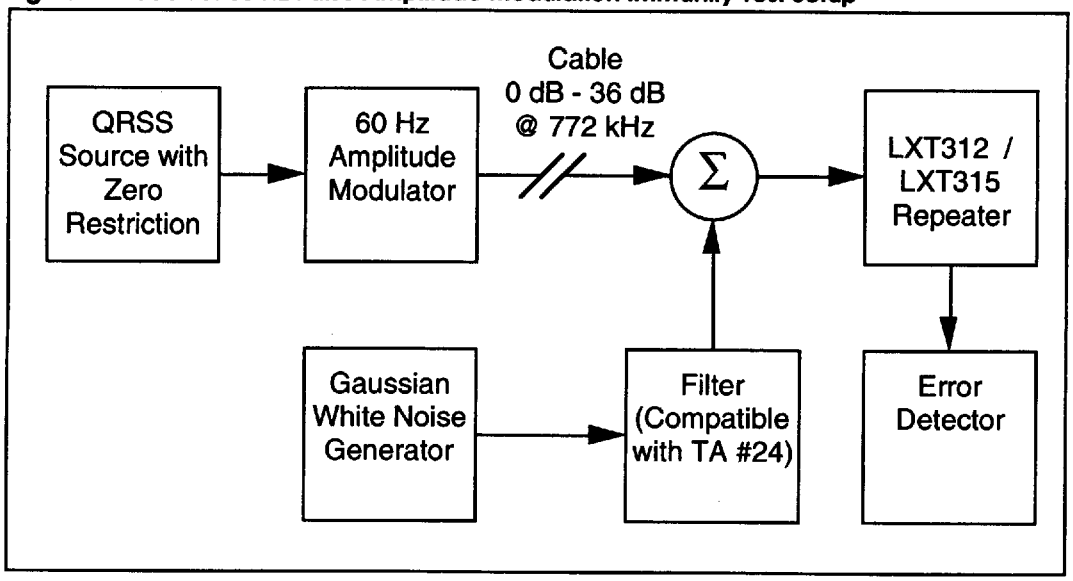
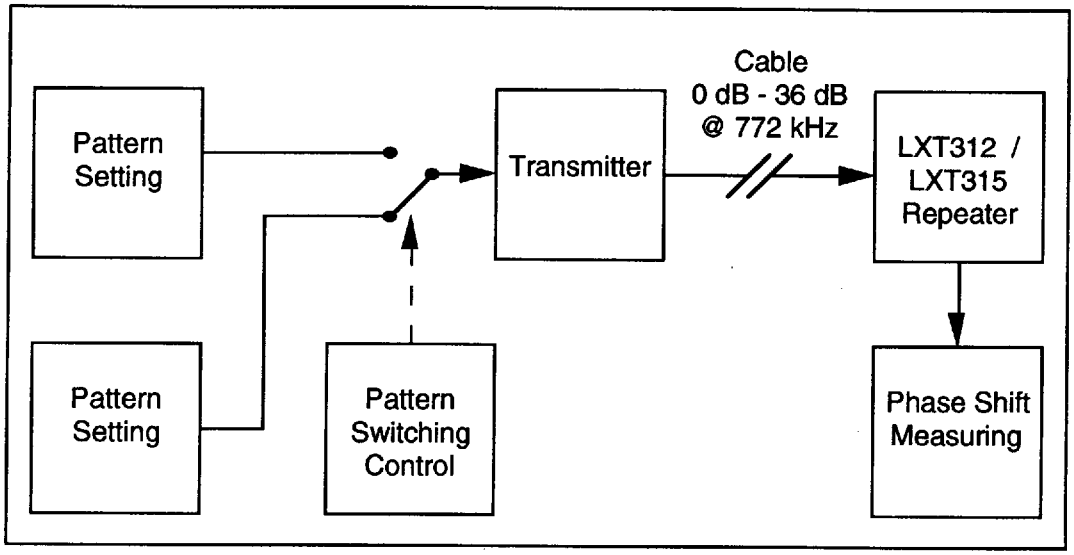


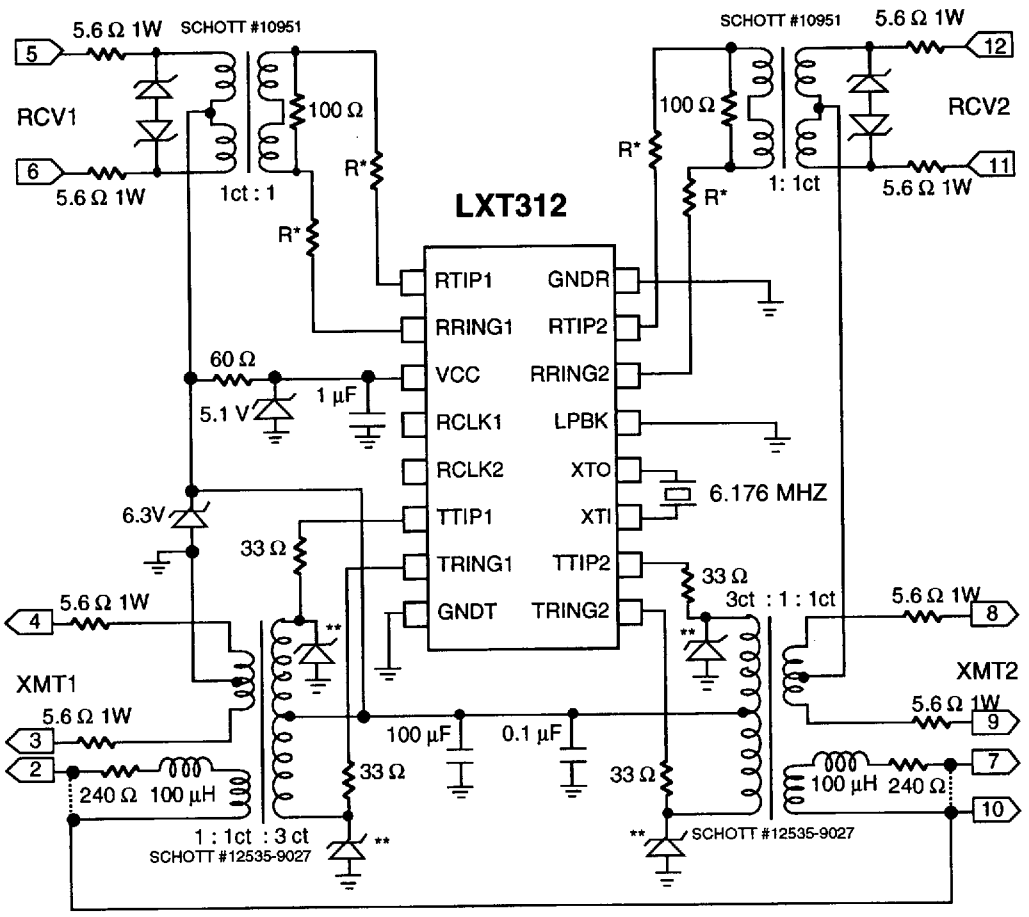
Figure 10: Receiver Timing Recovery Phase Shift Modulation Test Setup



Applications

Figure 11 is a typical T1 dual repeater application circuit showing standard repeater card edge connections. A jumper selectable shorting option for the fault location circuitry is also shown (dashed lines, connector pins 2 and 7).

Figure 11: Typical T1 Dual Repeater Application Diagram



Notes * RTIP/RRING Resistors are used to provide surge protection. Values can be 0 - 100 Ω.

** TTIP/TRING Zeners are used to to reduce surge susceptibility. Values can be 12 - 14 V.