ANALOG DEVICES

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APPLICATION NOTE

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8-Bit A/D Converter Mates Transducers with μPs

by Doug Mercer and Doug Grant

Through the innovative use of standard design concepts, a monolithic a-d converter simplifies the job of connecting transducers to a micropressor bus. The chip needs only +5 V.

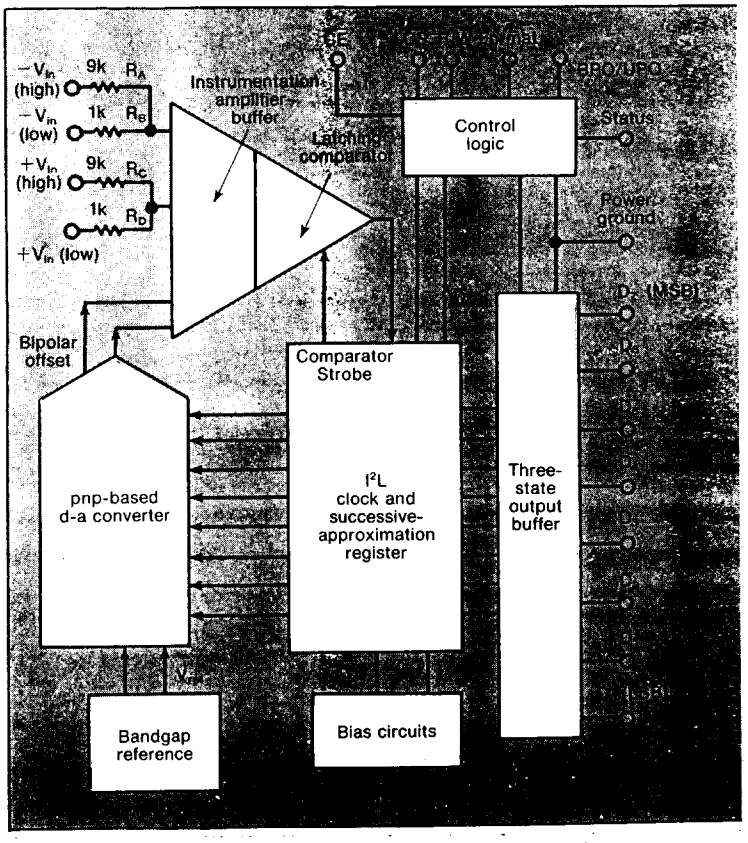
Monolithic 8-bit analog-to-digital converters usually operate slowly, require one or more external components (such as a voltage reference or clock), and frequently draw their power from both positive and negative supplies. Even more important, they can generally handle only high-level input signals between 2 and 5 V. As a result, placing them between transducers and microprocessors is not an easy design task.

Bucking tradition is a successive-approximation analog-to-digital converter that not only performs an 8-bit conversion in 10 μs, but also runs from a +5-V power supply. An impressive roster of internal circuits permits system designers to drop the monolithic converter directly onto a microprocessor bus without adding any external components.

Unlike other successive-approximation devices, the AD670 converter contains a combined instrumentation amplifier-buffer—with a true differential input—which lies between the signal sources and the conversion circuitry (Fig. 1). With this dual-purpose component and the chip's precision digital-to-analog converter (which is based on pnp rather than the more customary npn transistors), the 670 can connect directly to a low-level floating-output signal source, such as a strain gauge or other type of transducers. Together these two circuits give the chip a full-scale sensitivity of 255 mV, or 1 mV/LSB.

These features would mean nothing to the system designer if the analog-to-digital converter were internally too complicated to manufacture. To build this complete analog circuit, innovative design techniques merged with precision bipolar processing, laser wafer trimming of thin-film resistors, and integrated injection logic (I^2L)—all of which are proved technologies for high-volume production. The linear-compatible I^2L is the key to incorporating dense logic functions on a bipolar chip hosting precision linear components.

The conventional successive-approximation a-d converter, whether bipolar or CMOS, must be externally driven by a fast op amp or some other low-impedance component. A bipolar converter relies on



1. The instrumentation amplifier-buffer of the AD670 8-bit a-d converter works with millivolt-level transducer signals. The chip's design permits pin-strapping for a 1- or 10-Mv LSB. Two other pin-strapping or software-controlled options afford unipolar or bipolar operation, as well as two's complement or binary output coding.

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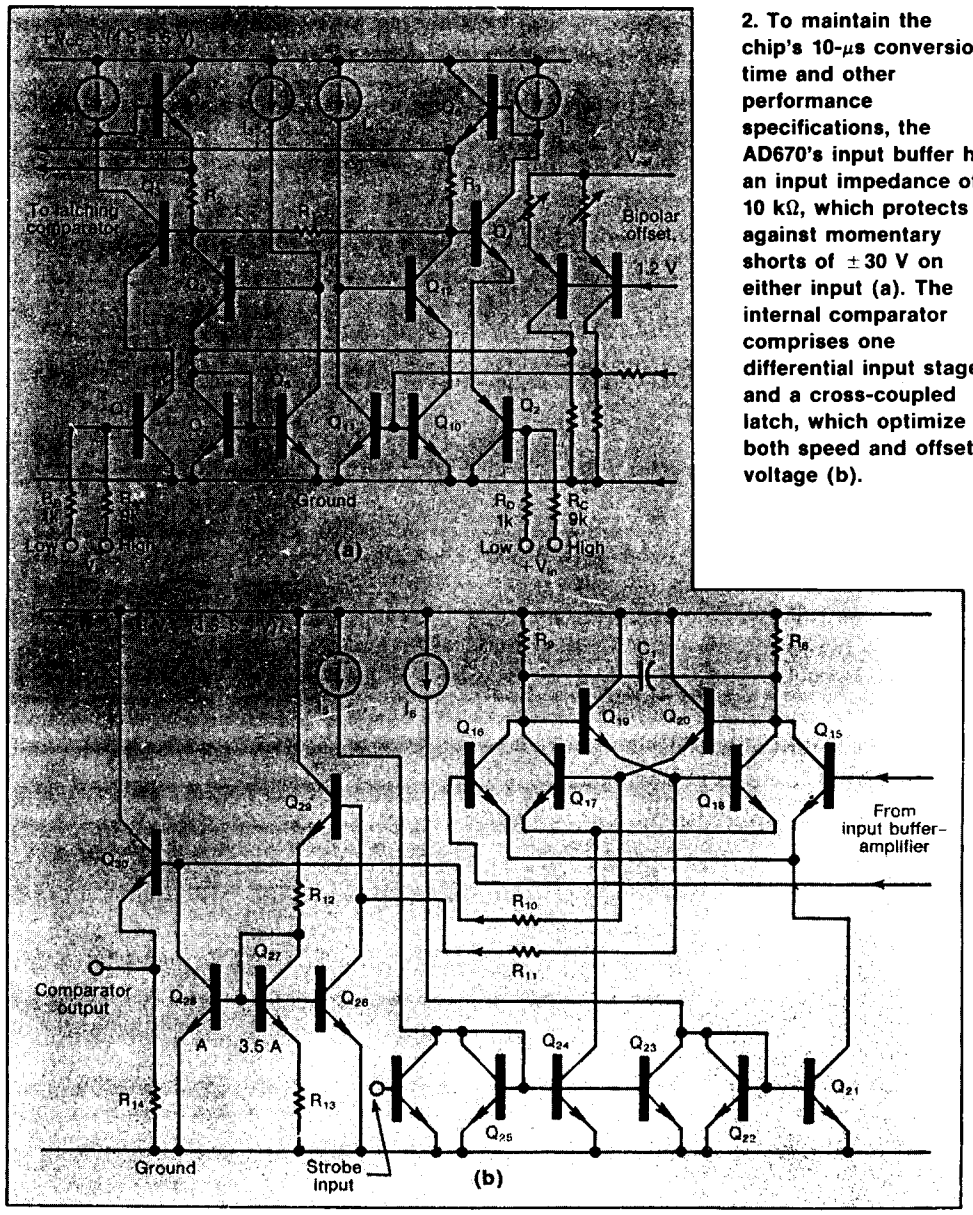
the amplifier to eliminate the effects caused when test-bit currents from the d-a converter are fed back into the signal source. The CMOS version, which must keep its settling time at a minimum, uses the op amp to lower the charge or discharge time constants for the capacitors in the data-sampling comparators. With the 670, in contrast, the combination of input buffer and comparator effectively negates the need for a separate, external amplifier.

The front end of the 670 is resistive and typically needs only 200 nA of input bias current. If the source impedances for the positive and negative voltages are reasonably well balanced, an offset current of 5 nA enables the source impedance to rise as high as 100 kΩ.

The basic input ranges of the converter are +255 mV and from −128 to +127 mV. At each input, an attenuator (R_AR_B and R_CR_D) provides a 10-to-1 attenuation factor, which increases the full-scale ranges to +2.55 V and from −1.28 V to +1.27 V. When operating in this higher voltage range, the nominal input impedance is 10 kΩ. The input resistors supply overrange protection from latch-up for momentary shorts of up to ±30 V on either input.

Within the input section of the instrumentation amplifier is a voltage-to-current converter (Fig. 2). Vertical pnp transistors (Q_1, Q_2) and npn emitter-followers (Q_3, Q_4) achieve the ground-inclusive common-mode range. The differential input voltage is applied across resistor R_1, leading differential current to flow through resistors R_2 and R_3. The signal voltage between the emitters of Q_5 and Q_6 is now twice the input voltage, V_{in}.

The outputs from both the pnp-based d-a con-



2. To maintain the chip's 10-μs conversion time and other performance specifications, the AD670's input buffer has an input impedance of 10 kΩ, which protects it against momentary shorts of ±30 V on either input (a). The internal comparator comprises one differential input stage and a cross-coupled latch, which optimize both speed and offset voltage (b).

verter and the bipolar current source are then reflected by the two Wilson current mirrors made up of Q_7–Q_9 and Q_{10}–Q_{12}. The output current from the mirrors is summed with the current in R_1, and the level-shifted difference between the amplifier's input and the d-a converter's output appears at the input to the latching comparator.

Since these signal levels are rather small (the full-scale signal at the comparator's input is only 512 mV), clamp diodes are no longer required. These small-signal conditions also increase bandwidth and eliminate the need to slew large voltages on stray capacitance.

A good heart

An a-d converter is only as accurate as its comparator. Therefore, like the input stage, the comparator in the 670 also embodies innovative design concepts (Fig. 2b). For example, the accuracy of the comparator lets the converter resolve a 1-mV LSB with less than 200 μV of code transition uncertainty. Its basic setup is exactly like that of the industry-standard 12-bit 574A a-d converter. The comparator's offset is adjusted by laser-trimming current sources I_1 and I_2, which are located in the input stage of the buffer amplifier.

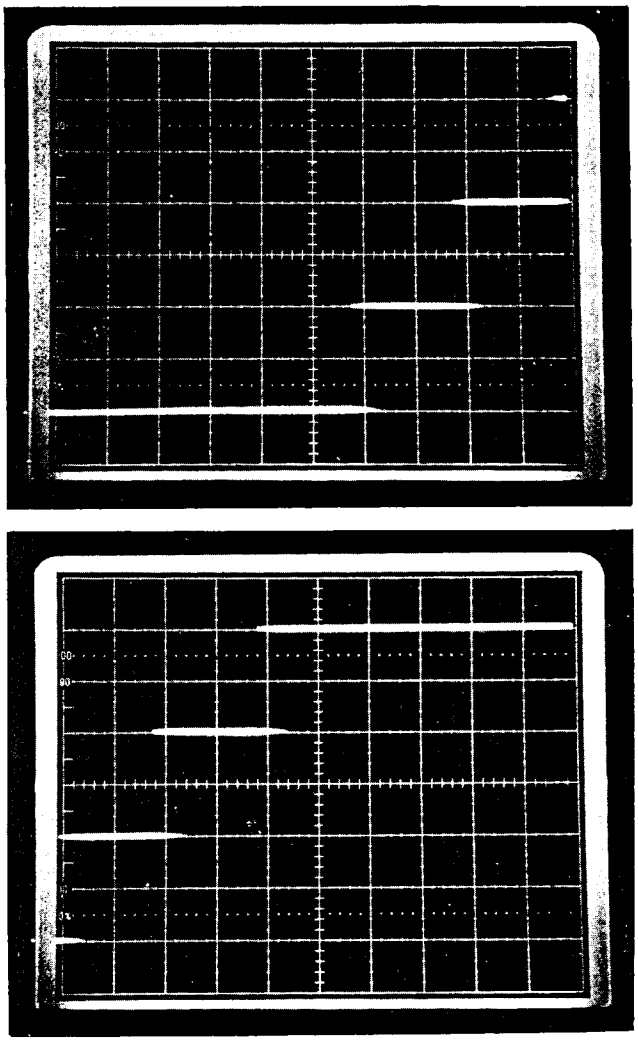
The comparator consists of a single differential stage (Q_{15}–Q_{16}) and a cross-coupled latch (Q_{17}–Q_{20}), which is activated and deactivated by diverting the current from I_3 through an I^2L gate. The differential output of the latch is converted into a single-ended signal by Q_{26}–Q_{30} through resistors R_{10} and R_{11}. The output of the comparator swings through a temperature-dependent amplitude that is centered at 1.2 V, a value set by the ratio of R_{12} to R_{13}. The dependence on temperature is essential for the comparator to interface properly with the I^2L latches that drive the pnp-based d-a converter.

The d-a converter employed in this design comprises eight identical 100-μA current sources, each built with a lateral pnp transistor. They drive an R-2R ladder, which binarily weights each bit. The converter uses the identical current sources for each bit, thereby avoiding the need to match the base-to-emitter voltage and the α current gain of the lateral transistors. Each switch in the converter contains one common-base stage, yielding the lowest charge transfer and the fastest current settling time of any switch configuration. Consequently, the converter settles to within ½ LSB in less than 200 ns.

A ninth current source generates the bipolar offset current. The output current from the converter and the bipolar source is mirrored and scaled in the input buffer and summed with the differential current from the input voltage. The result is a full-scale voltage of 512 mV at the input of the comparator.

Table 1. Code conversions for the AD670

BPO/UPO input	Format input	Address	Code
0	0	Base	Unipolar straight binary
1	0	Base + 1	Bipolar offset binary
0	1	Base + 2	Unipolar two's complement
1	1	Base + 3	Bipolar two's complement



3. The 670's reference reduces noise so that millivolt-level inputs can be digitized. Linearity cross-plots of the zero and full-scale codes (top, bottom) show that noise levels caused by the comparator are less than ¼ LSB. Noise is discerned by the overlapping between each trace step in the staircase, and the vertical lines mark off ½ LSB.

Another novel circuit in the a-d converter merges the classic functions of a voltage reference with those of its control amplifier. The dynamic loop behavior and dc performance of the all-in-one reference are superior to those achieved if the circuits were separate. Moreover, it substantially saves chip space.

Bandgap references are often thought of as hav-

ing more noise on their outputs than do buried zener diodes. However, a dynamic crossplot can demonstrate nonlinearity and noise at each bit-code transition. The plot is created by summing a small ac signal with an analog reference voltage at the converter's input while simultaneously dithering or sweeping around the output code of interest. A simple 2-bit d-a converter creates a four-step output, corresponding to the states of the two least-significant bits. The output is applied to the Y input of an oscilloscope, and the ac dither signal to the X input.

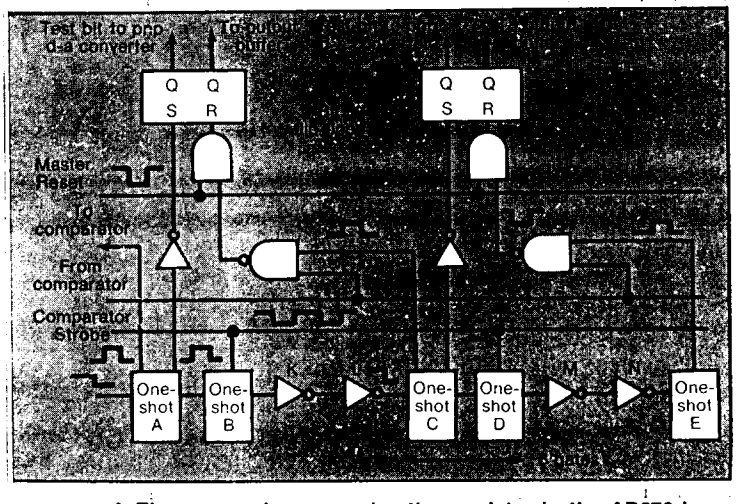
The reference in the 670 increases neither code-edge uncertainty nor noise significantly, as evident in linearity crossplots of the zero and full-scale codes (Fig. 3).

Getting on the bus

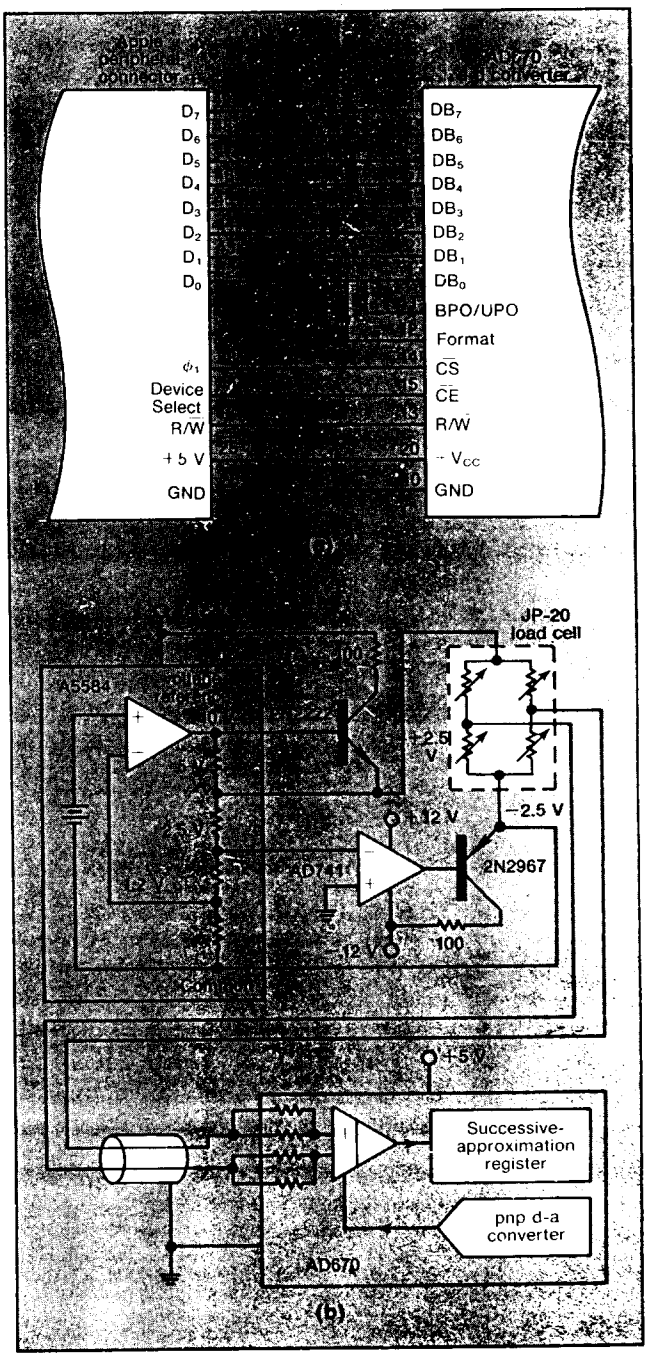
The microprocessor interface of the 670 consists of eight three-state output buffers, a Status output, and five control inputs, which are compatible with TTL, low-power Schottky TTL, and 5-V CMOS logic (see Fig. 1 again). The Chip Select and Chip Enable inputs ($\overline{CS}$ and $\overline{CE}$) are interchangeable and must be low to read data or to start a conversion.

Initiating a conversion entails a minimum pulse of 250 ns on $\overline{CS}$ and $\overline{CE}$, with the R/$\overline{W}$ line low. The normally low Status output will go high about 500 ns after $\overline{CE}$, $\overline{CS}$, and R/$\overline{W}$ go low, disabling the converter and telling it to ignore all inputs that might direct it to read or restart. If the same control lines are held low longer than the 10-μs conversion time, the 670 will convert continuously until one of the lines goes high. The rising edge of the high line must occur only when Status is high and not during the short times between cycles when the 670 is in a reset state prior to the next conversion cycle.

When $\overline{CS}$ or $\overline{CE}$ goes high, the data outputs remain in a high impedance state until a read cycle to the a-d converter is initiated by bringing $\overline{CS}$ and $\overline{CE}$ low, with R/$\overline{W}$ high. The outputs of the three-state buffers supply data to the bus within 250 ns.



4. The successive-approximation register in the AD670 has no shift register, relying instead on the inherent gate delays of 80 cascaded inverters. The eight taps along the delay line generate both the set or reset bits as well as the strobe for the comparator.



5. Through its microprocessor interface, the a-d converter links directly to the I/O bus of an Apple II (a). Thanks to the 670's differential input, the microcomputer can operate with signals from bridge circuits like load cells (b). The AD584 reference supplies a ±2.5-V excitation for a ±150-mV output when a force of ±20 lb is applied to the bridge. This is compatible with the 670's ±128-mV input range for a resolution of 2.1 oz/LSB.

During a write, or a start-conversion cycle, the Bipolar/Unipolar Offset input (BPO/UPO) and the Format input are latched into the converter. Tied to the data bus, these lines can be changed as each conversion commences. BPO/UPO controls the offset current: A logic 0 sets the converter to a unipolar range, and a logic 1 gives it a bipolar range (Table 1). The Format input selects either straight binary or two's complement as the form of the data output.

The inputs are latched on the first rising edge of $\overline{CS}$, $\overline{CE}$, R/$\overline{W}$, or Status, and the same edge initiates conversion, with the first cycle resetting the successive-approximation register. Conversion data may be read any number of times between conversions, but it is lost when a new conversion starts.

No circuit like an old circuit

Conventional successive-approximation registers are designed around shift registers and are basically static in nature. The speed at which they step from bit to bit is determined by an external clocking signal, which may range from dc to the maximum allowed by logic delays. (These delays can be significant in a linear-compatible I^2L process, since gate delays may be an order of magnitude longer than in, say, TTL.)

The register in the 670 is more dynamic because it has no shift register and needs no external clock to step through the successive-approximation algorithm. Instead, it relies on the inherent gate delay of the linear-compatible I^2L. The shift register is replaced by a delay line comprising 80 cascaded inverters, 10 for each bit.

The various pulses that set or reset bits and strobe the comparator are obtained by combining different taps along the inverter string. Sections of the delay line between the taps may be viewed as one-shots, whose outputs are delayed versions of their inputs. Strung one after another, the one-shots generate a series of properly timed pulses that execute the successive approximation. This technique is similar to the one used over 20 years ago in the first successive-approximation converters.

Looking at the delay line (Fig. 4), one-shot A unlatches the comparator, which samples the difference between the output of the pnp-based d-a converter and the 670's analog input. Once the d-a converter has settled, the rising edge of Comparator Strobe relatches the comparator.

Gates K and L delay the signal long enough to ensure that the comparator's output also has settled before gating it to the reset side of the bit flip-flop. A pulse coincident with the comparator's output sets the next bit, simultaneously switching one bit off and one bit on and thereby minimizing glitches in the output of the internal d-a converter.

Since the timing of the a-d converter is a function of gate delays, the design of its gates has been modified. Unlike the case with most I^2L circuits, the collector current rather than the injector current is controlled, supplying a first-order correction for transistor beta. As a result, gate delay is more consistent, ensuring a conversion time of no more than 10 μs.

Apple bites back

The control signals of the microprocessor interface make the 670 compatible with a variety of popular microcomputers, adding few if any extra parts. For example, when the chip is connected to an Apple II, the Device Select signal on the computer's peripheral connector serves as the converter's Chip Enable line (Fig. 5a). The $\overline{CS}$ line is connected to the computer's ϕ_1 clock, and the R/$\overline{W}$ lines are the same.

The simple, direct connections mean that no preamplifiers are needed for transducer-generated

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1 REM  PROGRAM IN APPLESOFT
2 REM  TO INTERFACE AD670
3 REM  8 BIT A/D CONVERTER
4 REM  TO DATA INSTRUMENTS
5 REM  MODEL JP-20 LOAD CELL
6 REM  WHICH HAS +/-150 mV
7 REM  OUTPUT FOR +/-20 POUNDS
8 REM  AND +/-2.5 VOLT INPUT
10  PRINT : PRINT : PRINT : PRINT
20  PRINT "TARE (T) OR WEIGH (W)";
30  INPUT A$
40  IF A$ <  > "T" GOTO 100
50  PRINT : PRINT "CLEAR SCALE"
60  FOR I = 1 TO 1000: NEXT I
65  GOSUB 670
70 TARE = W
80  PRINT "TARE IS ";TARE;" POUNDS"
90  PRINT : PRINT : PRINT
95  GOTO 20
100 REM  ACTUAL WEIGHT ROUTINE
105 PRINT "PUT THE OBJECT ON THE SCALE"
110 GOSUB 670
120 NETWT = W - TARE
125  PRINT : PRINT : PRINT : PRINT
130  PRINT "NET WEIGHT IS ";NETWT;" POUNDS"
140  PRINT : PRINT : PRINT
150  GOTO 110
670  REM  THIS ROUTINE INTERFACES
671  REM  THE AD670 TO THE APPLE
672  REM  AND AVERAGES 100 READINGS
673  REM  THEN CONVERTS THE ANSWER
674  REM  TO POUNDS
680  POKE 49360,2
681  REM  THE 2 SETS THE AD670 FOR
682  REM  OFFSET BINARY OPERATION
683  REM  AND BIPOLAR INPUT
684 W = 0
685  FOR I = 1 TO 100
690 X = PEEK (49360)
695 X = X - 128
700 X = (X / 150) * 20
710 W = W + X
720  NEXT I
730 W = INT (W / 10)
740 W = W / 10
750  RETURN
1000 END
```

signals. For instance, the 670 can link directly to semiconductor strain gauges, pressure transducers, and load cells, which typically produce 30 mV full scale per volt of excitation. With this setup, microprocessor-based systems can monitor real-world parameters, for example, in another application, the a-d converter can mate with Data Instruments' JP-20 load cell (Fig. 5b). Excited by ±2.5 V, the transducer delivers ±150 mV for a force of ±20 lb, providing a good match when the 670 is operating in a ±128-mV range. Resolution is about 2.1 oz/LSB over approximately ±17 lb, but it can be scaled down to exactly 2 oz/LSB by trimming the excitation voltage generated by the AD584 reference.

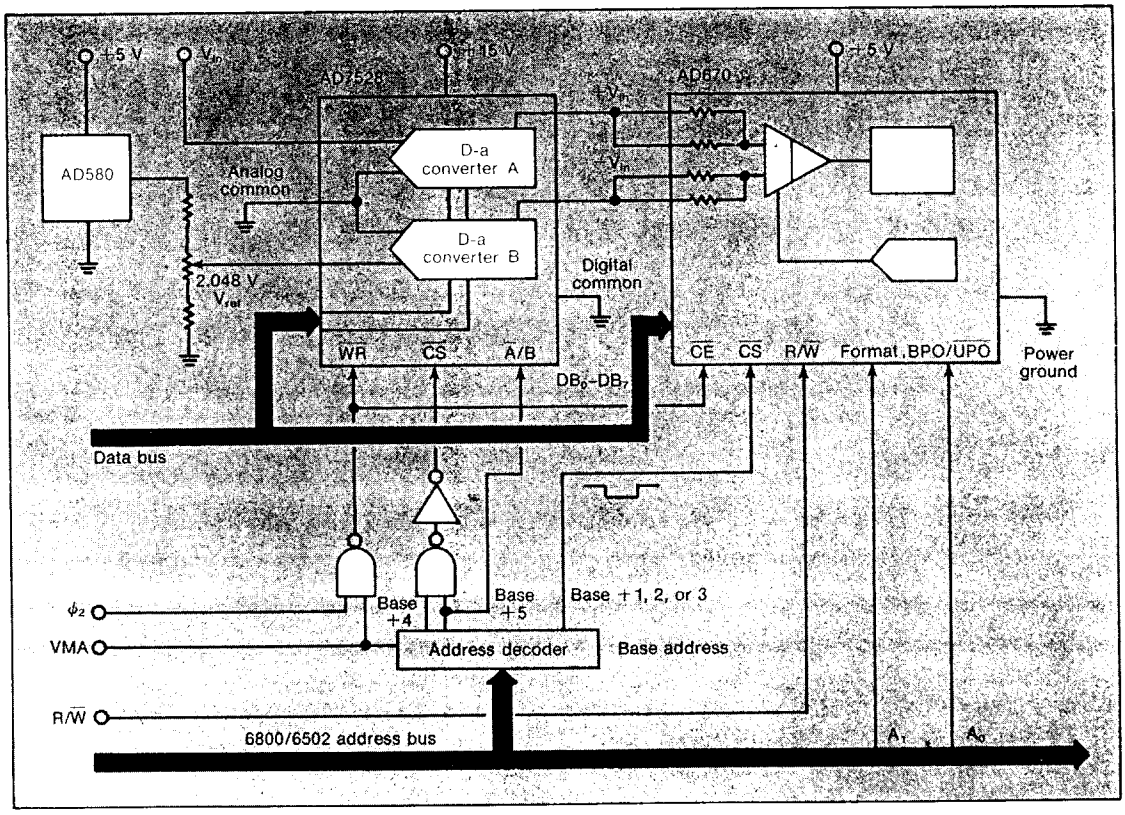
An Applesoft Basic program demonstrates how the converter meshes with both the Apple II and the load cell (Table 2). Coincidentally, the subroutine at line 670 creates the actual interface for the 670 a-d converter. The POKE instruction (line 680) configures the device for a bipolar input with offset binary output coding. It also initiates the conversion cycle, which the 670 completes in 10 μs. The results can be read immediately after POKE by the PEEK instruction. (In Applesoft Basic, "immediately" implies a delay of about 1 ms.) In the interest of reducing the probability of unstable readings or noise, the microcomputer averages 100 readings—doing so without slowing the program's execution.

Let the computer do it

As analog system designers finally come to the realization that microprocessors are their friends not their foes, they can revel in the true symbiotic relationship between converters and the processors.

Because of the 670's high input impedance, external circuits can be employed to scale the analog input. By placing one-half of a dual CMOS 8-bit multiplying d-a converter (AD7528) between V_{in} and the 670's positive input and the other half between V_{ref} and the negative input (Fig. 6), a microprocessor can control the a-d converter's gain and offset values. D-a converter A, acting as an attenuator, controls gain. D-a converter B sets the offset by controlling the voltage from the AD580 precision voltage reference.

Both CMOS converters work in the voltage-

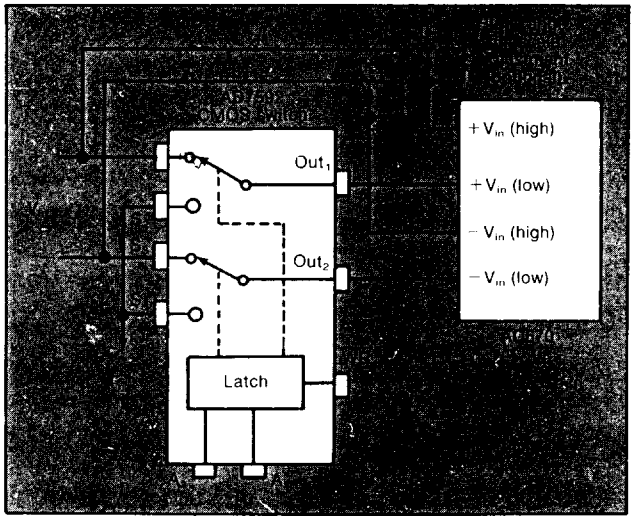


6. A dual 8-bit multiplying converter, the AD7528, controls the input levels of the 670 a-d converter. D-a converter A scales the voltage to the positive input of the 670, and converter B scales the voltage from the AD580 going to the negative input.

switching, or backward, mode, in which the reference inputs (pins 4 and 18) become the voltage outputs and the current outputs (pins 2 and 28) become the inputs. Their voltage swings about 2.5 V; thus they maintain an accuracy of 8 bits—more than enough accuracy for the 670, which has a common-mode range of about 2 V. Moreover, CMOS d-a converters working in this mode present a code-invariant impedance between their outputs and the analog common. Consequently, the offset caused by the input bias current of the 670 is constant, regardless of the code applied to the d-a converters.

The dual d-a converter and the a-d converter interface with a 6800/6502 bus. The address logic decodes a base address, setting A_0 and A_1 to a logic 0. The 670's $\overline{CS}$ input is low (true) for the base address, as well as for the base plus 1, 2, and 3.

The BPO/UPO and Format inputs are tied respectively to A_0 and A_1. Writing to the base address yields a unipolar offset with a straight binary output; to the base address plus 1, bipolar with offset binary; to the base address plus 2, unipolar with two's complement; and to the base address plus 3,



7. The gain ranges of the 670 can be regulated by a CMOS analog latching switch. When a microprocessor detects an overrange at 1-mV LSB, it automatically switches the converter to 10 mV/LSB.

bipolar with two's complement (see Table 1 again). The base address plus 4 loads d-a converter A, and the base address plus 5 loads d-a converter B. By reading any of the first four addresses, the microprocessor can find out the results of the a-d conversion.

D-a converter A scales down the positive input of the 670. A full-scale code (all 1s) goes through untouched with a gain of 255/256 (near unity), whereas a zero code cuts off the input completely. D-a converter B sets V_{ref}, which is connected to the negative input of the 670. The effective value of V_{in} is set by the following equation:

$$V_{in} = \frac{NC}{NA} 256\ mV + \frac{NB}{NA} V_{ref}$$

where:

NA = code fed into d-a converter A
NB = code fed into d-a converter B
NC = code generated by a-d converter
V_{ref} = 2.048 V

The gain and the offset of the 670 are controlled by software and can vary for different input signals.

Measurement can reach a resolution higher than 8 bits with a two-step conversion technique. Here converter A divides the input by eight and sets its code equal to 32; meanwhile converter B is setting its code to 0, and the 670 is completing a unipolar conversion. Converter B is then loaded with the result of that conversion, applying a fraction of V_{ref}, approximating V_{in}, to the 670's negative input. The fraction is then subtracted from the positive input voltage. If converter A is now set to full scale and the result of the subtraction undergoes a second a-d conversion (bipolar two's complement), the output of the 670 will resolve 1 mV over the input's common-mode range.

The V_{ref} input to d-a converter B could easily be changed to a second signal source rather than remain a fixed reference voltage. In this instance, the altered V_{ref} and V_{in} can be independently scaled by the dual d-a converter, with the difference between their outputs provided by the differential input stage of the 670, whose output is determined by the equation:

$$NC = \frac{(NA/256)\ V_A - (NB/256)V_B}{256\ mV}$$

where V_A and V_B are the input voltages for d-a converters A and B, respectively, and NC is the output code.

Switching gain-range

An analog CMOS switch, the AD7592, can shift the a-d converter's gain between high and low ranges (Fig. 7). The two positive inputs are tied together to obtain the converter's full-scale range of 0 to 255 mV. In the alternate position, the switch shorts the low V_{in} inputs to ground, creating a 10-to-1 division of V_{in} and changing the converter's range to 0 to 2.55 V.