International
IOR Rectifier

PD - 9.1282

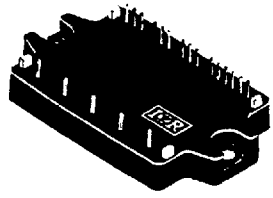
PROVISIONAL

PM20CMA060

IGBT INTELLIGENT MODULE

Features

- 3 phase IGBT bridge with drive and protection circuit.
- 3 kW output power at 300VDC, 8kHz, T_C = 85°C
- "UltraFast"™ IGBT and "HEXFRED"™ Ultrafast, Soft Recovery Diodes.
- Over current short circuit, earth fault, under voltage and over temperature protection.
- Fault feedback.
- Carrier frequencies up to 25kHz



PM

Description

The PM20CMA060 is a 3 phase intelligent IGBT bridge with gate drive and protection circuit. It contains IR "UltraFast"™ series IGBTs and "HEXFRED"™ Ultrafast, soft recovery diodes, rendering it suitable for 5 to 25 kHz switching frequencies. Built-in driver and protection circuit makes it the ideal building block for AC Motor Speed Controllers, Brushless Servo Drives, UPS and other inverter systems.

Absolute Maximum Ratings:

Power Circuit

	Parameter	Max.	Units
I_C @ T_C = 25°C	Continuous Collector Current, each IGBT, one IGBT in conduction	20	A
I_C @ T_C = 85°C	Continuous Collector Current, each IGBT, one IGBT in conduction	12	
V_{CE}	Continuous Collector-to-Emitter Voltage	600	V
V_{CC}	Supply Voltage Between P-N	450	
P_D @ T_C = 85°C	Power Dissipation, One IGBT in Conduction	33	W
T_J	Operating Junction Temperature Range	-20 to 150	°C

Driver and Protection Circuit

	Parameter	Max.	Units
V_D	Driver Supply Voltage	20	V
V_{IN}	Logic Input Voltage Between Input Pin and GND	-0.30 to 5.3	
V_{FO}	Open Collector Fault Output Voltage	-0.3 to V_D+0.3	
I_{DA}	Average Input Supply Current	15	mA
I_{FO}	Fault Output Current	20	

Total System

	Parameter	Max.	Units
V_{CC} (PROTECTED)	Supply Voltage Protected Against OC and SC Faults ①	400	V
V_{ISOL}	RMS Isolation Voltage, Any Terminal to Case, 1 Minute	2500	
T_C	Case Operating Temperature Range	-20 to 100	°C
T_{STG}	Storage Temperature	-40 to 125	
	Mounting Torque	2.0	N•m

Electrical Characteristics @ T_J = 25°C (unless otherwise specified):

Power Circuit

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{CE(on)}$	Collector to Emitter Saturation Voltage	—	2.7	—	V	V_{GE} = 15V, I_C = 20A, T_J = 150°C
V_{FM}	Diode Forward Voltage	—	—	2.4		I_C = 20A, T_J = 150 C
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{CE} = 600V, V_{GE} = 0V

Driver and Protection Circuit

	Parameter	Min.	Typ.	Max.	Units	Conditions
V_D	Supply Voltage	13.5	15	16.5	V	
V_{DUV+}	Under Voltage Set Level	—	—	+9.5		
V_{DUV-}	Under Voltage Reset Level	+8.2	—	—		
V_{IH}	Logic "0" Input Voltage (OUT=LO)	2.2	—	—		
V_{IL}	Logic "1" Input Voltage (OUT=HI)	—	—	0.8		
I_{DA}	Average Supply Current	—	11	15	mA	
I_{DP}	Peak Supply Current	—	—	600	mA	20µs Initial Bootstrap Charging
I_{IN+}	Logic "1" Input Bias Current (OUT=HI)	—		900	µA	
I_{IN-}	Logic "0" Input Bias Current (OUT=LO)	—		500		
f_C	PWM Carrier Frequency	—	—	25	kHz	
t_{DT}	Dead Time	—	2.5	—	µs	
$t_{FLT(IN)}$	Input Filter Time (All Six Inputs)	—	310	—	ns	V_{IN} = 0V & 5V
R_{IN}	Logic Input Pull-up Resistor	—	50	—	kΩ	
I_{SC}	Short Circuit Current Trip Level	—	40	—	A	
I_{OC}	Over Current Trip Level	21	24	—		
t_{OC}	Over Current Delay Time	—	20	—	µs	
I_{EF}	Earth Fault Current Trip Level	—	32	—	A	
t_{EF}	Earth Fault Delay Time	—	2.0	—	µs	
T_{OT}	Over Temperature Trip Level, at Case	—	100	—	°C	
t_{DET}	Fault Detect. to Power Stage Shut Down Delay	—	2.0	—	µs	
t_{D1}	Internal Shut Down to Fault Output "low" Delay	—	1.5	—		
$t_{FLT(OUT)}$	Fault Output Pulse Width	—	2.0	—	ms	
$t_{FLT(CLR)}$	Fault Clear Time, LIN U,V,W, Kept High	—	10	—	µs	
t_{D2}	Fault Clear Recognition to Fault Reset Delay	—	3.0	—		
$I_{F(OUT)}$	Open Collector Fault Current	—	—	20	mA	
C_{ISO}	Capacitance between Pin & Module Case	—	150	—	pF	

Thermal Resistance:

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (IGBT)	Junction-to-Case, each IGBT, one IGBT in conduction	—	2.0	°C/W
$R_{\theta JC}$ (DIODE)	Junction-to-Case, each diode, one diode in conduction	—	2.8	
$R_{\theta CS}$ (MODULE)	Case-to-Sink, flat, greased surface	0.05	—	
Wt	Weight of Module	80	—	g

Notes:

① V_D = 13.5 to 16.5V, T_J = 125°C at Start

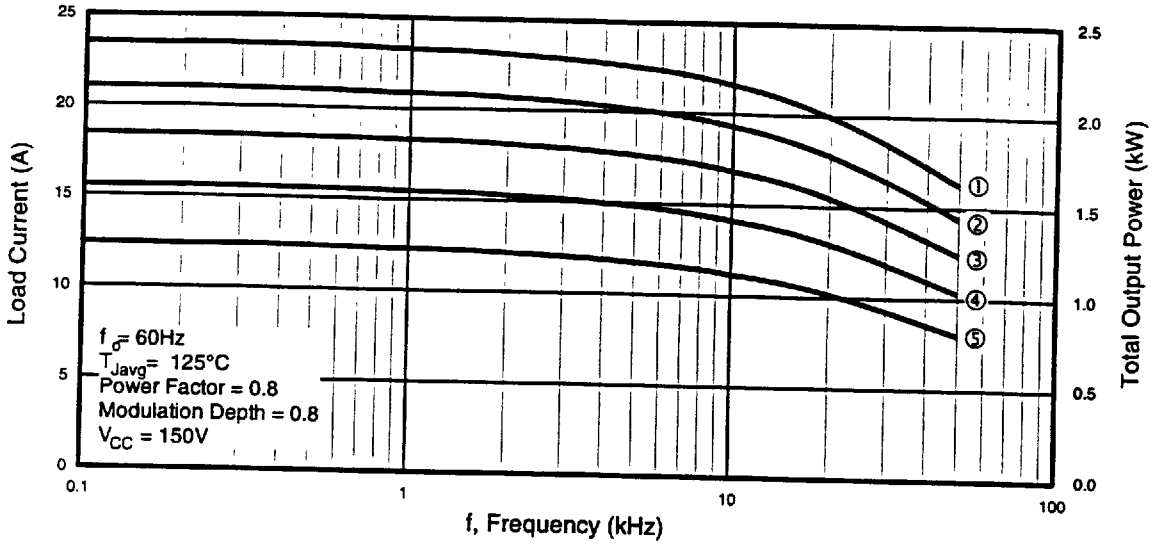


Fig. 1 - Typical Output Power and Current vs. Switching Frequency, at 150VDC

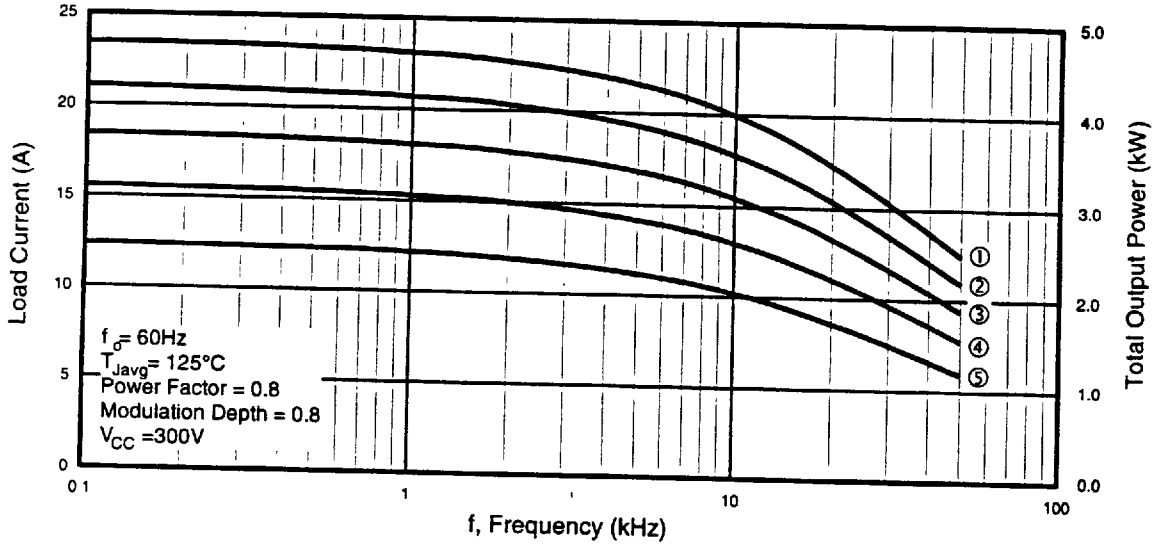


Fig. 2 - Typical Output Power and Current vs. Switching Frequency, at 300VDC

Curve	1	2	3	4	5
T_{SINK}, °C	60	70	80	90	100
P_D Total, W	194	164	135	105	75

Table Common for Figure 1 and Figure 2

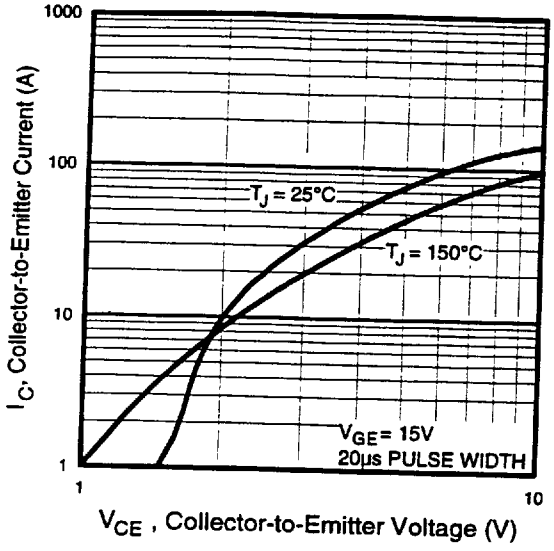


Fig. 3 - Typical Output Characteristics

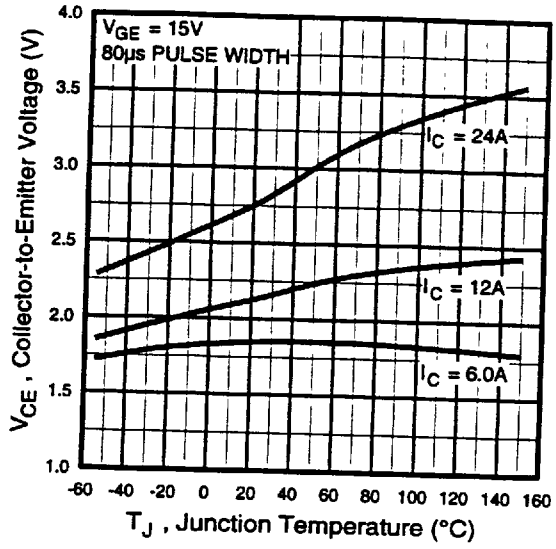


Fig. 4 - Collector-to-Emitter Voltage vs. Junction Temperature

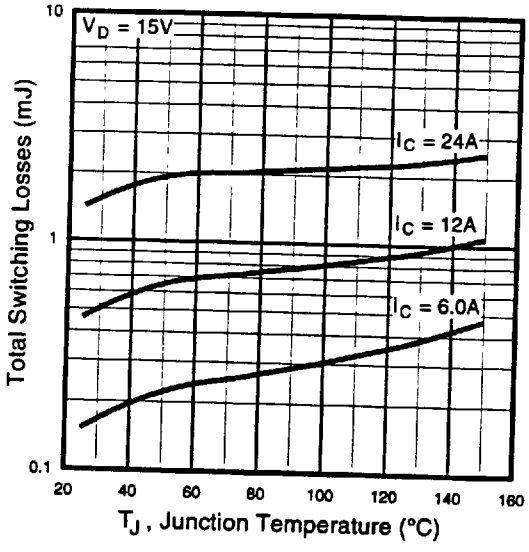


Fig. 5 - Typical Switching Losses vs. Junction Temperature

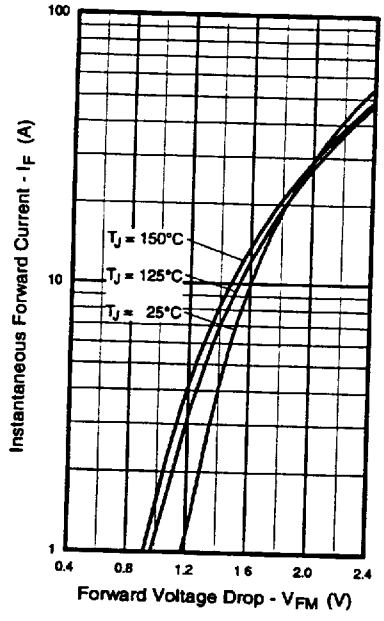


Fig. 6 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

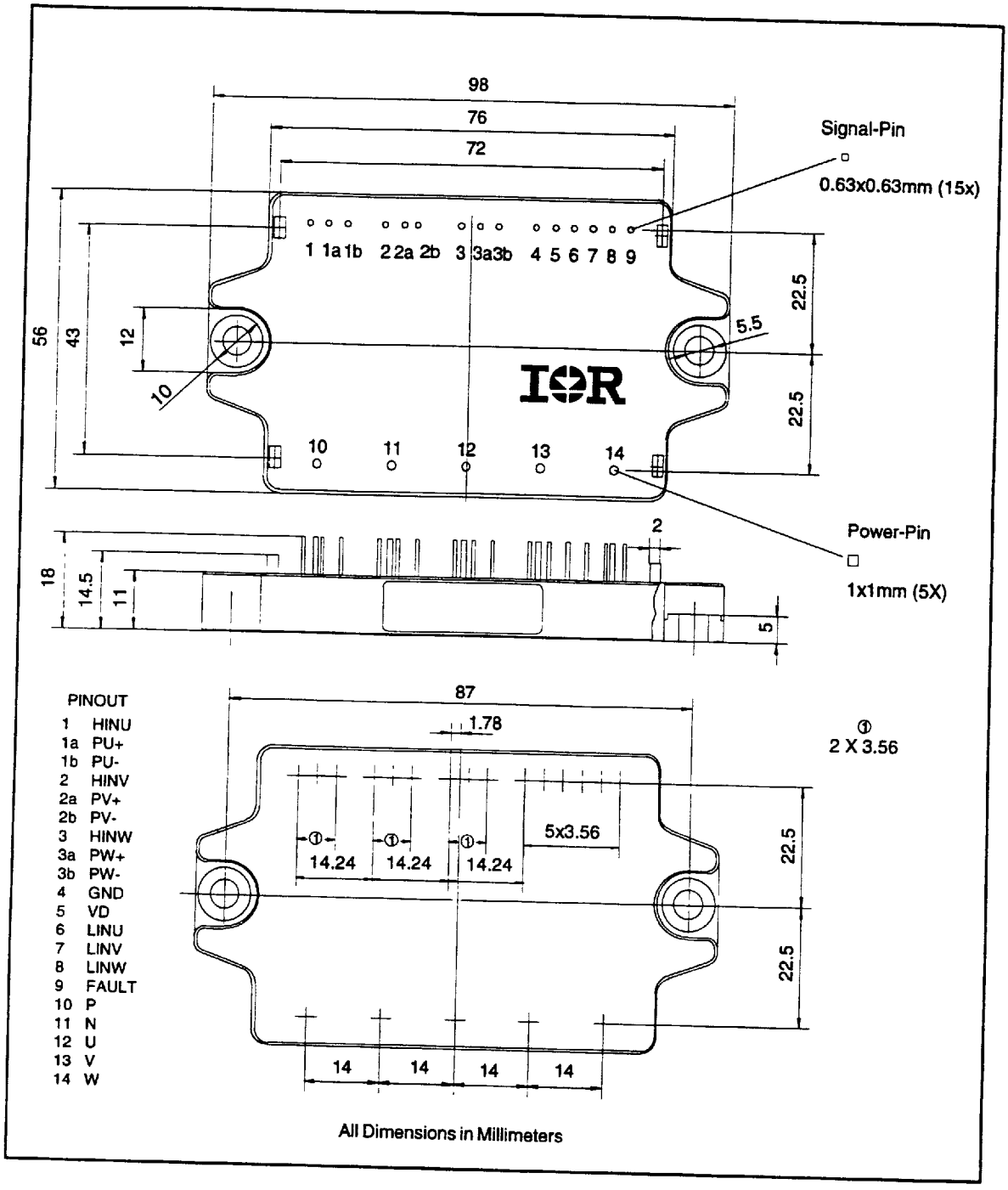


Fig. 7 - Package Outline

Application Information

Input Control Logic

Output of power stage is out of phase with input signal. Internal 50 kΩ pull-up resistor to V_D from all 6 inputs ensure that all transistors are off if the inputs are open circuited. A 300 ns filter at input prevents spurious triggering due to noise. Input logic provides deadtime when nearly coincident transitions take place at LIN and HIN pins of same channel and prevents shoot-through conditions. When driving the module inputs with open collector, external pull up resistor to V_D should be higher than 1 kΩ.

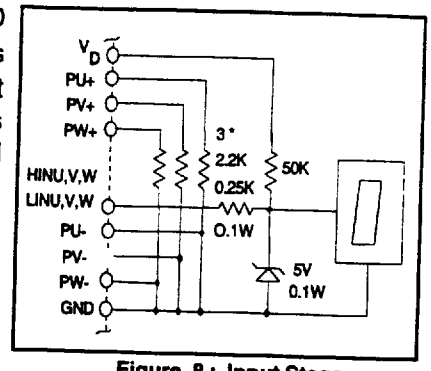


Figure 8 : Input Stage

Bootstrap Supply

The floating power supplies - PU, PV and PW are connected to resistive loads and the drive is generated through bootstrap technique. Each high side device has 2.2 µF bootstrap capacitor, fed through individual bootstrap diode and common 22 Ω charging resistor to V_D. At start-up or after an interruption in switching greater than 2 s, it is necessary to switch on all three low side transistors for at least 200µs before switching the high side transistors. Maximum on time for high side transistors is 200 ms.

Temperature Monitoring

Temperature is sensed in close proximity of the junction, minimizing errors caused by the module base plate thermal capacitance. Thermal protection is effective for symmetrical three phase loads.

Fault Logic

Short circuit, earth fault, over current, over temperature and V_D undervoltage conditions cause trips and are latched. Open collector FAULT output goes low for at least 2 ms when fault latch is set. It can be reset by holding all three LIN high for 12 µs or cycling V_D through undervoltage condition. Bootstrap supply of high side switches is individually monitored for undervoltage and has cycle by cycle shutdown for the particular switch and is not latched. Active low open collector FAULT pin can be connected to logic circuit, fault indicator LED or optocoupler for feedback to controller.

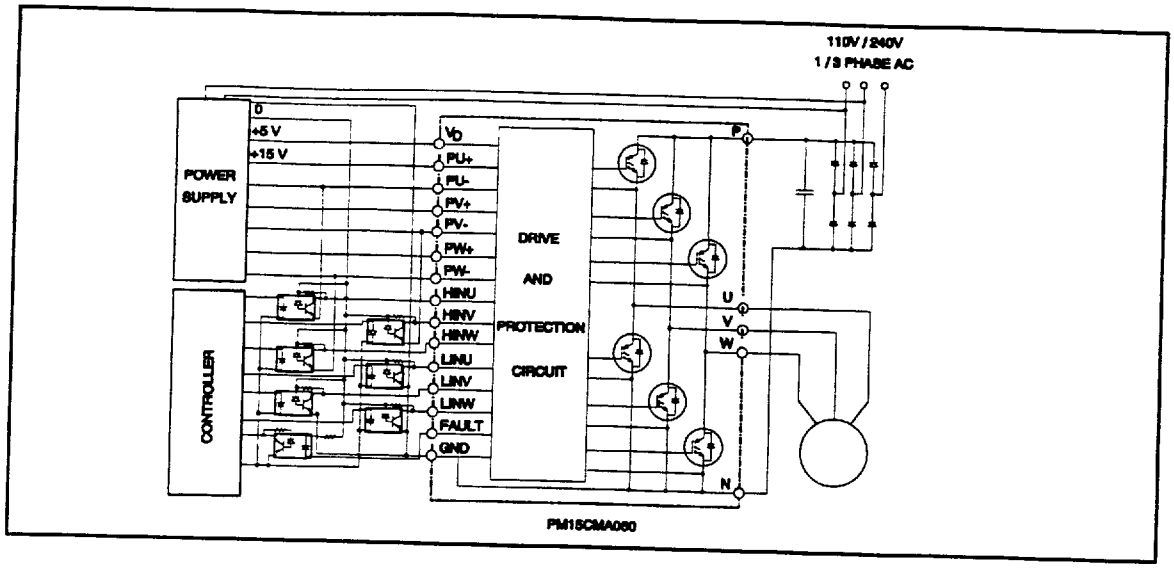


Fig. 9 - Typical Application Scheme

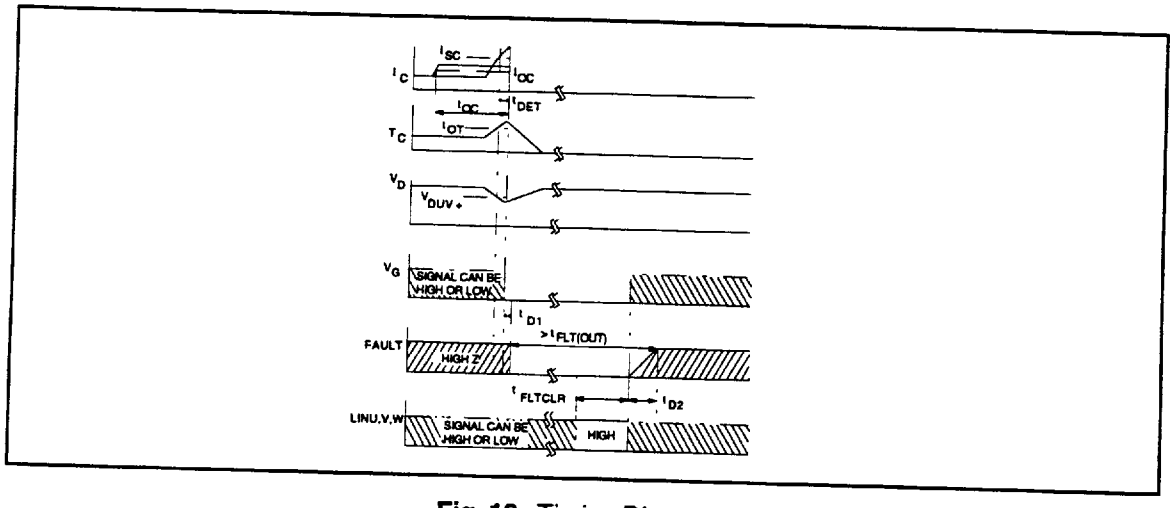


Fig. 10 - Timing Diagram

International IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: (44) 0883 713215
IR CANADA: 7321 Victoria Park Ave., Suite 201, Markham, Ontario L3R 3L1, Tel: (905) 475 1897 **IR GERMANY:** Saalburgstrasse 157, 61350 Bad Homburg Tel: 6172 37066 **IR ITALY:** Via Liguria 49, 10071 Borgaro, Torino Tel: (39) 1145 10111 **IR FAR EAST:** K&H Bldg., 2F, 3-30-4 Nishi-Ikeburo 3-Chome, Toshima-Ki, Tokyo 171 Tel: (03)3983 0641 **IR SOUTHEAST ASIA:** 315 Outram Road, #10-02 Tan Boon Liat Building, 0316 Tel: 65 221 8371