

397-763



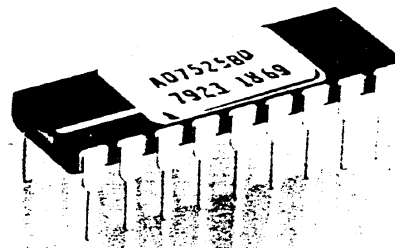
3 1/2 Digit BCD Monolithic CMOS Digitally Controlled Potentiometer

FEATURES

- Resolution: 3 1/2 Digit BCD (1999 Counts)
- Nonlinearity: $\pm 1/2$ LSB T_{min} to T_{max}
- Gain Error: $\pm 0.05\%$ FS
- Excellent Repeatability Accuracy
- Low Power Dissipation

APPLICATIONS

- Thumbwheel Switch Voltage Dividers
- Digitally Controlled Gain Circuits
- Digitally Controlled Attenuators
- BCD Multiplying DACs
- Low Power Converters



GENERAL DESCRIPTION

The AD7525 is a monolithic CMOS 3 1/2 digit BCD digitally controlled potentiometer designed for precision incremental voltage-divider applications.

With the addition of an external op amp, the output can be digitally controlled from 0 to $1.999V_{IN}$ with resolution of $0.001V_{IN}$.

AC or DC voltage up to $\pm 10V$ can be applied to the input providing high application flexibility in fields such as audio gain control, etc.

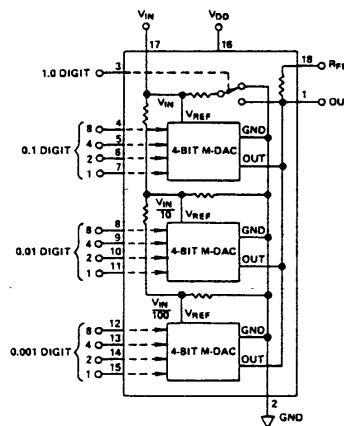
Digital control, excellent repeatability and 0.05% accuracy make the AD7525 an ideal replacement for 10-turn potentiometers or thumbwheel switch voltage dividers using discrete resistor networks.

Packaged in an 18-pin DIP, the AD7525 uses an advanced CMOS fabrication process combined with wafer laser trimming.

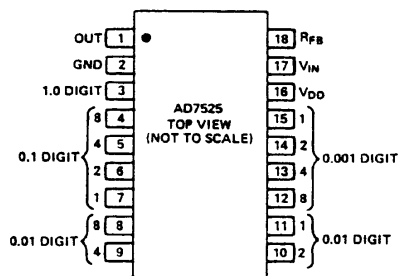
ORDERING INFORMATION

| Package and Temperature | Nonlinearity $\pm 1/2$ LSB | Nonlinearity ± 1 LSB |
|---|----------------------------|--------------------------|
| 18-Pin Plastic 0 to $+70^{\circ}C$ | AD7525LN | AD7525KN |
| 18-Pin Ceramic $-25^{\circ}C$ to $+85^{\circ}C$ | AD7525CD | AD7525BD |
| 18-Pin Ceramic $-55^{\circ}C$ to $+125^{\circ}C$ | AD7525UD | AD7525TD |

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

P.O. Box 280; Norwood, Massachusetts 02062 U.S.A.
Tel: 617/329-4700 Twx: 710/394-6577
Telex: 924491 Cables: ANALOG NORWOODMASS

SPECIFICATIONS (V_{DD} = +15V; V_{PIN1} = 0V; V_{IN} = +10V unless otherwise stated)

| PARAMETER | T _A = +25°C | T _A = Operating Temperature Range | CONDITION |
|---|---|---|---|
| ACCURACY | | | |
| Resolution ¹ | 1 part in 2000 | 1 part in 2000 | |
| Nonlinearity ² | | | |
| AD7525KN, BD, TD | ±1LSB max | ±1LSB max | BCD 0.000 to 1.999 |
| AD7525LN, CD, UD | ±1/2LSB max | ±1/2LSB max | BCD 0.000 to 1.999 |
| Gain Error ³ | ±0.05% FS typ | — | BCD = 1.999 |
| Gain TC | ±25ppm/°C max | — | BCD = 1.999 |
| Output Leakage Current (pin 1) | 100nA max | 400nA max | BCD = 0.0000 |
| DYNAMIC PERFORMANCE | | | |
| Switching Time | 1μs max ⁴ | 1μs max ⁵ | V _{IN} = +5V, R _{OUT} (pin 1) = 100Ω, Digital Inputs = V _{IL} to V _{IH} or V _{IL} , V _{PIN1} measured from 10% to 90% |
| Feedthrough Error | ±0.05%V _{IN} max ⁵ | ±0.1%V _{IN} ⁵ | V _{IN} = ±10V, 20kHz sinewave |
| ANALOG INPUT | | | |
| Input Resistance (pin 17) ⁶ | 2kΩ min/10kΩ max | 2kΩ min/10kΩ max | |
| V _{IN} Range (recommended) | ±10V max | ±10V max | |
| ANALOG OUTPUT | | | |
| Output Capacitance | | | |
| C _{OUT} (pin 1) | 60pF max ⁵ 200pF max ⁵ | 60pF max ⁵ 200pF max ⁵ | Digital Inputs = BCD 0000 Digital Inputs = BCD 1999 |
| R _{FB} Resistance (pin 18 to pin 1) ⁶ | 8kΩ min/40kΩ max | 8kΩ min/40kΩ max | |
| DIGITAL INPUTS | | | |
| Input HIGH Voltage | | | |
| V _{IH} | +14.5V min | +14.5V min | |
| Input LOW Voltage | | | |
| V _{IL} | +0.5V max | +0.5V max | |
| Input Leakage Current | ±1μA max | ±10μA max | Digital Input = 0V or V _{DD} |
| Input Capacitance | 5pF max ⁵ | 5pF max ⁵ | |
| Input Coding | 3¼ Digit BCD (1999 Counts) | 3¼ Digit BCD (1999 Counts) | |
| POWER SUPPLY | | | |
| V _{DD} Range | +5V to +17V | +5V to +17V | Functional with Degraded Performance |
| V _{DD} | +15V ±5% | +15V ±5% | Rated Accuracy |
| I _{DD} | 500μA max | 1mA max | Digital Inputs = V _{IL} or V _{IH} |

NOTES

¹ Commercial devices are sample tested over temperature.

² Monotonicity is guaranteed on the AD7525LN, CD and UD versions over T_{min} to T_{max}.

³ Gain Error is measured using the AD7525 internal feedback resistor. FS is "Full Scale" (BCD = 1.999).

⁴ AC parameter, sample tested at +25°C to ensure conformance to specification.

⁵ Guaranteed, not tested.

⁶ Thin-Film resistor temperature coefficient is approximately -300ppm/°C.

Specifications subject to change without notice.

CAUTION

1. ESD (electro-static discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.
2. Do not apply voltages more negative than GND or more positive than V_{DD} to any pin except V_{IN} (pin 17) and R_{FB} (pin 18).
3. The inputs of some IC amplifiers (especially high speed types) present a low impedance to $V-$ during power sequencing. To prevent the AD7525 OUT terminal (pin 1) from exceeding $-300mV$ (which causes catastrophic substrate current), a Schottky diode, HSCH 1001 or equivalent, is recommended. While not required for most amplifier types, provision for the diode should be made during layout. The diode should be connected between OUT (pin 1) and GND (pin 2) as shown in Figure 4. Protection Schottkys not required when using TRI-FET output amplifiers such as the AD542 or AD544.

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ C$ unless otherwise noted)

| | |
|--|-------------------|
| V_{DD} (to GND) | -0.3V, +17V |
| V_{IN} (to GND) | $\pm 25V$ |
| R_{FB} (to GND) | $\pm 25V$ |
| Digital Input Voltage (to GND) | -0.3V to V_{DD} |
| V_{PIN1} (to GND) | -0.3V to V_{DD} |
| Power Dissipation (Package) | |
| Plastic (Suffix N) | |
| To $+70^\circ C$ | 670mW |
| Derates above $+70^\circ C$ by | $.8.3mW/^\circ C$ |
| Ceramic (Suffix D) | |
| To $+75^\circ C$ | 450mW |
| Derates above $+75^\circ C$ by | $.6mW/^\circ C$ |

Operating Temperature

| | |
|--|---------------------------------|
| Commercial Plastic (KN, LN Versions) | 0 to $+70^\circ C$ |
| Industrial Ceramic (BD, CD Versions) | $-25^\circ C$ to $+85^\circ C$ |
| Extended Ceramic (TD, UD Versions) | $-55^\circ C$ to $+125^\circ C$ |

TERMINOLOGY

SWITCHING TIME: In a D/A converter, the switching time is the time taken for an analog switch to change to a new state from the previous one. It includes delay time, and rise time from 10% to 90%, but does not include settling time, which is a function of the output amplifier used.

OUTPUT CAPACITANCE: Capacitance from OUT terminal (pin 1) to ground.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{IN} (pin 17) to OUT (pin 1) with all digital inputs LOW.

PRINCIPLES OF OPERATION

CIRCUIT DESCRIPTION

The AD7525, a $3\frac{1}{2}$ digit BCD multiplying DAC, consists of a thin-film R/2R ladder, interquad voltage dividers and 13 N-channel MOS SPDT current steering switches. Most applications require the addition of only an external operational amplifier.

Referring to Figure 1, the "1.0 Digit" is a 1-bit multiplying DAC (composed of SW_1 and R_1) while the 0.1, 0.01, and 0.001 digits are 4-bit multiplying DAC's (DAC1, DAC2, and DAC3) connected by 10:1 dividers (composed of R_{IN2} , R_2 , R_3 and R_{IN3} , R_4 , R_5).

DAC1 is expanded to show the R/2R ladder and switch network. With input voltage V_{IN} , the currents in each shunt arm are (starting at the left) $V_{IN}/2R$, $V_{IN}/4R$, $V_{IN}/8R$ and $V_{IN}/16R$. A logic ONE applied to a digital input steers that shunt arm's current to OUT, while a logic ZERO steers the current to GND.

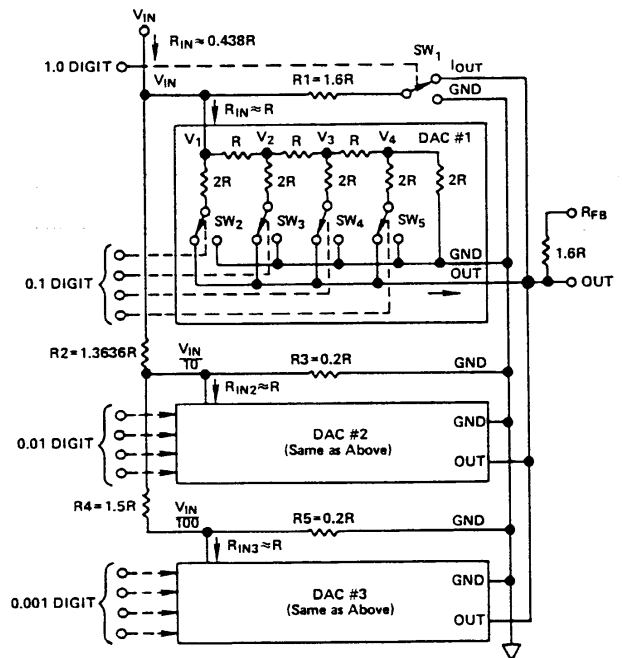


Figure 1. AD7525 Circuit Diagram

EQUIVALENT CIRCUIT

As shown in Figure 2, the AD7525 is a digitally controlled π -network attenuator with signal input "VIN" (pin 17), signal output "OUT" (pin 1), signal common "GND" (pin 2) and digital control "BCD input" (pins 3-15).

With OUT (pin 1) terminated at op amp virtual ground and R_{FB} (pin 18) connected to the op amp output, the nominal transfer equation is:

$$V_{OUT} = -V_{IN} BCD$$

where $0.000 \leq BCD \leq 1.999$

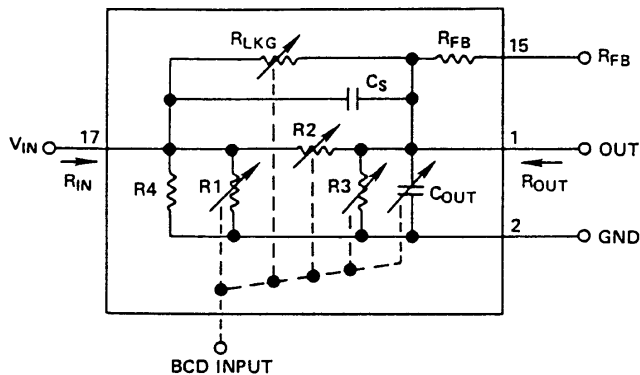


Figure 2. Functional Equivalent Circuit

OUTPUT AMPLIFIER CONSIDERATIONS

Amplifier Offset

The output resistance at OUT (pin 1) is code dependent, varying between ∞ to $0.35 R_{LDR}$. For a fixed feedback resistor of value $1.6 R_{LDR}$ (Figure 3), the output error for a fixed amplifier offset (V_{OS}) is:

$$V_{ERROR} = \left(1 + \frac{R_{FB}}{R_{OUT}}\right) V_{OS}$$

Case 1: ($R_{OUT} = \infty$)

$$V_{ERROR} = \left(1 + \frac{R_{FB}}{\infty}\right) V_{OS}$$

$$V_{ERROR} = V_{OS}$$

Case 2: ($R_{OUT} = 0.35 R_{LDR}$)

$$V_{ERROR} = \left(1 + \frac{1.6 R_{LDR}}{0.35 R_{LDR}}\right) V_{OS}$$

$$V_{ERROR} = (1 + 4.6)V_{OS} = 5.6 V_{OS}$$

Cases 1 and 2 show that amplifier offset in conjunction with a changing output resistance at OUT (pin 1) create nonlinearity error, in addition to a simple offset term.

It is therefore recommended that amplifier initial offset be adjusted to less than $100\mu V$ (as measured between the amplifier input terminals). The offset voltage over the temperature range of interest should not exceed $250\mu V$. See application hint #2, below.

Do not include the usual bias current compensation resistor in the amplifier noninverting terminal. Instead, the amplifier should have a bias current which is low over the temperature range of interest. Bias current causes "output offset" of magnitude $(I_B)R_{FB}$.

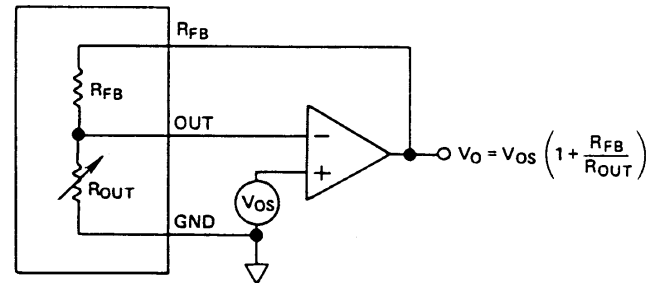


Figure 3. Noise Gain Equivalent Circuit

High Frequency Amplifiers

R_{FB} and C_{OUT} create a phase lag in the output amplifier's feedback circuit. This phase lag, in conjunction with the amplifier's phase lag, may cause ringing or oscillation. When using a high speed amplifier, shunting the amplifier input to output with $5-20pF$ of feedback capacitance ensures stability.

APPLICATION HINTS

1. If an output voltage range of ± 19.99 volts is required (i.e., AD7525 $V_{IN} = \pm 10V$, $BCD = 1.999$), a high voltage output amplifier with appropriate supply voltages must be used.
2. To maintain circuit linearity, the op amp offset voltage should not exceed 2% of the circuit resolution. (Resolution = $V_{IN} \div 1000$)
3. CMOS logic inputs exhibit an input impedance on the order of $100M\Omega$. Unused CMOS inputs must always be tied to a known logic state. If single-pole single-throw thumbwheel switches are used to drive the digital inputs of the AD7525, external $10k\Omega$ pull-down (pull-up if switch coding is complementary (BCD) resistors must be used.

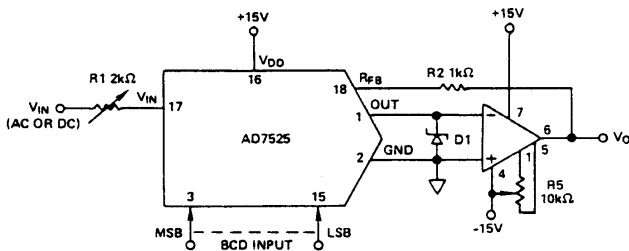


Figure 4. Digitally Controlled Attenuator Circuit

| BCD INPUT | | | | ANALOG OUTPUT | | |
|-----------|------|------|-------|--------------------------------|--------------|----------------|
| 1.0 | 0.1 | 0.01 | 0.001 | Equivalent Decimal Input | V_O/V_{IN} | V_O |
| 1 | 1001 | 1001 | 1001 | 1.999 | -1.999 | $-1.999V_{IN}$ |
| 1 | 0000 | 0000 | 0001 | 1.001 | -1.001 | $-1.001V_{IN}$ |
| 1 | 0000 | 0000 | 0000 | 1.000 | -1.000 | $-1.000V_{IN}$ |
| 0 | 1001 | 1001 | 1001 | 0.999 | -0.999 | $-0.999V_{IN}$ |
| 0 | 0101 | 0000 | 0000 | 0.500 | -0.500 | $-0.500V_{IN}$ |
| 0 | 0000 | 0000 | 0000 | 0.000 | 0 | 0 |

Note 1:

For proper BCD coding, the 0.1 digit, 0.01 digit or 0.001 digit must not exceed BCD "9" (1001).

Table 1. Analog Input/Output Relationship vs. Digital Input

CALIBRATION PROCEDURE

Offset Adjustment:

1. Apply BCD code 0.000 (0 0000 0000 0000) to the AD7525 digital inputs.
2. Connect a high resolution, high impedance voltmeter between V_O (amplifier output) and pin 2 of the AD7525.
3. Adjust amplifier's trimpot for minimum reading on the voltmeter ($<100\mu V$).

Gain Adjustment:

1. Apply BCD code 1.000 (1 0000 0000 0000) to the AD7525 digital input.
2. Apply +10V to the V_{IN} input of Figure 1.
3. Connect the voltmeter between V_O (amplifier output) and pin 2 of the AD7525.
4. Adjust R_1 until $V_O = -10V$.

APPLICATION – THUMBWHEEL SWITCH ATTENUATOR

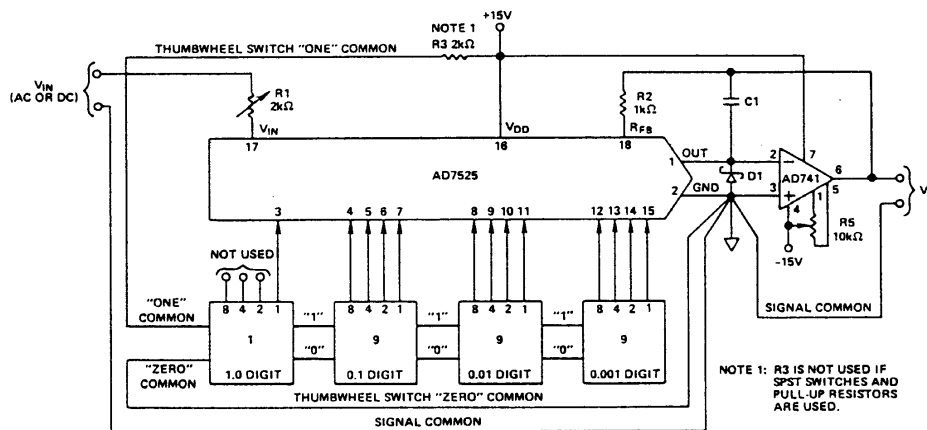


Figure 5. Thumbwheel Switch Attenuator

The circuit shown in Figure 5 is a precision voltage divider similar to 10-turn pots and thumbwheel switch incremental-voltage-divider assemblies. Advantages of the circuit are:

- Economy
- Low Output Impedance
- Resolution 0.1% V_{IN}
- Excellent Repeatability Accuracy
- Overrange Capability

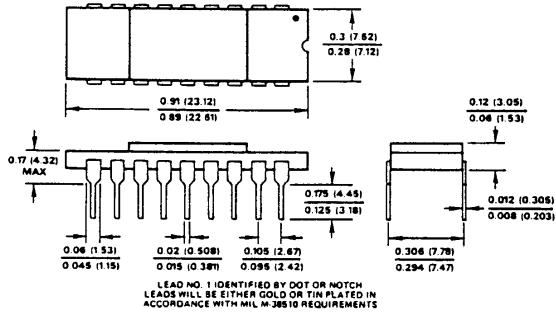
The BCD coded thumbwheel assembly applies BCD data to the AD7525 digital inputs. The switch assembly shown has single-pole-double-throw action, thus the BCD inputs are

pulled either to +15V or GND (available from AMP, Harrisburg, PA; CHERRY, Waukegan, Illinois; or SAE, Santa Clara, California). Resistor R_3 limits current if make-before-break switches are used. SPST switch assemblies can be used; however, appropriate pull-up or pull-down resistors must be used on each digital input, depending upon whether the switch coding is BCD or complementary BCD. This ensures each digital input has appropriate V_{IH} or V_{IL} levels applied.

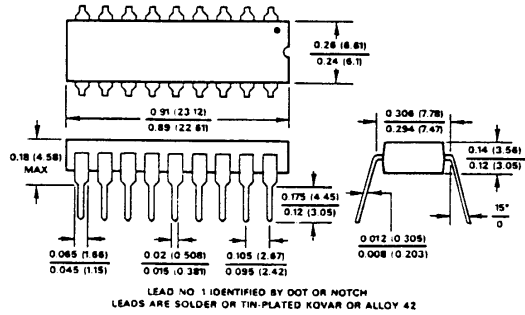
Resistors R_1 and R_2 provide gain adjustment capability. R_5 is used to adjust the amplifier input offset voltage to less than $100\mu V$. Diode D_1 (HSCH 1001) provides AD7525 output protection (see Caution note 3).

MECHANICAL INFORMATION
Dimensions shown in inches and (mm).

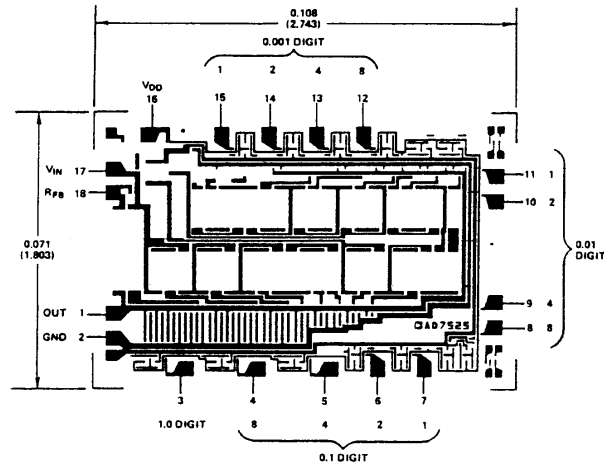
18-PIN CERAMIC DIP



18-PIN PLASTIC DIP



BONDING DIAGRAM



- NOTES:
1. PAD NUMBERS CORRESPOND TO PIN NUMBERS SHOWN IN PIN CONFIGURATION.
2. PAD 2 (GND) SHOULD BE BONDED FIRST TO MINIMIZE ESD HAZARDS.
3. PADS ARE 0.004in x 0.004in (0.102mm x 0.102mm).

SEE ANALOG DEVICES CHIP CATALOG
FOR ADDITIONAL CHIP INFORMATION

C543d-5-5/84

PRINTED IN U.S.A.