# SIEMENS

5-V Low-Drop Voltage Regulator TLE 4263

Features

- Output voltage tolerance $\leq \pm 2 \%$
- Low-drop voltage
- Very low standby current consumption
- Overtemperature protection
- Reverse polarity protection
- Short-circuit proof
- Settable reset threshold
- Watchdog
- Wide temperature range
- Suitable for use in automotive electronics
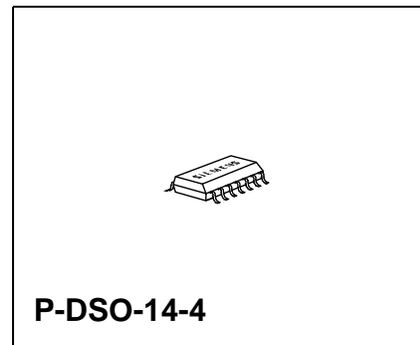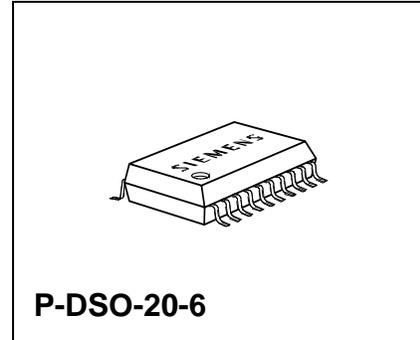
P-DSO-20-6

P-DSO-14-4

Type	Ordering Code	Package
TLE 4263 G	Q67006-A9095	P-DSO-20-6 (SMD)
▼ TLE 4263 GM	Q67006-A9357	P-DSO-14-4 (SMD)

▼ New type

Functional Description

TLE 4263 G is a 5-V low-drop voltage regulator in a P-DSO-20-6 SMD package. The maximum input voltage is 45 V. The maximum output current is more than 200 mA. The IC is short-circuit proof and incorporates temperature protection that disables the IC at overtemperature.

The IC regulates an input voltage V_I in the range of 6 V < V_I < 45 V to V_{Qrated} = 5.0 V. A reset signal is generated for an output voltage of V_Q < 4.5 V. This voltage threshold can be decreased to 3.5 V by external connection. The reset delay can be set externally by a capacitor. The integrated watchdog logic controls the connected microcontroller. The IC can be switched off via the inhibit input, which causes the current consumption to drop from 800 µA to < 50 µA.

## Dimensioning Information on External Components

The input capacitor C_I is necessary for compensating line influences. Using a resistor of approx. 1 Ω in series with C_I, the oscillating circuit consisting of input inductivity and input capacitance can be damped. The output capacitor is necessary for the stability of the regulating circuit. Stability is guaranteed at values $\geq 22\ \mu F$ and an ESR of $\leq 3\ \Omega$ within the operating temperature range. For small tolerances of the reset delay the spread of the capacitance of the delay capacitor and its temperature coefficient should be noted.

Pin Configuration
(top view)

TLE 4263 G

N.C.	1		20	INH
N.C.	2		19	N.C.
QRES	3		18	V_I
GND	4		17	GND
GND	5		16	GND
GND	6		15	GND
GND	7		14	GND
N.C.	8		13	N.C.
DRES	9		12	V_Q
SRES	10		11	W

AEP01099

TLE 4263 GM

N.C.	1	○	14	INH
QRES	2		13	V_I
GND	3		12	GND
GND	4		11	GND
GND	5		10	GND
DRES	6		9	V_Q
SRES	7		8	W

AEP02587
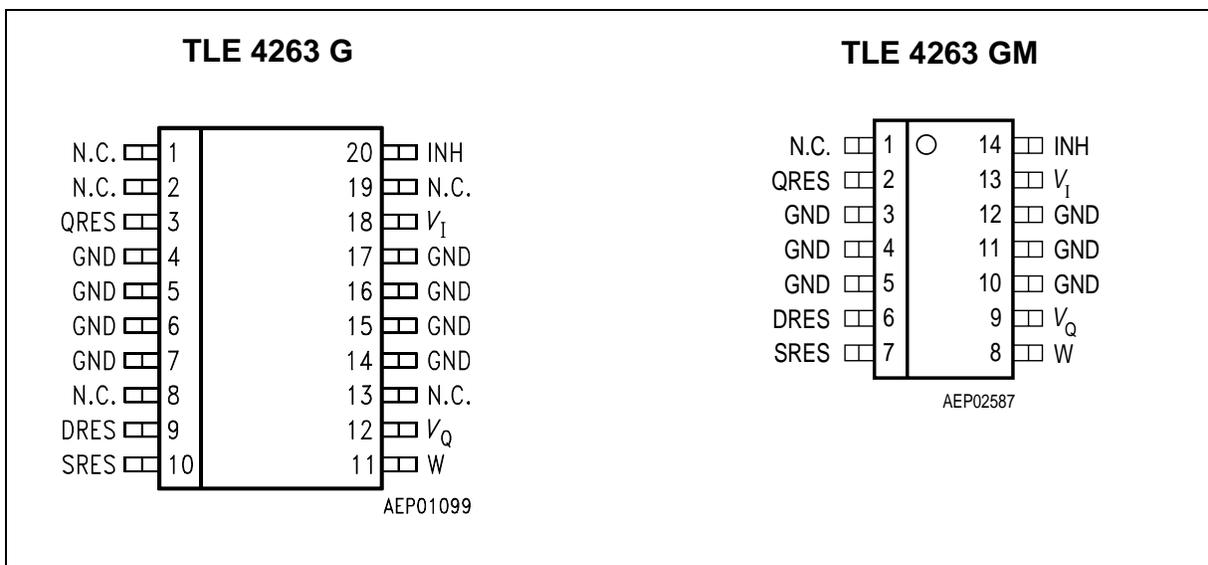
Pin Definitions and Functions

Pin	Symbol	Function
1, 2, 19, 13	N.C.	Not connected
3	QRES	**Reset output;** open-collector output connected to the output via a resistor of 30 kΩ.
4-7, 14-17	GND	**Ground**
9	DRES	**Reset delay;** connected to ground with a capacitor.
10	SRES	**Reset threshold;** for setting the switching threshold connect with a voltage divider from output to ground. If this input is connected to GND, reset is triggered at an output voltage of 4.5 V.
11	W	**Watchdog;** positive edge triggered input for monitoring a microcontroller.
12	V_Q	**5-V output voltage;** block to ground with a 22$-\mu$F capacitor.
18	V_I	**Input voltage;** block to ground directly at the IC with a ceramic capacitor.
20	INH	**Inhibit;** TTL-compatible, low-active input.

Circuit Description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element. If the externally scaled down output voltage at the reset threshold input drops below 1.35 V, the external reset delay capacitor is discharged by the reset generator. If the voltage on the capacitor reaches the lower threshold V_{ST}, a reset signal is issued on the reset output and not cancelled again until the upper threshold V_{dT} is exceeded. If the reset threshold input is connected to GND, reset is triggered at an output voltage of 4.5 V. A connected microcontroller is controlled by the watchdog logic. If pulses are missing, the reset output is set to low. The pulse sequence time can be set within a wide range with the reset delay capacitor. The IC can be switched at the TTL-compatible, low-active inhibit input. The IC also incorporates a number of internal circuits for protection against:

● Overload
● Overtemperature
● Reverse polarity
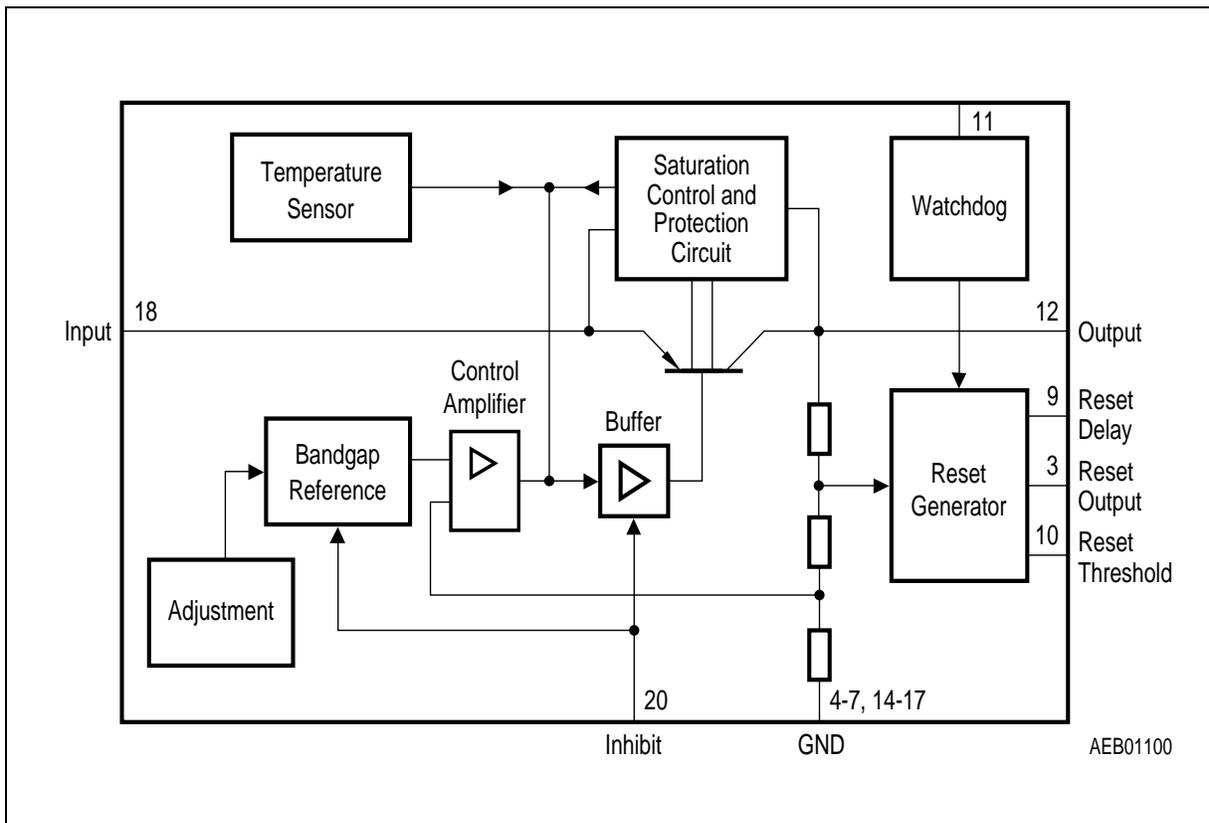
Block Diagram

Absolute Maximum Ratings

$T_j = - 40$ to $150\ °C$

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Input					
Input voltage	V_I	$- 42$	45	V	$-$
Input current	I_I	$-$	$-$	$-$	internally limited
Reset Output					
Voltage	V_R	$- 0.3$	42	V	$-$
Current	I_R	$-$	$-$	$-$	internally limited
Reset Input					
Reset threshold	V_{RE}	$- 0.3$	6	V	$-$
Reset Delay					
Voltage	V_d	$- 0.3$	42	V	$-$
Current	I_d	$-$	$-$	$-$	internally limited
Output					
Voltage	V_Q	$- 0.3$	7	V	$-$
Current	I_Q	$-$	$-$	$-$	internally limited
Inhibit					
Voltage	V_e	$- 42$	45	V	$-$
Watchdog					
Voltage	V_W	$- 0.3$	6	V	$-$
Ground					
Current	I_{GND}	$- 0.5$	$-$	A	$-$

Absolute Maximum Ratings (cont'd)

T_j = − 40 to 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Temperature					
Junction temperature	T_j	–	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–
Operating Range					
Input voltage	V_I	–	45	V	–
Junction temperature	T_j	– 40	150	°C	–
Thermal resistance junction-ambient junction-case	$R_{th\ JA}$ $R_{th\ JC}$	– –	70 25	K/W K/W	soldered –

Characteristics

V_I = 13.5 V; T_j = 25 °C; V_e > 3.5 V; (unless specified otherwise)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

Normal Operation

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
Output voltage	V_Q	4.90	5.00	5.10	V	5 mA $\leq I_Q \leq$ 150 mA; 6 V $\leq V_I \leq$ 28 V; − 40 °C $\leq T_j \leq$ 125 °C
Output voltage	V_Q	4.95	5.00	5.05	V	6 V $\leq V_I \leq$ 32 V; I_Q = 100 mA; T_j = 100 °C
Output current	I_Q	200	250	–	mA	–
Current consumption; $I_q = I_i - I_Q$	I_q	–	–	50	µA	V_e = 0
	I_q	–	800	1100	µA	I_Q = 0 mA
	I_q	–	10	15	mA	I_Q = 150 mA
	I_q	–	15	20	mA	I_Q = 150 mA; V_i = 4.5 V
Drop voltage	V_{Dr}	–	0.35	0.6	V	I_Q = 150 mA [*)]
Load regulation	ΔV_Q	–	–	25	mV	I_Q = 5 mA to 150 mA
Supply-voltage regulation	ΔV_Q	–	15	25	mV	V_I = 6 V to 28 V; I_Q = 150 mA
Ripple rejection	SVR	–	54	–	dB	f_r = 100 Hz; V_r = 0.5 Vpp

Reset Generator

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
Switching threshold	V_{RT}	4.2	4.5	4.8	V	V_{RE} = 0 V
Switching voltage	V_{RE}	1.28	1.35	1.42	V	V_Q > 3.5 V
Reset low voltage	V_R	–	0.10	0.40	V	I_R = 1 mA

Note: The reset output is low within the range V_Q = 1 V to V_{RT}

[*)] Drop voltage = $V_i - V_Q$ (measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input)

Characteristics (cont'd)

$V_I = 13.5$ V; $T_j = 25$ °C; $V_e > 3.5$ V; (unless specified otherwise)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Saturation voltage	V_C	–	50	100	mV	$V_Q < V_{RT}$
Delay switching threshold	V_{dT}	1.5	1.7	2.1	V	–
Switching threshold	V_{ST}	0.2	0.35	0.55	V	–
Charge current	I_d	40	60	80	µA	–
Delay time	t_d	–	2.8	–	ms	$C_d = 100$ nF
Delay time	t_t	–	2	–	µs	$C_d = 100$ nF

Watchdog

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Discharge current	I_{Cd}	4.4	6.25	8.2	µA	$V_C = 1.5$ V
Switching voltage	V_{Cd}	1.5	1.7	2.1	V	–
Pulse time	T_W	–	22.5	–	ms	$C_d = 100$ nF

Inhibit

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Switching voltage	$V_{e\,ON}$	3.5	–	–	V	IC turned on
Turn-OFF voltage	$V_{e\,OFF}$	–	–	0.8	V	IC turned off
Input current	I_e	5	10	15	µA	$V_e = 5$ V

Note: The reset output is low within the range $V_Q = 1$ V to V_{RT}

Application Circuit

$V_{Dr} = V_I - V_Q$ *)

$SVR = 20 \log \dfrac{V_r}{\Delta V_Q}$

*) Outside Control Range

AES01101

Test Circuit

AET01085
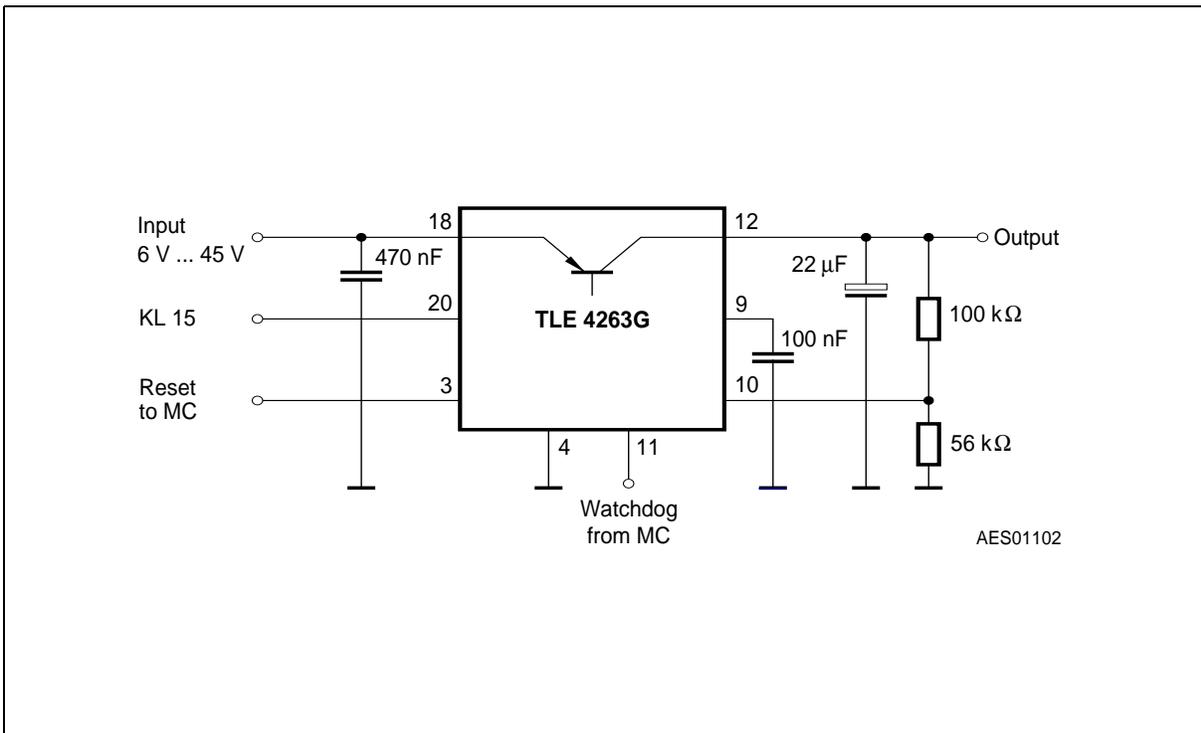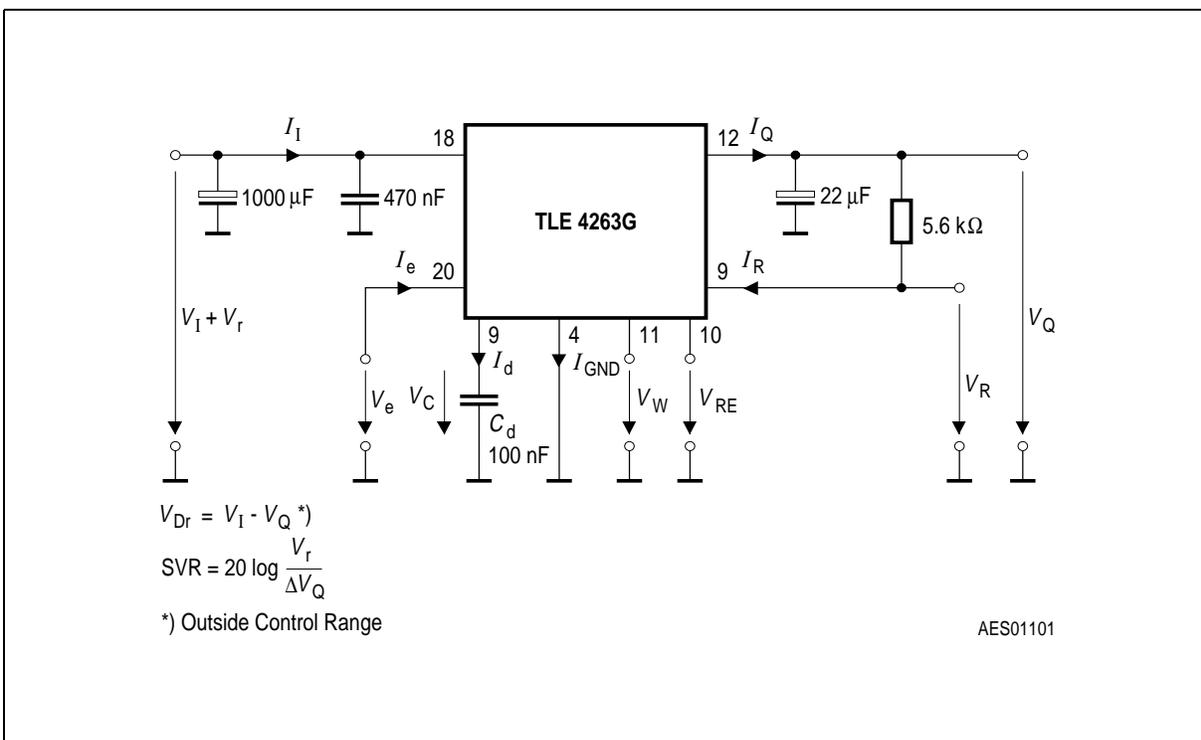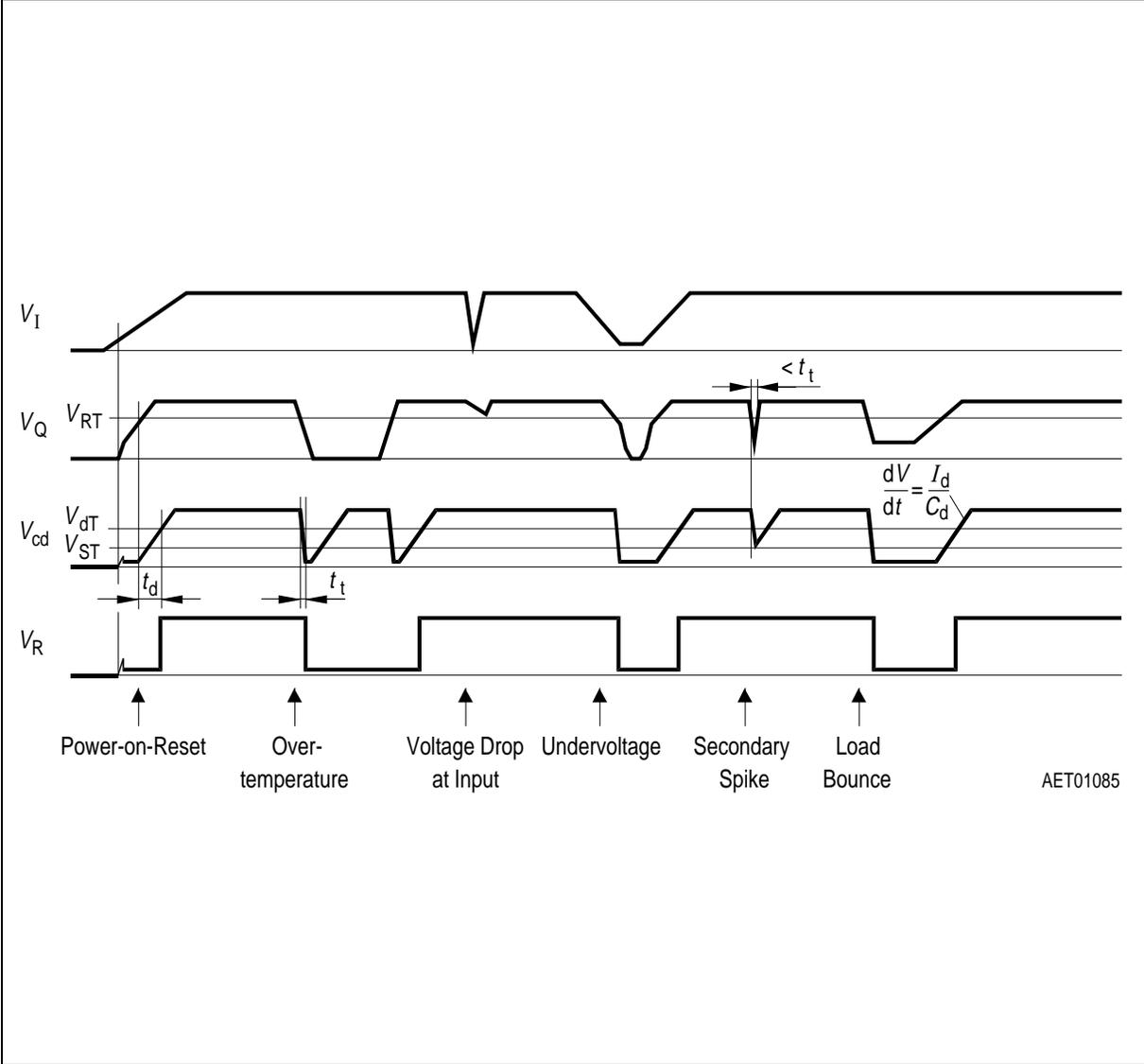
Time Response, Watchdog with High-Frequency Clock

Reset Threshold versus Output Voltage

AED01098

$V_I = 13.5$ V

V_{RE} / V vs V_Q / V
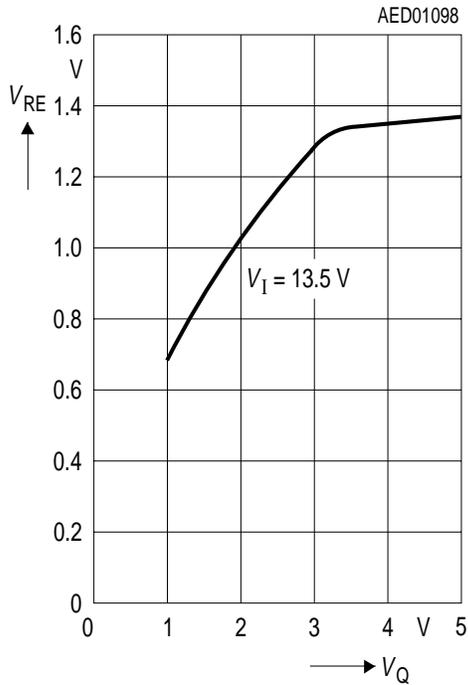
Switching Voltage V_{Cd}, V_{dT} and V_{ST} versus Temperature

AED01087

$V_I = 13.5$ V

V_{dT}, V_{cd}

V_{ST}

V / V vs T_j / °C
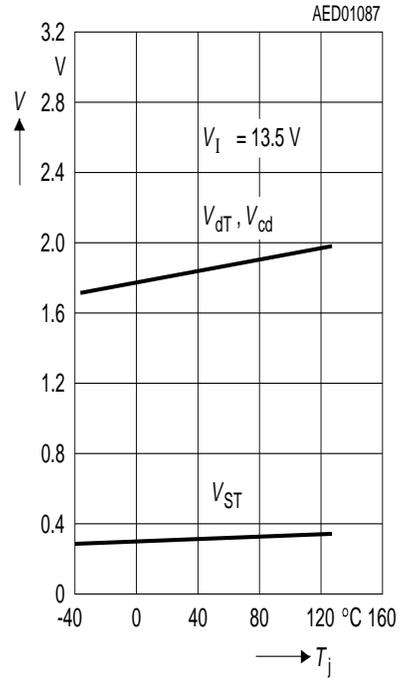
Reset Switching Threshold versus Temperature

AED01088

V_{RE} / V vs T_j / °C
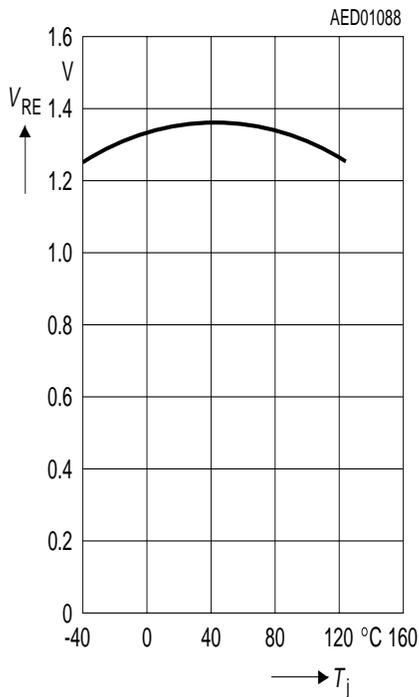
Current Consumption of Inhibit versus Temperature

AED01089

$V_e = 5$ V

I_e / µA vs T_j / °C
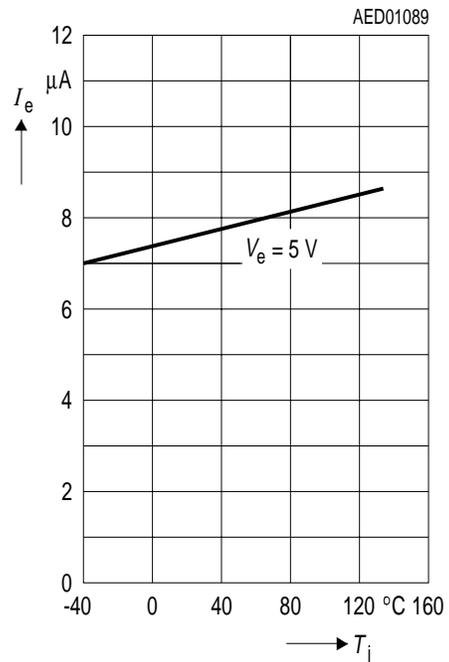
Drop Voltage versus OutputCurrent

AED01094

V_{Dr} (mV) versus I_Q (mA)

$T_j = 125\,^\circ C$
$25\,^\circ C$
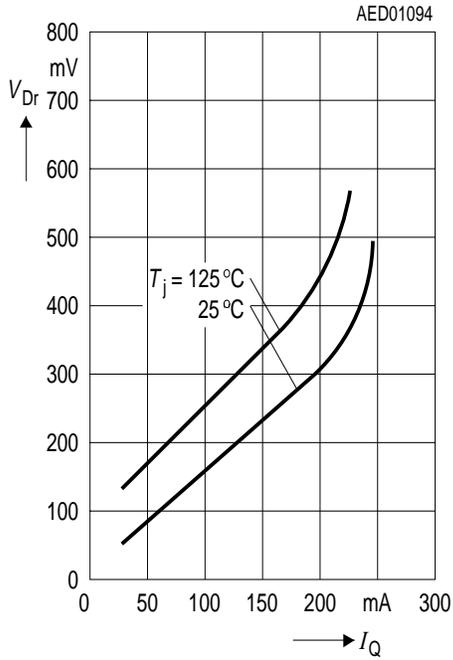
Current Consumption versus Output Current

AED01095

I_q (mA) versus I_Q (mA)

$V_I = 13.5\ V$
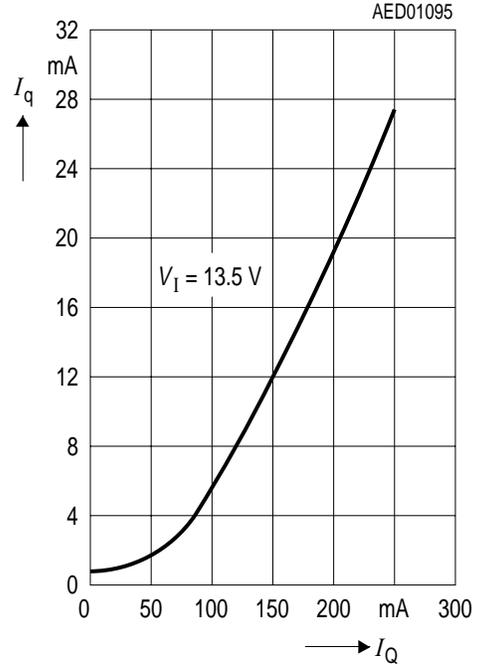
Current Consumption versus Input Voltage

AED01096

I_q (mA) versus V_I (V)

$R_L = 25\ \Omega$
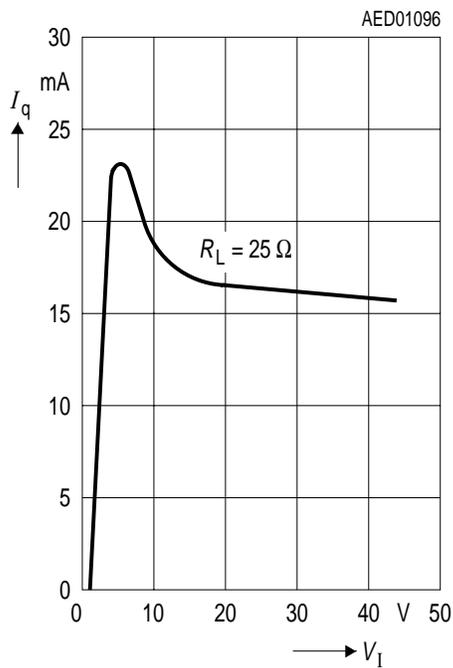
Output Voltage versus Input Voltage

AED01097

V_Q (V) versus V_I (V)

$R_L = 25\ \Omega$
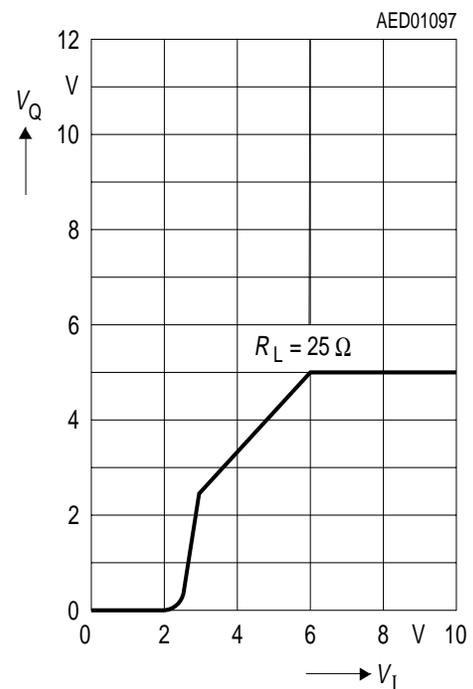
Charge Current and Discharge Current versus Temperature

AED01104

I_d

$V_I = 13.5$ V
$V_C = 1.5$ V

I_{Cd}

I / µA vs T_j / °C
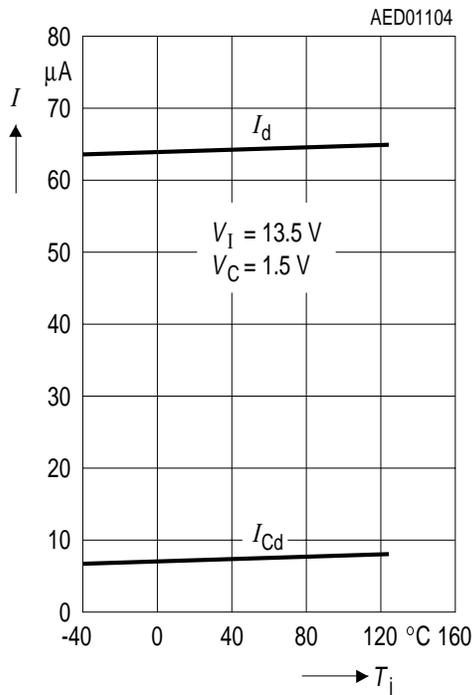
Output Voltage versus Temperature

AED01090

$V_e = 13.5$ V

V_Q / V vs T_j / °C
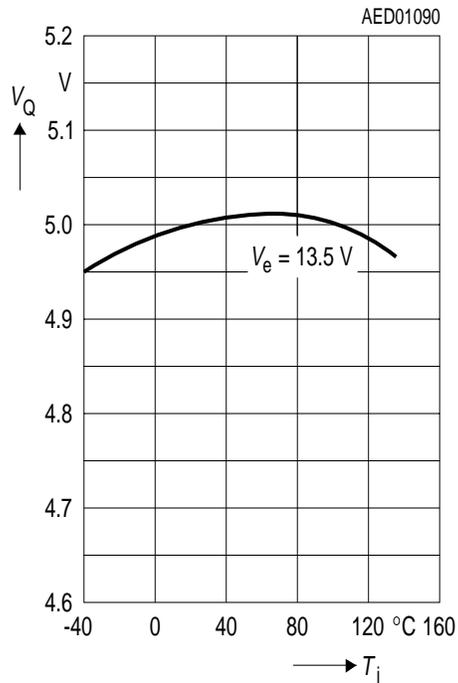
Pulse Time versus Temperature

AED01106

$V_I = 13.5$ V
$C_d = 100$ nF

T_W / ms vs T_j / °C

Input Response

AED01092

$t_r = t_f \simeq 1$ µs

ΔV_I / V

$C_Q = 22$ µF

ΔV_Q / mV vs t / µs
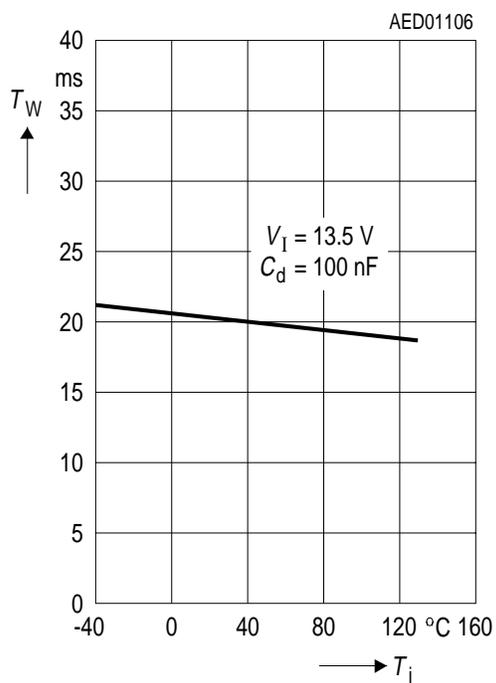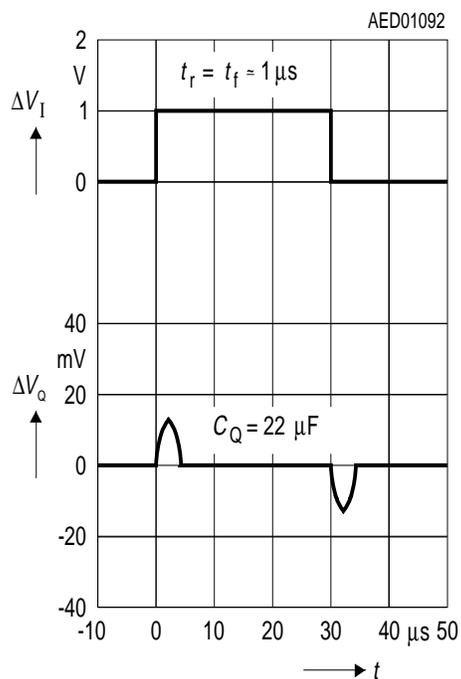
Output Current versus Input Voltage

Load Response

AED01091

$T_j = 25 \,^\circ C$

I_Q mA

300
250
200
150
100
50
0

0   10   20   30   40   V   50

V_I

AED01093

ΔI_Q mA

295
150
5

ΔV_Q mV

200
100
0
-100
-200

$C_Q = 22 \, \mu F$

-10   0   10   20   30   40 µs   50

t
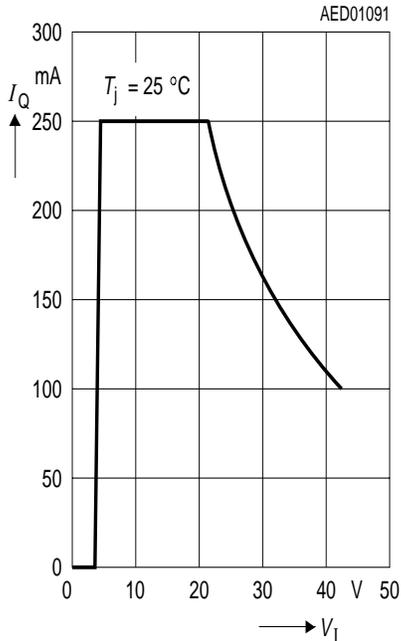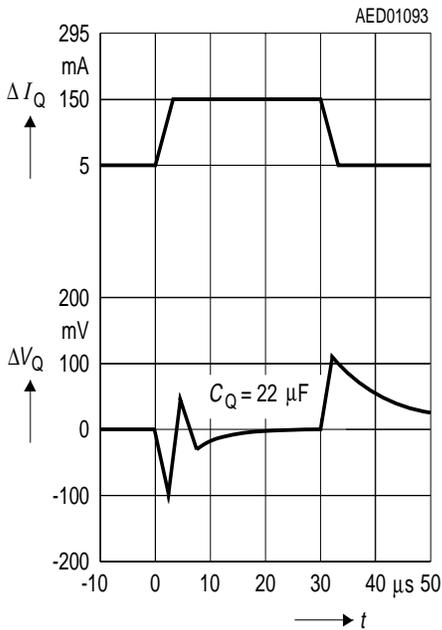
Package Outlines

P-DSO-20-6
(Plastic Dual Small Outline)

$0.2_{-0.1}$
$2.45_{-0.2}$
2.65 max
0.35 x 45°
$7.6_{-0.2}$ 1)
$0.23_{+0.09}$
8° max
1.27
$0.4^{+0.8}$
$0.35^{+0.15 2)}$
$\oplus$ 0.2 24x
0.1
$10.3^{\pm0.3}$

20   11

GPS05094

1    $12.8_{-0.2}$ 1)   10
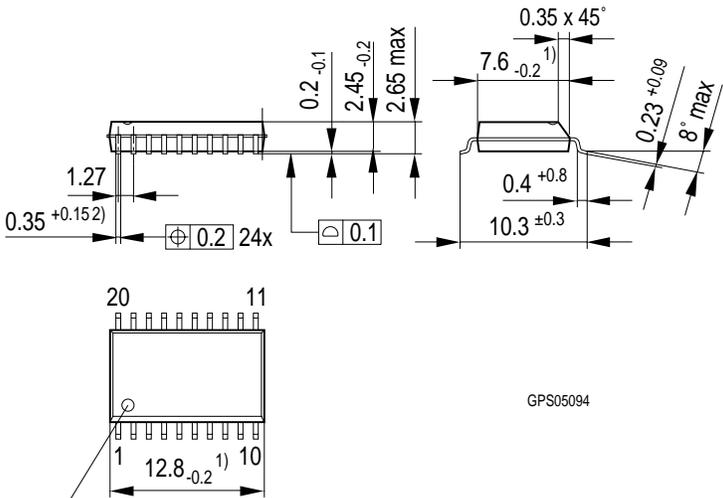
Index Marking

1) Does not include plastic or metal protrusions of 0.15 max per side
2) Does not include dambar protrusion of 0.05 max per side

Weight approx. 0.6 g

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our
Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

P-DSO-14-1

(Plastic Dual Small Outline)
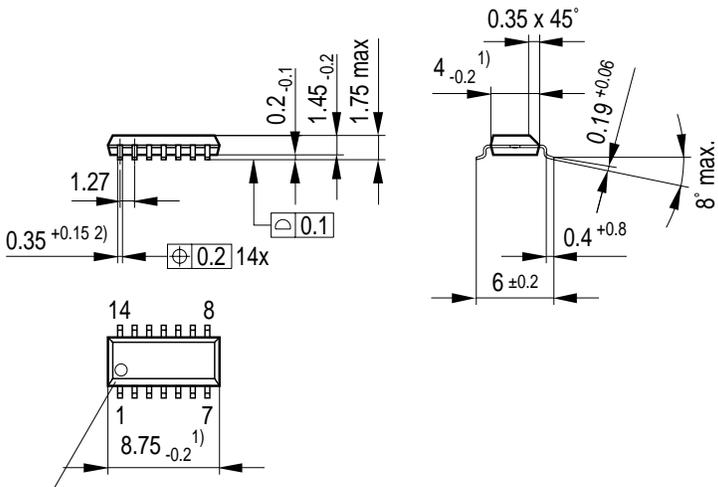
Index Marking

1) Does not include plastic or metal protrusion of 0.15 max. per side

2) Does not include dambar protrusion of 0.05 max. per side   GPS05093

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Dimensions in mm