

# SIEMENS

## Microcomputer Components

8-Bit CMOS Microcontroller

# C515A

Data Sheet 10.97

<b>C515A Data Sheet</b>		
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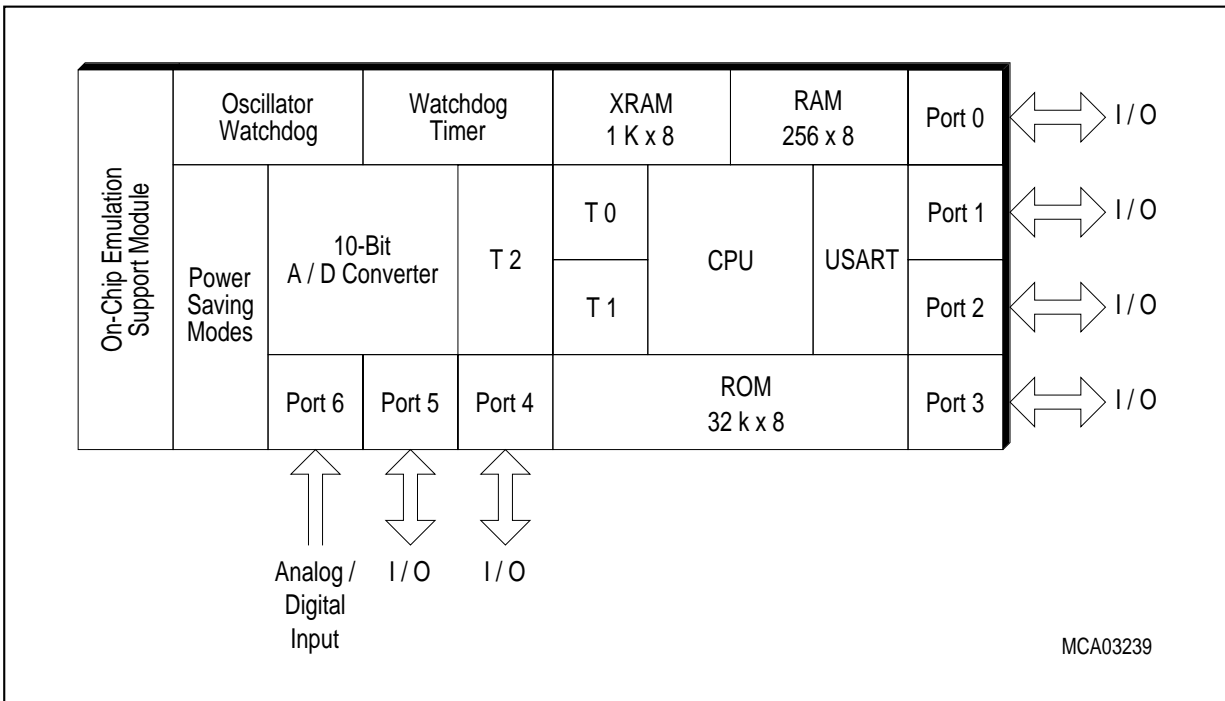
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### Advance Information

- Full upward compatibility with SAB 80C515A/83C515A-5
- Up to 24 MHz external operating frequency
  - 500 ns instruction cycle at 24 MHz operation
- 32K byte on-chip ROM (with optional ROM protection)
  - alternatively up to 64K byte external program memory
- Up to 64K byte external data memory
- 256 byte on-chip RAM
- 1K byte on-chip RAM (XRAM)
- Six 8-bit parallel I/O ports
- One input port for analog/digital input
- Full duplex serial interface (USART)
  - 4 operating modes, fixed or variable baud rates
- Three 16-bit timer/counters
  - Timer 0 / 1 (C501 compatible)
  - Timer 2 for 16-bit reload, compare, or capture functions

(further features are on next page)



**Figure 1**  
**C515A Functional Units**

### Features (cont'd):

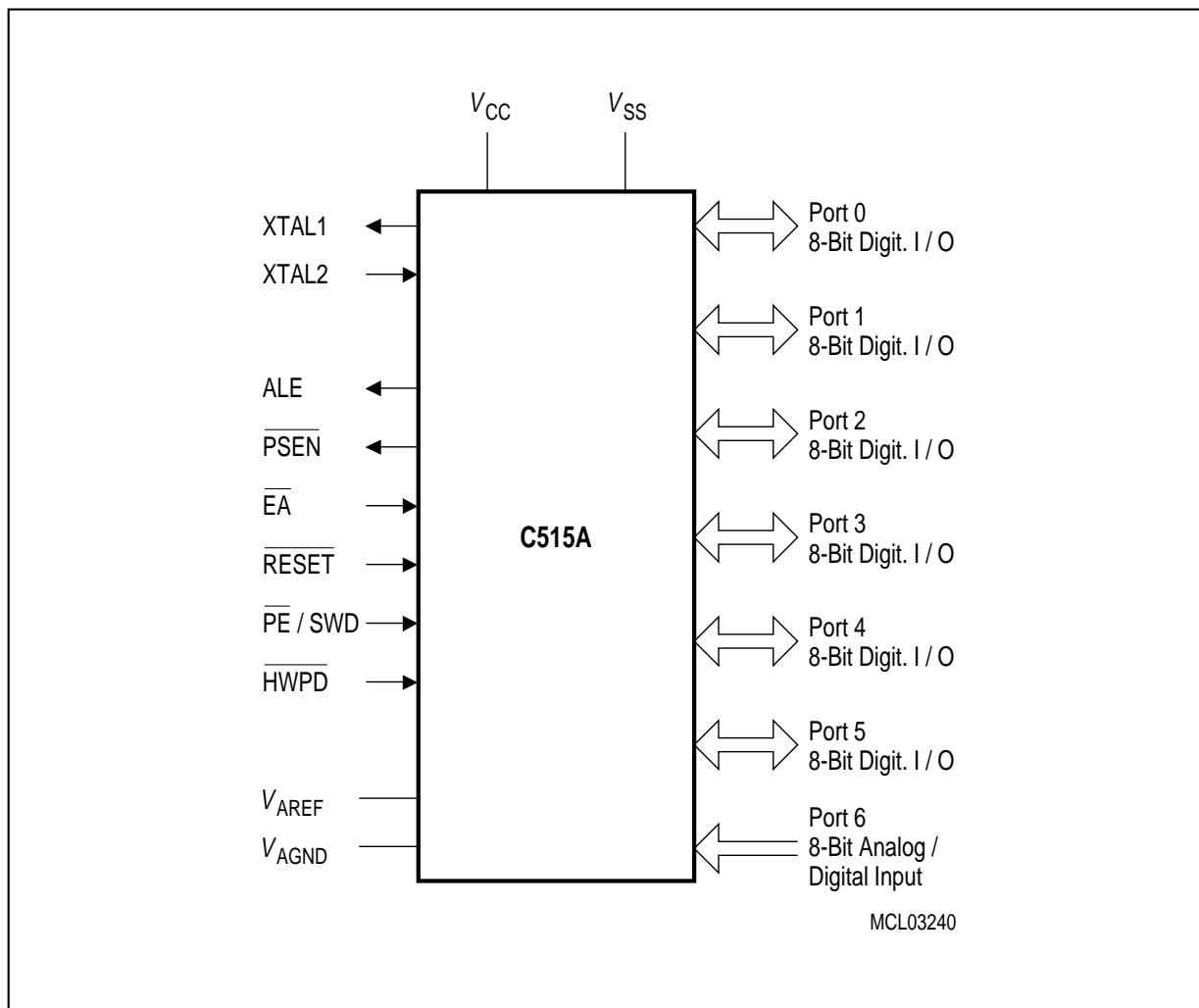
- 10-bit A/D converter
  - 8 multiplexed analog inputs
  - Built-in self calibration
- 16-bit watchdog timer
- Power saving modes
  - Slow down mode
  - Idle mode (can be combined with slow down mode)
  - Software power down mode with wake-up capability through  $\overline{\text{INT0}}$  pin
  - Hardware power down mode
- 12 interrupt sources (7 external, 5 internal) selectable at 4 priority levels
- ALE switch-off capability
- On-chip emulation support logic (Enhanced Hooks Technology™)
- P-MQFP-80-1 package
- Temperature Ranges:
  - SAB-C515A  $T_A = 0$  to  $70\text{ }^\circ\text{C}$
  - SAF-C515A  $T_A = -40$  to  $85\text{ }^\circ\text{C}$
  - SAH-C515A  $T_A = -40$  to  $85\text{ }^\circ\text{C}$
  - SAK-C515  $T_A = -40$  to  $110\text{ }^\circ\text{C}$  (max. operating frequency: 18 MHz)

The C515A is an upward compatible version of the SAB 80C515A/83C515A-5 8-bit microcontroller which additionally provides an improved 10-bit A/D converter, ALE switch-off capability, on-chip emulation support, ROM protection, and enhanced power saving mode capabilities. With a maximum external clock rate of 24 MHz it achieves a 500 ns instruction cycle time (1  $\mu\text{s}$  at 12 MHz). The C515A is mounted in a P-MQFP-80 package.

### Ordering Information

Type	Ordering Code	Package	Description (8-Bit CMOS microcontroller)
SAB-C515A-4RM	Q67121-DXXXX	P-MQFP-80-1	with mask programmable ROM (18 MHz)
SAF-C515A-4RM	Q67121-DXXXX	P-MQFP-80-1	with mask programmable ROM (18 MHz) ext. temp. $-40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$
SAB-C515A-4R24M	Q67121-DXXXX	P-MQFP-80-1	with mask programmable ROM (24 MHz)
SAF-C515A-4R24M	Q67121-DXXXX	P-MQFP-80-1	with mask programmable ROM (24 MHz) ext. temp. $-40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$
SAB-C515A-LM	Q67121-C1068	P-MQFP-80-1	for external memory (18 MHz)
SAF-C515A-LM	Q67121-C1069	P-MQFP-80-1	for external memory (18 MHz) ext. temp. $-40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$
SAB-C515A-L24M	Q67121-C1070	P-MQFP-80-1	for external memory (24 MHz)
SAF-C515A-L24M	Q67127-C2020	P-MQFP-80-1	for external memory (24 MHz) ext. temp. $-40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$

**Note:** Versions for extended temperature ranges  $-40\text{ }^\circ\text{C}$  to  $110\text{ }^\circ\text{C}$  and  $-40\text{ }^\circ\text{C}$  to  $125\text{ }^\circ\text{C}$  (SAH-C515A and SAK-C515A) are available on request. The ordering number of ROM types (DXXXX extensions) is defined after program release (verification) of the customer.

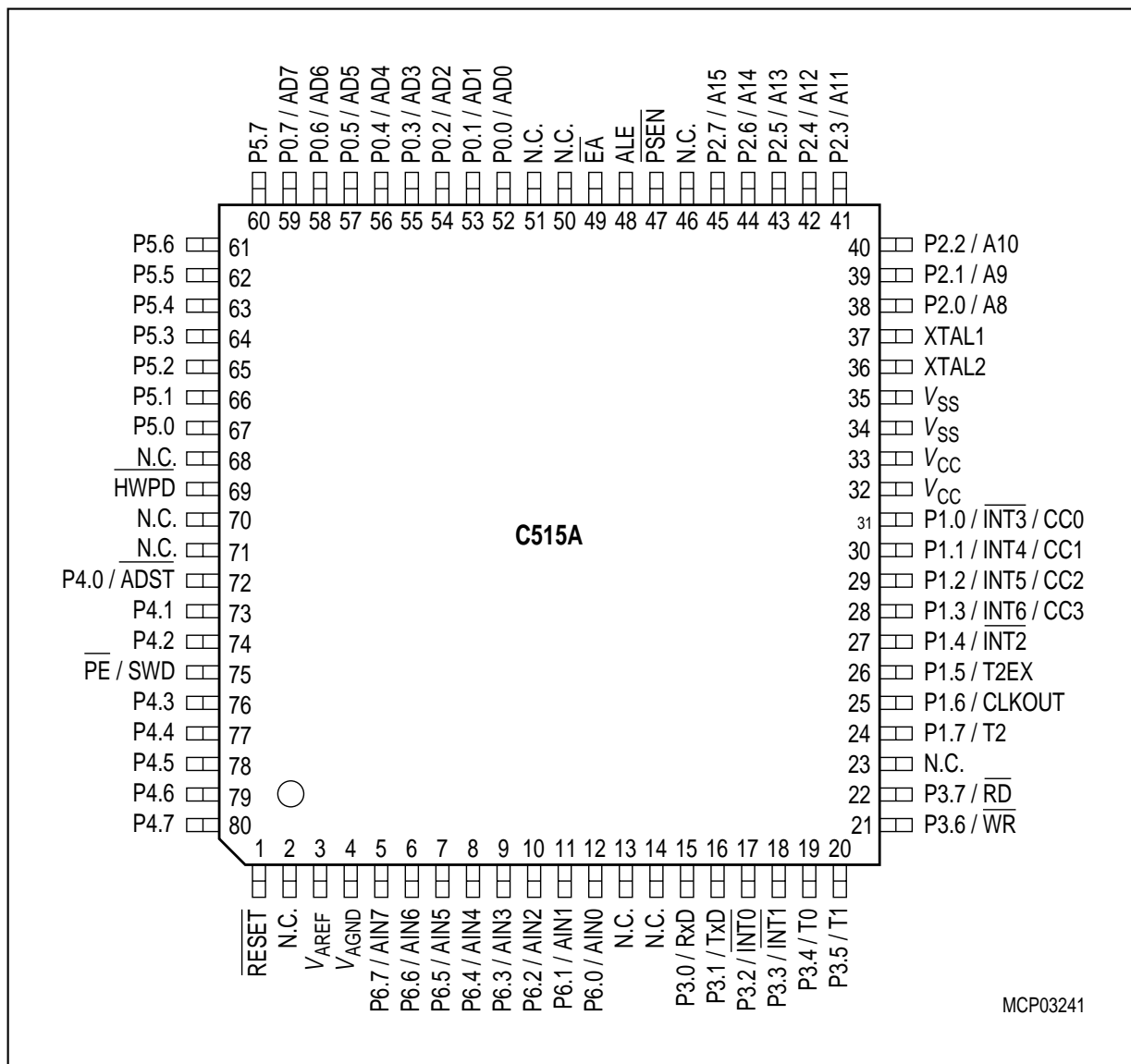


**Figure 2**  
**Logic Symbol**

**Additional Literature**

For further information about the C515A the following literature is available:

Title	Ordering Number
C515A 8-Bit CMOS Microcontroller User's Manual	B158-H7051-X-X-7600
C500 Microcontroller Family Architecture and Instruction Set User's Manual	B158-H6987-X-X-7600
C500 Microcontroller Family - Pocket Guide	B158-H6986-X-X-7600



**Figure 3**  
**Pin Configuration P-MQFP-80 Package (top view)**

**Table 1**  
**Pin Definitions and Functions**

Symbol	Pin Number (P-MQFP-80)	I/O*	Function
P4.0-P4.7	72-74, 76-80  72	I/O	<p><b>Port 4</b> is an 8-bit quasi-bidirectional I/O port with internal pull-up resistors. Port 4 pins that have 1's written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (<math>I_{IL}</math>, in the DC characteristics) because of the internal pull-up resistors. P4 also contains the external A/D converter control pin. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary function is assigned to port 6 as follows:</p> <p>P4.0 / <math>\overline{ADST}</math> external A/D converter start pin</p>
$\overline{PE}/SWD$	75	I	<p><b>Power Saving Mode Enable / Start Watchdog Timer</b> A low level on this pin allows the software to enter the power down, idle, and slow down mode. In case the low level is also seen during reset, the watchdog timer function is off on default. Use of the software controlled power saving modes is blocked when this pin is held on high level. A high level during reset performs an automatic start of the watchdog timer immediately after reset. When left unconnected this pin is pulled high by a weak internal pull-up resistor. <i>Note: If <math>\overline{PE}/SWD</math> is low and <math>V_{AREF}</math> is low the oscillator watchdog is disabled (testmode)!</i></p>
$\overline{RESET}$	1	I	<p><b><math>\overline{RESET}</math></b> A low level on this pin for the duration of two machine cycles while the oscillator is running resets the C515A. A small internal pullup resistor permits power-on reset using only a capacitor connected to <math>V_{SS}</math>.</p>
VAREF	3	–	<b>Reference Voltage</b> for the A/D converter
VAGND	4	–	<b>Reference Ground</b> for the A/D converter
P6.0-P6.7	12-5	I	<p><b>Port 6</b> is an 8-bit unidirectional input port to the A/D converter. Port pins can be used for digital input, if voltage levels simultaneously meet the specifications for high/low input voltages and for the eight multiplexed analog inputs.</p>

\*) I = Input  
O = Output

**Table 1**  
**Pin Definitions and Functions (cont'd)**

Symbol	Pin Number (P-MQFP-80)	I/O*	Function
P3.0-P3.7	15-22	I/O	<p><b>Port 3</b> is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 3 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (<math>I_{IL}</math>, in the DC characteristics) because of the internal pullup resistors. Port 3 also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows:</p>
	15		P3.0 / RxD Receiver data input (asynch.) or data input/output (synch.) of serial interface
	16		P3.1 / TxD Transmitter data output (asynch.) or clock output (synch.) of serial interface
	17		P3.2 / $\overline{INT0}$ External interrupt 0 input / timer 0 gate control input
	18		P3.3 / $\overline{INT1}$ External interrupt 1 input / timer 1 gate control input
	19		P3.4 / T0 Timer 0 counter input
	20		P3.5 / T1 Timer 1 counter input
	21		P3.6 / $\overline{WR}$ $\overline{WR}$ control output; latches the data byte from port 0 into the external data memory
	22		P3.7 / $\overline{RD}$ $\overline{RD}$ control output; enables the external data memory

\*) I = Input  
O = Output



**Table 1**  
**Pin Definitions and Functions (cont'd)**

Symbol	Pin Number (P-MQFP-80)	I/O*	Function
P1.0 - P1.7	31-24	I/O	<p><b>Port 1</b> is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (<math>I_{IL}</math>, in the DC characteristics) because of the internal pullup resistors. The port is used for the low-order address byte during program verification. Port 1 also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the port 1 pins as follows:</p> <p>31 P1.0 / <math>\overline{INT3}</math> / CC0 Interrupt 3 input / compare 0 output / capture 0 input</p> <p>30 P1.1 / INT4 / CC1 Interrupt 4 input / compare 1 output / capture 1 input</p> <p>29 P1.2 / INT5 / CC2 Interrupt 5 input / compare 2 output / capture 2 input</p> <p>28 P1.3 / INT6 / CC3 Interrupt 6 input / compare 3 output / capture 3 input</p> <p>27 P1.4 / <math>\overline{INT2}</math> Interrupt 2 input</p> <p>26 P1.5 / T2EX Timer 2 external reload / trigger input</p> <p>25 P1.6 / CLKOUT System clock output</p> <p>24 P1.7 / T2 Counter 2 input</p>
V <sub>CC</sub>	32, 33	–	<b>Supply Voltage</b> during normal, idle, and power down mode.
V <sub>SS</sub>	34, 35	–	<b>Ground (0V)</b> during normal, idle, and power down operation.

\*) I = Input  
O = Output

**Table 1**  
**Pin Definitions and Functions (cont'd)**

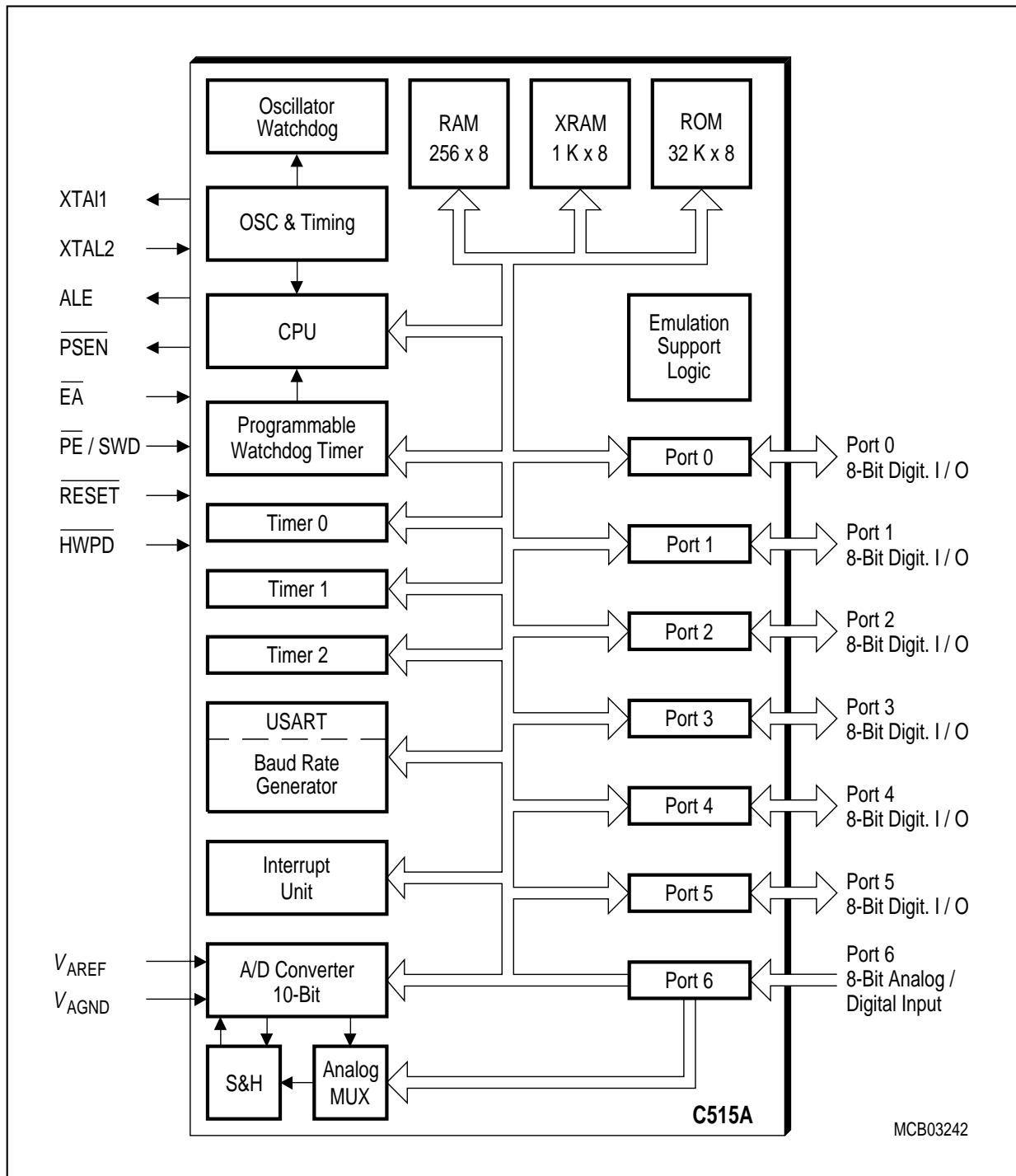
Symbol	Pin Number (P-MQFP-80)	I/O*	Function
XTAL2	36	–	<b>XTAL2</b> Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is left unconnected. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics must be observed.
XTAL1	37	–	<b>XTAL1</b> Output of the inverting oscillator amplifier.
P2.0-P2.7	38-45	I/O	<b>Port 2</b> is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current ( $I_{IL}$ , in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullup resistors when issuing 1's. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.
$\overline{\text{PSEN}}$	47	O	The <b>Program Store Enable</b> output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. The signal remains high during internal program execution.
ALE	48	O	The <b>Address Latch Enable</b> output is used for latching the address into external memory during normal operation. It is activated every six oscillator periods, except during an external data memory access. ALE can be switched off when the program is executed internally.

\*) I = Input  
O = Output

**Table 1**  
**Pin Definitions and Functions (cont'd)**

Symbol	Pin Number (P-MQFP-80)	I/O*	Function
$\overline{EA}$	49	I	<b>External Access Enable</b> When held high, the C515A executes instructions from the internal ROM (C515A-4R) as long as the PC is less than 8000 <sub>H</sub> . When held low, the C515A fetches all instructions from external program memory. For the C515A-L this pin must be tied low.
P0.0-P0.7	52-59	I/O	<b>Port 0</b> is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1's. Port 0 also outputs the code bytes during program verification in the C515A-4R. External pullup resistors are required during program verification.
P5.0-P5.7	67-60	I/O	<b>Port 5</b> is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 5 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 5 pins being externally pulled low will source current ( $I_{IL}$ , in the DC characteristics) because of the internal pullup resistors.
$\overline{HWPD}$	69	I	<b>Hardware Power Down</b> A low level on this pin for the duration of one machine cycle while the oscillator is running resets the C515A. A low level for a longer period will force the C515A into Hardware Power Down Mode with the pins floating.
N.C.	2, 13, 14, 23, 46, 50, 51, 68, 70, 71	–	<b>Not connected</b> These pins of the P-MQFP-80 package need not be connected.

\*) I = Input  
O = Output



**Figure 4**  
**Block Diagram of the C515A**

## CPU

The C515A is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44 % one-byte, 41 % two-byte, and 15% three-byte instructions. With a 18 MHz crystal, 58% of the instructions are executed in 666 ns (24 MHz : 500 ns).

### Special Function Register PSW (Address D0<sub>H</sub>)

Reset Value : 00<sub>H</sub>

Bit No.	MSB							LSB	
	D7 <sub>H</sub>	D6 <sub>H</sub>	D5 <sub>H</sub>	D4 <sub>H</sub>	D3 <sub>H</sub>	D2 <sub>H</sub>	D1 <sub>H</sub>	D0 <sub>H</sub>	
D0 <sub>H</sub>	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

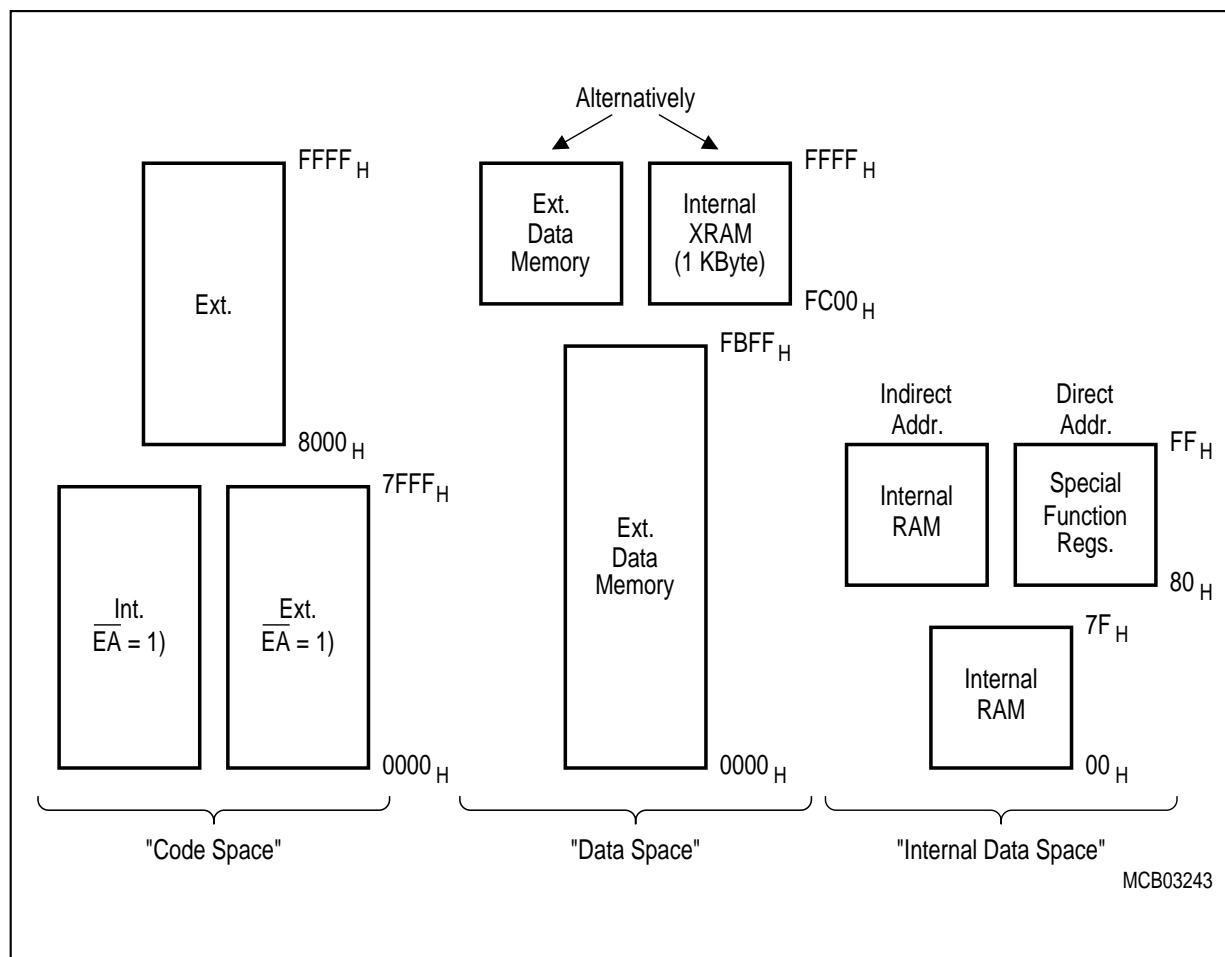
Bit	Function															
CY	Carry Flag Used by arithmetic instruction.															
AC	Auxiliary Carry Flag Used by instructions which execute BCD operations.															
F0	General Purpose Flag															
RS1 RS0	Register Bank select control bits These bits are used to select one of the four register banks.															
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">RS1</th> <th style="text-align: center;">RS0</th> <th style="text-align: left;">Function</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td>Bank 0 selected, data address 00<sub>H</sub>-07<sub>H</sub></td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td>Bank 1 selected, data address 08<sub>H</sub>-0F<sub>H</sub></td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td>Bank 2 selected, data address 10<sub>H</sub>-17<sub>H</sub></td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td>Bank 3 selected, data address 18<sub>H</sub>-1F<sub>H</sub></td> </tr> </tbody> </table>	RS1	RS0	Function	0	0	Bank 0 selected, data address 00 <sub>H</sub> -07 <sub>H</sub>	0	1	Bank 1 selected, data address 08 <sub>H</sub> -0F <sub>H</sub>	1	0	Bank 2 selected, data address 10 <sub>H</sub> -17 <sub>H</sub>	1	1	Bank 3 selected, data address 18 <sub>H</sub> -1F <sub>H</sub>
RS1	RS0	Function														
0	0	Bank 0 selected, data address 00 <sub>H</sub> -07 <sub>H</sub>														
0	1	Bank 1 selected, data address 08 <sub>H</sub> -0F <sub>H</sub>														
1	0	Bank 2 selected, data address 10 <sub>H</sub> -17 <sub>H</sub>														
1	1	Bank 3 selected, data address 18 <sub>H</sub> -1F <sub>H</sub>														
OV	Overflow Flag Used by arithmetic instruction.															
F1	General Purpose Flag															
P	Parity Flag Set/cleared by hardware after each instruction to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.															

**Memory Organization**

The C515A CPU manipulates operands in the following five address spaces:

- up to 64 Kbyte of program memory (32K on-chip program memory for C515A-4R)
- up to 64 Kbyte of external data memory
- 256 bytes of internal data memory
- 1K bytes of internal XRAM data memory
- a 128 byte special function register area

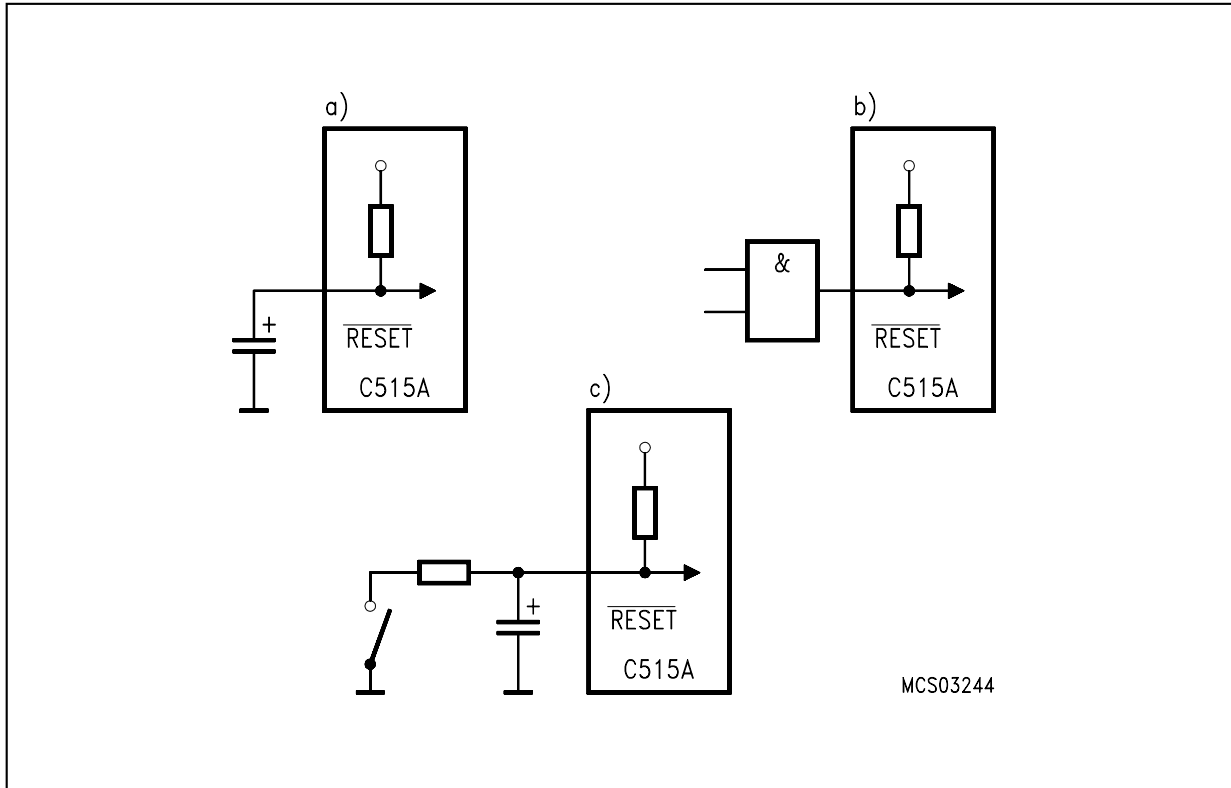
Figure 5 illustrates the memory address spaces of the C515A.



**Figure 5**  
**C515A Memory Map**

**Reset and System Clock**

The reset input is an active low input at pin  $\overline{\text{RESET}}$ . Since the reset is synchronized internally, the  $\overline{\text{RESET}}$  pin must be held low for at least two machine cycles (24 oscillator periods) while the oscillator is running. A pullup resistor is internally connected to  $V_{CC}$  to allow a power-up reset with an external capacitor only. An automatic reset can be obtained when  $V_{CC}$  is applied by connecting the  $\overline{\text{RESET}}$  pin to  $V_{SS}$  via a capacitor. **Figure 6** shows the possible reset circuitries.



**Figure 6**  
**Reset Circuitries**

Figure 7 shows the recommended oscillator circuitries for crystal and external clock operation.

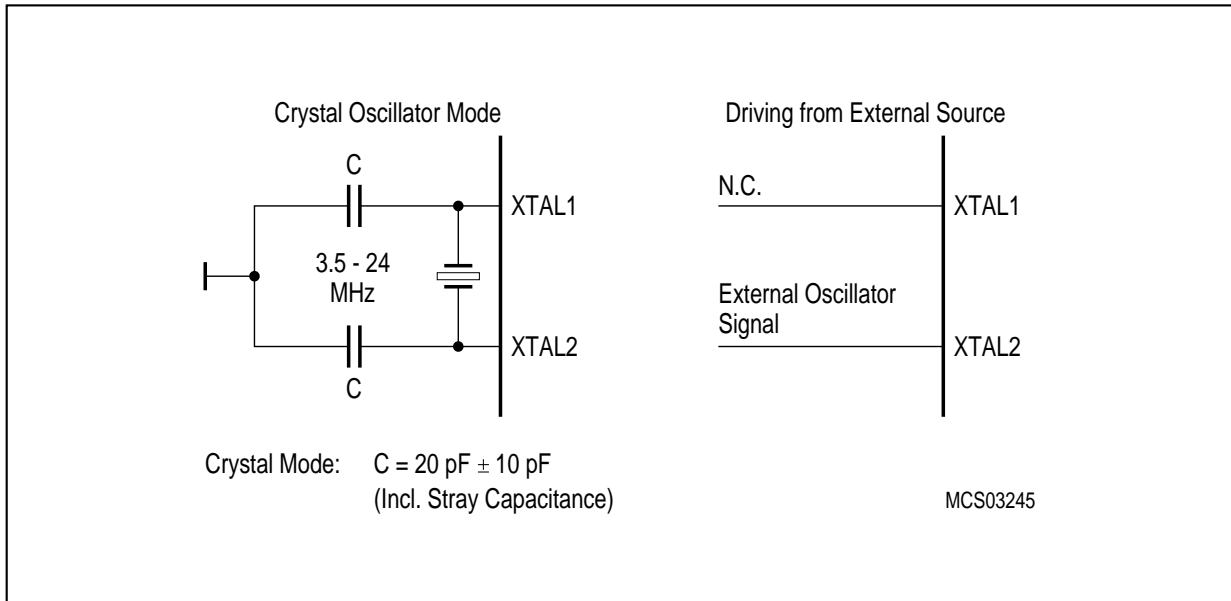


Figure 7  
Recommended Oscillator Circuitries

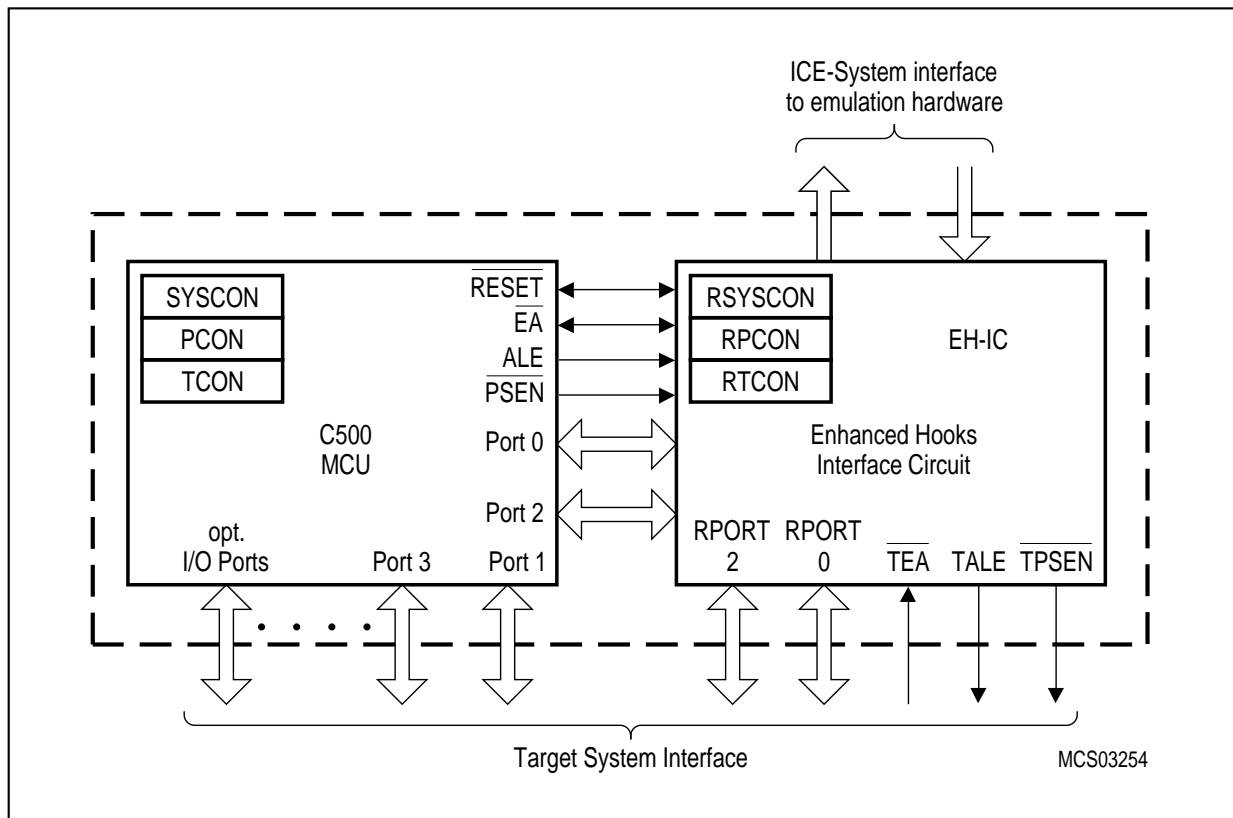


**Enhanced Hooks Emulation Concept**

The Enhanced Hooks Emulation Concept of the C500 microcontroller family is a new, innovative way to control the execution of C500 MCUs and to gain extensive information on the internal operation of the controllers. Emulation of on-chip ROM based programs is possible, too.

Each production chip has built-in logic for the support of the Enhanced Hooks Emulation Concept. Therefore, no costly bond-out chips are necessary for emulation. This also ensure that emulation and production chips are identical.

The Enhanced Hooks Technology<sup>TM 1)</sup>, which requires embedded logic in the C500 allows the C500 together with an EH-IC to function similar to a bond-out chip. This simplifies the design and reduces costs of an ICE-system. ICE-systems using an EH-IC and a compatible C500 are able to emulate all operating modes of the different versions of the C500 microcontrollers. This includes emulation of ROM, ROM with code rollover and ROMless modes of operation. It is also able to operate in single step mode and to read the SFRs after a break.



**Figure 8**  
**Basic C500 MCU Enhanced Hooks Concept Configuration**

Port 0, port 2 and some of the control lines of the C500 based MCU are used by Enhanced Hooks Emulation Concept to control the operation of the device during emulation and to transfer informations about the program execution and data transfer between the external emulation hardware (ICE-system) and the C500 MCU.

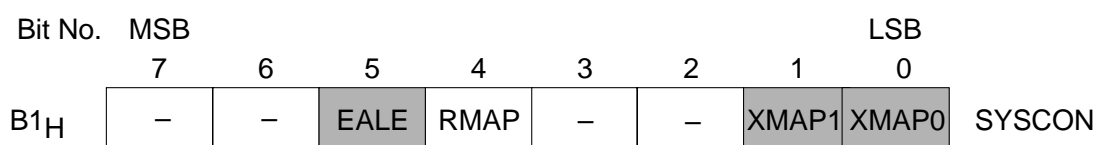
1 "Enhanced Hooks Technology" is a trademark and patent of Metalink Corporation licensed to Siemens.

**Special Function Registers**

The registers, except the program counter and the four general purpose register banks, reside in the special function register area. The special function register area consists of two portions: the standard special function register area and the mapped special function register area. One special function register of the C515A (PCON1) is located in the mapped special function register area. For accessing this mapped special function register, bit RMAP in special function register SYSCON must be set. All other special function registers are located in the standard special function register area which is accessed when RMAP is cleared (“0”).

**Special Function Register SYSCON (Address B1<sub>H</sub>)**

**Reset Value : XX10XX01<sub>B</sub>**



The functions of the shaded bits are not described in this section.

Bit	Function
RMAP	Special function register map bit RMAP = 0: The access to the non-mapped (standard) special function register area is enabled. RMAP = 1: The access to the mapped special function register area (SFR PCON1) is enabled.
-	Reserved bits for future use. Read by CPU returns undefined values.

As long as bit RMAP is set, the mapped special function register area (SFR PCON1) can be accessed. This bit is not cleared by hardware automatically. Thus, when non-mapped/mapped registers are to be accessed, the bit RMAP must be cleared/set respectively by software.

The 49 special function registers (SFRs) in the standard and mapped SFR area include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. All SFRs with addresses where address bits 0-2 are 0 (e.g. 80<sub>H</sub>, 88<sub>H</sub>, 90<sub>H</sub>, 98<sub>H</sub>, ..., F8<sub>H</sub>, FF<sub>H</sub>) are bitaddressable. The SFRs of the C515A are listed in **table 2** and **table 3**. In **table 2** they are organized in groups which refer to the functional blocks of the C515A. **Table 3** illustrates the contents of the SFRs in numeric order of their addresses.

**Table 2**  
**Special Function Registers - Functional Blocks**

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	<b>E0H</b> <sup>1)</sup>	00H
	B	B-Register	<b>F0H</b> <sup>1)</sup>	00H
	DPH	Data Pointer, High Byte	83H	00H
	DPL	Data Pointer, Low Byte	82H	00H
	PSW	Program Status Word Register	<b>D0H</b> <sup>1)</sup>	00H
	SP	Stack Pointer	81H	07H
	SYSCON <sup>2)</sup>	System/XRAM Control Register	B1H	XX10 XX01B <sup>3)</sup>
A/D- Converter	ADCON0 <sup>2)</sup>	A/D Converter Control Register 0	<b>D8H</b> <sup>1)</sup>	00H
	ADCON1	A/D Converter Control Register 1	DC <sub>H</sub>	0XXX X000B <sup>3)</sup>
	ADDATH	A/D Converter Data Register, High Byte	D9 <sub>H</sub>	00H
	ADDATL	A/D Converter Data Register, low Byte	DA <sub>H</sub> <sup>4)</sup>	00XX XXXXB <sup>3)</sup>
Interrupt System	IEN0 <sup>2)</sup>	Interrupt Enable Register 0	<b>A8H</b> <sup>1)</sup>	00H
	IEN1 <sup>2)</sup>	Interrupt Enable Register 1	<b>B8H</b> <sup>1)</sup>	00H
	IP0 <sup>2)</sup>	Interrupt Priority Register 0	A9 <sub>H</sub>	00H
	IP1 <sup>2)</sup>	Interrupt Priority Register 1	B9 <sub>H</sub>	XX00 0000B <sup>3)</sup>
	IRCON	Interrupt Request Control Register	<b>C0H</b> <sup>1)</sup>	00H
	TCON <sup>2)</sup>	Timer Control Register	<b>88H</b> <sup>1)</sup>	00H
	T2CON <sup>2)</sup>	Timer 2 Control Register	<b>C8H</b> <sup>1)</sup>	00H
	SCON <sup>2)</sup>	Serial Channel Control Register	<b>98H</b> <sup>1)</sup>	00H
Timer 0/ Timer 1	TCON <sup>2)</sup>	Timer 0/1 Control Register	<b>88H</b> <sup>1)</sup>	00H
	TH0	Timer 0, High Byte	8C <sub>H</sub>	00H
	TH1	Timer 1, High Byte	8D <sub>H</sub>	00H
	TL0	Timer 0, Low Byte	8A <sub>H</sub>	00H
	TL1	Timer 1, Low Byte	8B <sub>H</sub>	00H
	TMOD	Timer Mode Register	89 <sub>H</sub>	00H
Compare/ Capture Unit / Timer 2	CCEN	Comp./Capture Enable Reg.	C1 <sub>H</sub>	00H
	CCH1	Comp./Capture Reg. 1, High Byte	C3 <sub>H</sub>	00H
	CCH2	Comp./Capture Reg. 2, High Byte	C5 <sub>H</sub>	00H
	CCH3	Comp./Capture Reg. 3, High Byte	C7 <sub>H</sub>	00H
	CCL1	Comp./Capture Reg. 1, Low Byte	C2 <sub>H</sub>	00H
	CCL2	Comp./Capture Reg. 2, Low Byte	C4 <sub>H</sub>	00H
	CCL3	Comp./Capture Reg. 3, Low Byte	C6 <sub>H</sub>	00H
	CRCH	Com./Rel./Capt. Reg. High Byte	CB <sub>H</sub>	00H
	CRCL	Com./Rel./Capt. Reg. Low Byte	CA <sub>H</sub>	00H
	TH2	Timer 2, High Byte	CD <sub>H</sub>	00H
	TL2	Timer 2, Low Byte	CC <sub>H</sub>	00H
	T2CON <sup>2)</sup>	Timer 2 Control Register	<b>C8H</b> <sup>1)</sup>	00H

1) Bit-addressable special function registers

2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

3) "X" means that the value is undefined and the location is reserved

**Table 2**  
**Special Function Registers - Functional Blocks (cont'd)**

Block	Symbol	Name	Address	Contents after Reset
Ports	P0	Port 0	<b>80H</b> <sup>1)</sup>	FF <sub>H</sub>
	P1	Port 1	<b>90H</b> <sup>1)</sup>	FF <sub>H</sub>
	P2	Port 2	<b>A0H</b> <sup>1)</sup>	FF <sub>H</sub>
	P3	Port 3	<b>B0H</b> <sup>1)</sup>	FF <sub>H</sub>
	P4	Port 4	<b>E8H</b> <sup>1)</sup>	FF <sub>H</sub>
	P5	Port 5	<b>F8H</b> <sup>1)</sup>	FF <sub>H</sub>
	P6	Port 6, Analog/Digital Input	DB <sub>H</sub>	–
XRAM	XPAGE	Page Address Register for Extended On-Chip RAM	91 <sub>H</sub>	00 <sub>H</sub>
	SYSCON <sup>2)</sup>	System/XRAM Control Register	B1 <sub>H</sub>	XX10 XX01 <sub>B</sub> <sup>3)</sup>
Serial Channel	ADCON0 <sup>2)</sup>	A/D Converter Control Register	<b>D8H</b> <sup>1)</sup>	00 <sub>H</sub>
	PCON <sup>2)</sup>	Power Control Register	87 <sub>H</sub>	00 <sub>H</sub>
	SBUF	Serial Channel Buffer Register	99 <sub>H</sub>	XX <sub>H</sub> <sup>3)</sup>
	SCON <sup>2)</sup>	Serial Channel Control Register	<b>98H</b> <sup>1)</sup>	00 <sub>H</sub>
	SRELL	Serial Channel Reload Register, Low Byte	AA <sub>H</sub>	D9 <sub>H</sub>
	SRELH	Serial Channel Reload Register, High Byte	BA <sub>H</sub>	XXXX XX11 <sub>B</sub> <sup>3)</sup>
Watchdog	IEN0 <sup>2)</sup>	Interrupt Enable Register 0	<b>A8H</b> <sup>1)</sup>	00 <sub>H</sub>
	IEN1 <sup>2)</sup>	Interrupt Enable Register 1	<b>B8H</b> <sup>1)</sup>	00 <sub>H</sub>
	IP0 <sup>2)</sup>	Interrupt Priority Register 0	A9 <sub>H</sub>	00 <sub>H</sub>
	IP1 <sup>2)</sup>	Interrupt Priority Register 1	B9 <sub>H</sub>	XX00 0000 <sub>B</sub> <sup>3)</sup>
	WDTREL	Watchdog Timer Reload Register	86 <sub>H</sub>	00 <sub>H</sub>
Power Saving Modes	PCON <sup>2)</sup>	Power Control Register	87 <sub>H</sub>	00 <sub>H</sub>
	PCON1 <sup>4)</sup>	Power Control Register 1	88 <sub>H</sub>	0XXX XXXX <sub>B</sub> <sup>3)</sup>

1) Bit-addressable special function registers

2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

3) "X" means that the value is undefined and the location is reserved.

4) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

**Table 3**  
**Contents of the SFRs, SFRs in numeric order of their addresses**

Addr	Register	Content after Reset <sup>1)</sup>	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80 <sub>H</sub> <sup>2)</sup>	P0	FF <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
81 <sub>H</sub>	SP	07 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
82 <sub>H</sub>	DPL	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
83 <sub>H</sub>	DPH	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
86 <sub>H</sub>	WDTREL	00 <sub>H</sub>	WDT PSEL	.6	.5	.4	.3	.2	.1	.0
87 <sub>H</sub>	PCON	00 <sub>H</sub>	SMOD	PDS	IDLS	SD	GF1	GF0	PDE	IDLE
88 <sub>H</sub> <sup>2)</sup>	TCON	00 <sub>H</sub>	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
88 <sub>H</sub> <sup>3)</sup>	PCON1	0XXX- XXXX <sub>B</sub>	EWPD	–	–	–	–	–	–	–
89 <sub>H</sub>	TMOD	00 <sub>H</sub>	GATE	C $\bar{T}$	M1	M0	GATE	C $\bar{T}$	M1	M0
8A <sub>H</sub>	TL0	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
8B <sub>H</sub>	TL1	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
8C <sub>H</sub>	TH0	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
8D <sub>H</sub>	TH1	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
90 <sub>H</sub> <sup>2)</sup>	P1	FF <sub>H</sub>	T2	CLK- OUT	T2EX	$\bar{INT}2$	INT6	INT5	INT4	$\bar{INT}3$
91 <sub>H</sub>	XPAGE	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
98 <sub>H</sub> <sup>2)</sup>	SCON	00 <sub>H</sub>	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99 <sub>H</sub>	SBUF	XX <sub>H</sub>	T2	.6	.5	.4	.3	.2	.1	.0
A0 <sub>H</sub> <sup>2)</sup>	P2	FF <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
A8 <sub>H</sub> <sup>2)</sup>	IEN0	00 <sub>H</sub>	EAL	WDT	ET2	ES	ET1	EX1	ET0	EX0
A9 <sub>H</sub>	IP0	00 <sub>H</sub>	OWDS	WDTS	.5	.4	.3	.2	.1	.0
AA <sub>H</sub>	SRELL	D9 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
B0 <sub>H</sub> <sup>2)</sup>	P3	FF <sub>H</sub>	RD	WR	T1	T0	INT1	INT0	TxD	RxD
B1 <sub>H</sub>	SYSCON	XX10- XX01 <sub>B</sub>	–	–	EALE	RMAP	–	–	XMAP1	XMAP0
B8 <sub>H</sub> <sup>2)</sup>	IEN1	00 <sub>H</sub>	EXEN2	SWDT	EX6	EX5	EX4	EX3	EX2	EADC
B9 <sub>H</sub>	IP1	XX00- 0000 <sub>B</sub>	–	–	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved

2) Bit-addressable special function registers

3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

**Table 3**  
**Contents of the SFRs, SFRs in numeric order of their addresses (cont'd)**

Addr	Register	Content after Reset <sup>1)</sup>	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BA <sub>H</sub>	SRELH	XXXX-XX11 <sub>B</sub>	–	–	–	–	–	–	.1	.0
C0 <sub>H</sub> <sup>2)</sup>	IRCON	00 <sub>H</sub>	EXF2	TF2	IEX6	IEX5	IEX4	IEX3	IEX2	IADC
C1 <sub>H</sub>	CCEN	00 <sub>H</sub>	COCA H3	COCAL 3	COCA H2	COCAL 2	COCA H1	COCAL 1	COCA H0	COCAL 0
C2 <sub>H</sub>	CCL1	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
C3 <sub>H</sub>	CCH1	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
C4 <sub>H</sub>	CCL2	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
C5 <sub>H</sub>	CCH2	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
C6 <sub>H</sub>	CCL3	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
C7 <sub>H</sub>	CCH3	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
C8 <sub>H</sub> <sup>2)</sup>	T2CON	00 <sub>H</sub>	T2PS	I3FR	I2FR	T2R1	T2R0	T2CM	T2I1	T2I0
CA <sub>H</sub>	CRCL	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
CB <sub>H</sub>	CRCH	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
CC <sub>H</sub>	TL2	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
CD <sub>H</sub>	TH2	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
D0 <sub>H</sub> <sup>2)</sup>	PSW	00 <sub>H</sub>	CY	AC	F0	RS1	RS0	OV	F1	P
D8 <sub>H</sub> <sup>2)</sup>	ADCON0	00 <sub>H</sub>	BD	CLK	ADEX	BSY	ADM	MX2	MX1	MX0
D9 <sub>H</sub>	ADDATH	00 <sub>H</sub>	.9	.8	.7	.6	.5	.4	.3	.2
DA <sub>H</sub>	ADDATL	00XX-XXXX <sub>B</sub>	.1	.0	–	–	–	–	–	–
DB <sub>H</sub>	P6	–	.7	.6	.5	.4	.3	.2	.1	.0
DC <sub>H</sub>	ADCON1	0XXX-X000 <sub>B</sub>	ADCL	–	–	–	–	MX2	MX1	MX0
E0 <sub>H</sub> <sup>2)</sup>	ACC	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
E8 <sub>H</sub> <sup>2)</sup>	P4	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
F0 <sub>H</sub> <sup>2)</sup>	B	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
F8 <sub>H</sub> <sup>2)</sup>	P5	FF <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved

2) Bit-addressable special function registers

### Digital I/O Ports

The C515A allows for digital I/O on 48 lines grouped into 6 bidirectional 8-bit ports. Each port bit consists of a latch, an output driver and an input buffer. Read and write accesses to the I/O ports P0 through P5 are performed via their corresponding special function registers P0 to P5.

The output drivers of port 0 and 2 and the input buffers of port 0 are also used for accessing external memory. In this application, port 0 outputs the low byte of the external memory address, time-multiplexed with the byte being written or read. Port 2 outputs the high byte of the external memory address when the address is 16 bits wide. Otherwise, the port 2 pins continue emitting the P2 SFR contents.

### Analog Input Ports

Port 6 is available as input port only and provides two functions. When used as digital inputs, the corresponding SFR P6 contains the digital value applied to the port 6 lines. When used for analog inputs the desired analog channel is selected by a three-bit field in SFR ADCON0. Of course, it makes no sense to output a value to these input-only ports by writing to the SFR P6. This will have no effect.

If a digital value is to be read, the voltage levels are to be held within the input voltage specifications ( $V_{IL}/V_{IH}$ ). Since P6 is not bit-addressable, all input lines of P6 are read at the same time by byte instructions.

Nevertheless, it is possible to use port 6 simultaneously for analog and digital input. However, care must be taken that all bits of P6 that have an undetermined value caused by their analog function are masked.

Timer / Counter 0 and 1

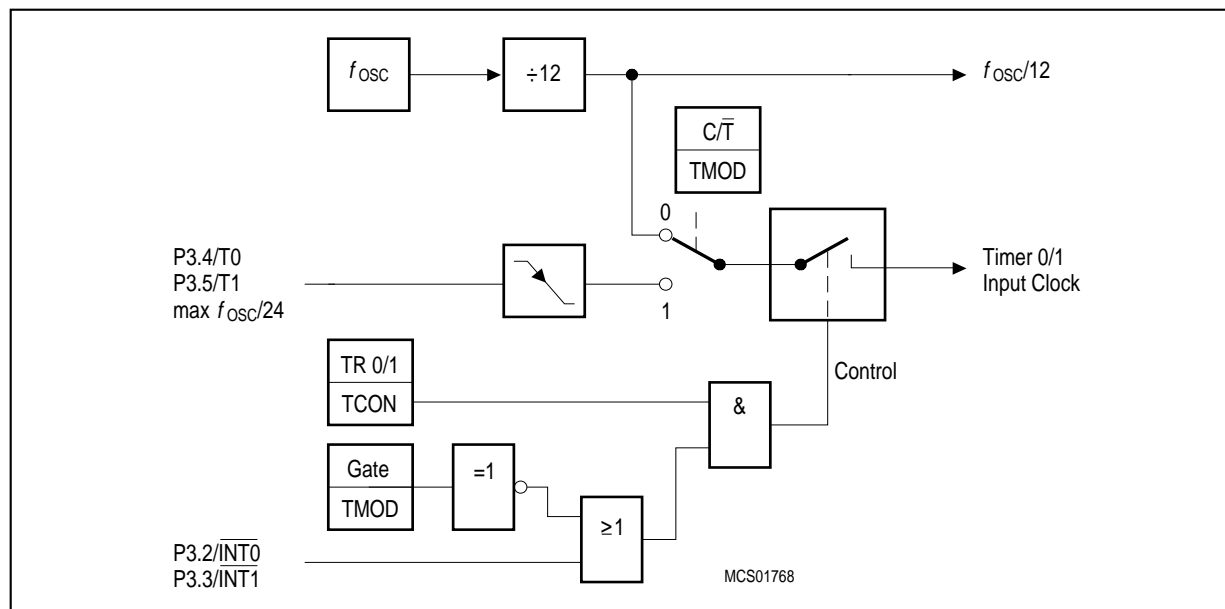
Timer/Counter 0 and 1 can be used in four operating modes as listed in **table 4**:

**Table 4**  
Timer/Counter 0 and 1 Operating Modes

Mode	Description	TMOD		Input Clock	
		M1	M0	internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	0	0	$f_{osc}/12 \times 32$	$f_{osc}/24 \times 32$
1	16-bit timer/counter	1	1	$f_{osc}/12$	$f_{osc}/24$
2	8-bit timer/counter with 8-bit autoreload	1	0		
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	1	1		

In the “timer” function (C/T = ‘0’) the register is incremented every machine cycle. Therefore the count rate is  $f_{osc}/12$ .

In the “counter” function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is  $f_{osc}/24$ . External inputs INT0 and INT1 (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 9** illustrates the input clock logic.



**Figure 9**  
Timer/Counter 0 and 1 Input Clock Logic

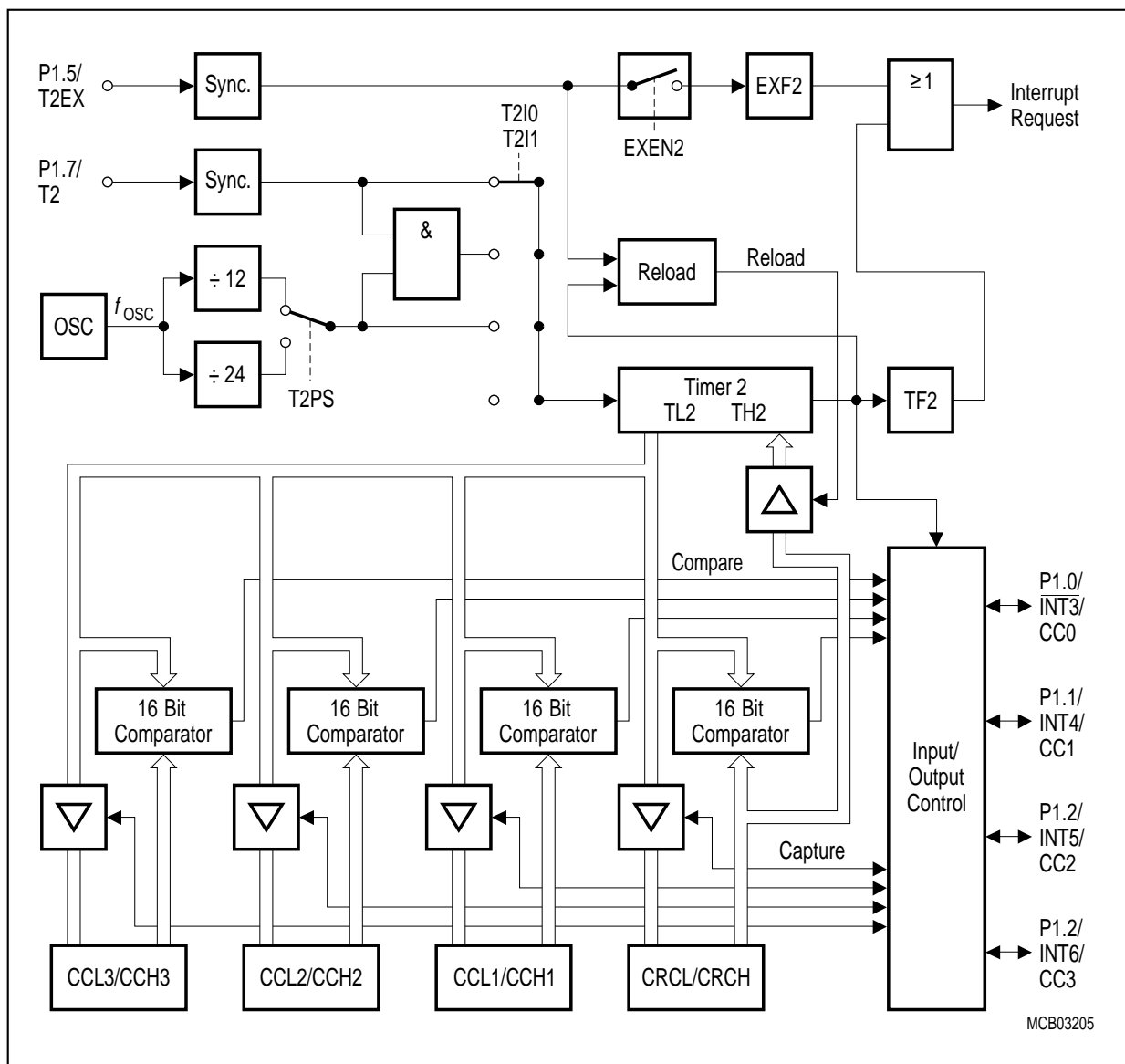


**Timer/Counter 2 with Compare/Capture/Reload**

The timer 2 of the C515A provides additional compare/capture/reload features. which allow the selection of the following operating modes:

- Compare : up to 4 PWM signals with 16-bit/500 ns resolution
- Capture : up to 4 high speed capture inputs with 500 ns resolution
- Reload : modulation of timer 2 cycle time

The block diagram in **figure 10** shows the general configuration of timer 2 with the additional compare/capture/reload registers. The I/O pins which can be used for timer 2 control are located as multifunctional port functions at port 1.



**Figure 10**  
**Timer 2 Block Diagram**

## Timer 2 Operating Modes

The timer 2, which is a 16-bit-wide register, can operate as timer, event counter, or gated timer. A roll-over of the count value in TL2/TH2 from all 1's to all 0's sets the timer overflow flag TF2 in SFR IRCON, which can generate an interrupt. The bits in register T2CON are used to control the timer 2 operation.

Timer Mode: In timer function, the count rate is derived from the oscillator frequency. A prescaler offers the possibility of selecting a count rate of 1/12 or 1/24 of the oscillator frequency.

Gated Timer Mode: In gated timer function, the external input pin T2 (P1.7) functions as a gate to the input of timer 2. If T2 is high, the internal clock input is gated to the timer. T2 = 0 stops the counting procedure. This facilitates pulse width measurements. The external gate signal is sampled once every machine cycle.

Event Counter Mode: In the event counter function, the timer 2 is incremented in response to a 1-to-0 transition at its corresponding external input pin T2 (P1.7). In this function, the external input is sampled every machine cycle. Since it takes two machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it must be held for at least one full machine cycle.

Reload of Timer 2: Two reload modes are selectable:

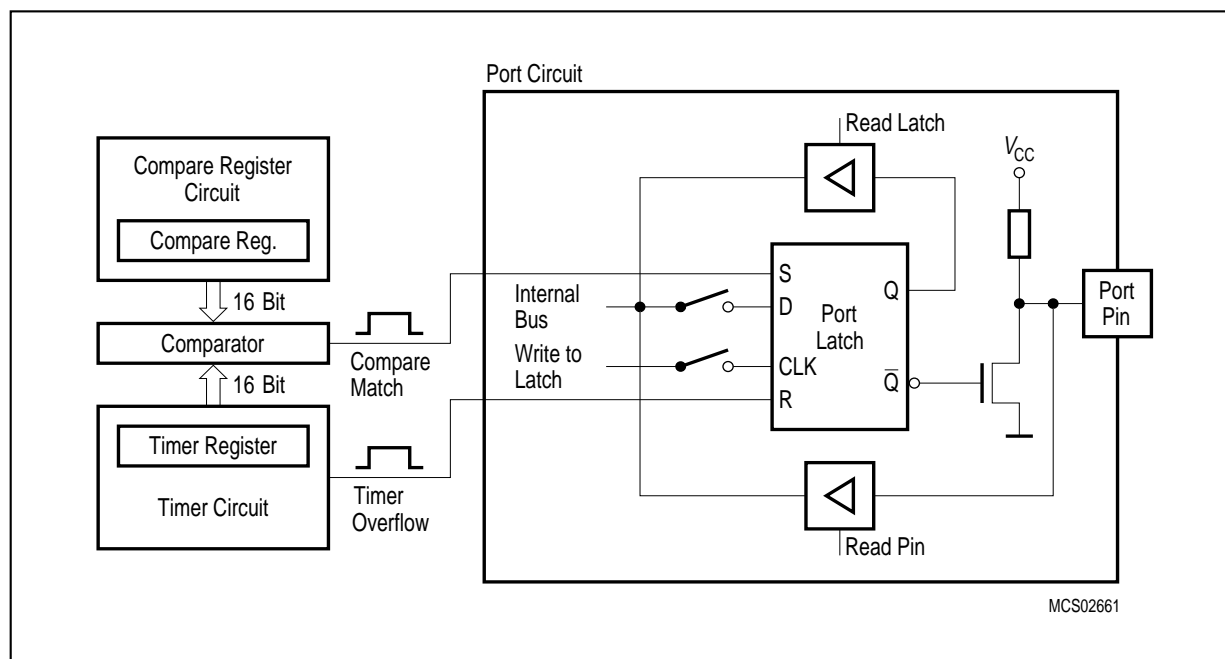
In mode 0, when timer 2 rolls over from all 1's to all 0's, it not only sets TF2 but also causes the timer 2 registers to be loaded with the 16-bit value in the CRC register, which is preset by software. In mode 1, a 16-bit reload from the CRC register is caused by a negative transition at the corresponding input pin P1.5/T2EX. This transition will also set flag EXF2 if bit EXEN2 in SFR IEN1 has been set.

**Timer 2 Compare Modes**

The compare function of a timer/register combination operates as follows: the 16-bit value stored in a compare or compare/capture register is compared with the contents of the timer register; if the count value in the timer register matches the stored value, an appropriate output signal is generated at a corresponding port pin and an interrupt can be generated.

Compare Mode 0

In compare mode 0, upon matching the timer and compare register contents, the output signal changes from low to high. It goes back to a low level on timer overflow. As long as compare mode 0 is enabled, the appropriate output pin is controlled by the timer circuit only and writing to the port will have no effect. **Figure 11** shows a functional diagram of a port circuit when used in compare mode 0. The port latch is directly controlled by the timer overflow and compare match signals. The input line from the internal bus and the write-to-latch line of the port latch are disconnected when compare mode 0 is enabled.

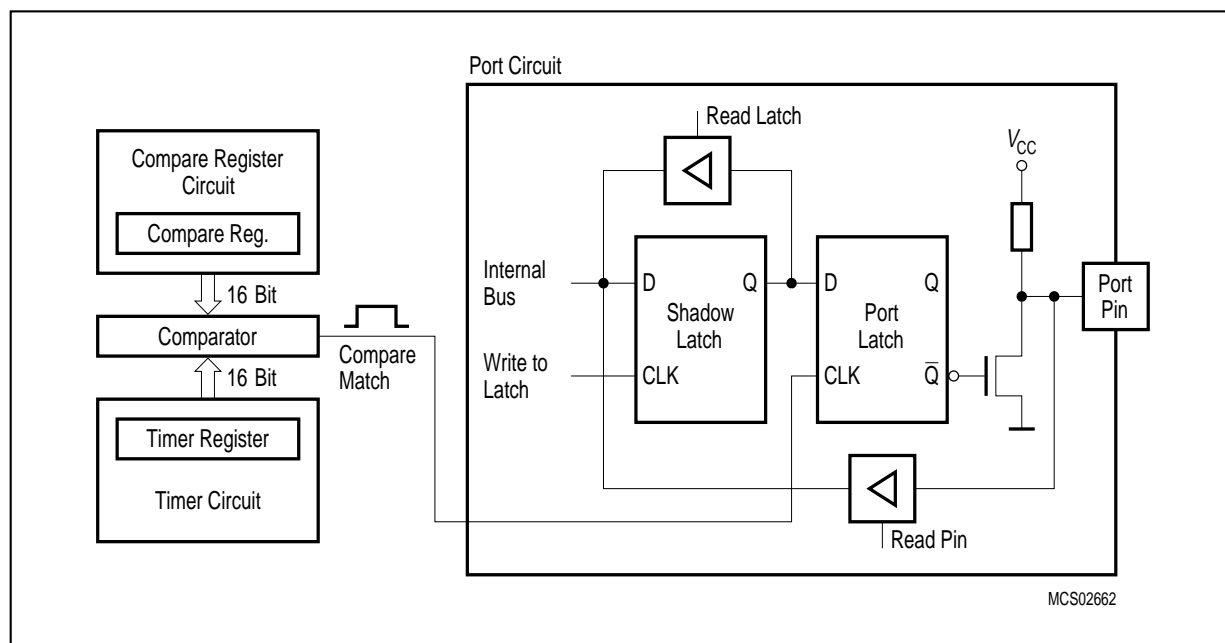


**Figure 11**  
**Port Latch in Compare Mode 0**

Compare Mode 1

If compare mode 1 is enabled and the software writes to the appropriate output latch at the port, the new value will not appear at the output pin until the next compare match occurs. Thus, it can be chosen whether the output signal has to make a new transition (1-to-0 or 0-to-1, depending on the actual pin-level) or should keep its old value at the time when the timer value matches the stored compare value.

In compare mode 1 (see **figure 12**) the port circuit consists of two separate latches. One latch (which acts as a “shadow latch”) can be written under software control, but its value will only be transferred to the port latch (and thus to the port pin) when a compare match occurs.



**Figure 12**  
**Compare Function in Compare Mode 1**

**Serial Interface (USART)**

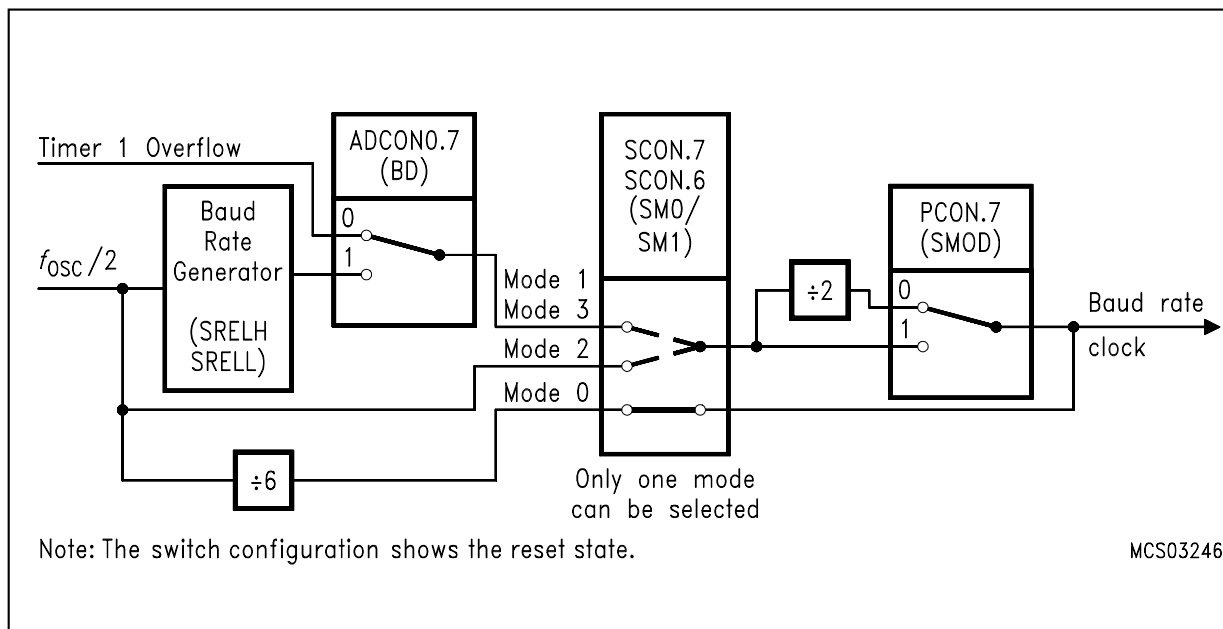
The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in **table 5**. The possible baudrates can be calculated using the formulas given in **table 5**.

**Table 5**  
**USART Operating Modes**

Mode	SCON		Description
	SM0	SM1	
0	0	0	Shift register mode Serial data enters and exits through RxD/ TxD outputs the shift clock; 8-bit are transmitted/received (LSB first); fixed baud rate
1	0	1	8-bit UART, variable baud rate 10 bits are transmitted (through TxD) or received (at RxD)
2	1	0	9-bit UART, fixed baud rate 11 bits are transmitted (through TxD) or received (at RxD)
3	1	1	9-bit UART, variable baud rate Like mode 2

For clarification some terms regarding the difference between “baud rate clock” and “baud rate” should be mentioned. In the asynchronous modes the serial interfaces require a clock rate which is 16 times the baud rate for internal synchronization. Therefore, the baud rate generators/timers have to provide a “baud rate clock” (output signal in **figure 13** to the serial interface which - there divided by 16 - results in the actual “baud rate”. Further, the abbreviation  $f_{OSC}$  refers to the oscillator frequency (crystal or external clock operation).

The variable baud rates for modes 1 and 3 of the serial interface can be derived from either timer 1 or a dedicated baud rate generator (see **figure 13**).



**Figure 13**  
**Block Diagram of Baud Rate Generation for the Serial Interface**

Table 6 below lists the values/formulas for the baud rate calculation of the serial interface with its dependencies of the control bits BD and SMOD.

**Table 6**  
**Serial Interface - Baud Rate Dependencies**

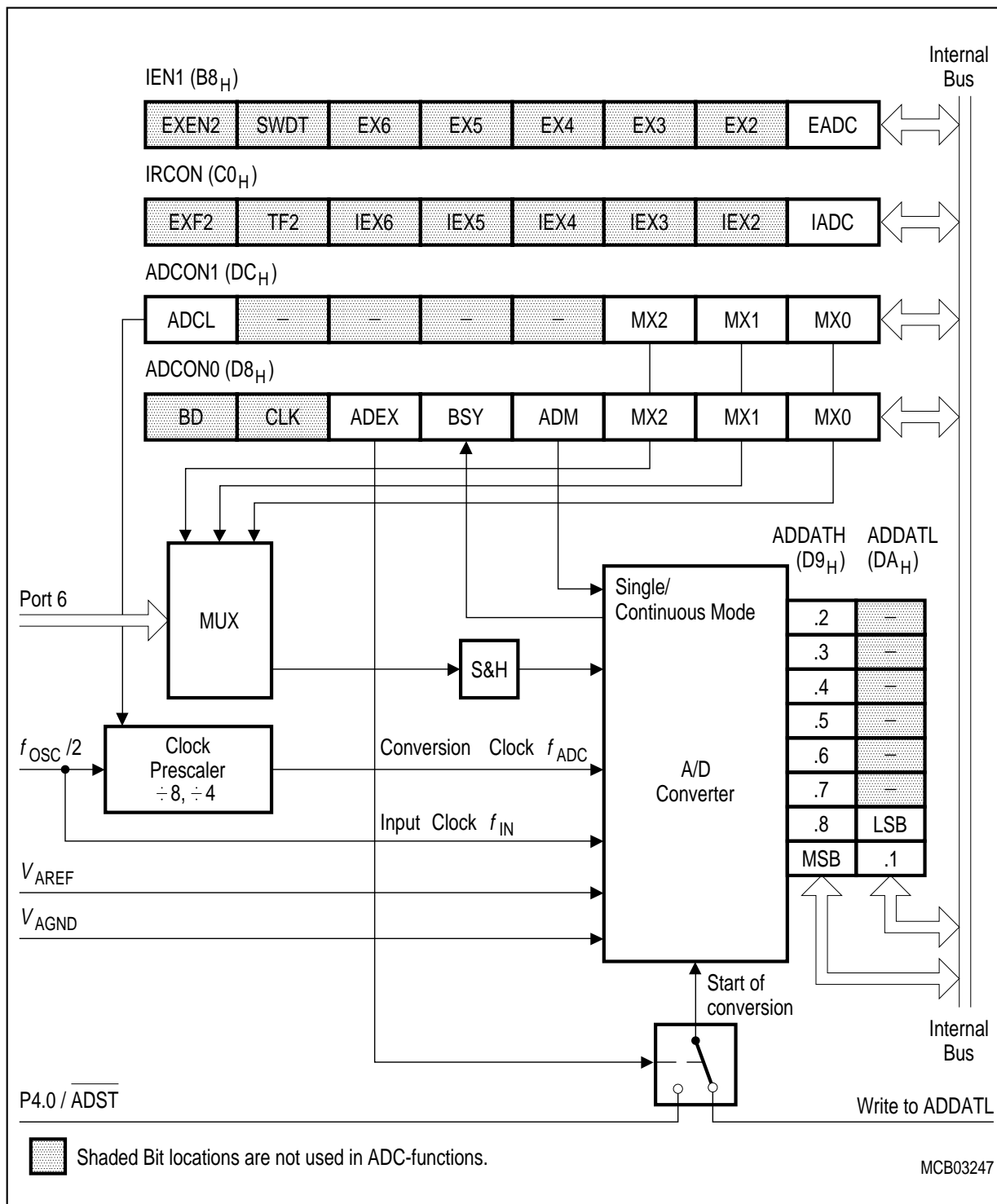
Serial Interface 0 Operating Modes	Active Control Bits		Baud Rate Calculation
	BD	SMOD	
Mode 0 (Shift Register)	–	–	$f_{osc} / 12$
Mode 1 (8-bit UART) Mode 3 (9-bit UART)	0	X	Controlled by timer 1 overflow: $(2^{SMOD} \times \text{timer 1 overflow rate}) / 32$
	1	X	Controlled by baud rate generator $(2^{SMOD} \times f_{osc}) / (64 \times \text{baud rate generator overflow rate})$
Mode 2 (9-bit UART)	–	0	$f_{osc} / 64$
		1	$f_{osc} / 32$

### 10-Bit A/D Converter

The C515A provides an A/D converter with the following features:

- 8 multiplexed input channels (port 6), which can also be used as digital inputs
- 10-bit resolution
- Single or continuous conversion mode
- Internal or external start-of-conversion trigger capability
- Interrupt request generation after each conversion
- Using successive approximation conversion technique via a capacitor array
- Built-in hidden calibration of offset and linearity errors

The A/D converter operates with a successive approximation technique and uses self calibration mechanisms for reduction and compensation of offset and linearity errors. The externally applied reference voltage range has to be held on a fixed value within the specifications. The main functional blocks of the A/D converter are shown in **figure 14**.



**Figure 14**  
A/D Converter Block Diagram



## Interrupt System

The C515A provides 12 interrupt sources with four priority levels. Five interrupts can be generated by the on-chip peripherals (timer 0, timer 1, timer 2, A/D converter, and serial interface) and seven interrupts may be triggered externally (P3.2/INT0, P3.3/INT1, P1.4/INT2, P1.0/ $\overline{\text{INT3}}$ , P1.1/INT4, P1.2/INT5, P1.3/INT6). The wake-up from power-down mode interrupt has a special functionality which allows to exit from the software power-down mode by a short low pulse at pin P3.2/ $\overline{\text{INT0}}$ .

This chapter shows the interrupt structure, the interrupt vectors and the interrupt related special function registers. **Figure 15** and **16** give a general overview of the interrupt sources and illustrate the request and the control flags which are described in the next sections.

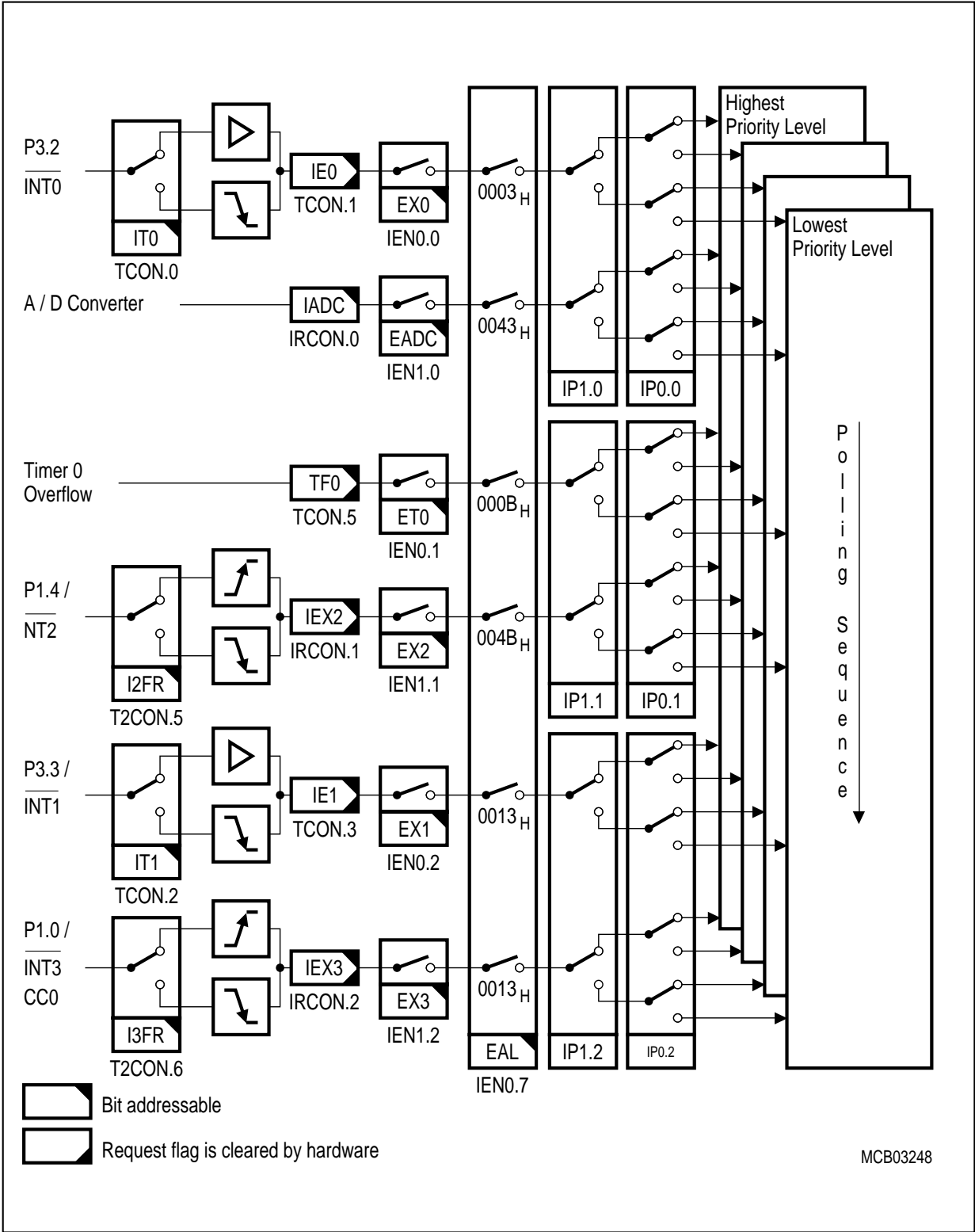
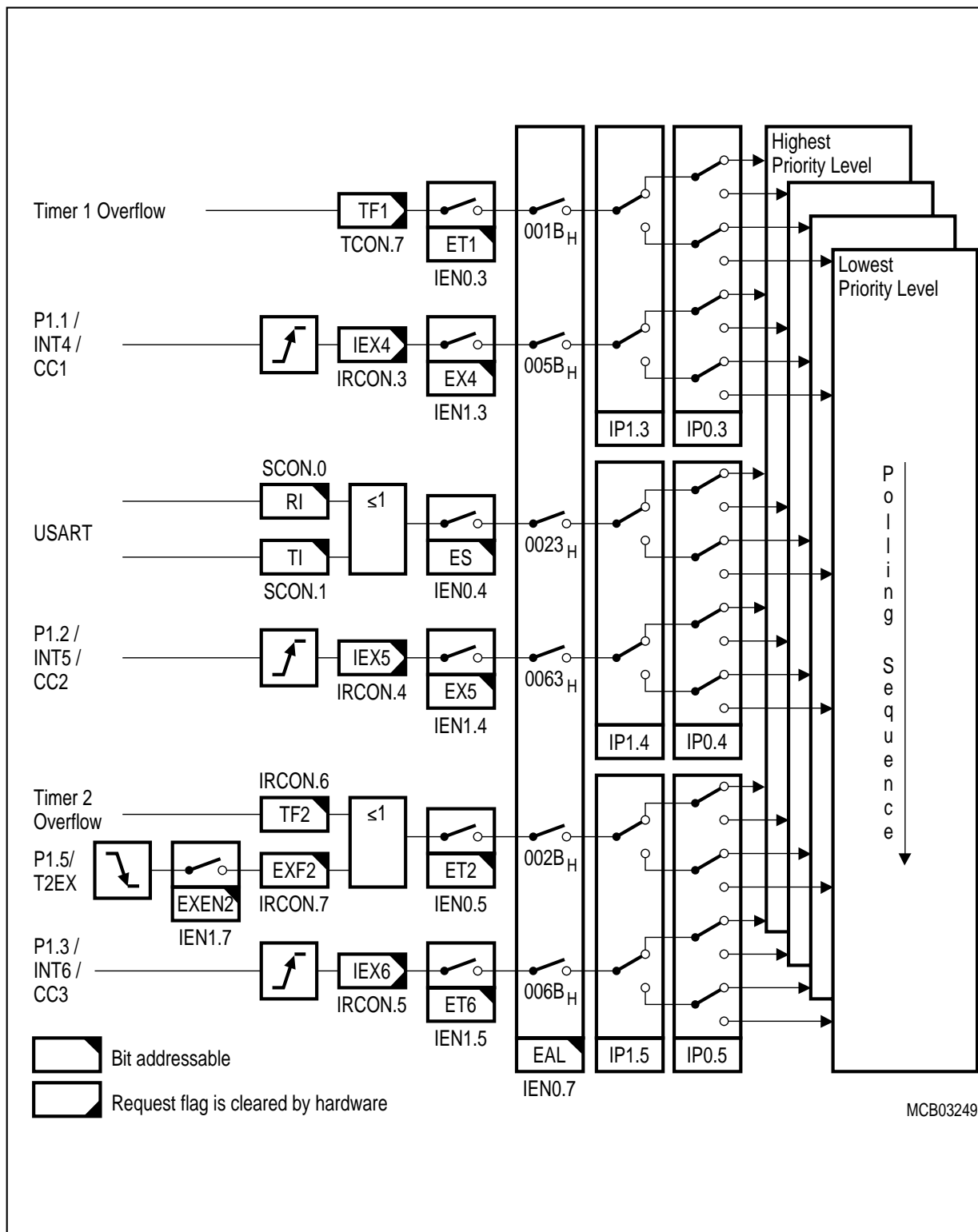


Figure 15  
Interrupt Request Sources (Part 1)



**Figure 16**  
**Interrupt Request Sources (Part 2)**

**Table 7**  
**Interrupt Source and Vectors**

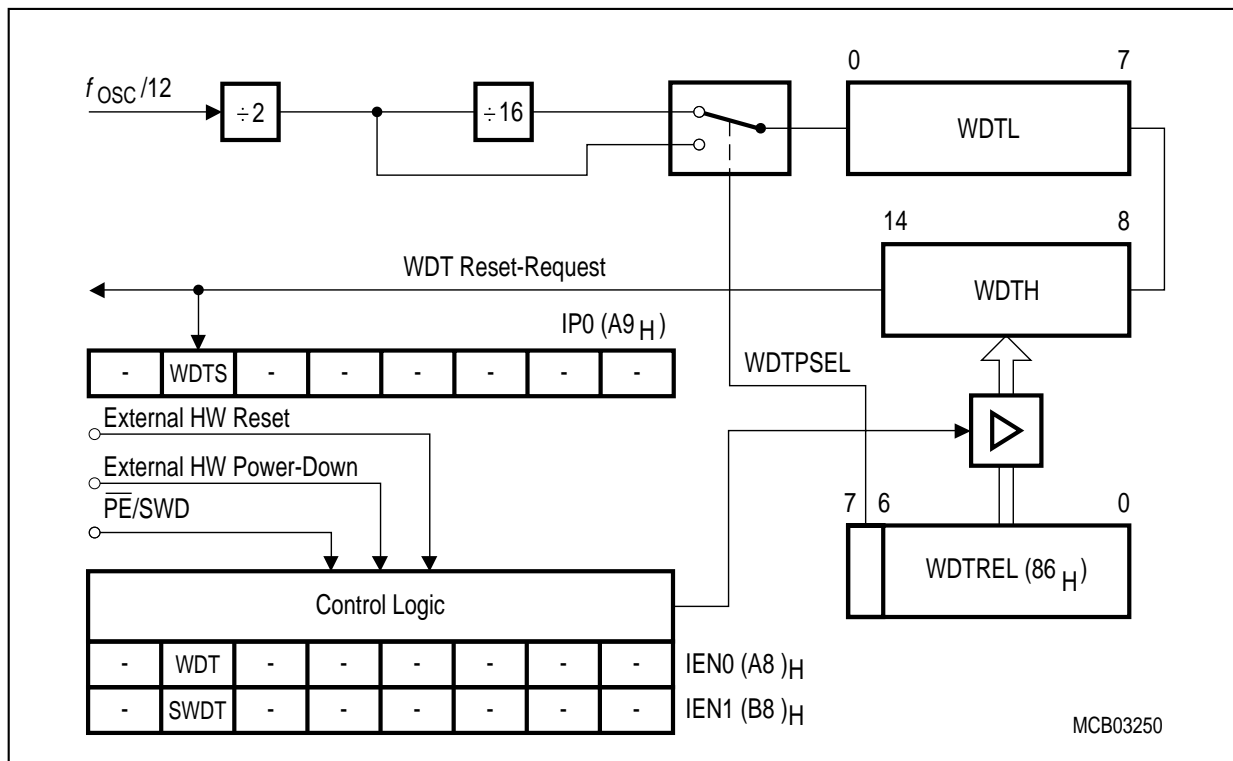
<b>Interrupt Source</b>	<b>Interrupt Vector Address</b>	<b>Interrupt Request Flags</b>
External Interrupt 0	0003 <sub>H</sub>	IE0
Timer 0 Overflow	000B <sub>H</sub>	TF0
External Interrupt 1	0013 <sub>H</sub>	IE1
Timer 1 Overflow	001B <sub>H</sub>	TF1
Serial Channel	0023 <sub>H</sub>	RI / TI
Timer 2 Overflow / Ext. Reload	002B <sub>H</sub>	TF2 / EXF2
A/D Converter	0043 <sub>H</sub>	IADC
External Interrupt 2	004B <sub>H</sub>	IEX2
External Interrupt 3	0053 <sub>H</sub>	IEX3
External Interrupt 4	005B <sub>H</sub>	IEX4
External Interrupt 5	0063 <sub>H</sub>	IEX5
External Interrupt 6	006B <sub>H</sub>	IEX6
Wake-up from power-down mode	007B <sub>H</sub>	–

**Fail Save Mechanisms**

The C515A offers enhanced fail safe mechanisms, which allow an automatic recovery from software upset or hardware failure:

- a programmable watchdog timer (WDT), with variable time-out period from 512  $\mu$ s up to approx. 1.1 s at 12 MHz (256  $\mu$ s up to approx. 0.65 s at 24 MHz)
- an oscillator watchdog (OWD) which monitors the on-chip oscillator and forces the microcontroller into reset state in case the on-chip oscillator fails; it also provides the clock for a fast internal reset after power-on.

The watchdog timer in the C515A is a 15-bit timer, which is incremented by a count rate of  $f_{osc}/24$  up to  $f_{osc}/384$ . The system clock of the C515A is divided by two prescalers, a divide-by-two and a divide-by-16 prescaler. For programming of the watchdog timer overflow rate, the upper 7 bit of the watchdog timer can be written. **Figure 15** shows the block diagram of the watchdog timer unit.



**Figure 17**  
**Block Diagram of the Watchdog Timer**

The watchdog timer can be started by software (bit SWDT) or by hardware through pin  $\overline{PE}/SWD$ , but it cannot be stopped during active mode of the C515A. If the software fails to refresh the running watchdog timer an internal reset will be initiated on watchdog timer overflow. For refreshing of the watchdog timer the content of the SFR WDTREL is transferred to the upper 7-bit of the watchdog timer. The refresh sequence consists of two consecutive instructions which set the bits WDT and SWDT each. The reset cause (external reset or reset caused by the watchdog) can be examined by software (flag WDTS). It must be noted, however, that the watchdog timer is halted during the idle mode and power down mode of the processor.

## Oscillator Watchdog

The oscillator watchdog unit serves for four functions:

- **Monitoring of the on-chip oscillator's function**

The watchdog supervises the on-chip oscillator's frequency; if it is lower than the frequency of the auxiliary RC oscillator in the watchdog unit, the internal clock is supplied by the RC oscillator and the device is brought into reset; if the failure condition disappears (i.e. the on-chip oscillator has a higher frequency than the RC oscillator), the part executes a final reset phase of typ. 1 ms in order to allow the oscillator to stabilize; then the oscillator watchdog reset is released and the part starts program execution again.

- **Fast internal reset after power-on**

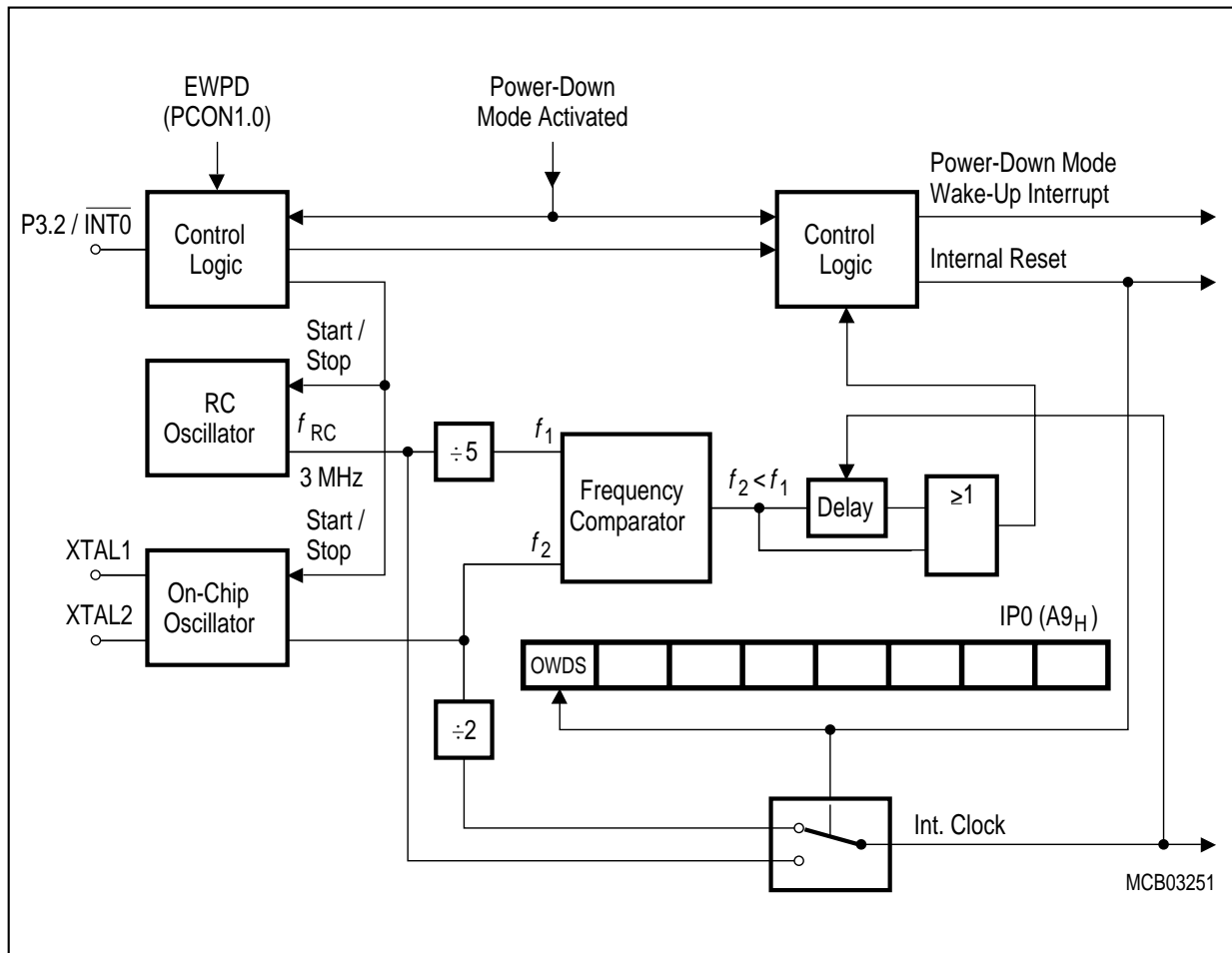
The oscillator watchdog unit provides a clock supply for the reset before the on-chip oscillator has started. The oscillator watchdog unit also works identically to the monitoring function.

- **Restart from the hardware power down mode.**

If the hardware power down mode is terminated the oscillator watchdog has to control the correct start-up of the on-chip oscillator and to restart the program. The oscillator watchdog function is only part of the complete hardware power down sequence; however, the watchdog works identically to the monitoring function.

- **Control of external wake-up from software power-down mode**

When the software power-down mode is left by a low level at the P3.2/ $\overline{\text{INT0}}$  pin, the oscillator watchdog unit assures that the microcontroller resumes operation (execution of the power-down wake-up interrupt) with the nominal clock rate. In the power-down mode the RC oscillator and the on-chip oscillator are stopped. Both oscillators are started again when power-down mode is released. When the on-chip oscillator has a higher frequency than the RC oscillator, the microcontroller starts operation after a final delay of typ. 1 ms in order to allow the on-chip oscillator to stabilize.



**Figure 18**  
**Block Diagram of the Oscillator Watchdog**

## Power Saving Modes

The C515A provides two basic power saving modes, the idle mode and the power down mode. Additionally, a slow down mode is available. This power saving mode reduces the internal clock rate in normal operating mode and it can be also used for further power reduction in idle mode.

- **Idle mode**

The CPU is gated off from the oscillator. All peripherals are still provided with the clock and are able to work. Idle mode is entered by software and can be left by an interrupt or reset.

- **Slow down mode**

The controller keeps up the full operating functionality, but its normal clock frequency is internally divided by 8. This slows down all parts of the controller, the CPU and all peripherals, to 1/8th of their normal operating frequency and also reduces power consumption.

- **Software power down mode**

The operation of the C515 is completely stopped and the oscillator is turned off. This mode is used to save the contents of the internal RAM with a very low standby current. This power down mode is entered by software and can be left by reset or by a short low pulse at pin P3.2/ $\overline{\text{INT0}}$ .

- **Hardware Power down mode**

If pin HYPD gets active (low level) the part enters the hardware power down mode and starts a complete internal reset sequence. Thereafter, both oscillators of the chip are stopped and the port pins and several control lines enter a floating state.

In the power down mode of operation,  $V_{CC}$  can be reduced to minimize power consumption. It must be ensured, however, that  $V_{CC}$  is not reduced before the power down mode is invoked, and that  $V_{CC}$  is restored to its normal operating level, before the power down mode is terminated. **Table 8** gives a general overview of the entry and exit procedures of the power saving modes.



**Table 8  
Power Saving Modes Overview**

<b>Mode</b>	<b>Entering 2-Instruction Example</b>	<b>Leaving by</b>	<b>Remarks</b>
Idle mode	ORL PCON, #01H ORL PCON, #20H	Occurrence of an interrupt from a peripheral unit	CPU clock is stopped; CPU maintains their data; peripheral units are active (if enabled) and provided with clock
		Hardware Reset	
Slow Down Mode	In normal mode: ORL PCON,#10H	ANL PCON,#0EFH or Hardware Reset	Internal clock rate is reduced to 1/8 of its nominal frequency
	With idle mode: ORL PCON,#01H ORL PCON, #30H	Occurrence of an interrupt from a peripheral unit  Hardware reset	CPU clock is stopped; CPU maintains their data; peripheral units are active (if enabled) and provided with 1/8 of its nominal frequency
Software Power Down Mode	ORL PCON, #02H ORL PCON, #40H	Hardware Reset	Oscillator is stopped; contents of on-chip RAM and SFR's are maintained;
		Short low pulse at pin P3.2/INT0	
Hardware Power Down Mode	$\overline{HWPD} = 0$	$\overline{HWPD} = 1$	Oscillator is stopped; internal reset is executed;

**Absolute Maximum Ratings**

Ambient temperature under bias ( $T_A$ ) .....	- 40 to + 125 °C
Storage temperature ( $T_{stg}$ ) .....	- 65 °C to 150 °C
Voltage on $V_{CC}$ pins with respect to ground ( $V_{SS}$ ) .....	- 0.5 V to 6.5 V
Voltage on any pin with respect to ground ( $V_{SS}$ ) .....	- 0.5 V to $V_{CC} + 0.5$ V
Input current on any pin during overload condition .....	- 10 mA to 10 mA
Absolute sum of all input currents during overload condition .....	100 mA
Power dissipation of package .....	TBD

**Note:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ( $V_{IN} > V_{CC}$  or  $V_{IN} < V_{SS}$ ) the Voltage on  $V_{CC}$  pins with respect to ground ( $V_{SS}$ ) must not exceed the values defined by the absolute maximum ratings.

## DC Characteristics

$V_{CC} = 5\text{ V} + 10\%, -15\%$ ;  $V_{SS} = 0\text{ V}$

$T_A = 0\text{ to }70\text{ }^\circ\text{C}$

for the SAB-C515A

$T_A = -40\text{ to }85\text{ }^\circ\text{C}$

for the SAF-C515A

$T_A = -40\text{ to }110\text{ }^\circ\text{C}$

for the SAH-C515A

$T_A = -40\text{ to }125\text{ }^\circ\text{C}$

for the SAK-C515A

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage					
Pins except $\overline{\text{EA}}$ , $\overline{\text{RESET}}$ , $\overline{\text{HWPD}}$	$V_{IL}$	-0.5	$0.2 V_{CC} - 0.1$	V	-
$\overline{\text{EA}}$ pin	$V_{IL1}$	-0.5	$0.2 V_{CC} - 0.3$	V	-
$\overline{\text{HWPD}}$ and $\overline{\text{RESET}}$ pins	$V_{IL2}$	-0.5	$0.2 V_{CC} + 0.1$	V	-
Input high voltage					
pins except $\overline{\text{RESET}}$ , XTAL2 and $\overline{\text{HWPD}}$	$V_{IH}$	$0.2 V_{CC} + 0.9$	$V_{CC} + 0.5$	V	-
XTAL2 pin	$V_{IH1}$	$0.7 V_{CC}$	$V_{CC} + 0.5$	V	-
$\overline{\text{RESET}}$ and $\overline{\text{HWPD}}$ pin	$V_{IH2}$	$0.6 V_{CC}$	$V_{CC} + 0.5$	V	-
Output low voltage					
Ports 1, 2, 3, 4, 5	$V_{OL}$	-	0.45	V	$I_{OL} = 1.6\text{ mA}^1)$
Port 0, ALE, $\overline{\text{PSEN}}$	$V_{OL1}$	-	0.45	V	$I_{OL} = 3.2\text{ mA}^1)$
Output high voltage					
Ports 1, 2, 3, 4, 5	$V_{OH}$	2.4	-	V	$I_{OH} = -80\text{ }\mu\text{A}$
		$0.9 V_{CC}$	-	V	$I_{OH} = -10\text{ }\mu\text{A}$
Port 0 in external bus mode, ALE, $\overline{\text{PSEN}}$	$V_{OH1}$	2.4	-	V	$I_{OH} = -800\text{ }\mu\text{A}^2)$
		$0.9 V_{CC}$	-	V	$I_{OH} = -80\text{ }\mu\text{A}^2)$
Logic 0 input current					
Ports 1, 2, 3, 4, 5	$I_{LI}$	-10	-70	$\mu\text{A}$	$V_{IN} = 0.45\text{ V}$
Logical 0-to-1 transition current, Ports 1, 2, 3, 4, 5	$I_{TL}$	-65	-650	$\mu\text{A}$	$V_{IN} = 2\text{ V}$
Input leakage current					
Port 0 and 6, $\overline{\text{EA}}$ , $\overline{\text{HWPD}}$	$I_{LI}$	-	$\pm 1$	$\mu\text{A}$	$0.45 < V_{IN} < V_{CC}$
Input low current to $\overline{\text{RESET}}$ for reset	$I_{IL2}$	-10	-100	$\mu\text{A}$	$V_{IN} = 0.45\text{ V}$
XTAL2	$I_{IL3}$	-	-15	$\mu\text{A}$	$V_{IN} = 0.45\text{ V}$
$\overline{\text{PE/SWD}}$	$I_{IL4}$	-	-20	$\mu\text{A}$	$V_{IN} = 0.45\text{ V}$
Pin capacitance	$C_{IO}$	-	10	pF	$f_C = 1\text{ MHz}$ , $T_A = 25\text{ }^\circ\text{C}$
Overload current	$I_{OV}$	-	$\pm 5$	mA	<sup>8) 9)</sup>

Notes see next page

## Power Supply Current

Parameter		Symbol	Limit Values		Unit	Test Condition
			typ. <sup>10)</sup>	max. <sup>11)</sup>		
Active mode	18 MHz	$I_{CC}$	16.9	23.1	mA	4)
	24 MHz	$I_{CC}$	21.7	29.4	mA	
Idle mode	18 MHz	$I_{CC}$	8.5	12.1	mA	5)
	24 MHz	$I_{CC}$	11.0	15.0	mA	
Active mode with slow-down enabled	18 MHz	$I_{CC}$	5.6	8.0	mA	6)
	24 MHz	$I_{CC}$	6.6	9.6	mA	
Active mode with slow-down enabled	18 MHz	$I_{CC}$	3.0	4.1	mA	7)
	24 MHz	$I_{CC}$	3.3	4.7	mA	
Power-down mode		$I_{PD}$	10	50	$\mu$ A	$V_{CC} = 2 \dots 5.5 \text{ V}^{3)}$

### Notes:

- Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the  $V_{OL}$  of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.
- Capacitive loading on ports 0 and 2 may cause the  $V_{OH}$  on ALE and PSEN to momentarily fall below the 0.9  $V_{CC}$  specification when the address lines are stabilizing.
- $I_{PD}$  (software power-down mode) is measured under following conditions:  
EA = RESET = Port 0 = Port 6 =  $V_{CC}$ ; XTAL1 = N.C.; XTAL2 =  $V_{SS}$ ;  $\overline{\text{PE/SWD}} = V_{SS}$ ;  $\overline{\text{HWPD}} = V_{CC}$ ;  $V_{AGND} = V_{SS}$ ;  $V_{AREF} = V_{CC}$ ; all other pins are disconnected.  
 $I_{PD}$  (hardware power-down mode): independent from any particular pin connection.
- $I_{CC}$  (active mode) is measured with:  
XTAL2 driven with  $t_{CLCH}, t_{CHCL} = 5 \text{ ns}$ ,  $V_{IL} = V_{SS} + 0.5 \text{ V}$ ,  $V_{IH} = V_{CC} - 0.5 \text{ V}$ ; XTAL1 = N.C.;  
EA =  $\overline{\text{PE/SWD}}$  = Port 0 = Port 6 =  $V_{CC}$ ;  $\overline{\text{HWPD}} = V_{CC}$ ;  $\overline{\text{RESET}} = V_{SS}$ ;  
all other pins are disconnected.  $I_{CC}$  would be slightly higher if a crystal oscillator is used (appr. 1 mA).
- $I_{CC}$  (idle mode) is measured with all output pins disconnected and with all peripherals disabled;  
XTAL2 driven with  $t_{CLCH}, t_{CHCL} = 5 \text{ ns}$ ,  $V_{IL} = V_{SS} + 0.5 \text{ V}$ ,  $V_{IH} = V_{CC} - 0.5 \text{ V}$ ; XTAL1 = N.C.;  
 $\overline{\text{RESET}} = V_{CC}$ ;  $\overline{\text{HWPD}} = \text{Port 0} = \text{Port 6} = V_{CC}$ ; EA =  $\overline{\text{PE/SWD}} = V_{SS}$ ; all other pins are disconnected;
- $I_{CC}$  (active mode with slow-down mode) is measured with all output pins disconnected and with all peripherals disabled; XTAL2 driven with  $t_{CLCH}, t_{CHCL} = 5 \text{ ns}$ ,  $V_{IL} = V_{SS} + 0.5 \text{ V}$ ,  $V_{IH} = V_{CC} - 0.5 \text{ V}$ ; XTAL1 = N.C.;  
 $\overline{\text{RESET}} = V_{CC}$ ;  $\overline{\text{HWPD}} = \text{Port 6} = V_{CC}$ ; EA =  $\overline{\text{PE/SWD}} = V_{SS}$ ; all other pins are disconnected; the microcontroller is put into slow-down mode by software;
- $I_{CC}$  (idle mode with slow-down mode) is measured with all output pins disconnected and with all peripherals disabled; XTAL2 driven with  $t_{CLCH}, t_{CHCL} = 5 \text{ ns}$ ,  $V_{IL} = V_{SS} + 0.5 \text{ V}$ ,  $V_{IH} = V_{CC} - 0.5 \text{ V}$ ; XTAL1 = N.C.;  
 $\overline{\text{RESET}} = V_{CC}$ ;  $\overline{\text{HWPD}} = \text{Port 6} = V_{CC}$ ; EA =  $\overline{\text{PE/SWD}} = V_{SS}$ ; all other pins are disconnected; the microcontroller is put into idle mode with slow-down mode enabled by software;
- Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e.  $V_{OV} > V_{CC} + 0.5 \text{ V}$  or  $V_{OV} < V_{SS} - 0.5 \text{ V}$ ). The supply voltage  $V_{CC}$  and  $V_{SS}$  must remain within the specified limits. The absolute sum of input currents on all port pins may not exceed 50 mA.
- Not 100% tested, guaranteed by design characterization
- The typical  $I_{CC}$  values are periodically measured at  $T_A = +25 \text{ }^\circ\text{C}$  and  $V_{CC} = 5 \text{ V}$  but not 100% tested.
- The maximum  $I_{CC}$  values are measured under worst case conditions ( $T_A = 0 \text{ }^\circ\text{C}$  or  $-40 \text{ }^\circ\text{C}$  and  $V_{CC} = 5.5 \text{ V}$ )

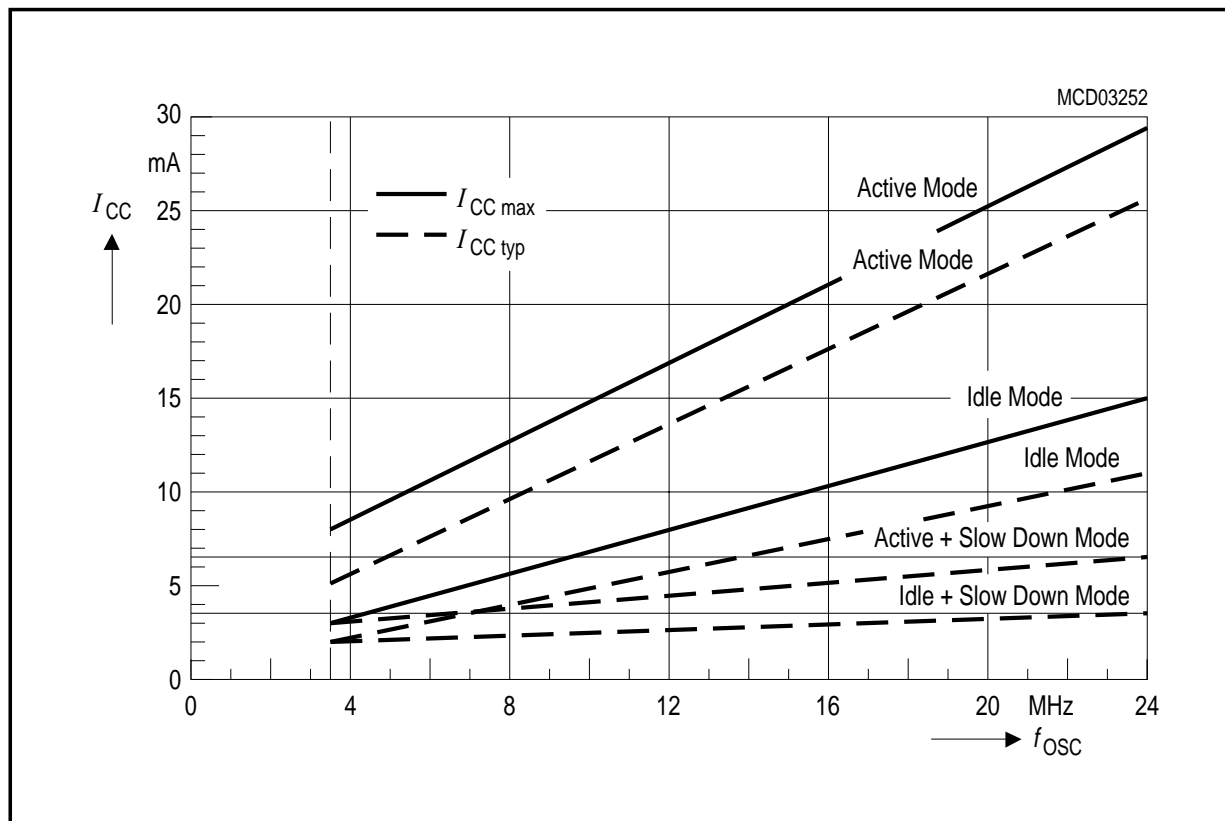


Figure 19  
ICC Diagram

Table 9  
Power Supply Current Calculation Formulas

Parameter	Symbol	Formula
Active mode	$I_{CC\ typ}$	$0.79 * f_{OSC} + 2.7$
	$I_{CC\ max}$	$1.04 * f_{OSC} + 4.4$
Idle mode	$I_{CC\ typ}$	$0.43 * f_{OSC} + 0.7$
	$I_{CC\ max}$	$0.48 * f_{OSC} + 3.5$
Active mode with slow-down enabled	$I_{CC\ typ}$	$0.17 * f_{OSC} + 2.5$
	$I_{CC\ max}$	$0.28 * f_{OSC} + 2.9$
Idle mode with slow-down enabled	$I_{CC\ typ}$	$0.06 * f_{OSC} + 1.9$
	$I_{CC\ max}$	$0.09 * f_{OSC} + 2.5$

Note:  $f_{osc}$  is the oscillator frequency in MHz.  $I_{CC}$  values are given in mA.

### A/D Converter Characteristics

$$V_{CC} = 5 \text{ V} + 10\%, -15\%; V_{SS} = 0 \text{ V}$$

$$T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$$

for the SAB-C515A

$$T_A = -40 \text{ to } 85 \text{ }^\circ\text{C}$$

for the SAF-C515A

$$T_A = -40 \text{ to } 110 \text{ }^\circ\text{C}$$

for the SAH-C515A

$$T_A = -40 \text{ to } 125 \text{ }^\circ\text{C}$$

for the SAK-C515A

$$4 \text{ V} \leq V_{AREF} \leq V_{CC} + 0.1 \text{ V}; V_{SS} - 0.1 \text{ V} \leq V_{AGND} \leq V_{SS} + 0.2 \text{ V}$$

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Analog input voltage	$V_{AIN}$	$V_{AGND}$	$V_{AREF}$	V	<sup>1)</sup>
Sample time	$t_S$	—	$16 \times t_{IN}$ $8 \times t_{IN}$	ns	Prescaler $\div 8$ Prescaler $\div 4$ <sup>2)</sup>
Conversion cycle time	$t_{ADCC}$	—	$96 \times t_{IN}$ $48 \times t_{IN}$	ns	Prescaler $\div 8$ Prescaler $\div 4$ <sup>3)</sup>
Total unadjusted error	$T_{UE}$	—	$\pm 2$	LSB	$V_{SS} + 0.5 \text{ V} \leq V_{IN} \leq V_{CC} - 0.5 \text{ V}$ <sup>4)</sup>
Internal resistance of reference voltage source	$R_{AREF}$	—	$t_{ADC} / 250$ — 1	k $\Omega$	$t_{ADC}$ in [ns] <sup>5) 6)</sup>
Internal resistance of analog source	$R_{ASRC}$	—	$t_S / 500$ — 0.8	k $\Omega$	$t_S$ in [ns] <sup>2) 6)</sup>
ADC input capacitance	$C_{AIN}$	—	50	pF	<sup>6)</sup>

Notes see next page.

### Clock calculation table:

Clock Prescaler Ratio	ADCL	$t_{ADC}$	$t_S$	$t_{ADCC}$
$\div 8$	1	$8 \times t_{IN}$	$16 \times t_{IN}$	$96 \times t_{IN}$
$\div 4$	0	$4 \times t_{IN}$	$8 \times t_{IN}$	$48 \times t_{IN}$

Further timing conditions:  $t_{ADC} \text{ min} = 500 \text{ ns}$   
 $t_{IN} = 2 / f_{OSC} = 2 t_{CLCL}$

**Notes:**

- 1)  $V_{AIN}$  may exceed  $V_{AGND}$  or  $V_{AREF}$  up to the absolute maximum ratings. However, the conversion result in these cases will be  $X000_H$  or  $X3FF_H$ , respectively.
- 2) During the sample time the input capacitance  $C_{AIN}$  can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach their final voltage level within  $t_S$ . After the end of the sample time  $t_S$ , changes of the analog input voltage have no effect on the conversion result.
- 3) This parameter includes the sample time  $t_S$ , the time for determining the digital result and the time for the calibration. Values for the conversion clock  $t_{ADC}$  depend on programming and can be taken from the table on the previous page.
- 4)  $T_{UE}$  is tested at  $V_{AREF} = 5.0\text{ V}$ ,  $V_{AGND} = 0\text{ V}$ ,  $V_{CC} = 4.9\text{ V}$ . It is guaranteed by design characterization for all other voltages within the defined voltage range.  
If an overload condition occurs on maximum 2 not selected analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA, an additional conversion error of 1/2 LSB is permissible.
- 5) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference source must allow the capacitance to reach their final voltage level within the indicated time. The maximum internal resistance results from the programmed conversion timing.
- 6) Not 100% tested, but guaranteed by design characterization.

### AC Characteristics (18 MHz)

$V_{CC} = 5\text{ V} + 10\%, -15\%$ ;  $V_{SS} = 0\text{ V}$

$T_A = 0\text{ to }70\text{ }^\circ\text{C}$  for the SAB-C515A  
 $T_A = -40\text{ to }85\text{ }^\circ\text{C}$  for the SAF-C515A  
 $T_A = -40\text{ to }110\text{ }^\circ\text{C}$  for the SAH-C515A  
 $T_A = -40\text{ to }125\text{ }^\circ\text{C}$  for the SAK-C515A

( $C_L$  for port 0, ALE and PSEN outputs = 100 pF;  $C_L$  for all other outputs = 80 pF)

### Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		18 MHz Clock		Variable Clock $1/t_{CLCL} = 3.5\text{ MHz to }18\text{ MHz}$		
		min.	max.	min.	max.	
ALE pulse width	$t_{LHLL}$	71	–	$2 t_{CLCL} - 40$	–	ns
Address setup to ALE	$t_{AVLL}$	26	–	$t_{CLCL} - 30$	–	ns
Address hold after ALE	$t_{LLAX}$	26	–	$t_{CLCL} - 30$	–	ns
ALE low to valid instruction in	$t_{LLIV}$	–	122	–	$4 t_{CLCL} - 100$	ns
ALE to PSEN	$t_{LLPL}$	31	–	$t_{CLCL} - 25$	–	ns
PSEN pulse width	$t_{PLPH}$	132	–	$3 t_{CLCL} - 35$	–	ns
PSEN to valid instruction in	$t_{PLIV}$	–	92	–	$3 t_{CLCL} - 75$	ns
Input instruction hold after PSEN	$t_{PXIX}$	0	–	0	–	ns
Input instruction float after PSEN	$t_{PXIZ}^{\text{*)}$	–	46	–	$t_{CLCL} - 10$	ns
Address valid after PSEN	$t_{PXAV}^{\text{*)}$	48	–	$t_{CLCL} - 8$	–	ns
Address to valid instr in	$t_{AVIV}$	–	180	–	$5 t_{CLCL} - 98$	ns
Address float to PSEN	$t_{AZPL}$	0	–	0	–	ns

<sup>\*)</sup> Interfacing the C515A to devices with float times up to 48 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.



AC Characteristics (18 MHz, cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		18 MHz Clock		Variable Clock $1/t_{CLCL} = 3.5 \text{ MHz to } 18 \text{ MHz}$		
		min.	max.	min.	max.	
RD pulse width	$t_{RLRH}$	233	—	$6 t_{CLCL} - 100$	—	ns
WR pulse width	$t_{WLWH}$	233	—	$6 t_{CLCL} - 100$	—	ns
Address hold after ALE	$t_{LLAX2}$	81	—	$2 t_{CLCL} - 30$	—	ns
RD to valid data in	$t_{RLDV}$	—	128	—	$5 t_{CLCL} - 150$	ns
Data hold after RD	$t_{RHDX}$	0	—	0	—	ns
Data float after RD	$t_{RHDZ}$	—	51	—	$2 t_{CLCL} - 60$	ns
ALE to valid data in	$t_{LLDV}$	—	294	—	$8 t_{CLCL} - 150$	ns
Address to valid data in	$t_{AVDV}$	—	335	—	$9 t_{CLCL} - 165$	ns
ALE to WR or RD	$t_{LLWL}$	117	217	$3 t_{CLCL} - 50$	$3 t_{CLCL} + 50$	ns
Address valid to WR or RD	$t_{AVWL}$	92	—	$4 t_{CLCL} - 130$	—	ns
WR or RD high to ALE high	$t_{WHLH}$	16	96	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns
Data valid to WR transition	$t_{QVWX}$	11	—	$t_{CLCL} - 45$	—	ns
Data setup before WR	$t_{QVWH}$	239	—	$7 t_{CLCL} - 150$	—	ns
Data hold after WR	$t_{WHQX}$	16	—	$t_{CLCL} - 40$	—	ns
Address float after RD	$t_{RLAZ}$	—	0	—	0	ns

External Clock Drive Characteristics

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 18 MHz		
		min.	max.	
Oscillator period	$t_{CLCL}$	55.6	285.7	ns
High time	$t_{CHCX}$	15	$t_{CLCL} - t_{CLCX}$	ns
Low time	$t_{CLCX}$	15	$t_{CLCL} - t_{CHCX}$	ns
Rise time	$t_{CLCH}$	—	15	ns
Fall time	$t_{CHCL}$	—	15	ns

### AC Characteristics (24 MHz)

$V_{CC} = 5\text{ V} + 10\%, -15\%$ ;  $V_{SS} = 0\text{ V}$

$T_A = 0\text{ to }70\text{ }^\circ\text{C}$

for the SAB-C515A

$T_A = -40\text{ to }85\text{ }^\circ\text{C}$

for the SAF-C515A

$T_A = -40\text{ to }110\text{ }^\circ\text{C}$

for the SAH-C515A

( $C_L$  for port 0, ALE and PSEN outputs = 100 pF;  $C_L$  for all other outputs = 80 pF)

### Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		24 MHz Clock		Variable Clock $1/t_{CLCL} = 3.5\text{ MHz to }24\text{ MHz}$		
		min.	max.	min.	max.	
ALE pulse width	$t_{LHLL}$	43	–	$2 t_{CLCL} - 40$	–	ns
Address setup to ALE	$t_{AVLL}$	17	–	$t_{CLCL} - 25$	–	ns
Address hold after ALE	$t_{LLAX}$	17	–	$t_{CLCL} - 25$	–	ns
ALE low to valid instruction in	$t_{LLIV}$	–	80	–	$4 t_{CLCL} - 87$	ns
ALE to PSEN	$t_{LLPL}$	22	–	$t_{CLCL} - 20$	–	ns
PSEN pulse width	$t_{PLPH}$	95	–	$3t_{CLCL} - 30$	–	ns
PSEN to valid instruction in	$t_{PLIV}$	–	60	–	$3 t_{CLCL} - 65$	ns
Input instruction hold after PSEN	$t_{PXIX}$	0	–	0	–	ns
Input instruction float after PSEN	$t_{PXIZ}^*)$	–	32	–	$t_{CLCL} - 10$	ns
Address valid after PSEN	$t_{PXAV}^*)$	37	–	$t_{CLCL} - 5$	–	ns
Address to valid instr in	$t_{AVIV}$	–	148	–	$5 t_{CLCL} - 60$	ns
Address float to PSEN	$t_{AZPL}$	0	–	0	–	ns

<sup>\*)</sup> Interfacing the C515A to devices with float times up to 37 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

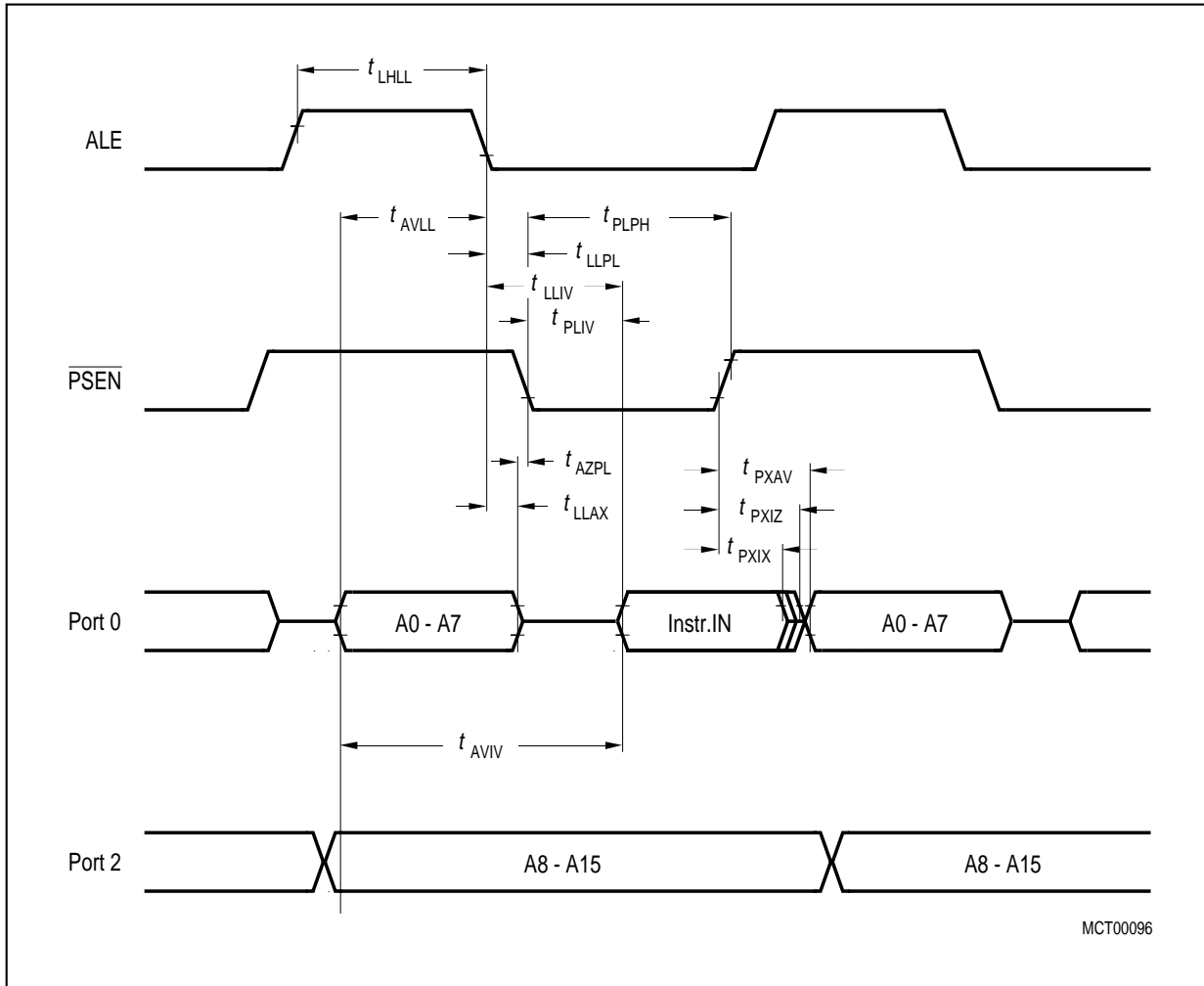
AC Characteristics (24 MHz, cont'd)

External Data Memory Characteristics

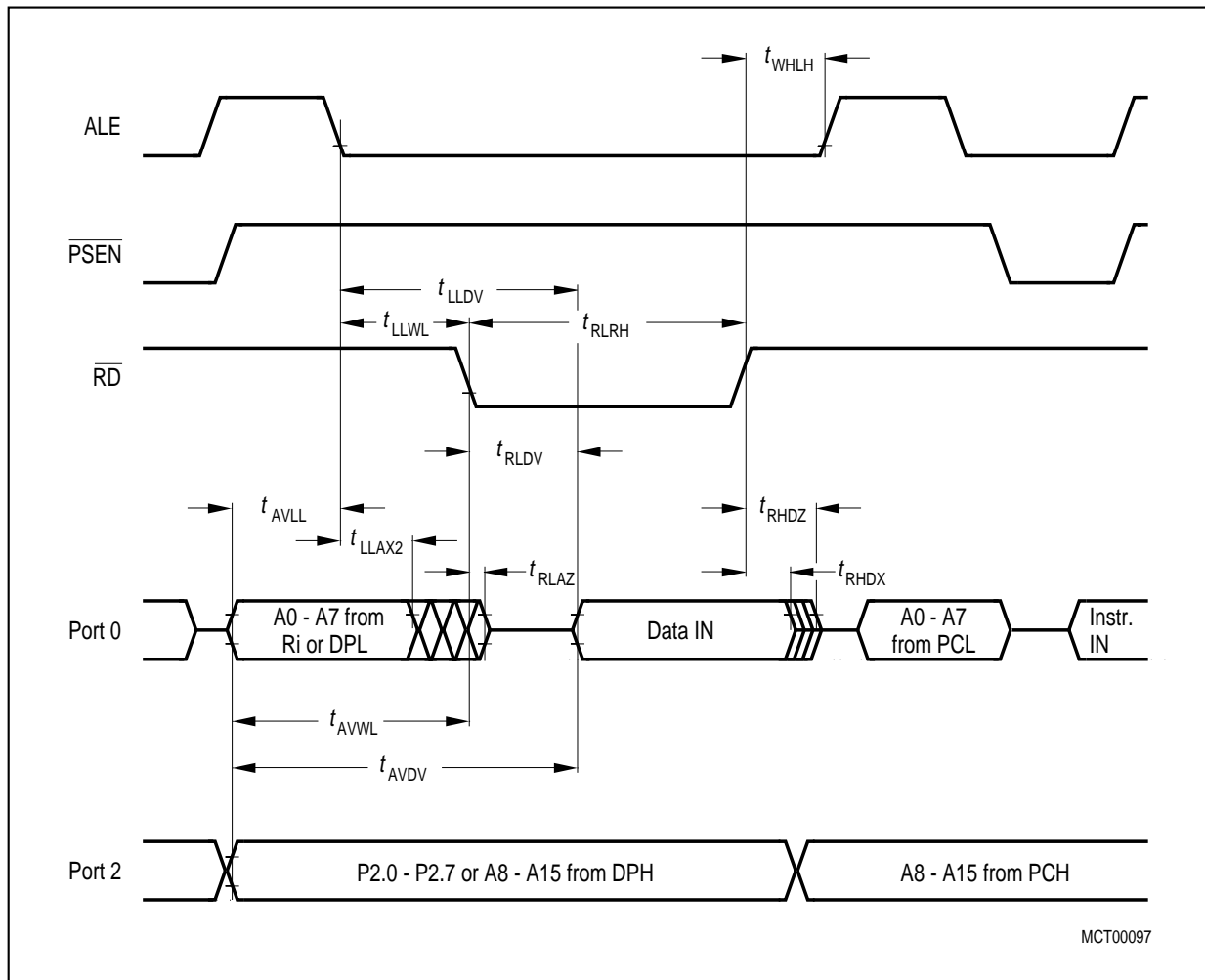
Parameter	Symbol	Limit Values				Unit
		24 MHz Clock		Variable Clock $1/t_{CLCL} = 3.5 \text{ MHz to } 24 \text{ MHz}$		
		min.	max.	min.	max.	
RD pulse width	$t_{RLRH}$	180	—	$6 t_{CLCL} - 70$	—	ns
WR pulse width	$t_{WLWH}$	180	—	$6 t_{CLCL} - 70$	—	ns
Address hold after ALE	$t_{LLAX2}$	56	—	$2 t_{CLCL} - 27$	—	ns
RD to valid data in	$t_{RLDV}$	—	118	—	$5 t_{CLCL} - 90$	ns
Data hold after RD	$t_{RHDX}$	0	—	0	—	ns
Data float after RD	$t_{RHDZ}$	—	63	—	$2 t_{CLCL} - 20$	ns
ALE to valid data in	$t_{LLDV}$	—	200	—	$8 t_{CLCL} - 133$	ns
Address to valid data in	$t_{AVDV}$	—	220	—	$9 t_{CLCL} - 155$	ns
ALE to WR or RD	$t_{LLWL}$	75	175	$3 t_{CLCL} - 50$	$3 t_{CLCL} + 50$	ns
Address valid to WR or RD	$t_{AVWL}$	67	—	$4 t_{CLCL} - 97$	—	ns
WR or RD high to ALE high	$t_{WHLH}$	17	67	$t_{CLCL} - 25$	$t_{CLCL} + 25$	ns
Data valid to WR transition	$t_{QVWX}$	5	—	$t_{CLCL} - 37$	—	ns
Data setup before WR	$t_{QVWH}$	170	—	$7 t_{CLCL} - 122$	—	ns
Data hold after WR	$t_{WHQX}$	15	—	$t_{CLCL} - 27$	—	ns
Address float after RD	$t_{RLAZ}$	—	0	—	0	ns

External Clock Drive Characteristics

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 24 MHz		
		min.	max.	
Oscillator period	$t_{CLCL}$	41.7	285.7	ns
High time	$t_{CHCX}$	12	$t_{CLCL} - t_{CLCX}$	ns
Low time	$t_{CLCX}$	12	$t_{CLCL} - t_{CHCX}$	ns
Rise time	$t_{CLCH}$	—	12	ns
Fall time	$t_{CHCL}$	—	12	ns

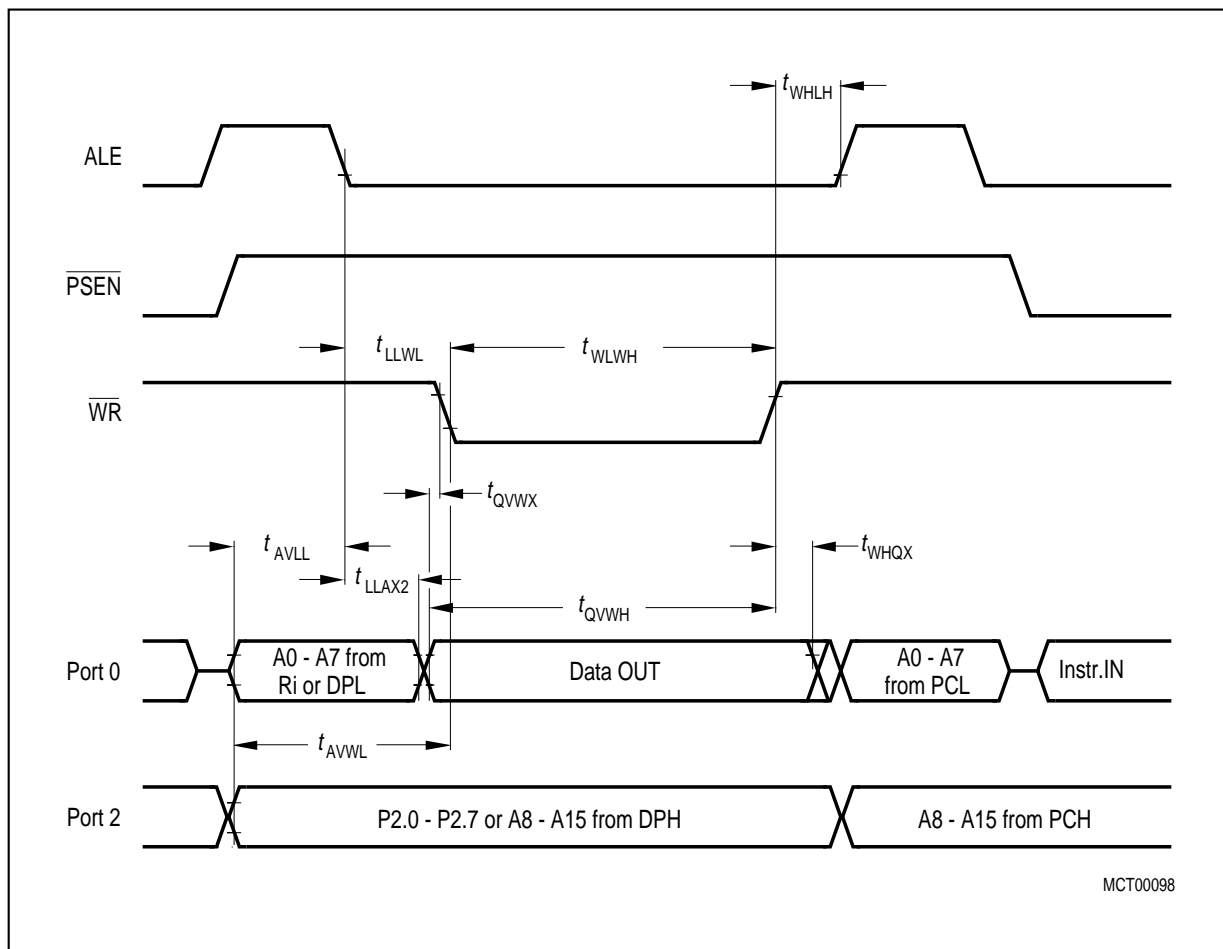


**Figure 20**  
**Program Memory Read Cycle**

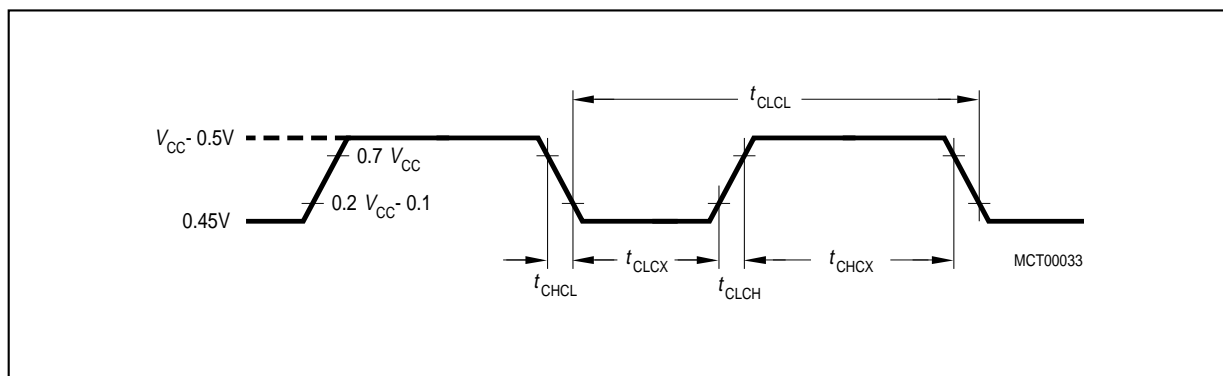


MCT00097

**Figure 21**  
Data Memory Read Cycle



**Figure 22**  
Data Memory Write Cycle



**Figure 23**  
External Clock Drive on XTAL2

ROM Verification Characteristics for the C515A-1RM

ROM Verification Mode 1

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	$t_{AVQV}$	—	$10 t_{CLCL}$	ns

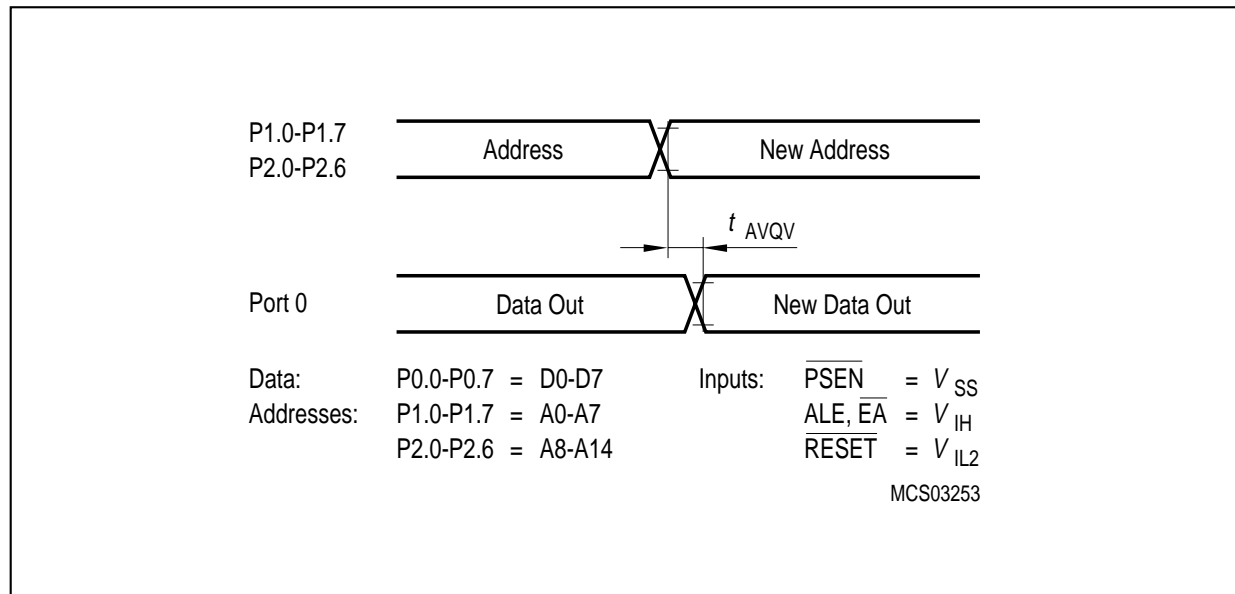


Figure 24  
ROM Verification Mode 1

ROM Verification Mode 2

Parameter	Symbol	Limit Values			Unit
		min.	typ	max.	
ALE pulse width	$t_{AWD}$	—	$2 t_{CLCL}$	—	ns
ALE period	$t_{ACY}$	—	$12 t_{CLCL}$	—	ns
Data valid after ALE	$t_{DVA}$	—	—	$4 t_{CLCL}$	ns
Data stable after ALE	$t_{DSA}$	$8 t_{CLCL}$	—	—	ns
P3.5 setup to ALE low	$t_{AS}$	—	$t_{CLCL}$	—	ns
Oscillator frequency	$1/t_{CLCL}$	3.5	—	24	MHz

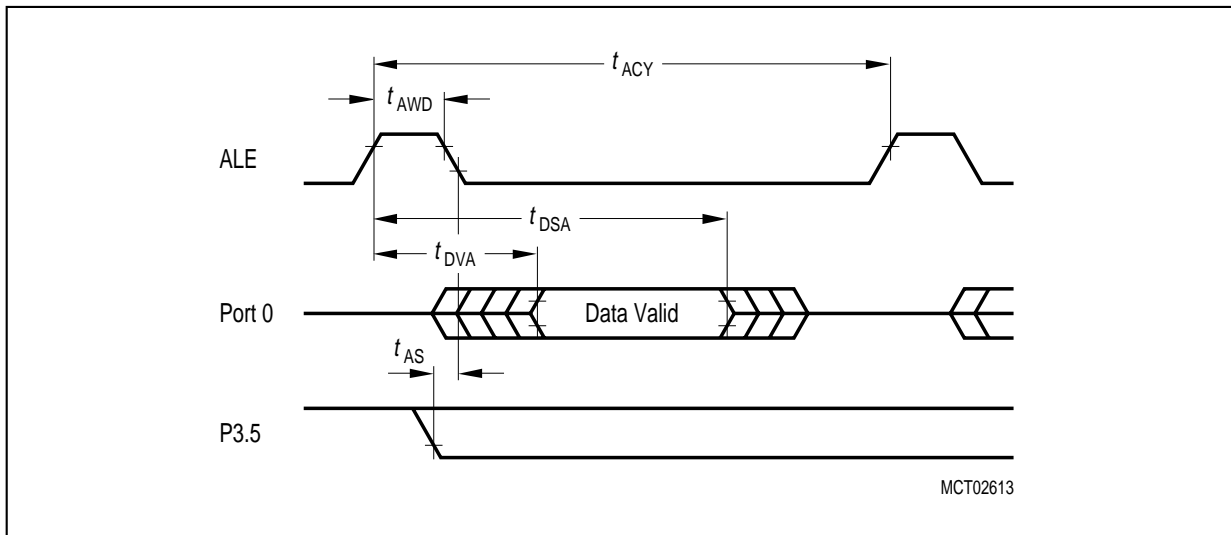
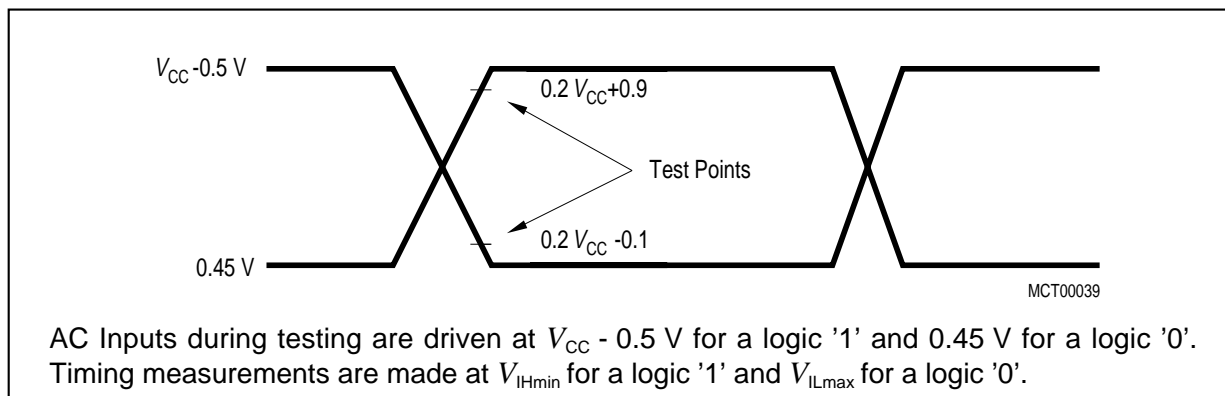
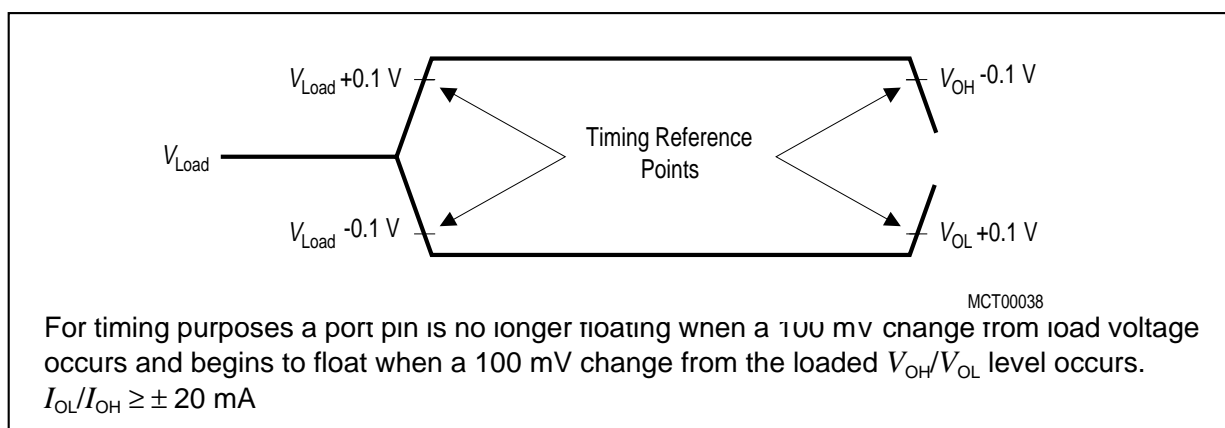


Figure 25  
ROM Verification Mode 2

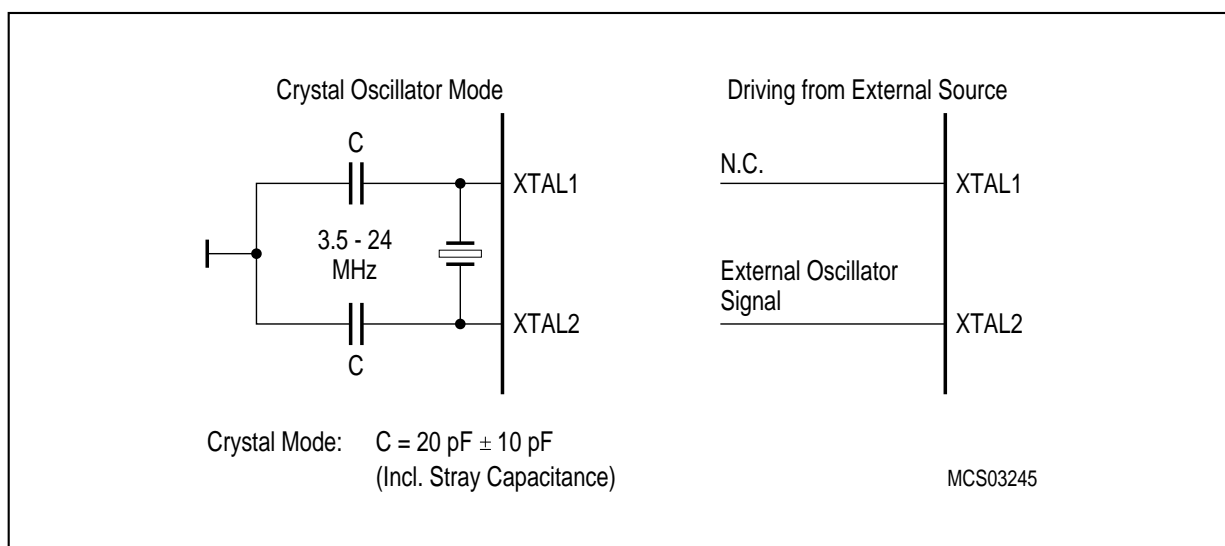




**Figure 26**  
**AC Testing: Input, Output Waveforms**



**Figure 27**  
**AC Testing : Float Waveforms**



**Figure 28**  
**Recommended Oscillator Circuits for Crystal Oscillator**

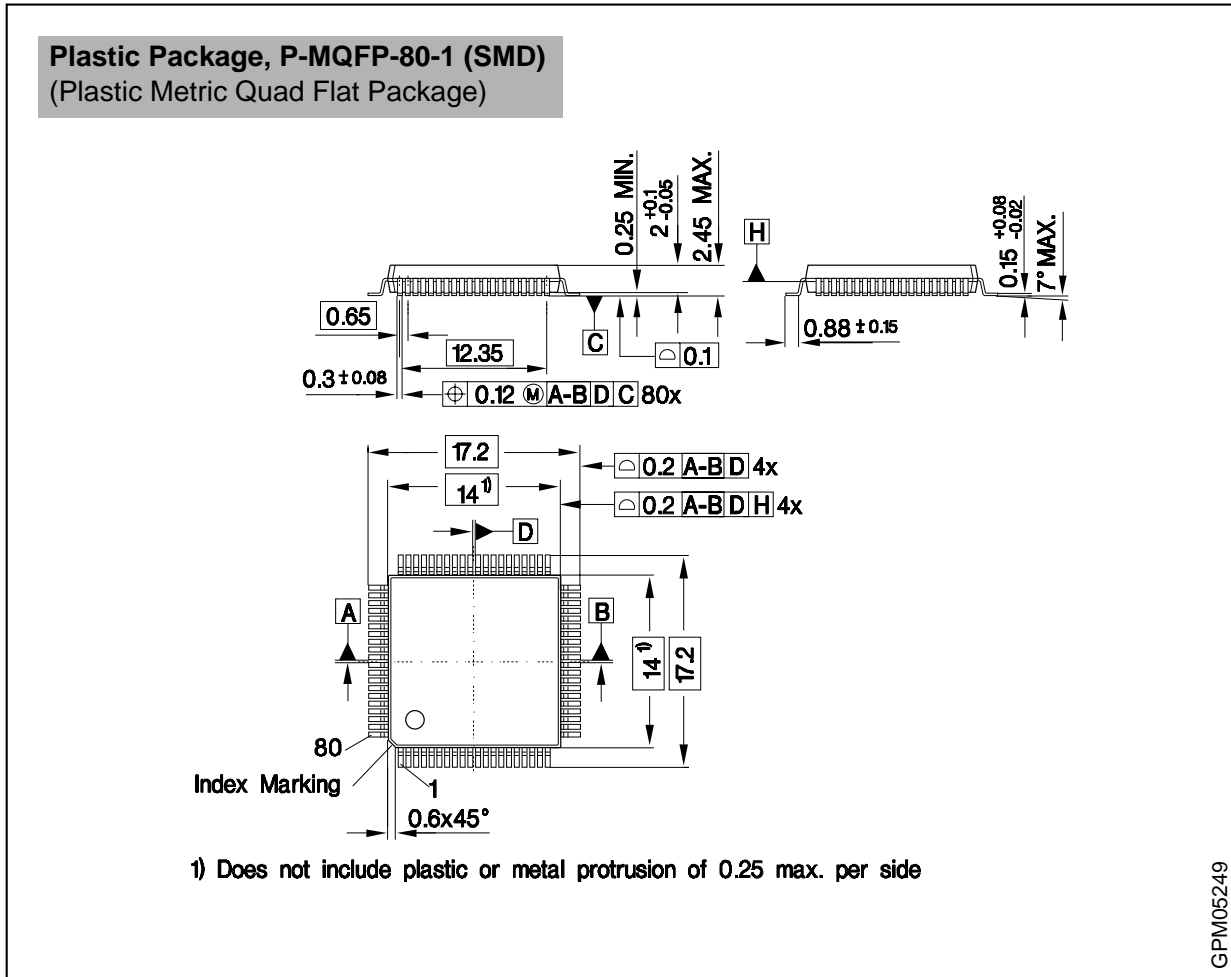


Figure 29  
 P-MQFP-80-1 Package Outline

**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information"

SMD = Surface Mounted Device

Dimensions in mm