Freescale Semiconductor
Technical Data

Document Number: MRF7S18170H
Rev. 0, 10/2006

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

MRF7S18170HR3
MRF7S18170HSR3

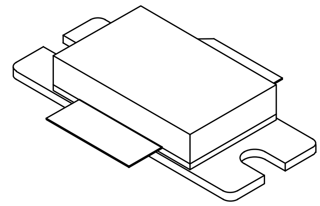
1805-1880 MHz, 50 W AVG., 28 V SINGLE W-CDMA LATERAL N-CHANNEL RF POWER MOSFETs

Designed for CDMA base station applications with frequencies from 1805 to 1880 MHz. Suitable for CDMA and multicarrier amplifier applications. To be used in Class AB and Class C for PCN-PCS/cellular radio and WLL applications.

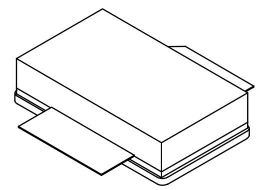
- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ} = 1400 mA, P_{out} = 50 Watts Avg., Full Frequency Band, 3GPP Test Model 1, 64 DPCH with 50% Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.
  Power Gain — 17.5 dB
  Drain Efficiency — 31%
  Device Output Signal PAR — 6.2 dB @ 0.01% Probability on CCDF
  ACPR @ 5 MHz Offset — -37 dBc in 3.84 MHz Channel Bandwidth
- Capable of Handling 5:1 VSWR, @ 32 Vdc, 1840 MHz, 170 Watts CW Peak Tuned Output Power
- P_{out} @ 1 dB Compression Point ≥ 170 Watts CW

Features

- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.



CASE 465B-03, STYLE 1
NI-880
MRF7S18170HR3



CASE 465C-02, STYLE 1
NI-880S
MRF7S18170HSR3

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 84°C, 170 W CW Case Temperature 79°C, 50 W CW	$R_{\theta JC}$	 0.27 0.30	°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	IA (Minimum)
Machine Model (per EIA/JESD22-A115)	B (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 372 μAdc)	$V_{GS(th)}$	1.2	2	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 1400 mAdc)	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage (1) (V_{DS} = 28 Vdc, I_D = 1400 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	4	5.4	7.6	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 3.72 Adc)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc
Dynamic Characteristics (2)					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	0.87	—	pF
Output Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	703	—	pF

Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, P_{out} = 50 W Avg., f = 1807.5 MHz and f = 1877.5 MHz, Single-Carrier W-CDMA, 3GPP Test Model 1, 64 DPCH, 50% Clipping, PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

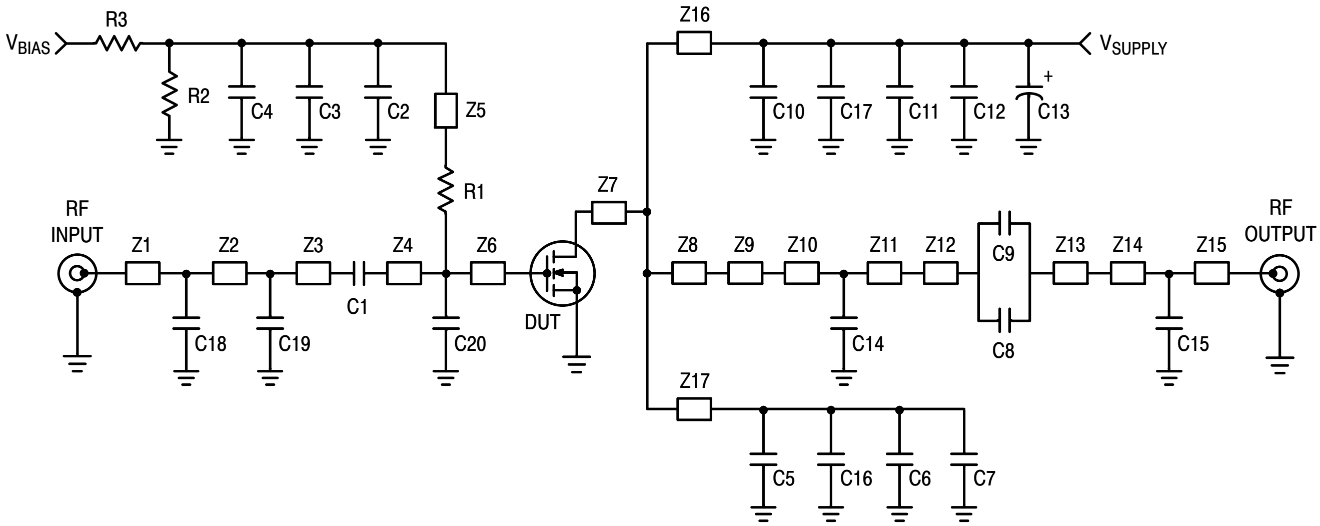
Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	G_{ps}	16	17.5	19	dB
Drain Efficiency	η_D	29	31	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR				dB
MRF7S18170HR3		5.8	6.2	—	
MRF7S18170HSR3		5.7	6.2	—	
Adjacent Channel Power Ratio	ACPR	—	-37	-35	dBc
Input Return Loss	IRL	—	-15	-9	dB

1. V_{GG} = 2 x $V_{GS(Q)}$. Parameter measured on Freescale Test Fixture, due to resistive divider network on the board. Refer to Test Circuit schematic.
2. Part internally matched both on input and output.

(continued)

Table 4. Electrical Characteristics (T_C = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, 1805-1880 MHz Bandwidth					
Video Bandwidth (Tone Spacing from 100 kHz to VBW) ΔIMD3 = IMD3 @ VBW frequency - IMD3 @ 100 kHz <1 dBc (both sidebands)	VBW	—	25	—	MHz
Gain Flatness in 75 MHz Bandwidth @ P_{out} = 170 W CW	G_F	—	0.4	—	dB
Deviation from Linear Phase in 75 MHz Bandwidth @ P_{out} = 170 W CW	Φ	—	2.5	—	°
Group Delay @ P_{out} = 170 W CW, f = 1840 MHz	Delay	—	4.2	—	ns
Part-to-Part Insertion Phase Variation @ P_{out} = 170 W CW, f = 1840 MHz	ΔΦ	—	15	—	°
Gain Variation over Temperature	ΔG	—	0.015	—	dB/°C
Output Power Variation over Temperature	ΔP1dB	—	0.01	—	dBm/°C



Z1	0.410″ x 0.083″ Microstrip		Z10*	0.900″ x 0.161″ Microstrip
Z2*	0.480″ x 0.083″ Microstrip		Z11*	0.140″ x 0.161″ Microstrip
Z3*	0.710″ x 0.083″ Microstrip		Z12	0.094″ x 0.220″ Microstrip
Z4	0.180″ x 0.147″ Microstrip		Z13	0.070″ x 0.220″ Microstrip
Z5	0.850″ x 0.091″ Microstrip		Z14*	0.140″ x 0.083″ Microstrip
Z6	0.383″ x 1.109″ Microstrip		Z15*	0.160″ x 0.083″ Microstrip
Z7	1.110″ x 1.360″ Microstrip		Z16, Z17	1.120″ x 0.080″ Microstrip
Z8	0.480″ x 1.360″ Microstrip		PCB	Taconic TLX8-0300, 0.030″, ε_r = 2.55
Z9	0.060″ x 1.098″ Microstrip			

* Variable for tuning

Figure 1. MRF7S18170HR3 Test Circuit Schematic — NI-880

Table 5. MRF7S18170HR3 Test Circuit Component Designations and Values — NI-880

Part	Description	Part Number	Manufacturer
C1	0.8 pF Chip Capacitor	100B0R8BW	ATC
C2, C8, C9	6.8 pF Chip Capacitors	100B6R8BW	ATC
C3	100 pF Chip Capacitor	100B101JW	ATC
C4	100 nF Chip Capacitor	100B104JW	ATC
C5, C10	5.6 pF Chip Capacitors	100B5R6BW	ATC
C6, C7, C11, C12	10 μF Chip Capacitors	C5750X5R1H106MT	TDK
C13	470 μF, 63 V Electrolytic Capacitor, Radial	13661471	Philips
C14	0.5 pF Chip Capacitor	600B0R5BW	ATC
C15, C20	0.2 pF Chip Capacitors	100B0R2BW	ATC
C16, C17	4.7 pF Chip Capacitors	100B4R7BW	ATC
C18	2 pF Chip Capacitor	600B2R0BW	ATC
C19	0.3 pF Chip Capacitor	100B0R3BW	ATC
R1	10 Ω, 1/4 W Chip Resistor	232272461009	Phycomp
R2, R3	10 kΩ, 1/4 W Chip Resistors	232272461003	Phycomp

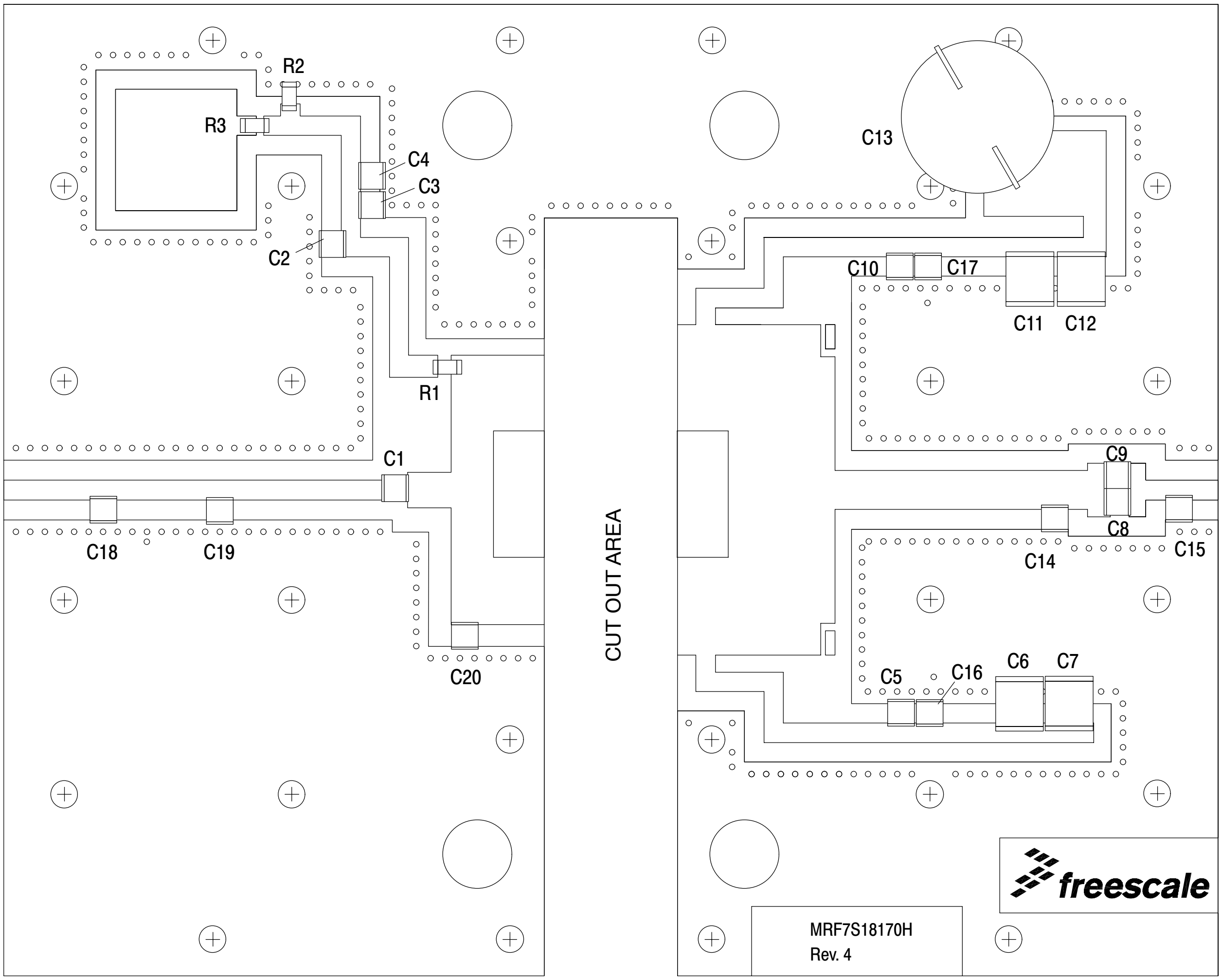
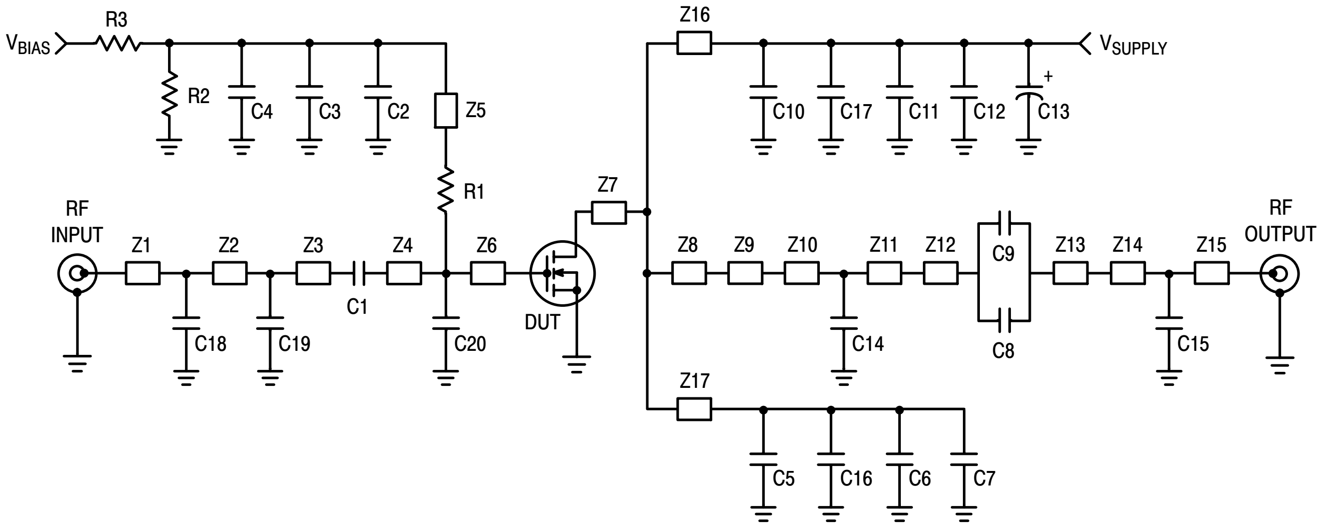


Figure 2. MRF7S18170HR3 Test Circuit Component Layout — NI-880



Z1*	0.500″ x 0.083″ Microstrip	Z10*	0.900″ x 0.161″ Microstrip
Z2*	0.290″ x 0.083″ Microstrip	Z11*	0.140″ x 0.161″ Microstrip
Z3*	0.810″ x 0.083″ Microstrip	Z12	0.094″ x 0.220″ Microstrip
Z4	0.180″ x 0.147″ Microstrip	Z13	0.070″ x 0.220″ Microstrip
Z5	0.850″ x 0.091″ Microstrip	Z14*	0.140″ x 0.083″ Microstrip
Z6	0.383″ x 1.109″ Microstrip	Z15*	0.160″ x 0.083″ Microstrip
Z7	1.110″ x 1.360″ Microstrip	Z16, Z17	1.120″ x 0.080″ Microstrip
Z8	0.480″ x 1.360″ Microstrip	PCB	Taconic TLX8-0300, 0.030″, ε_r = 2.55
Z9	0.060″ x 1.098″ Microstrip		

* Variable for tuning

Figure 3. MRF7S18170HSR3 Test Circuit Schematic — NI-880S

Table 6. MRF7S18170HSR3 Test Circuit Component Designations and Values — NI-880S

Part	Description	Part Number	Manufacturer
C1	0.8 pF Chip Capacitor	100B0R8BW	ATC
C2, C8, C9	6.8 pF Chip Capacitors	100B6R8BW	ATC
C3	100 pF Chip Capacitor	100B101JW	ATC
C4	100 nF Chip Capacitor	100B104JW	ATC
C5, C10	5.6 pF Chip Capacitors	100B5R6BW	ATC
C6, C7, C11, C12	10 μF Chip Capacitors	C5750X5R1H106MT	TDK
C13	470 μF, 63 V Electrolytic Capacitor, Radial	13661471	Philips
C14	0.5 pF Chip Capacitor	600B0R5BW	ATC
C15	0.2 pF Chip Capacitor	100B0R2BW	ATC
C16, C17	4.7 pF Chip Capacitors	100B4R7BW	ATC
C18	2 pF Chip Capacitor	600B2R0BW	ATC
C19	0.3 pF Chip Capacitor	100B0R3BW	ATC
C20	0.1 pF Chip Capacitor	100B0R2BW	ATC
R1	10 Ω, 1/4 W Chip Resistor	232272461003	Phycomp
R2, R3	10 kΩ, 1/4 W Chip Resistors	232272461009	Phycomp

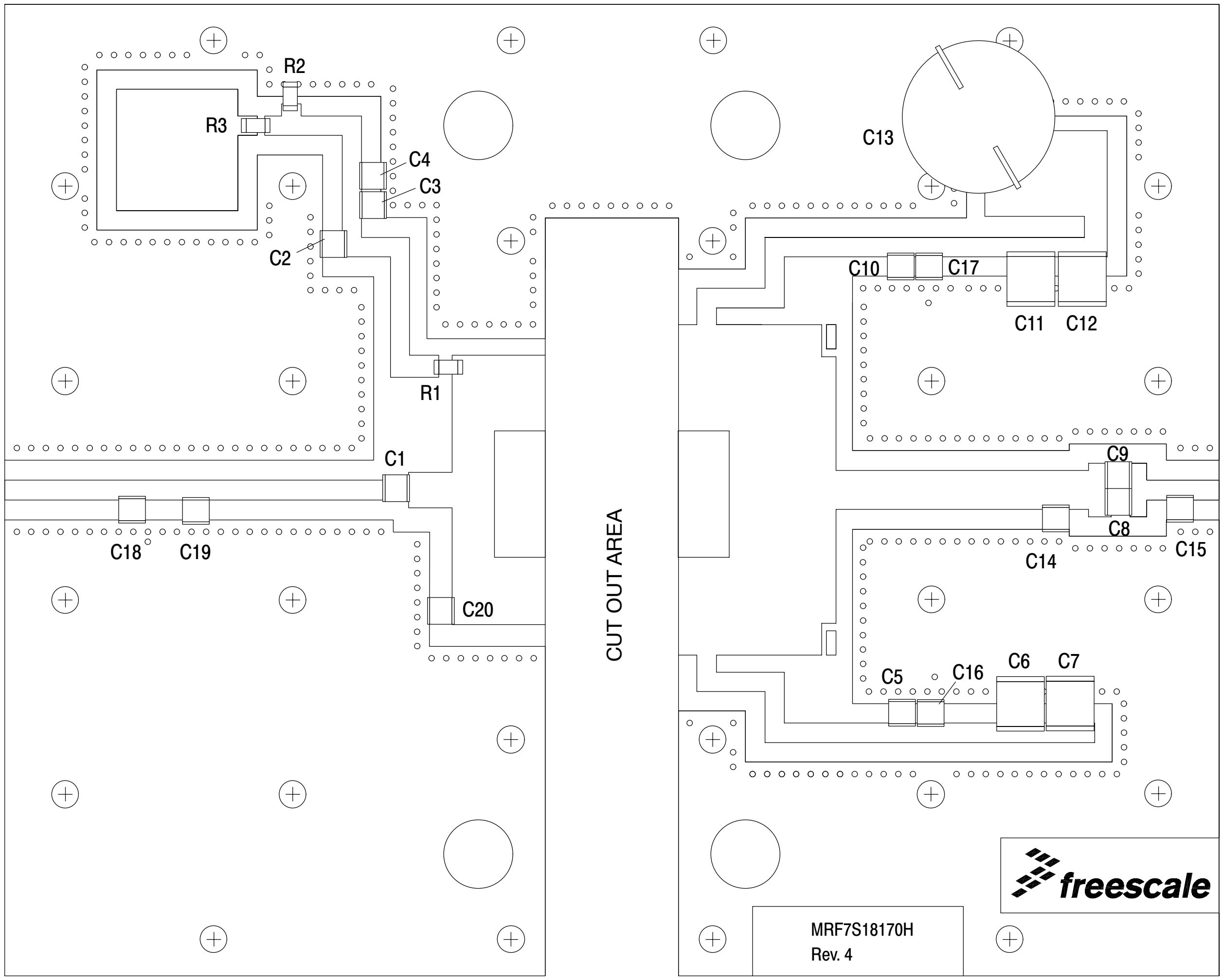


Figure 4. MRF7S18170HSR3 Test Circuit Component Layout — NI-880S

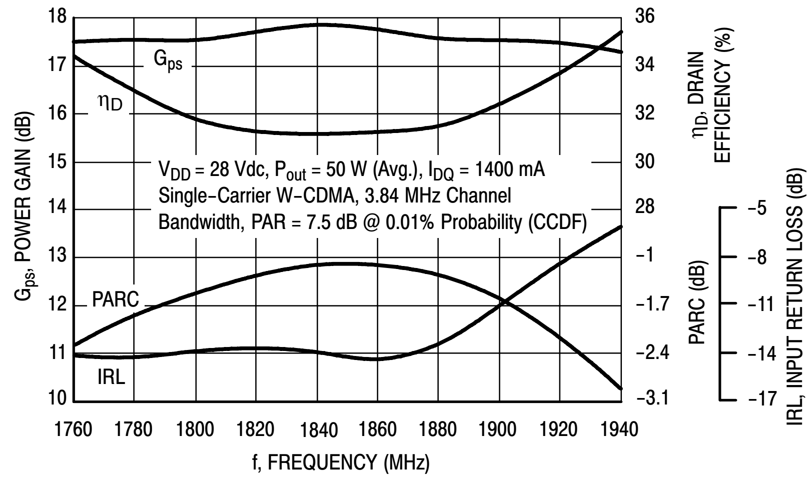


Figure 5. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 50 Watts Avg.

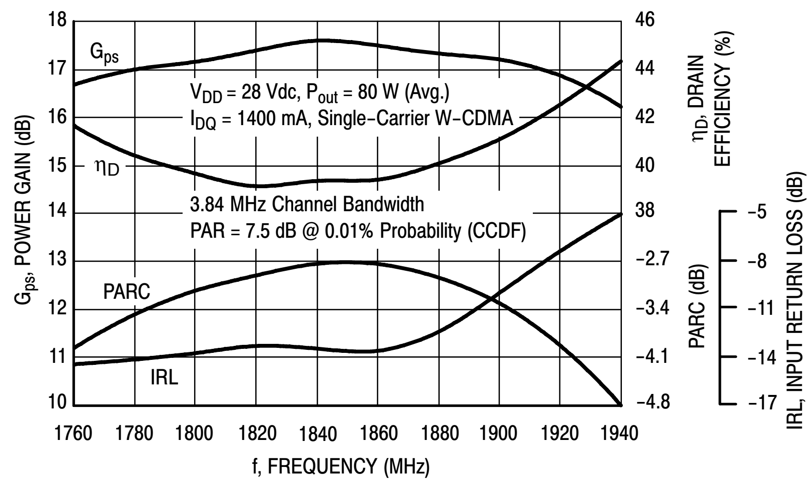


Figure 6. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 80 Watts Avg.

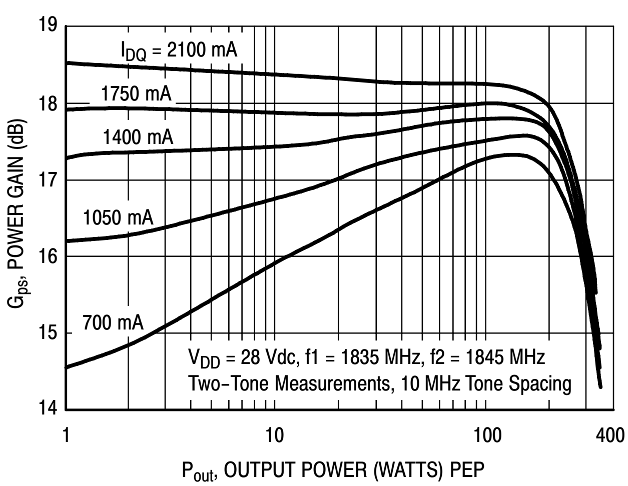


Figure 7. Two-Tone Power Gain versus Output Power

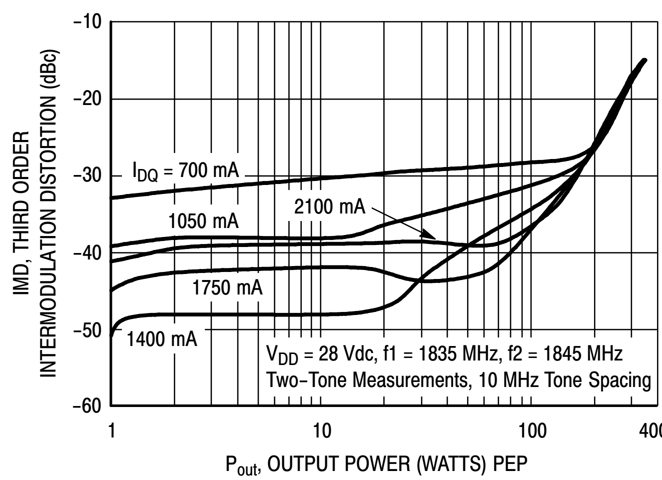


Figure 8. Third Order Intermodulation Distortion versus Output Power

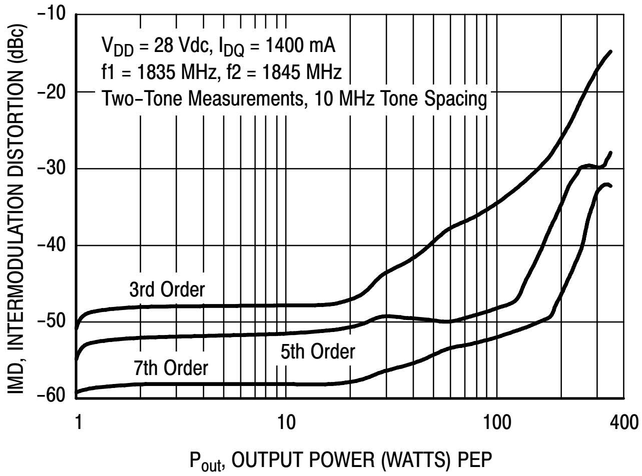


Figure 9. Intermodulation Distortion Products versus Output Power

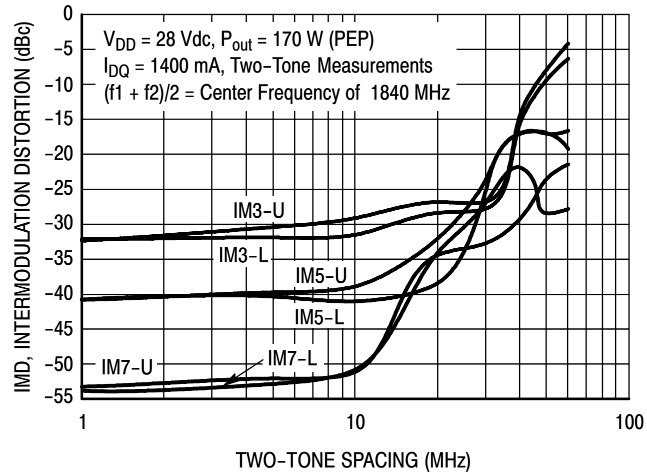


Figure 10. Intermodulation Distortion Products versus Tone Spacing

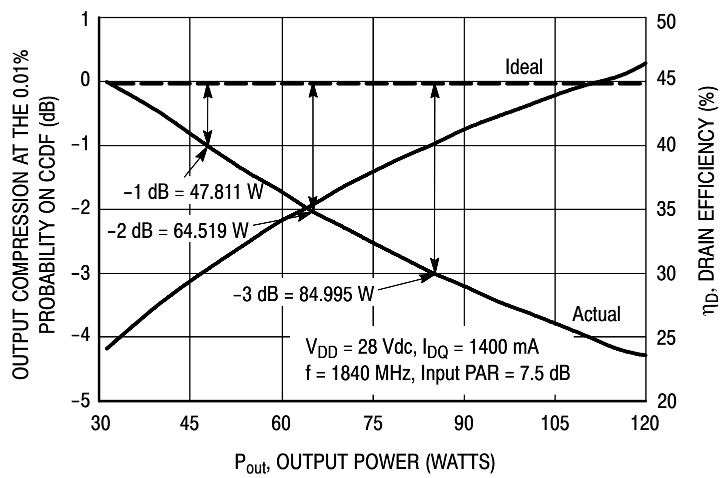


Figure 11. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

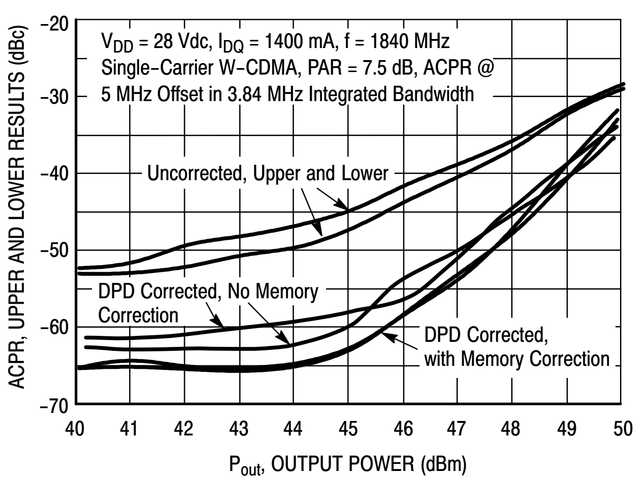


Figure 12. Digital Predistortion Correction versus ACPR and Output Power

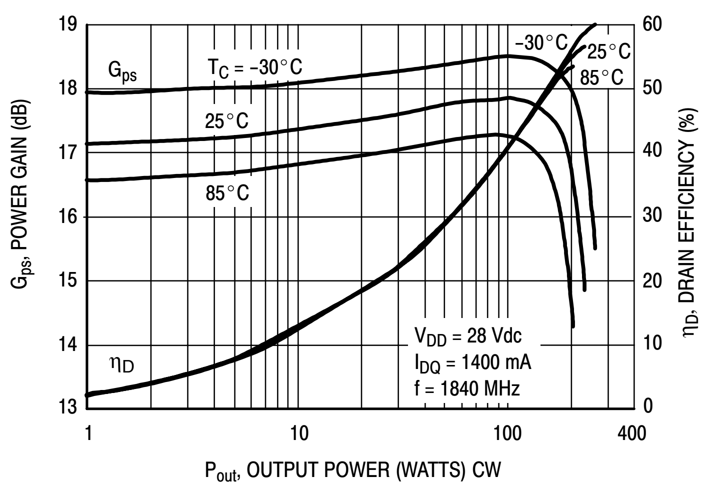


Figure 13. Power Gain and Drain Efficiency versus CW Output Power

TYPICAL CHARACTERISTICS

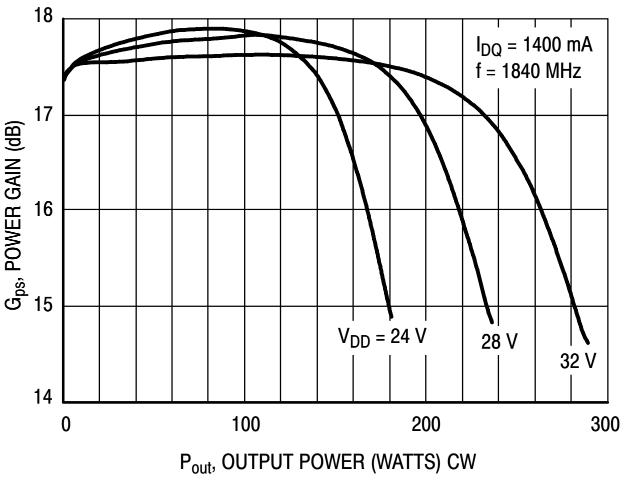
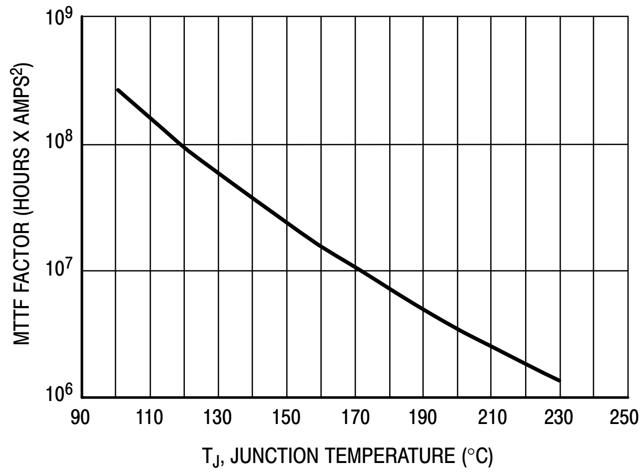


Figure 14. Power Gain versus Output Power



This above graph displays calculated MTTF in hours x ampere^2 drain current. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTTF factor by I_D^2 for MTTF in a particular application.

Figure 15. MTTF Factor versus Junction Temperature

W-CDMA TEST SIGNAL

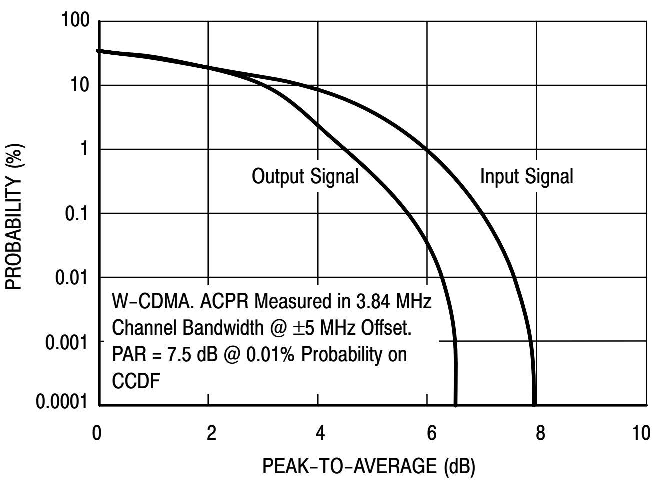


Figure 16. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 50% Clipping, Single-Carrier Test Signal

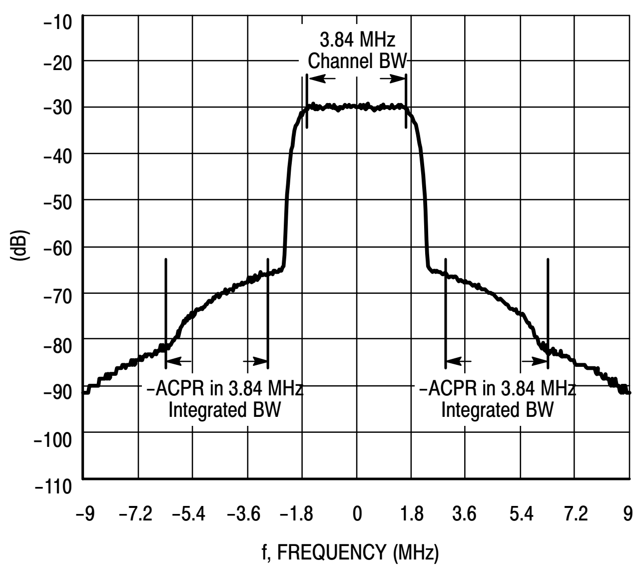
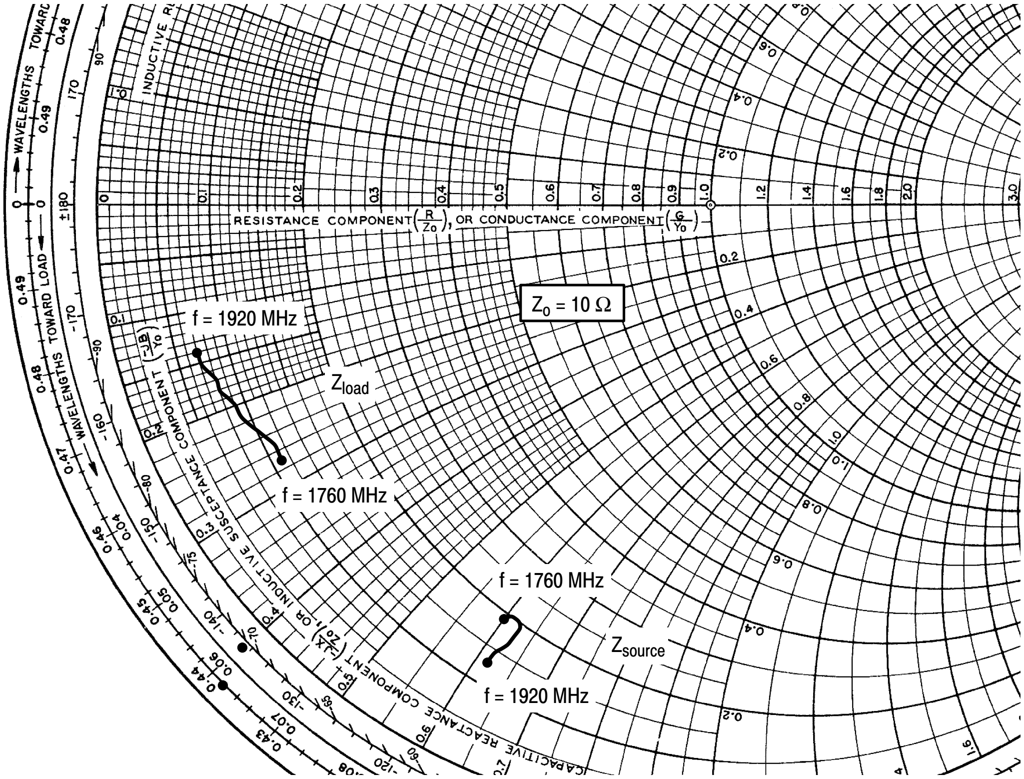


Figure 17. Single-Carrier W-CDMA Spectrum



$V_{DD} = 28$ Vdc, $I_{DQ} = 1400$ mA, $P_{out} = 50$ W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
1760	1.93 - j6.00	1.13 - j2.65
1780	1.95 - j6.10	1.05 - j2.45
1800	1.99 - j6.18	0.97 - j2.29
1820	1.95 - j6.22	0.90 - j2.12
1840	1.85 - j6.30	0.85 - j2.00
1860	1.71 - j6.26	0.81 - j1.84
1880	1.55 - j6.25	0.75 - j1.70
1900	1.39 - j6.20	0.70 - j1.54
1920	1.23 - j6.15	0.67 - j1.38

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

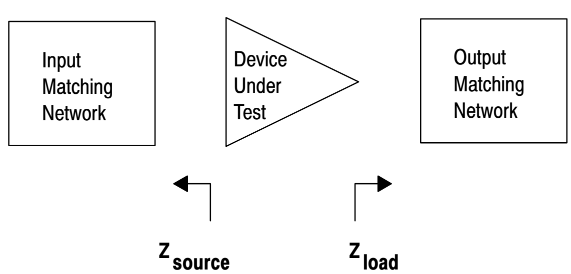
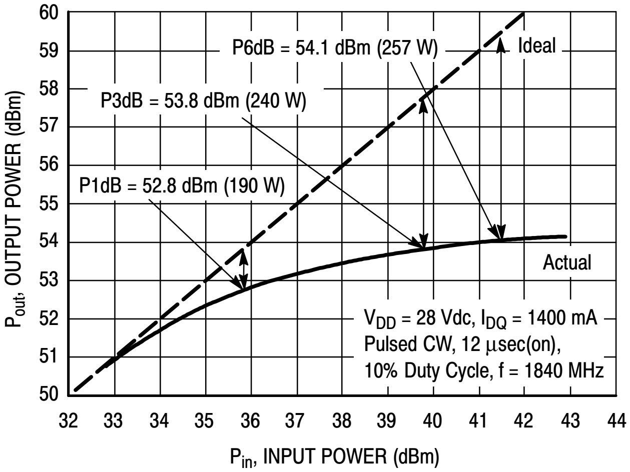


Figure 18. Series Equivalent Source and Load Impedance

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS

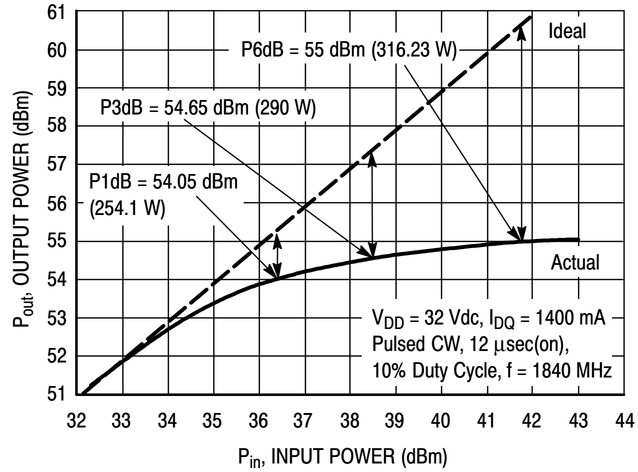


NOTE: Measured in a Peak Tuned Load Pull Fixture

Test Impedances per Compression Level

	Z_{source} Ω	Z_{load} Ω
3dB	1.23 - j7.91	0.88 - j2.81

Figure 19. Pulsed CW Output Power versus Input Power



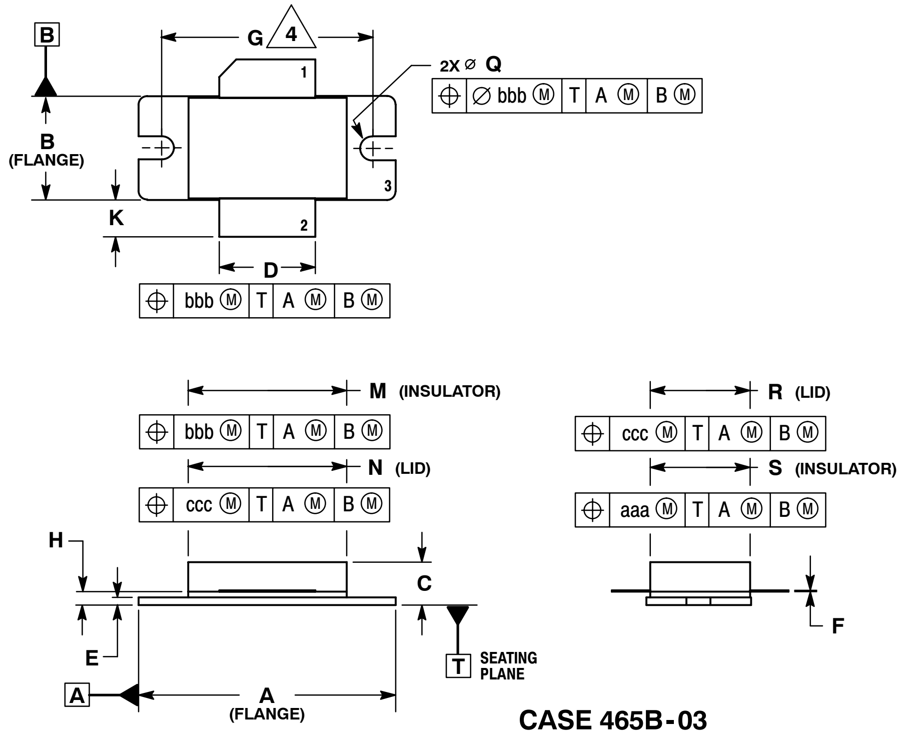
NOTE: Measured in a Peak Tuned Load Pull Fixture

Test Impedances per Compression Level

	Z_{source} Ω	Z_{load} Ω
P3dB	1.23 - j7.91	1.03 - j2.65

Figure 20. Pulsed CW Output Power versus Input Power

PACKAGE DIMENSIONS

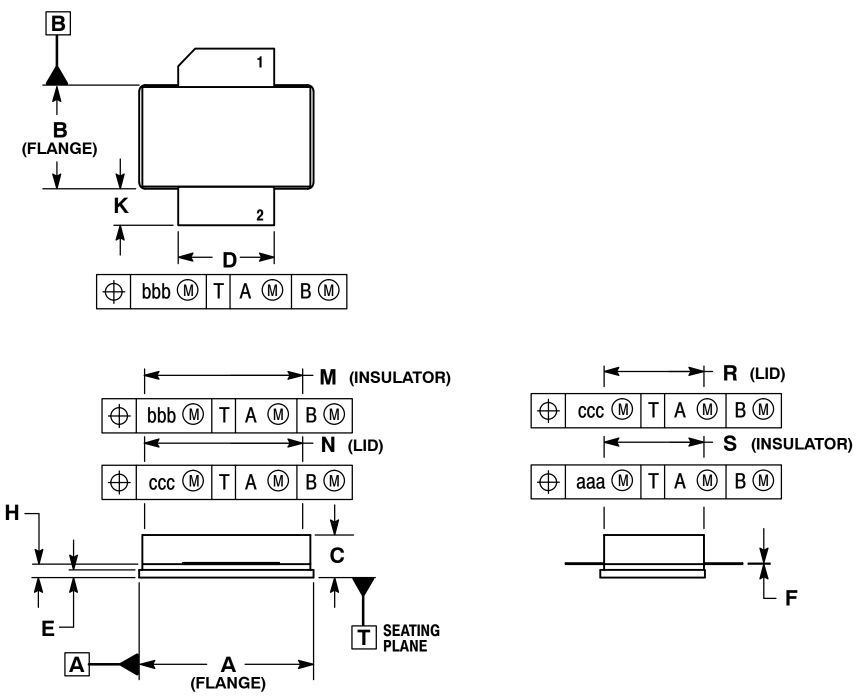


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M−1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
4. RECOMMENDED BOLT CENTER DIMENSION OF 1.16 (29.57) BASED ON M3 SCREW.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.335	1.345	33.91	34.16
B	0.535	0.545	13.6	13.8
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.175	0.205	4.44	5.21
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
Q	Ø.118	Ø.138	Ø3.00	Ø3.51
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007 REF		0.178 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465B-03
ISSUE D
NI-880
MRF7S18170HR3



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M−1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.905	0.915	22.99	23.24
B	0.535	0.545	13.60	13.80
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007 REF		0.178 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465C-02
ISSUE D
NI-880S
MRF7S18170HSR3

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Oct. 2006	• Initial Release of Data Sheet

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