

**1M × 16-Bit Dynamic RAM  
1k Refresh  
(Hyper Page Mode-EDO)**

**HYB 5118165BSJ/BST-50/-60  
HYB 3118165BSJ/BST-50/-60**

**Advanced Information**

- 1 048 576 words by 16-bit organization
- 0 to 70 °C operating temperature
- Hyper Page Mode-EDO-operation
- Performance:

		-50	-60	
$t_{\text{RAC}}$	$\overline{\text{RAS}}$ access time	50	60	ns
$t_{\text{CAC}}$	$\overline{\text{CAS}}$ access time	13	15	ns
$t_{\text{AA}}$	Access time from address	25	30	ns
$t_{\text{RC}}$	Read/Write cycle time	84	104	ns
$t_{\text{HPC}}$	Hyper page mode (EDO) cycle time	20	25	ns

- Power Dissipation, Refresh & Addressing:

	HYB5118165		HYB3118165		
	-50	-60	-50	-60	
Power Supply	5 V ± 10 %		3.3 V ± 0.3 V		
Addressing	10/10		10/10		
Refresh	1024 cycles / 16 ms				
Active	715	632	468	414	mW
TTL Standby	11		7.2		mW
CMOS Standby	5.5		3.6		mW

- Read, write, read-modify-write,  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh,  $\overline{\text{RAS}}$ -only refresh and hidden refresh
- All inputs, outputs and clocks fully TTL (5 V versions) and LV-TTL (3.3 V version)-compatible
- Plastic Package: P-SOJ-42-1      400 mil  
P-TSOPII-50/44-1 400 mil

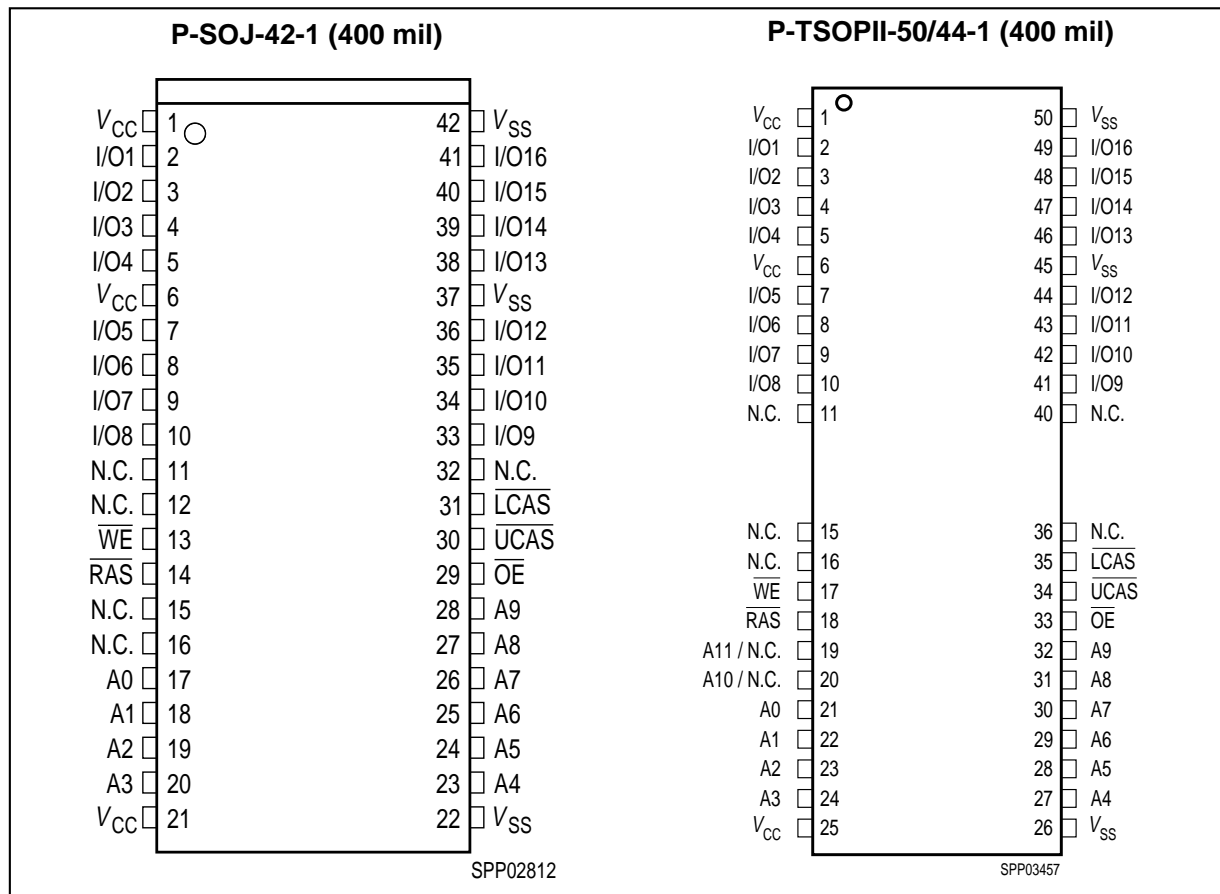
The HYB 5(3)118165 are 16 MBit dynamic RAMs based on die revisions "G" & "F" and organized as 1 048 576 words by 16-bits. The HYB 5(3)118165 utilizes a submicron CMOS silicon gate process technology, as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 5(3)118165 to be packaged in a standard SOJ-42 and TSOPII-50/44 plastic package with 400 mil width. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment.

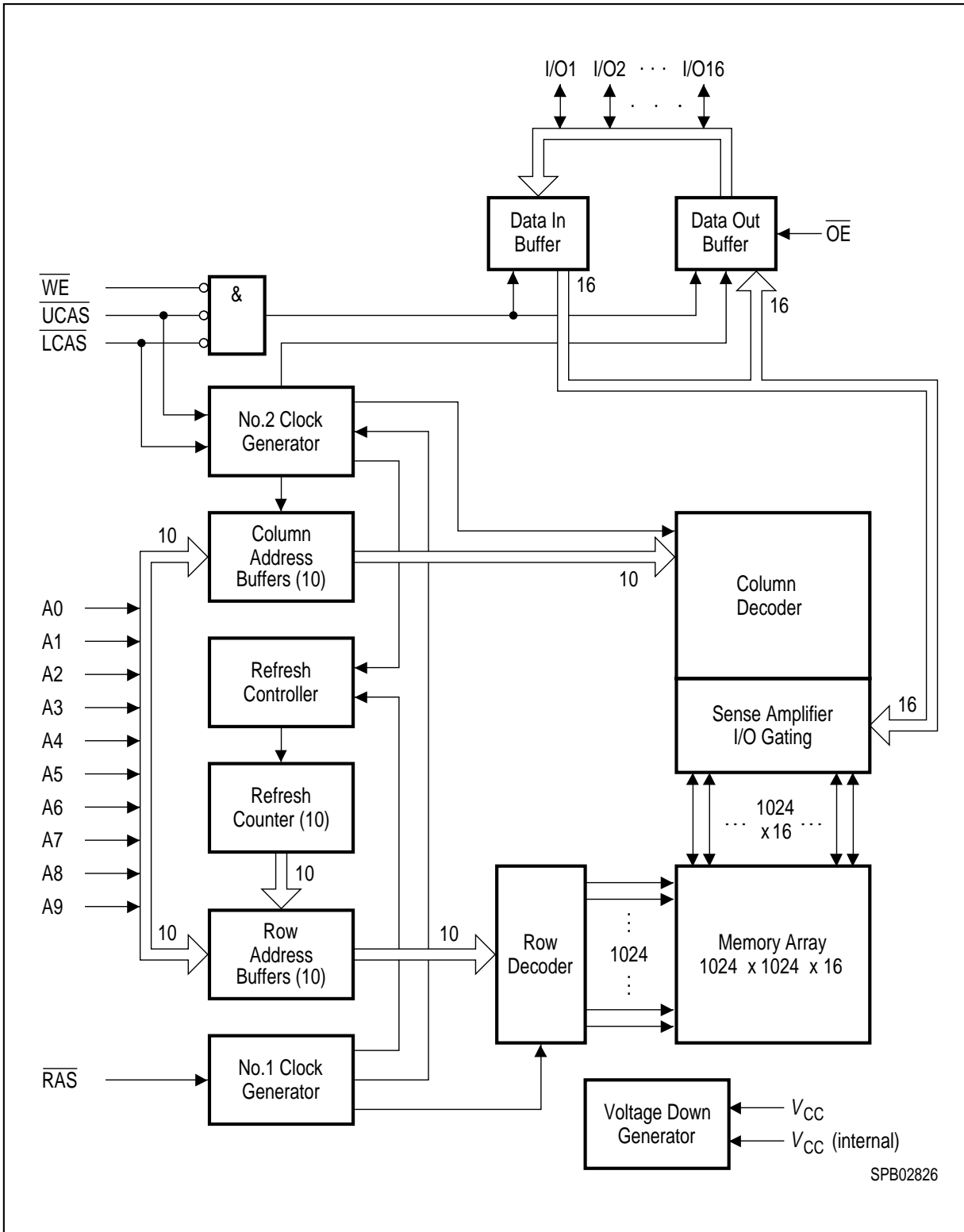
**Ordering Information**

Type	Ordering Code	Package	Descriptions
HYB 5118165BSJ-50	Q67100-Q1107	P-SOJ-42-1 400 mil	5 V 50 ns EDO-DRAM
HYB 5118165BSJ-60	Q67100-Q1108	P-SOJ-42-1 400 mil	5 V 60 ns EDO-DRAM
HYB 3118165BSJ-50	on request	P-SOJ-42-1 400 mil	3.3 V 50 ns EDO-DRAM
HYB 3118165BSJ-60	on request	P-SOJ-42-1 400 mil	3.3 V 60 ns EDO-DRAM
HYB 5118165BST-50	on request	P-TSOPII-50/44-1 400 mil	5 V 50 ns EDO-DRAM
HYB 5118165BST-60	on request	P-TSOPII-50/44-1 400 mil	5 V 60 ns EDO-DRAM
HYB 3118165BST-50	on request	P-TSOPII-50/44-1 400 mil	3.3 V 50 ns EDO-DRAM
HYB 3118165BST-60	on request	P-TSOPII-50/44-1 400 mil	3.3 V 60 ns EDO-DRAM

### Pin Names and Configuration

	<b>HYB 5(3)118165</b>
Row Address Inputs	A0 - A9
Column Address Inputs	A0 - A9
Row Address Strobe	$\overline{\text{RAS}}$
Upper Column Address Strobe	UCAS
Lower Column Address Strobe	LCAS
Output Enable	$\overline{\text{OE}}$
Data Input/Output	I/O1 - I/O16
Read/Write Input	$\overline{\text{WE}}$
Power Supply	$V_{\text{CC}}$
Ground (0 V)	$V_{\text{SS}}$
Not Connected	N.C.





**Block Diagram for HYB 5118165BSJ**

### Absolute Maximum Ratings

Operating temperature range .....	0 to 70 °C
Storage temperature range.....	– 55 to 150 °C
Input/output voltage (5 V versions) .....	– 0.5 to min ( $V_{CC} + 0.5$ , 7.0) V
Input/output voltage (3.3 V versions) .....	– 0.5 to min ( $V_{CC} + 0.5$ , 4.6) V
Power supply voltage (5 V versions) .....	– 1.0 V to 7.0 V
Power supply voltage (3.3 V versions) .....	– 1.0 V to 4.6 V
Power dissipation (5 V versions) .....	1.0 W
Power dissipation (3.3 V versions) .....	0.5 W
Data out current (short circuit) .....	50 mA

*Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

### DC Characteristics

$T_A = 0$  to 70 °C,  $V_{SS} = 0$  V,  $t_T = 2$  ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		

#### 5 V Versions

Power supply voltage	$V_{CC}$	4.5	5.5	V	
Input high voltage	$V_{IH}$	2.4	$V_{CC} + 0.5$	V	<sup>1</sup>
Input low voltage	$V_{IL}$	– 0.5	0.8	V	<sup>1</sup>
Output high voltage ( $I_{OUT} = -5$ mA)	$V_{OH}$	2.4	–	V	<sup>1</sup>
Output low voltage ( $I_{OUT} = 4.2$ mA)	$V_{OL}$	–	0.4	V	<sup>1</sup>

#### 3.3 V Versions

Power supply voltage	$V_{CC}$	3.0	3.6	V	
Input high voltage	$V_{IH}$	2.0	$V_{CC} + 0.5$	V	<sup>1</sup>
Input low voltage	$V_{IL}$	– 0.5	0.8	V	<sup>1</sup>
TTL Output high voltage ( $I_{OUT} = -2$ mA)	$V_{OH}$	2.4	–	V	<sup>1</sup>
TTL Output low voltage ( $I_{OUT} = 2$ mA)	$V_{OL}$	–	0.4	V	<sup>1</sup>
CMOS Output high voltage ( $I_{OUT} = -100$ μA)	$V_{OH}$	$V_{CC} - 0.2$	–	V	
CMOS Output low voltage ( $I_{OUT} = 100$ μA)	$V_{OL}$	–	0.2	V	

#### DC Characteristics (cont'd)

$T_A = 0$  to  $70$  °C,  $V_{SS} = 0$  V,  $t_T = 2$  ns

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
<b>Common Parameters</b>					
Input leakage current ( $0 \text{ V} \leq V_{IH} \leq V_{CC} + 0.3 \text{ V}$ , all other pins = 0 V)	$I_{I(L)}$	- 10	10	$\mu\text{A}$	1
Output leakage current (DO is disabled, $0 \text{ V} \leq V_{OUT} \leq V_{CC} + 0.3 \text{ V}$ )	$I_{O(L)}$	- 10	10	$\mu\text{A}$	1
Average $V_{CC}$ supply current -50 ns version -60 ns version ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , address cycling: $t_{RC} = t_{RC \text{ MIN.}}$ )	$I_{CC1}$	-	130 115	mA mA	2, 3, 4 2, 3, 4
Standby $V_{CC}$ supply current ( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$ )	$I_{CC2}$	-	2	mA	-
Average $V_{CC}$ supply current, during $\overline{\text{RAS}}$ -only refresh cycles -50 ns version -60 ns version ( $\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH}$ , $t_{RC} = t_{RC \text{ MIN.}}$ )	$I_{CC3}$	-	130 115	mA mA	2, 4 2, 4
Average $V_{CC}$ supply current, during hyper page mode (EDO) -50 ns version -60 ns version ( $\overline{\text{RAS}} = V_{IL}$ , $\overline{\text{CAS}}$ , address cycling: $t_{PC} = t_{PC \text{ MIN.}}$ )	$I_{CC4}$	-	50 40	mA mA	2, 3, 4 2, 3, 4
Standby $V_{CC}$ supply current ( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{CC} - 0.2 \text{ V}$ )	$I_{CC5}$	-	1	mA	1
Average $V_{CC}$ supply current, during $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh mode -50 ns version -60 ns version ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ cycling: $t_{RC} = t_{RC \text{ MIN.}}$ )	$I_{CC6}$	-	130 115	mA mA	2, 4 2, 4

### Capacitance

$T_A = 0$  to  $70$  °C,  $f = 1$  MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11)	$C_{I1}$	–	5	pF
Input capacitance ( $\overline{RAS}$ , $\overline{UCAS}$ , $\overline{LCAS}$ , $\overline{WE}$ , $\overline{OE}$ )	$C_{I2}$	–	7	pF
I/O capacitance (I/O1 - I/O16)	$C_{IO}$	–	7	pF

### AC Characteristics <sup>5, 6</sup>

$T_A = 0$  to  $70$  °C,  $V_{CC} = 5$  V  $\pm$  10 % /  $V_{CC} = 3.3$  V  $\pm$  0.3 V,  $t_T = 2$  ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		

### Common Parameters

Random read or write cycle time	$t_{RC}$	84	–	104	–	ns	
$\overline{RAS}$ precharge time	$t_{RP}$	30	–	40	–	ns	
$\overline{RAS}$ pulse width	$t_{RAS}$	50	10k	60	10k	ns	
$\overline{CAS}$ pulse width	$t_{CAS}$	8	10k	10	10k	ns	
Row address setup time	$t_{ASR}$	0	–	0	–	ns	
Row address hold time	$t_{RAH}$	8	–	10	–	ns	
Column address setup time	$t_{ASC}$	0	–	0	–	ns	
Column address hold time	$t_{CAH}$	8	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	$t_{RCD}$	12	37	14	45	ns	
$\overline{RAS}$ to column address delay	$t_{RAD}$	10	25	12	30	ns	
$\overline{RAS}$ hold time	$t_{RSH}$	13	–	15	–	ns	
$\overline{CAS}$ hold time	$t_{CSH}$	40	–	50	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	$t_{CRP}$	5	–	5	–	ns	
Transition time (rise and fall)	$t_T$	1	50	1	50	ns	<sup>7</sup>
Refresh period for 1k-refresh version	$t_{REF}$	–	16	–	16	ms	

### Read Cycle

Access time from $\overline{RAS}$	$t_{RAC}$	–	50	–	60	ns	8, 9
Access time from $\overline{CAS}$	$t_{CAC}$	–	13	–	15	ns	8, 9
Access time from column address	$t_{AA}$	–	25	–	30	ns	8, 10
$\overline{OE}$ access time	$t_{OEA}$	–	13	–	15	ns	

#### AC Characteristics (cont'd) <sup>5, 6</sup>

$T_A = 0$  to  $70$  °C,  $V_{CC} = 5\text{ V} \pm 10\%$  /  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $t_T = 2\text{ ns}$

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
Column address to $\overline{\text{RAS}}$ lead time	$t_{\text{RAL}}$	25	–	30	–	ns	
Read command setup time	$t_{\text{RCS}}$	0	–	0	–	ns	
Read command hold time	$t_{\text{RCH}}$	0	–	0	–	ns	11
Read command hold time referenced to $\overline{\text{RAS}}$	$t_{\text{RRH}}$	0	–	0	–	ns	11
$\overline{\text{CAS}}$ to output in low-Z	$t_{\text{CLZ}}$	0	–	0	–	ns	8
Output buffer turn-off delay	$t_{\text{OFF}}$	0	13	0	15	ns	12
Output turn-off delay from $\overline{\text{OE}}$	$t_{\text{OEZ}}$	0	13	0	15	ns	12
Data to $\overline{\text{CAS}}$ low delay	$t_{\text{DZC}}$	0	–	0	–	ns	13
Data to $\overline{\text{OE}}$ low delay	$t_{\text{DZO}}$	0	–	0	–	ns	13
$\overline{\text{CAS}}$ high to data delay	$t_{\text{CDD}}$	10	–	13	–	ns	14
$\overline{\text{OE}}$ high to data delay	$t_{\text{ODD}}$	10	–	13	–	ns	14

#### Write Cycle

Write command hold time	$t_{\text{WCH}}$	8	–	10	–	ns	
Write command pulse width	$t_{\text{WP}}$	8	–	10	–	ns	
Write command setup time	$t_{\text{WCS}}$	0	–	0	–	ns	15
Write command to $\overline{\text{RAS}}$ lead time	$t_{\text{RWL}}$	8	–	10	–	ns	
Write command to $\overline{\text{CAS}}$ lead time	$t_{\text{CWL}}$	8	–	10	–	ns	
Data setup time	$t_{\text{DS}}$	0	–	0	–	ns	16
Data hold time	$t_{\text{DH}}$	8	–	10	–	ns	16

#### Read-Modify-Write Cycle

Read-write cycle time	$t_{\text{RWC}}$	113	–	138	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	$t_{\text{RWD}}$	64	–	77	–	ns	15
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	$t_{\text{CWD}}$	27	–	32	–	ns	15
Column address to $\overline{\text{WE}}$ delay time	$t_{\text{AWD}}$	39	–	47	–	ns	15
$\overline{\text{OE}}$ command hold time	$t_{\text{OEH}}$	10	–	13	–	ns	

#### Hyper Page Mode (EDO) Cycle

Hyper page mode (EDO) cycle time	$t_{\text{HPC}}$	20	–	25	–	ns	
$\overline{\text{CAS}}$ precharge time	$t_{\text{CP}}$	8	–	10	–	ns	



#### AC Characteristics (cont'd) <sup>5, 6</sup>

$T_A = 0$  to  $70$  °C,  $V_{CC} = 5$  V ± 10 % /  $V_{CC} = 3.3$  V ± 0.3 V,  $t_T = 2$  ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
Access time from $\overline{\text{CAS}}$ precharge	$t_{\text{CPA}}$	–	27	–	32	ns	<sup>7</sup>
Output data hold time	$t_{\text{COH}}$	5	–	5	–	ns	
$\overline{\text{RAS}}$ pulse width in EDO mode	$t_{\text{RAS}}$	50	200k	60	200k	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{RAS}}$ delay	$t_{\text{RHCP}}$	27	–	32	–	ns	
$\overline{\text{OE}}$ setup time prior to $\overline{\text{CAS}}$	$t_{\text{OES}}$	5	–	5	–	5	–

#### Hyper Page Mode (EDO) Read-Modify-Write Cycle

Hyper page mode (EDO) read-write cycle time	$t_{\text{PRWC}}$	58	–	68	–	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$	$t_{\text{CPWD}}$	41	–	49	–	ns	

#### $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle

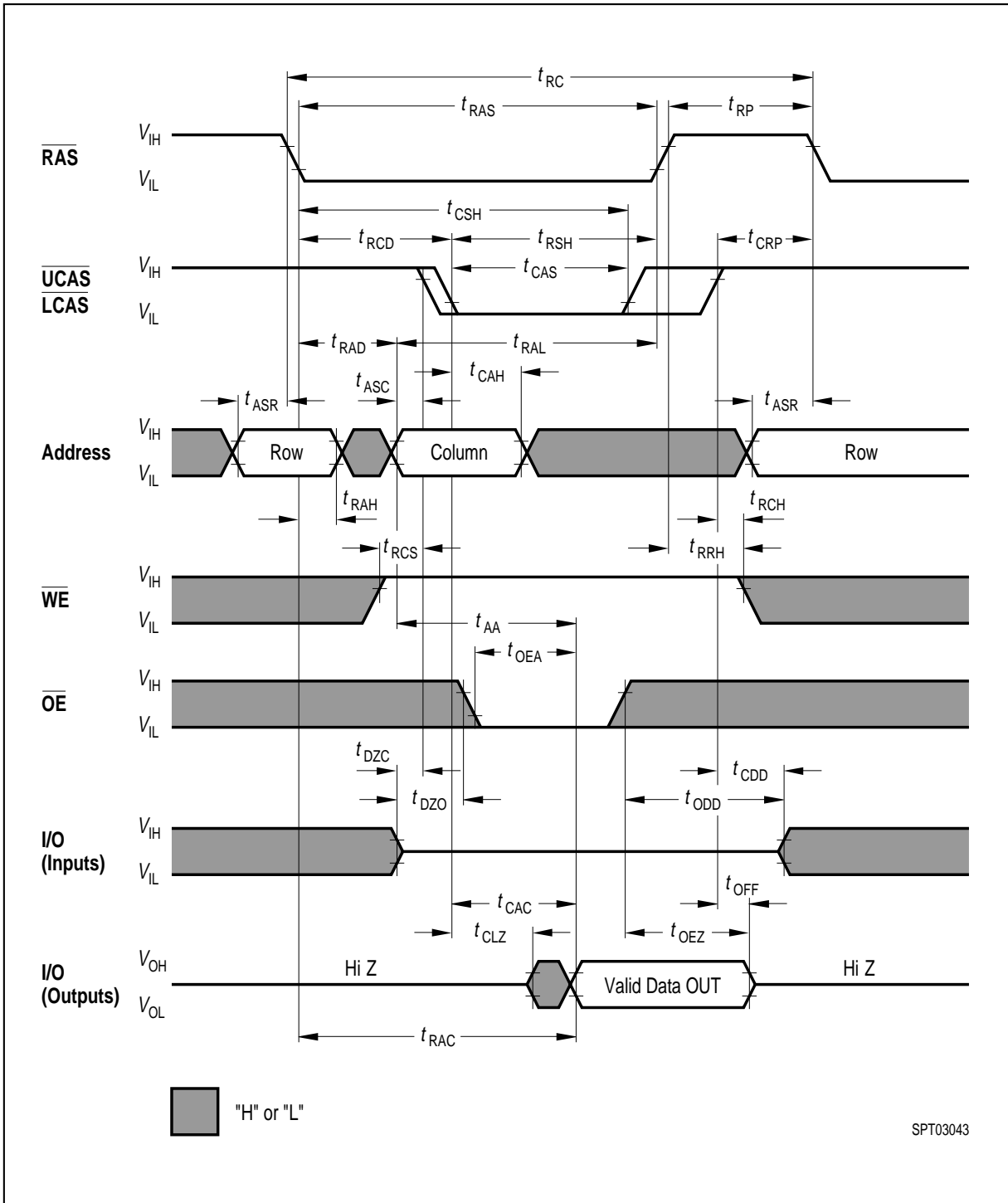
$\overline{\text{CAS}}$ setup time	$t_{\text{CSR}}$	10	–	10	–	ns	
$\overline{\text{CAS}}$ hold time	$t_{\text{CHR}}$	10	–	10	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	$t_{\text{RPC}}$	5	–	5	–	ns	
Write to $\overline{\text{RAS}}$ precharge time	$t_{\text{WRP}}$	10	–	10	–	ns	
Write hold time referenced to $\overline{\text{RAS}}$	$t_{\text{WRH}}$	10	–	10	–	ns	

#### $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Counter Test Cycle

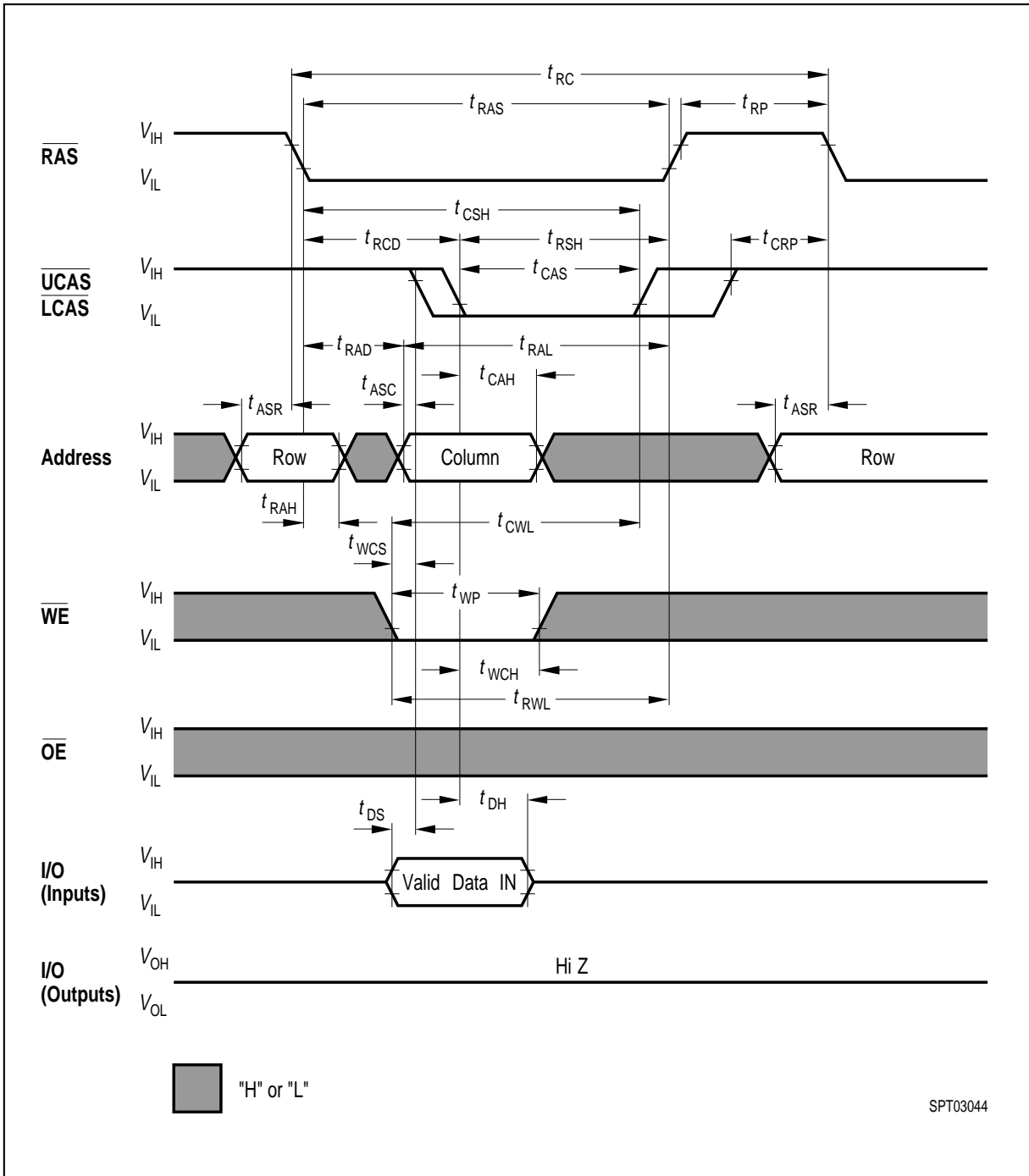
$\overline{\text{CAS}}$ precharge time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ counter test cycle)	$t_{\text{CPT}}$	35	–	40	–	ns	
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## Notes

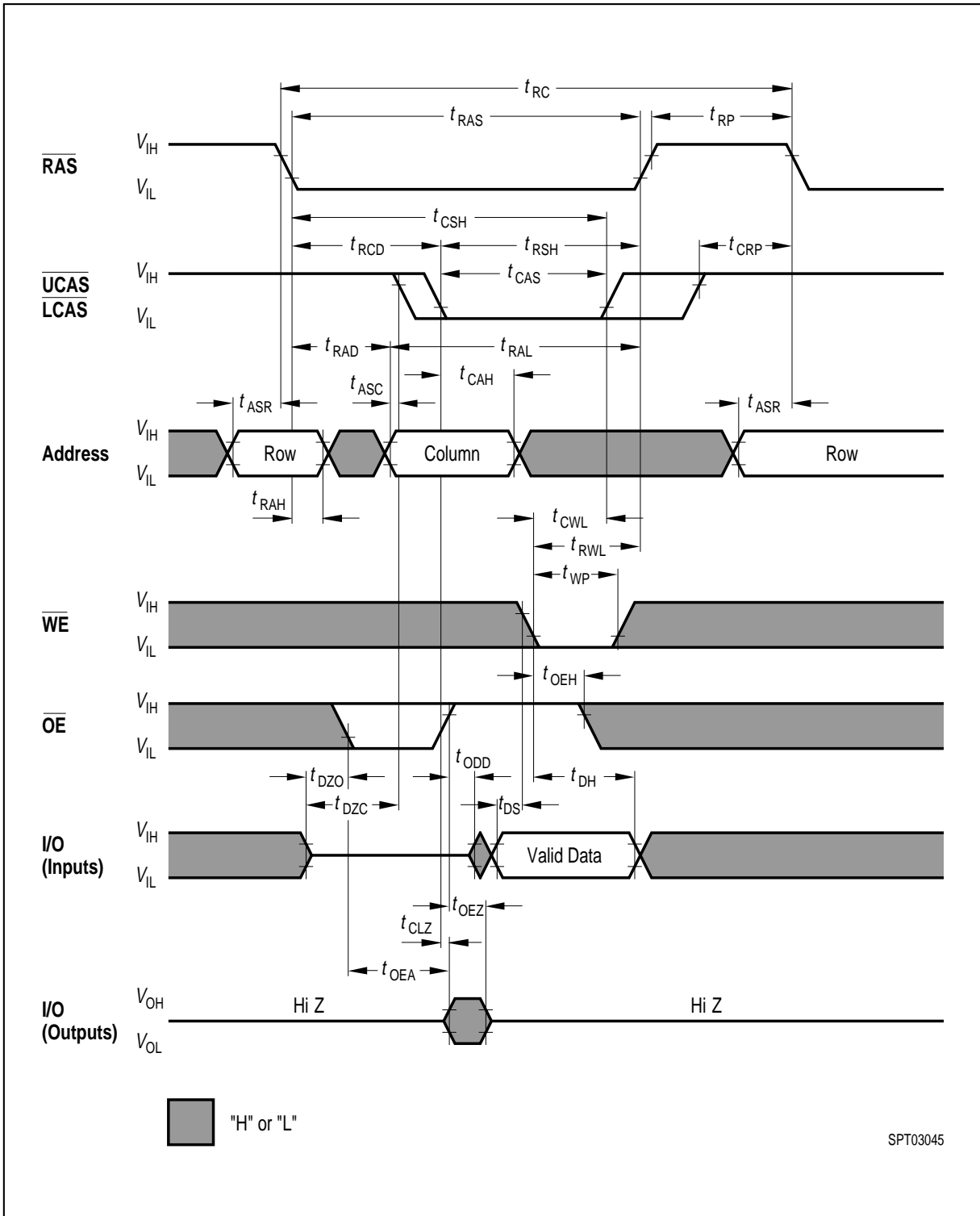
1. All voltages are referenced to  $V_{SS}$ .
2.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$  and  $I_{CC6}$  depend on cycle rate.
3.  $I_{CC1}$  and  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
4. Address can be changed once or less while  $\overline{RAS} = V_{IL}$ . In case of  $I_{CC4}$  it can be changed once or less during a hyper page mode (EDO) cycle
5. An initial pause of 200  $\mu s$  is required after power-up followed by 8  $\overline{RAS}$  cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8  $\overline{CAS}$ -before- $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
6. AC measurements assume  $t_T = 2$  ns.
7.  $V_{IH(MIN)}$  and  $V_{IL(MAX)}$  are reference levels for measuring timing of input signals. Transition times are also measured between  $V_{IH}$  and  $V_{IL}$ .
8. Measured with the specified current load and 100 pF at  $V_{OL} = 0.8$  V and  $V_{OH} = 2.0$  V. Access time is determined by the latter of  $t_{RAC}$ ,  $t_{CAC}$ ,  $t_{AA}$ ,  $t_{CPA}$ ,  $t_{OEA}$ .  $t_{CAC}$  is measured from tristate.
9. Operation within the  $t_{RCD(MAX)}$  limit ensures that  $t_{RAC(MAX)}$  can be met.  $t_{RCD(MAX)}$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD(MAX)}$  limit, then access time is controlled by  $t_{CAC}$ .
10. Operation within the  $t_{RAD(MAX)}$  limit ensures that  $t_{RAC(MAX)}$  can be met.  $t_{RAD(MAX)}$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD(MAX)}$  limit, then access time is controlled by  $t_{AA}$ .
11. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
12.  $t_{OFF(MAX)}$ ,  $t_{OEZ(MAX)}$  define the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels.  $t_{OFF}$  is referenced from the rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ , whichever occurs last.
13. Either  $t_{DZC}$  or  $t_{DZO}$  must be satisfied.
14. Either  $t_{CDD}$  or  $t_{ODD}$  must be satisfied.
15.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} > t_{WCS(MIN)}$ , the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if  $t_{RWD} > t_{RWD(MIN)}$ ,  $t_{CWD} > t_{CWD(MIN)}$  and  $t_{AWD} > t_{AWD(MIN)}$ , the cycle is a read-write cycle and I/O will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of I/O (at access time) is indeterminate.
16. These parameters are referenced to the  $\overline{CAS}$  leading edge in early write cycles and to the  $\overline{WE}$  leading edge in read-write cycles.



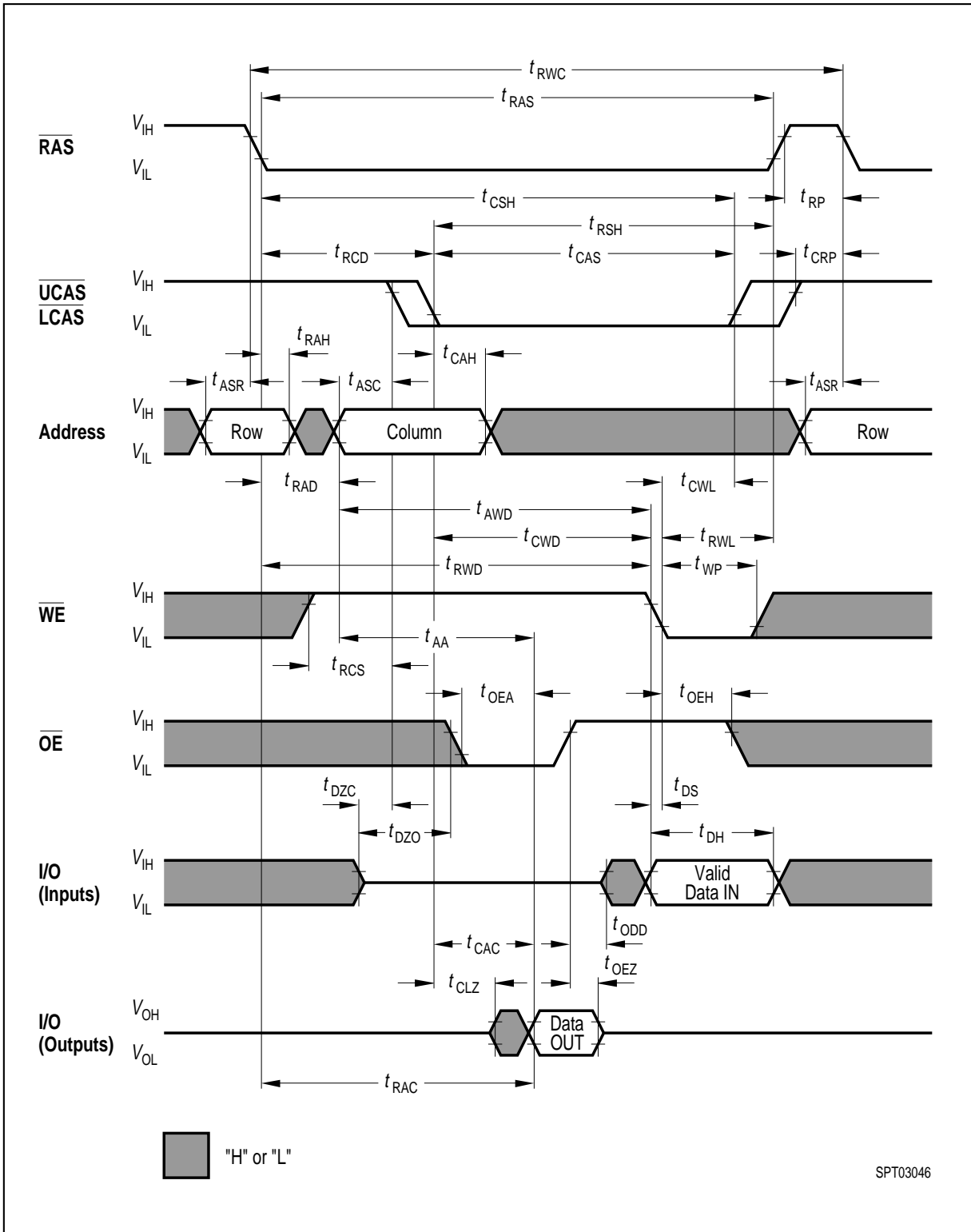
Read Cycle



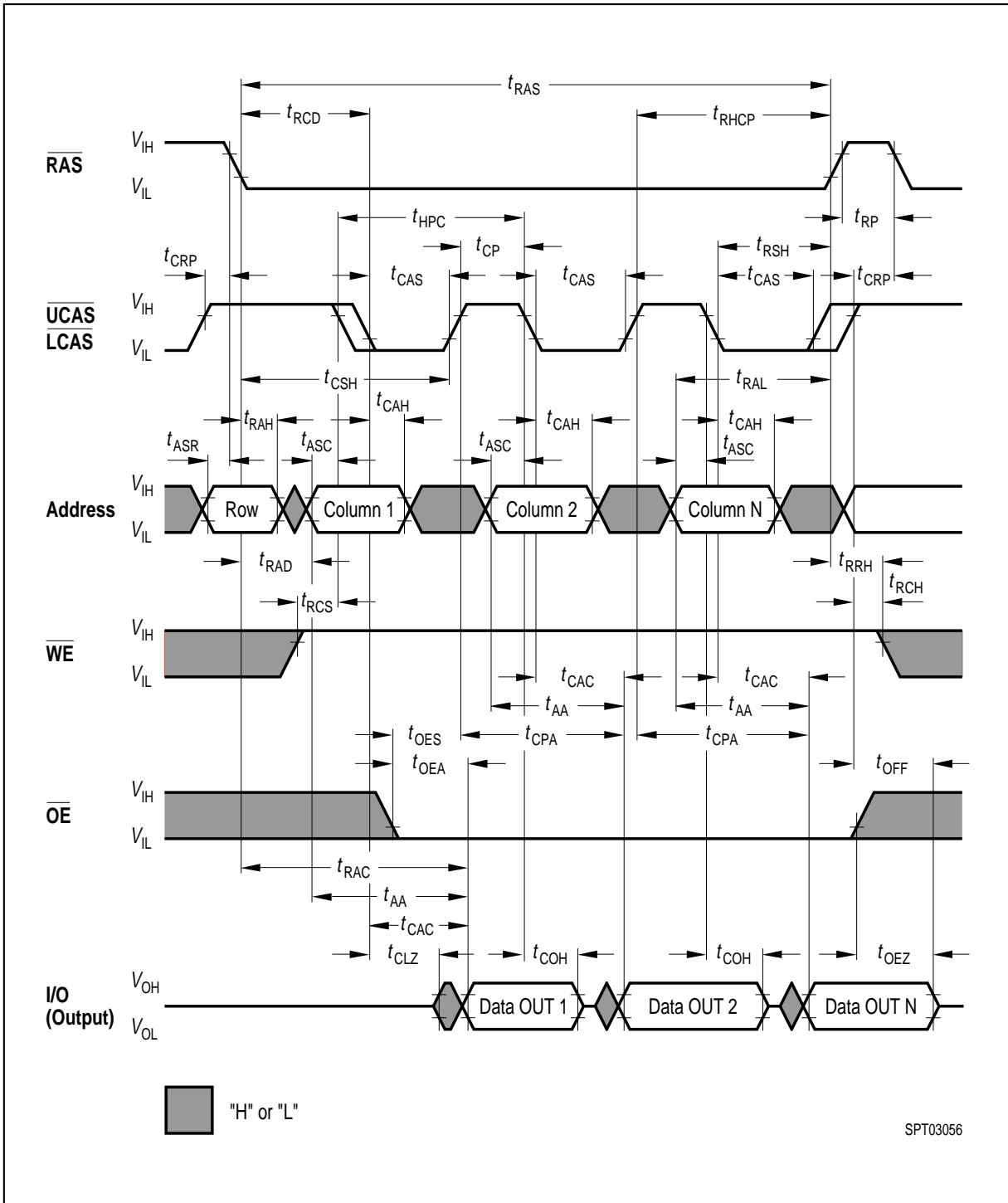
Write Cycle (Early Write)



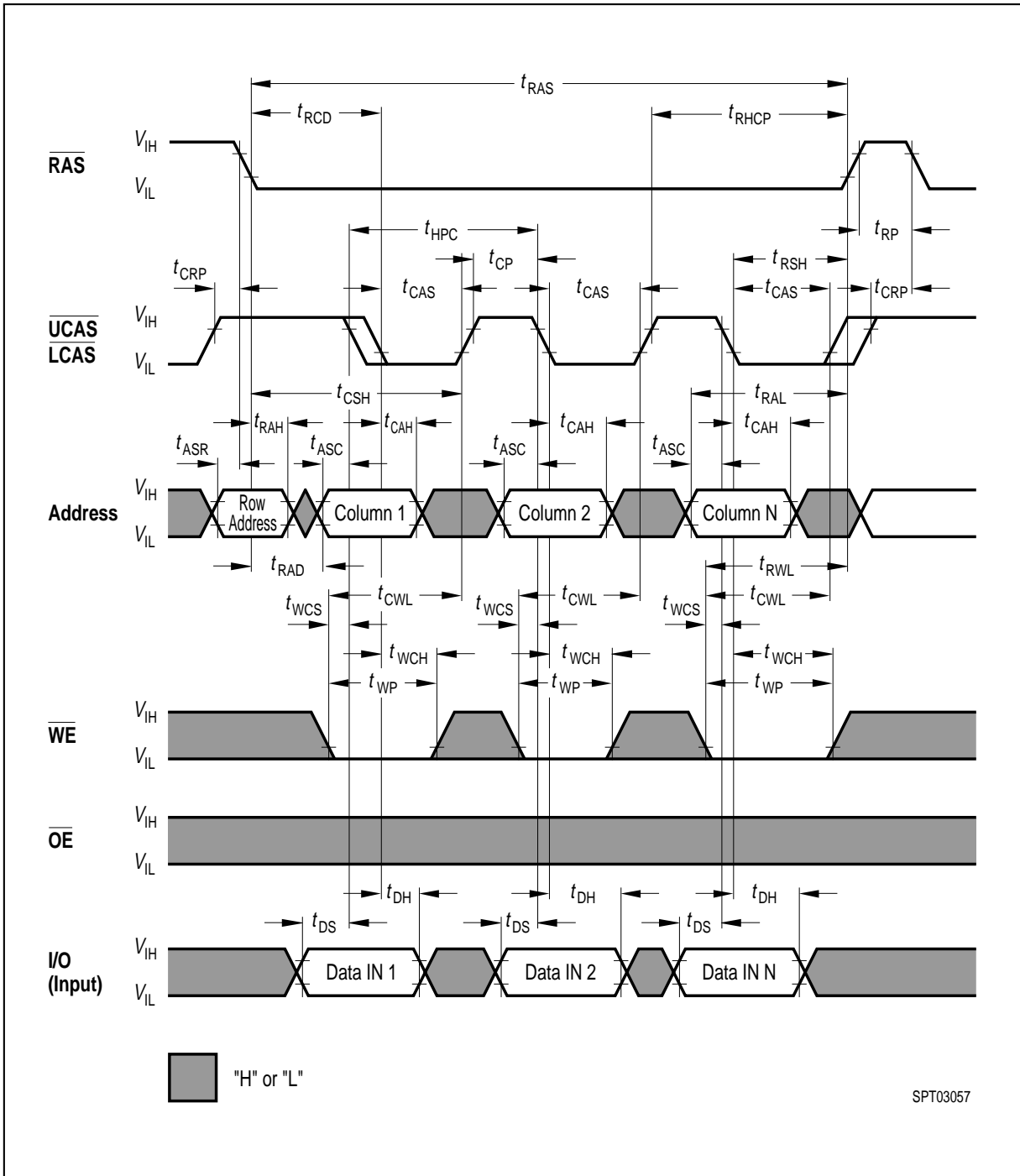
Write Cycle ( $\overline{OE}$  Controlled Write)



Read-Write (Read-Modify-Write) Cycle



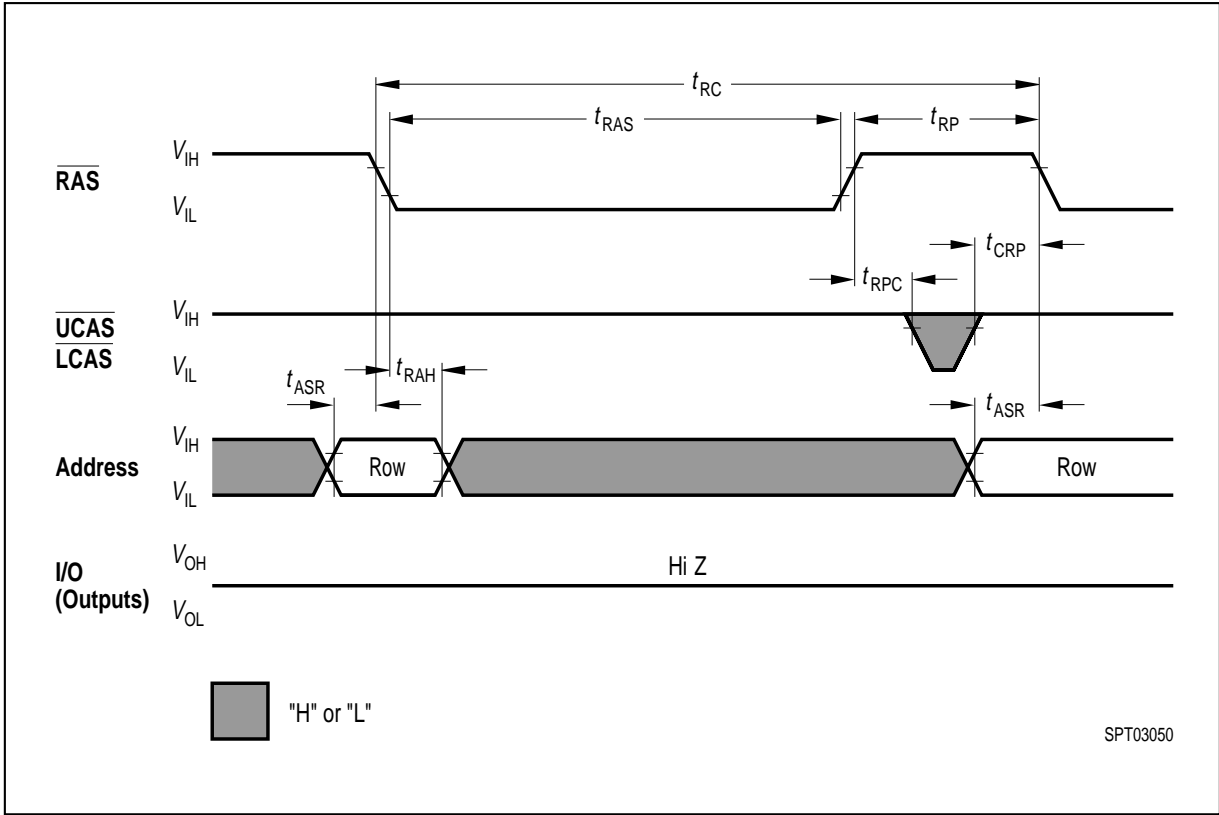
Hyper Page Mode (EDO) Read Cycle



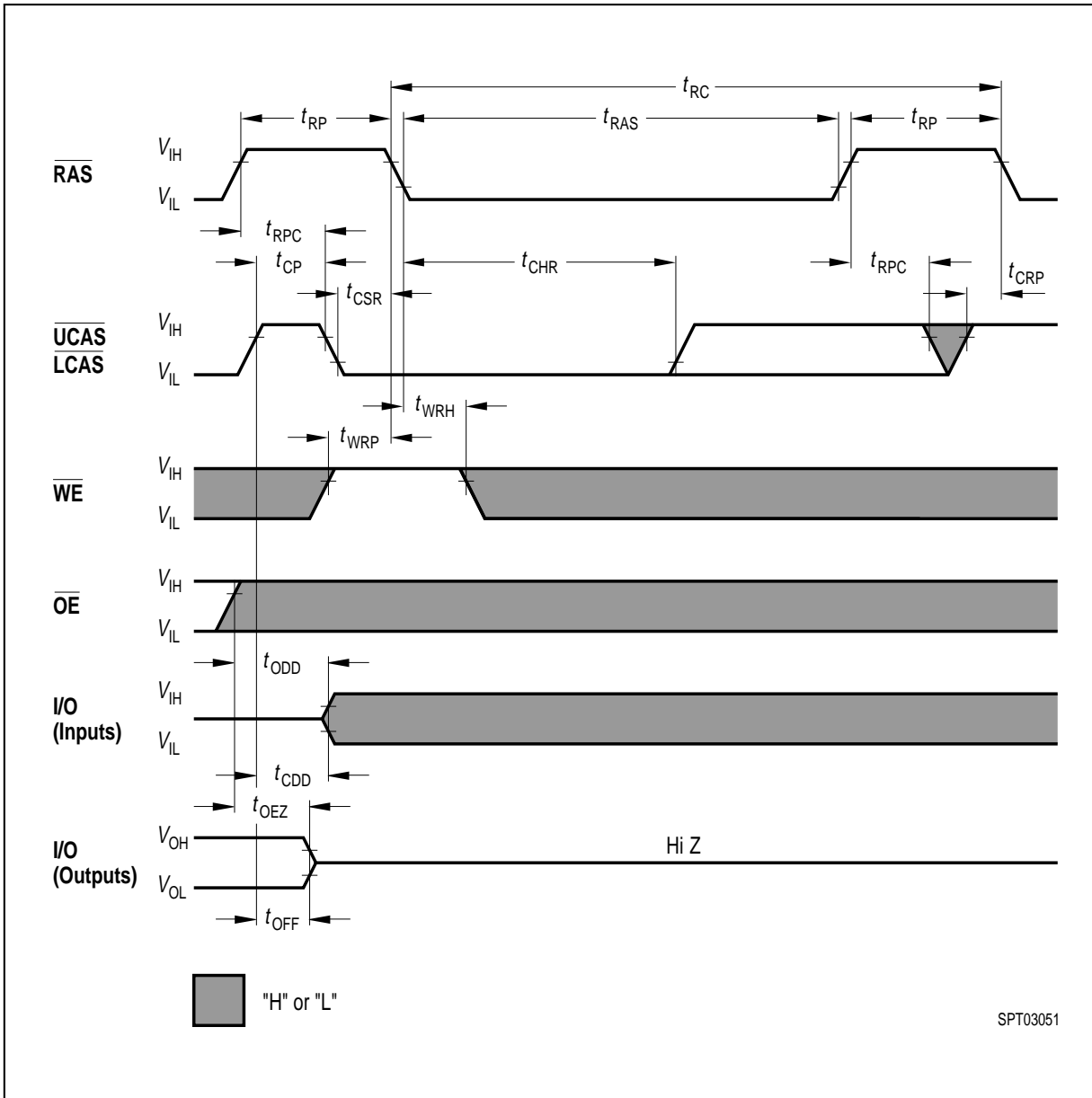
Hyper Page Mode (EDO) Early Write Cycle



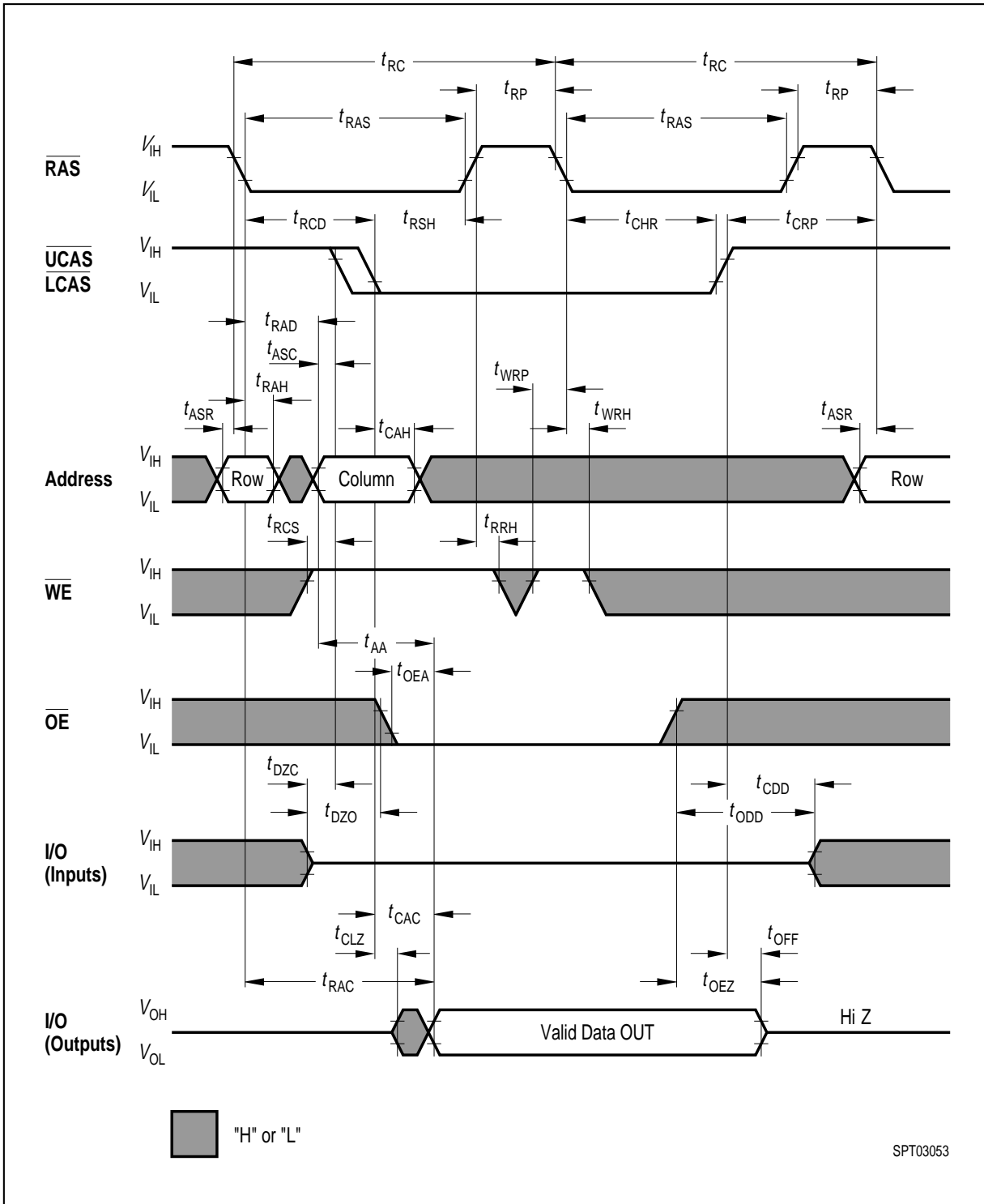




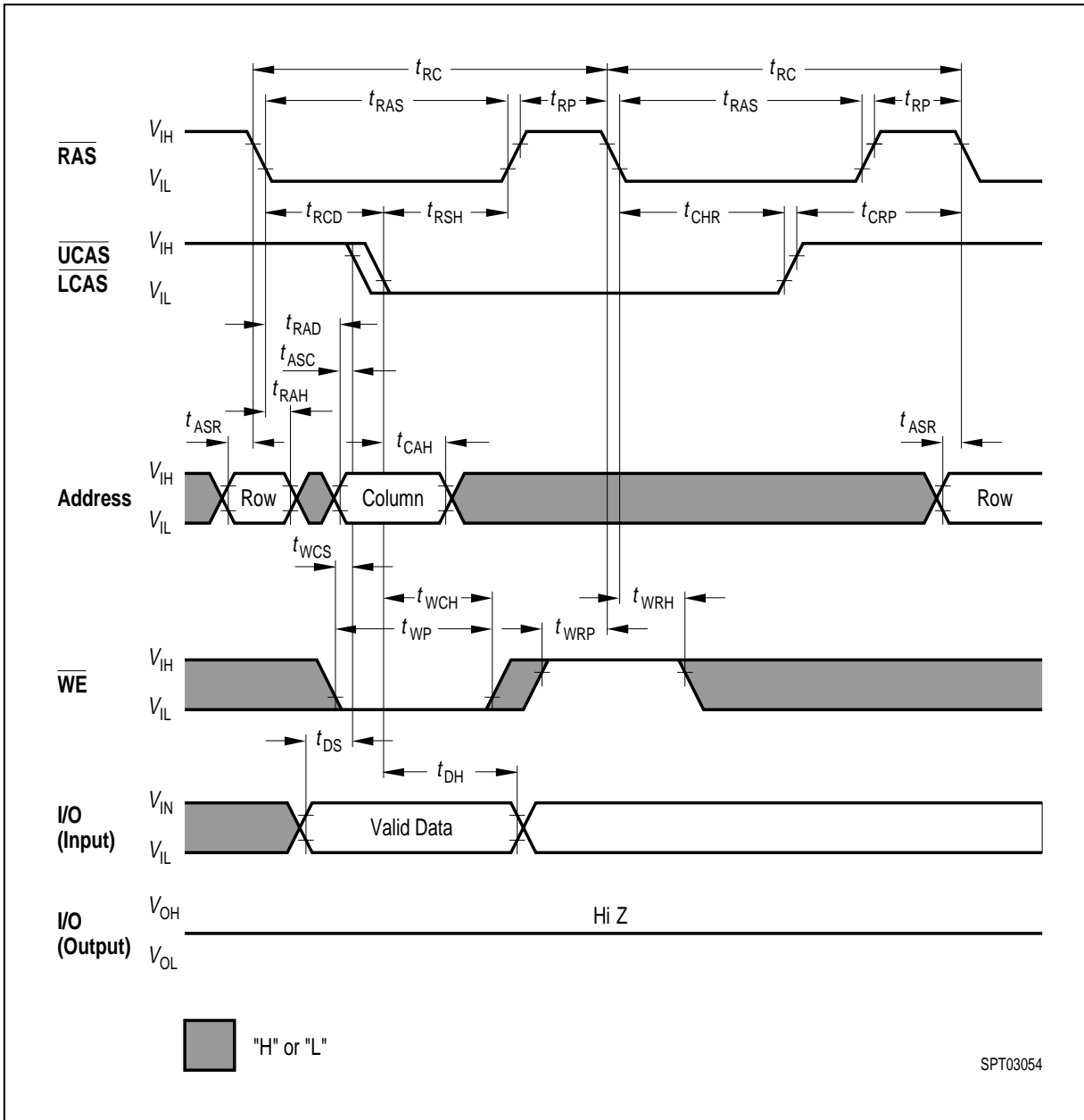
RAS-only Refresh Cycle



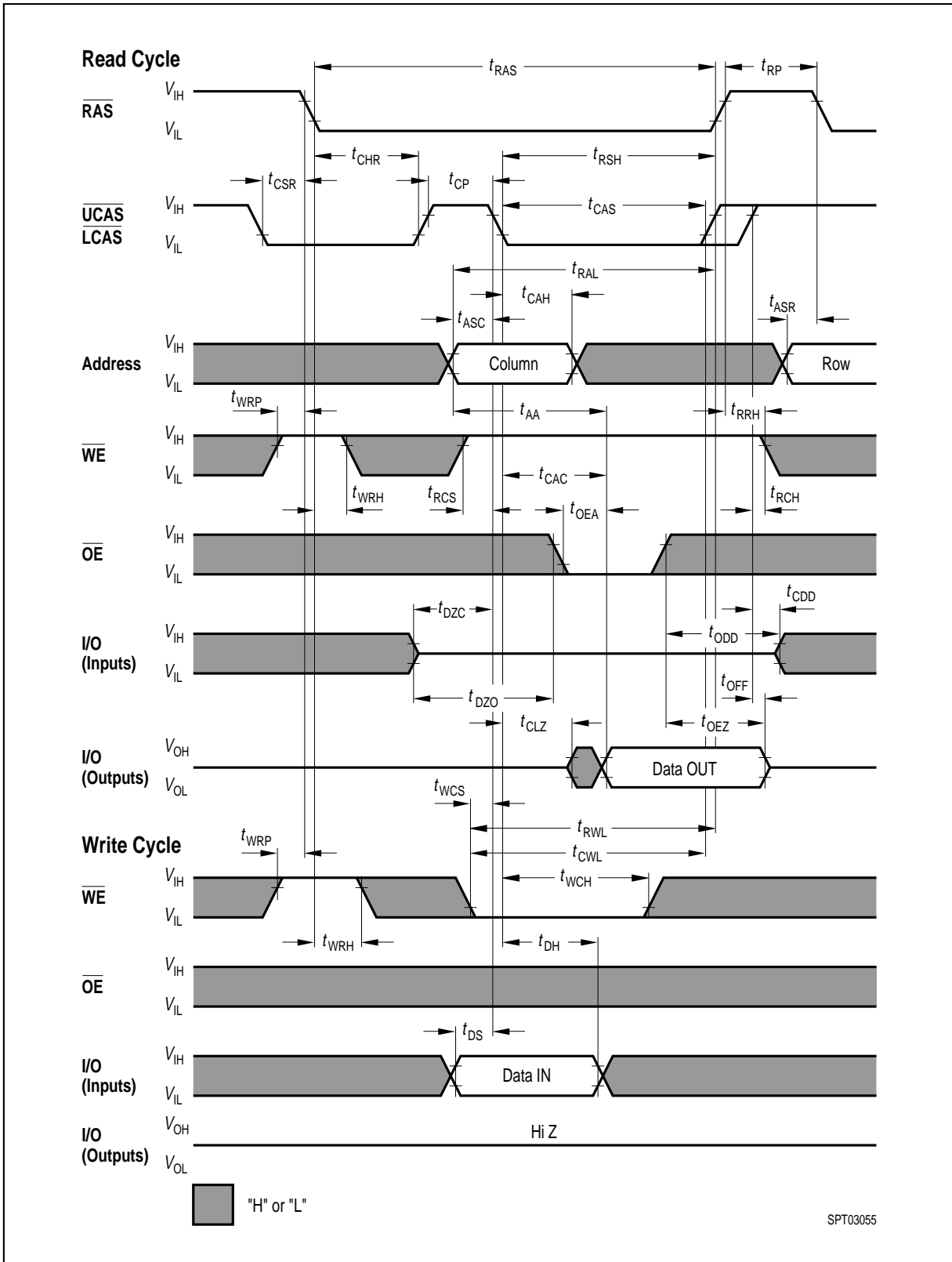
CAS-before-RAS Refresh Cycle



Hidden Refresh Cycle (Read)

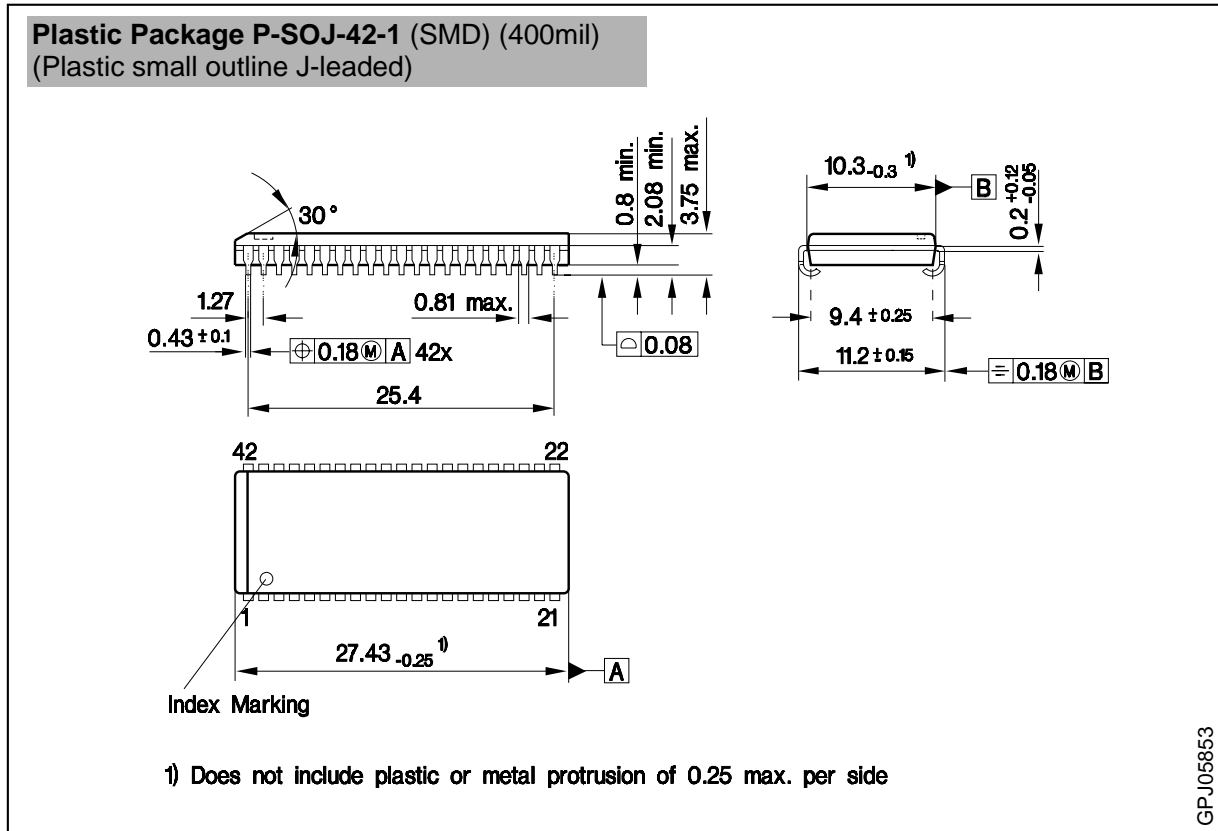


Hidden Refresh Cycle (Early Write)



CAS-before-RAS Refresh Counter Test Cycle

**Package Outlines**



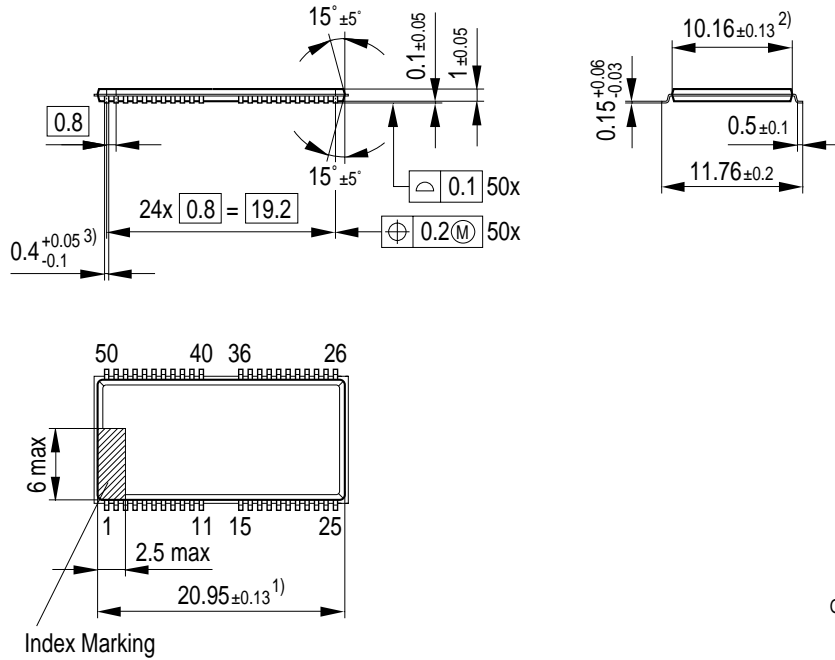
**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

**Plastic Package P-TSOPII-50/44-1 (400 mil) (SMD)**  
 (Plastic Thin Small Outline Package (Type II))



GPX05958

- 1) Does not include plastic or metal protrusion of 0.15 max per side
- 2) Does not include plastic protrusion of 0.25 max per side
- 3) Does not include dambar protrusion of 0.13 max per side

**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

**SMD = Surface Mounted Device**

Dimensions in mm