PCI 9054

PCI Bus Master I/O Accelerator Chip

- PCI v2.2 compliant 32-bit 33MHz Bus Master Interface Controller enables PCI Burst Transfers up to 132Mbytes/second
- General Purpose Bus Master Interface featuring an advanced Data Pipe Architecture™ which includes two DMA engines, pro-grammable Target and Initiator data transfer modes and PCI messaging functions
- PCI v2.2 Power Management Spec compatible
- PCI v2.2 Vital Product Data (VPD) configuration support
- PCI Dual Address Cycle (DAC) support
- Programmable Interrupt Generator
- Programmable Burst Management
- Supports Type 0 and Type 1 Configuration Cycles
- Supports Local Bus Direct-Connect to MPC 850/860 PowerQUICC, Intel i960, and IBM PPC 401 CPUs and similar bus protocol devices
- 3.3V, 5V Tolerant PCI signaling supports Universal PCI Adapter designs
- Flexible 3.3V, 5V Tolerant Local Bus operation up to 50MHz
- 32-Bit Multiplexed, or Non-Multiplexed Local Bus Supports 8-, 16-, and 32-Bit Peripheral and Memory devices
- CompactPCI Hot Swap Friendly
- I$_2$O v1.5 Ready Messaging Unit
- Industrial Temp Range Operation
- 3.3V CMOS in 176-pin PQFP or 225-ball PBGA packages

Continuing our tradition of providing the world's most advanced and highest performance PCI-to-Local bus devices, PLX is offering the PCI 9054 Bus Master I/O Accelerator. The PCI 9054 is an ideal solution for high performance Motorola MPC 850/860 PowerQUICC® designs, CompactPCI® Hot Swap adapters, PCI bus master adapters, and embedded host designs. The PCI 9054 offers a variety of technological advances and features designed to simplify complex telecom, networking and I/O adapter embedded designs.

Motorola MPC 850/860 PowerQUICC Designs

The 3.3V PCI 9054 is a perfect match for high performance MPC 850/860 adapter designs. The PCI 9054 provides an advanced Data Pipe Architecture™ with two DMA engines, an enhanced direct-connect interface to the MPC 850/860, a 50MHz Local bus, and an industrial temperature range 225-ball PBGA.

CompactPCI Hot Swap Adapter Designs

To address the expanding CompactPCI Hot Swap market, the PCI 9054 offers a configurable Local Bus, unlimited bursting, and Hot Swap Friendly features like the Hot Swap Configuration Register, and resources for software connection control of the ENUM# signal, ejector switch, and the status LED.

Additional PCI Bus Master Features

For advanced high performance adapter designs, the PCI 9054 also offers Hot Plug compatibility, power management and incorporates PLX's proven industry standard I$_2$O v1.5 Ready messaging unit.

The flexible PCI 9054 local bus allows easy connection to a wide variety of memory, I/O peripherals and CPUs including direct connections to the Motorola MPC 850/860, Intel i960, IBM PPC 401 processors and many others. Take advantage of what industry leaders already know: PLX PCI Accelerators are *the* solution for leading telecom, networking, and I/O adapter designs.

PCI 9054 I/O Accelerator

The PCI 9054, a 32-bit 33MHz Bus Master I/O Accelerator, is the most advanced general purpose bus master device available. It offers a robust PCI v2.2 specification implementation enabling burst transfers up to 132Mbytes/second. The PCI 9054 incorporates PLX's industry leading Data Pipe Architecture™ including DMA engines, programmable PCI Initiator and Target data transfer modes and PCI messaging functions.

Data Pipe Architecture™

Dual DMA Channels
- Dual independent channels–provides flexible prioritization scheme
- Direct H/W control of DMA
  -Demand mode DMA operation
  -Block Mode or Scatter/Gather operation
  -End of Transfer (EOT) signal
- Programmable burst length including unlimited burst
- Shuttle mode DMA channel support
  –Automatic invalidation of used DMA descriptors
- Unaligned transfer support

PCI Initiator
- Type 0 and Type 1 configuration cycles
- All PCI Memory and I/O cycles supported
- Initiator READ prefetching
- Burst length control–programmable threshold pointer
- Unaligned transfer control
- Endian swapping

PCI Target
- Multiple independent address spaces
- Dynamic local bus width control
- Target READ prefetching
- Endian swapping
- Local bus priority control
- Latency timer

PCI Messaging
- Complete messaging unit with mailbox registers, doorbell registers
- Queue management pointers which can be used for message passing under the I_2O protocol or a custom protocol.

PCI 9054 PCI Applications

High performance Motorola MPC 850/860 PowerQUICC Designs

A key application for the PCI 9054 is Motorola MPC 850/860 based adapters for telecom and networking applications.

850/860 processor. The PCI 9054's flexible, 3.3V, 5V tolerant I/O buffers combined with a local bus operation up to 50MHz is ideally suited for current and future PowerQUICC processors. The PCI 9054 also provides support for the MPC860 IDMA channel for movement of data between internal MPC860 I/O and the PCI bus. In addition, the PCI 9054 also makes use of the advanced Data Pipe Architecture including unlimited burst capability as shown in figure 1.

1 For PowerQUICC IDMA operation, the PCI 9054 transfers data to PCI under the control of the IDMA handshake protocol.

2 At the same time, the PCI 9054 Data Pipe Architecture™ DMA can be operated bi-directionally, with the PCI 9054 as the master for both buses, to manage transfers of data from the local bus to the PCI bus or from the PCI bus to the local bus. This is a prime example of how the PCI 9054 provides superior general purpose bus master performance and gives the designer using the PowerQUICC processor greater flexibility in implementing multiple simultaneous I/O transfers. The PCI 9054 has unlimited bursting capability which enhances any MPC860 PowerQUICC design.
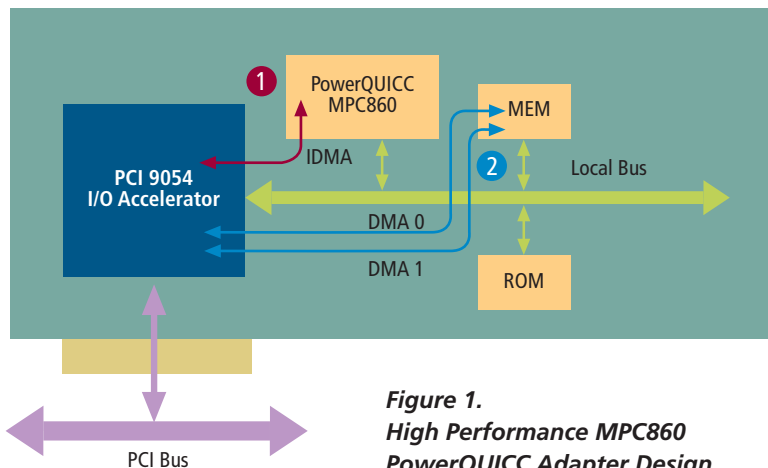
High Performance CompactPCI Adapter Designs

Another key application for the PCI 9054 is CompactPCI adapters for telecom and networking applications. These applications include high performance communications like WAN/LAN controller cards, high speed modem cards, frame relay cards, and telephony cards for telecom switches and remote access systems.

The PCI 9054 has intergrated key features to enable live-insertion of Hot Swap CompactPCI adapters. The PCI 9054 PICMG 2.1 compatible Hot Swap Friendly PCI interface includes both Hot Swap Capable and Friendly features:

Hot Swap Capable
- PCI specification v2.1 or better
- Tolerant of V_{CC} from early power
- Tolerant of asynchronous reset
- Tolerant of precharge voltage

Figure 1.
High Performance MPC860
PowerQUICC Adapter Design

- Supports PCI bus mastering from local slave-only devices
- Scatter/Gather list management
  -Descriptors can be in the PCI or local bus memory
  -Allows independent scatter/gather ring management

These applications include high performance communications like WAN/LAN controller cards, high speed modem cards, frame relay cards, and networking cards for routers and switches to name a few. The PCI 9054 simplifies designs by providing an industry leading enhanced direct-connect interface to the MPC

- Has limited I/O pin leakage at precharge voltage

Hot Swap Friendly

- Incorporates the Hot Swap Control/Status register (HS_CSR)

Figure 2. High Performance CompactPCI Adapter

- Incorporates an Extended Capability Pointer (ECP) mechanism
- Incorporates added resources for software control of ENUM#, the ejector switch, and the status LED, which indicates to the user insertion/removal

PCI Bus Embedded Host Design

Another application for the PCI 9054 is PCI host embedded system designs such as network switches and routers, printer engines, set-top boxes and industrial equipment. In this configuration, the PCI 9054 Data Pipe Architecture allows high performance transfer modes. In addition, the PCI 9054 supports both Type 0 and Type 1 PCI configuration cycles which allows the PCI 9054 to configure other PCI devices or cards in the system.

Additional Features

General Purpose Bus Master Operation
- Advanced Data Pipe Architecture includes DMA engines, PCI Initiator, PCI Target, and PCI messaging functions.
- Dual independently programmable Data Pipe Architecture DMA engines with programmable FIFOs. Each channel supports block and scatter/gather DMA modes.
- 5V Tolerant Operation–The PCI 9054 requires 3.3 V_{CC}. It provides 3.3V signaling with 5V I/O tolerance on both the PCI and Local Buses.

mode data. The PCI 9054 reads single data (8-, 16-, or 32-bit) if the master initiates a single cycle; otherwise, the PCI 9054 prefetches the programmed size.

- Six Programmable FIFOs for concurrent burst transactions
- Zero wait state burst operation
- Serial EEPROM Interface–Contains an interface for an optional serial EEPROM that can be used to load configuration information. The PCI 9054 can also be configured by a local CPU.
- Clock–The Local Bus interface runs from a local TTL clock and asserts the necessary internal clocks. This clock runs asynchronously to the PCI clock.
- Big/Little Endian Conversion–Supports dynamic switching between Big Endian and Little Endian data for PCI Initiator, PCI Target, DMA, and internal register accesses on the Local Bus
- Fully supports the Vital Product Data (VPD) PCI extension–Provides an alternate access method other than Expansion ROM for Vital Product Data
- Interrupt Generator– Can assert PCI and local interrupts from external and internal sources

- Programmable Prefetch Counter–The PCI 9054 can be programmed to prefetch data during PCI Initiator and PCI Target operations. The prefetch size can be programmed to match the master burst length or can be used as Read Ahead
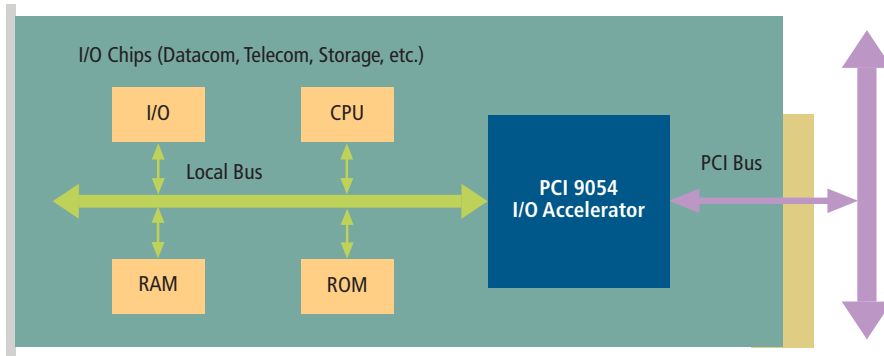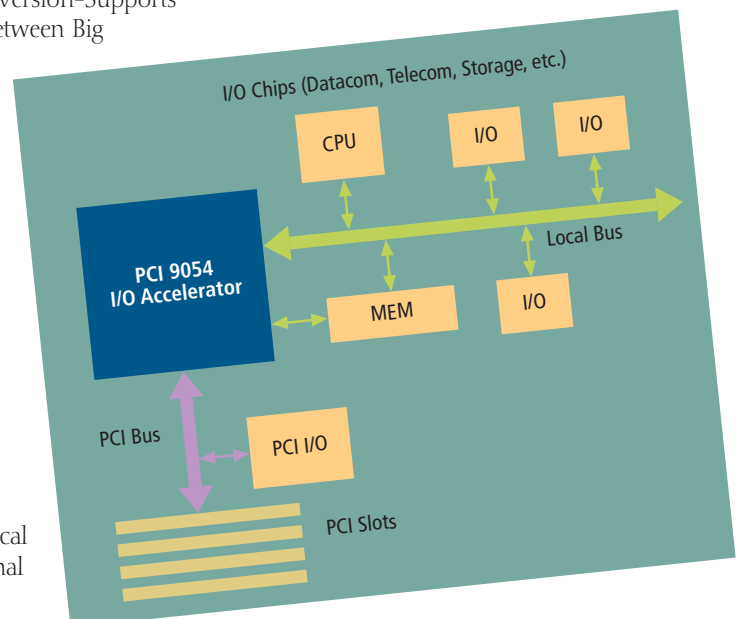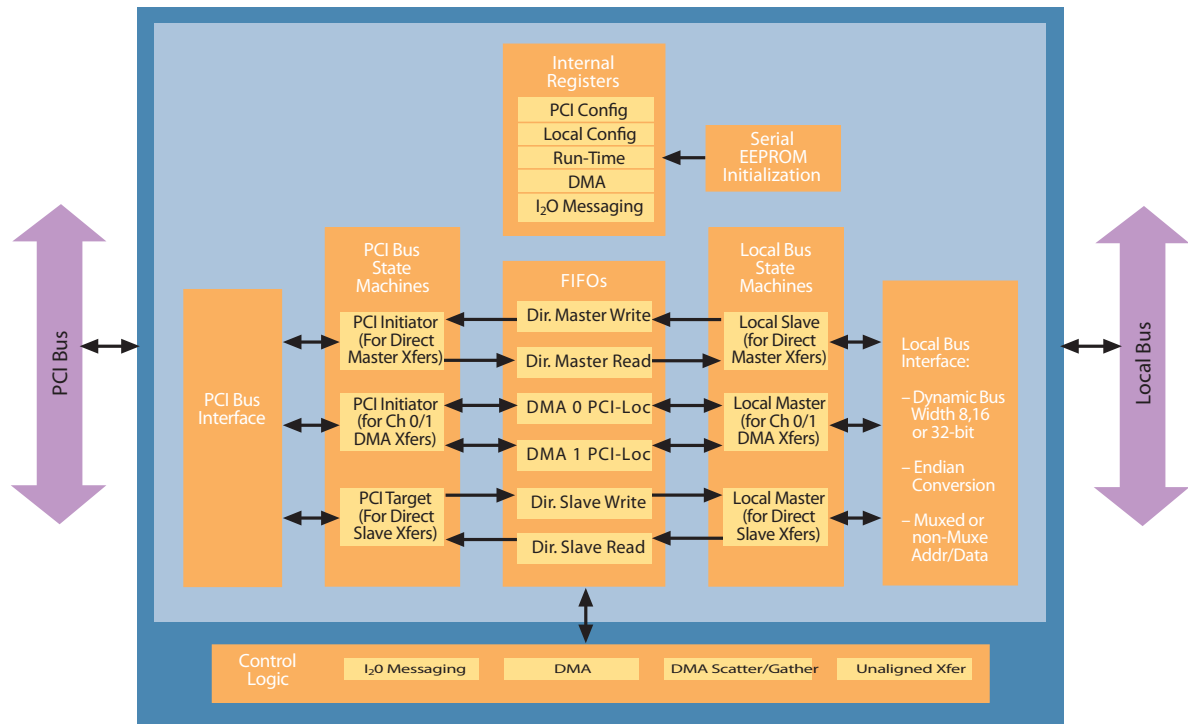
- Posted Memory Writes–Supports Posted Memory Writes (PMW) for maximum performance and to avoid potential deadlock situations

PCI Bus Operation
- PCI Dual-Address Cycle (DAC)–Support (64-bit Address Space) enables 64-bit addressing in 64-bit PCI host systems
- PCI Power Management–Supports four power states for PCI functions D_0, D_1, D_2, and D_{3hot} and the Power Management Event interrupt (PME#)
- New Capabilities Structure–Supports New Capabilities registers to define additional capabilities of PCI functions

Local Bus Operation
- Programmable Local Bus–Runs up to 50MHz and supports non-multiplexed 32-bit address/data, multiplexed 32-bit, and slave accesses of 8-, 16-, or 32-bit Local Bus devices. Allows Local Bus bursting up to 200Mbytes/second.
- Three PCI-to-Local Address Spaces–The PCI 9054 supports three PCI-to-Local Address spaces when the PCI 9054 is in PCI Target mode. These spaces (Space 0, Space 1, and Expansion ROM spaces) allow any PCI Bus Master to access the local memory spaces with programmable wait states, bus width, and burst capabilities.

**Figure 3.
PCI Bus Embedded
Host Design**

PCI 9054 Internal Block Diagram

Development Tool Support

PLX recognizes that software often represents the largest investment in development. The PCI 9054 is supported by a variety of development tools designed to assist the designer in the form of Reference Design Kits (RDK), and Software Design Kits (SDK). These Kits enable designers to quickly bring new designs to production without worrying about the complexities of implementing PCI and I$_2$O.

The PCI 9054 is fully compatible with PLX's PCI SDK and I$_2$O SDK software development kits which allow quick and easy development of high performance local and host PCI software through standard APIs, I$_2$O messaging protocols, PCI debug tools, and example drivers.

PCI 9054 design support is provided through RDKs which provide a flexible PCI development board, complete with Orcad schematics, documentation, and software.

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Product Ordering Information

PCI 9054-AC50BI	PCI to Local Bus Master I/O Accelerator Chip PBGA Package
PCI 9054-AC50BI F	PCI to Local Bus Master I/O Accelerator Chip PBGA Package (Lead-Free)
PCI 9054-AC50PI	PCI to Local Bus Master I/O Accelerator Chip PQFP Package
PCI 9054-AC50PI F	PCI to Local Bus Master I/O Accelerator Chip PQFP Package (Lead-Free)
CompactPCI 9054RDK-86	PCI 9054 Reference Design Kit with Motorola MPC860 PowerQUICC CPU
PCI SDK	PCI Software Development Kit for Motorola MPC860 PowerQUICC CPU
I$_2$O SDK	I$_2$O Software Development Kit for Motorola MPC860 PowerQUICC CPU

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