



## LU6612 FASTCAT™ Single-FET for 10Base-T/100Base-TX

### Features

#### 10 Mbits/s Transceiver

- Compatible with *IEEE*\* 802.3u 10Base-T standard for twisted-pair cable
- Autopolarity detection and correction
- Adjustable squelch level for extended wire line length capability (2 levels)
- Interfaces with *IEEE* 802.3u media independent interface (MII)
- On-chip filtering eliminates the need for external filters
- Half- and full-duplex operations

#### 100 Mbits/s Transceiver

- Compatible with *IEEE* 802.3u MII (clause 22), PCS (clause 23), PMA (clause 24), autonegotiation (clause 28), and PMD (clause 25) specifications
- Scrambler/descrambler bypass
- Encoder/decoder bypass
- 3-statable MII in 100 Mbits/s mode
- Selectable carrier sense signal generation (CRS asserted during either transmission or reception in half duplex, CRS asserted during reception only in full duplex)
- Selectable MII or 5-bit code group interface
- Half- or full-duplex operations
- On-chip filtering and adaptive equalization that eliminates the need for external filters

### General

- Autonegotiation (*IEEE* 802.3u clause 28):
  - Fast link pulse (FLP) burst generator
  - Arbitration function
  - Accepts preamble suppression
  - Operates up to 12.5 MHz
- Supports the station management protocol and frame format (clause 22):
  - Basic and extended registers
  - Supports next-page function
  - Accepts preamble suppression
  - Operates up to 12.5 MHz
- Supports the following management functions via pins if station management is unavailable:
  - Speed select
  - Encoder/decoder bypass
  - Scrambler/descrambler bypass
  - Full duplex
  - Autonegotiation
- Supports half- and full-duplex operations
- Provides four status signals: receive/transmit activity, full duplex, link integrity, and speed indication
- Powerdown mode for 10 Mbits/s and 100 Mbits/s operation
- Loopback for 10 Mbits/s and 100 Mbits/s operation
- 0.35  $\mu\text{m}$  low-power CMOS technology
- 64-pin TQFP
- Single 5 V power supply

\* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Note: Advisories are issued as needed to update product information. When using this data sheet for design purposes, please contact your Lucent Technologies Microelectronics Group Account Manager to obtain the latest advisory on this product.

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## Description

The LU6612 is a single-channel, single-chip complete transceiver designed specifically for dual-speed 10Base-T and 100Base-TX repeaters and switches.

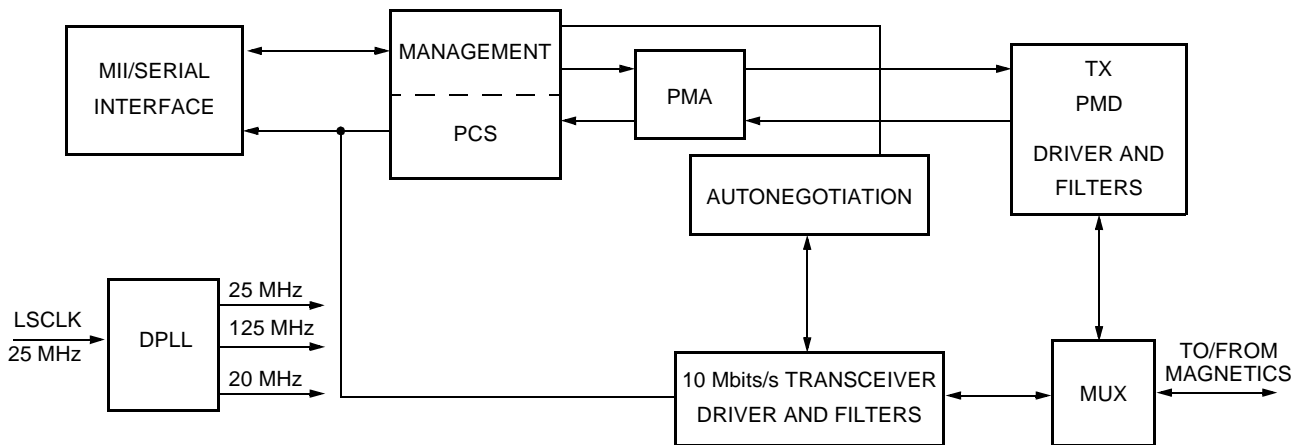
LU6612 implements:

- The 10Base-T transceiver function of *IEEE* 802.3u.
- The physical coding sublayer (PCS) of *IEEE* 802.3u.
- The physical medium attachment (PMA) of *IEEE* 802.3u.

- Autonegotiation of *IEEE* 802.3u.
- MII management of *IEEE* 802.3u.
- Physical medium dependent (PMD) of *IEEE* 802.3u.

This device supports operation over category 3 unshielded twisted-pair (UTP) cable, according to *IEEE* 802.3u 10Base-T specification, and over category 5, Type 1, UTP and Type 1 shielded twisted-pair cable, according to *IEEE* 802.3u 100Base-X specification.

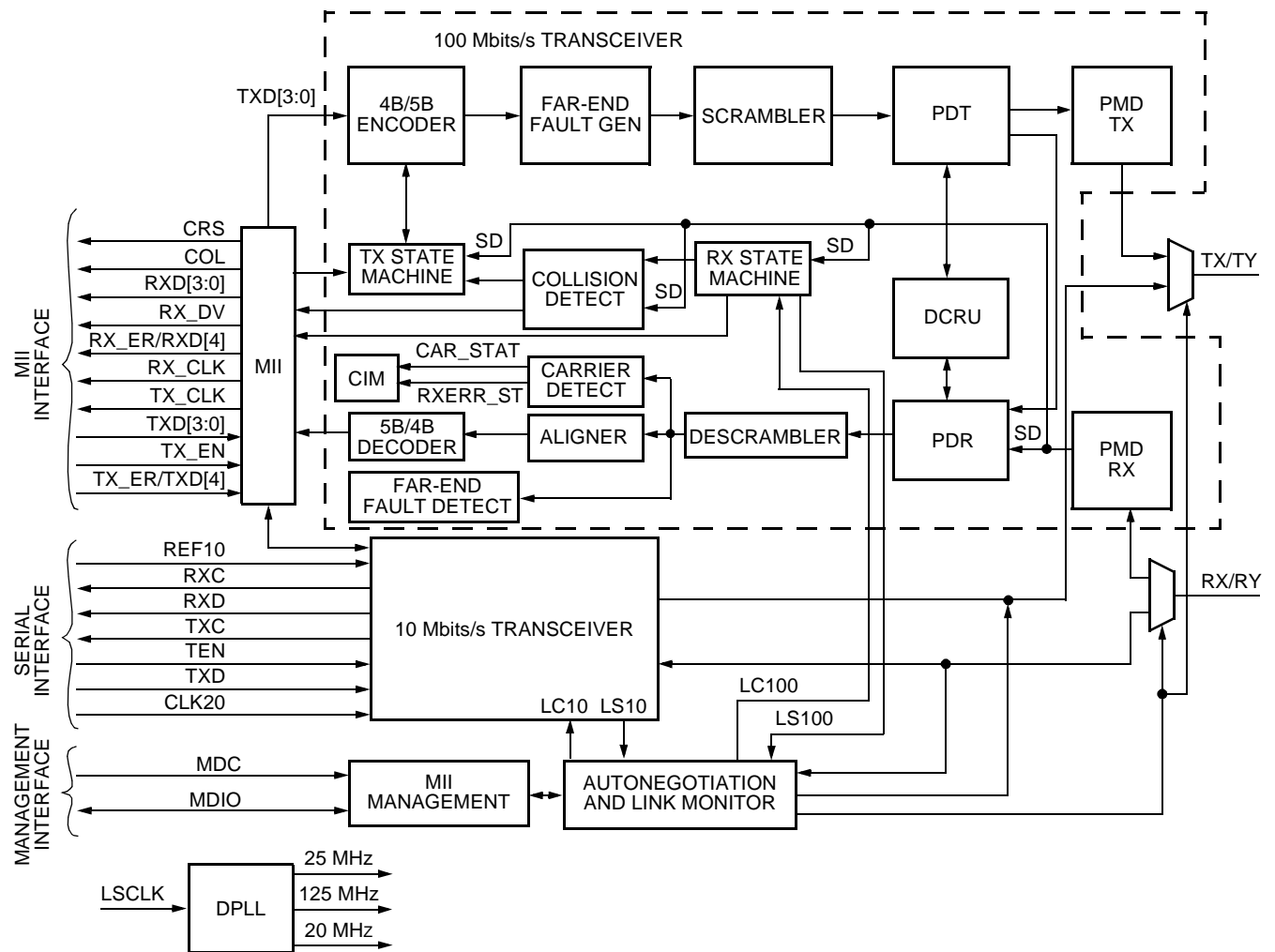
Figure 1 illustrates a functional overview of the LU6612 while Figure 2 details the functions. Figure 3 shows how the LU6612 interfaces to the twisted pair.



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Figure 1. Functional Block Diagram: Device Overview

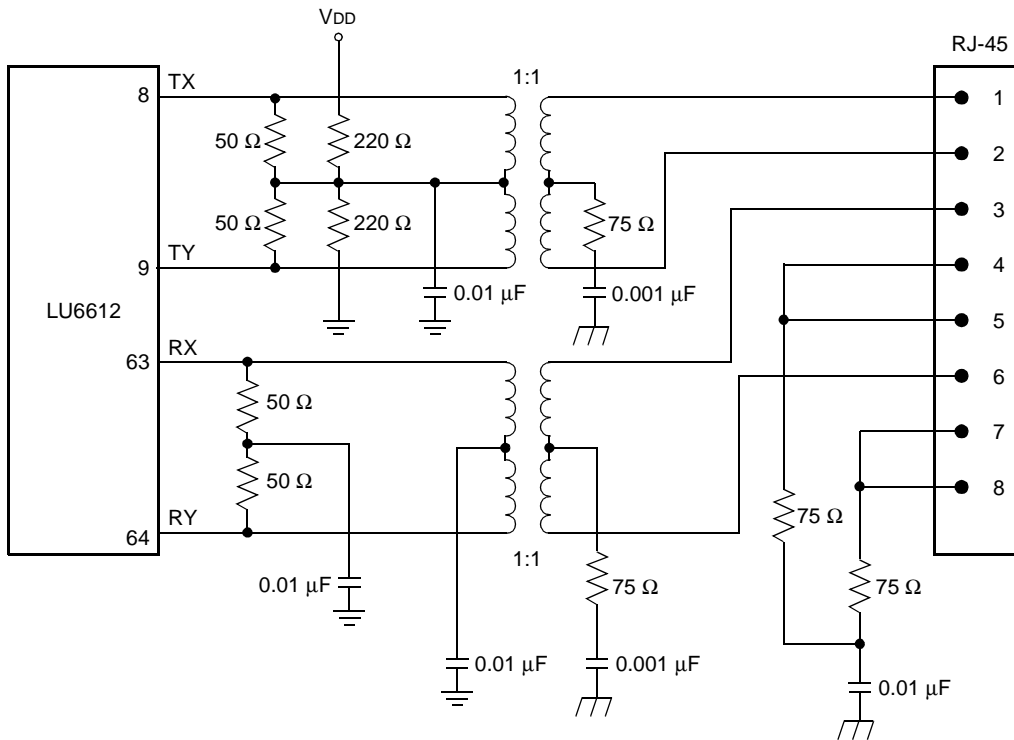
Description (continued)



5-5136(F).cr1

Figure 2. Functional Block Diagram: Device Detail

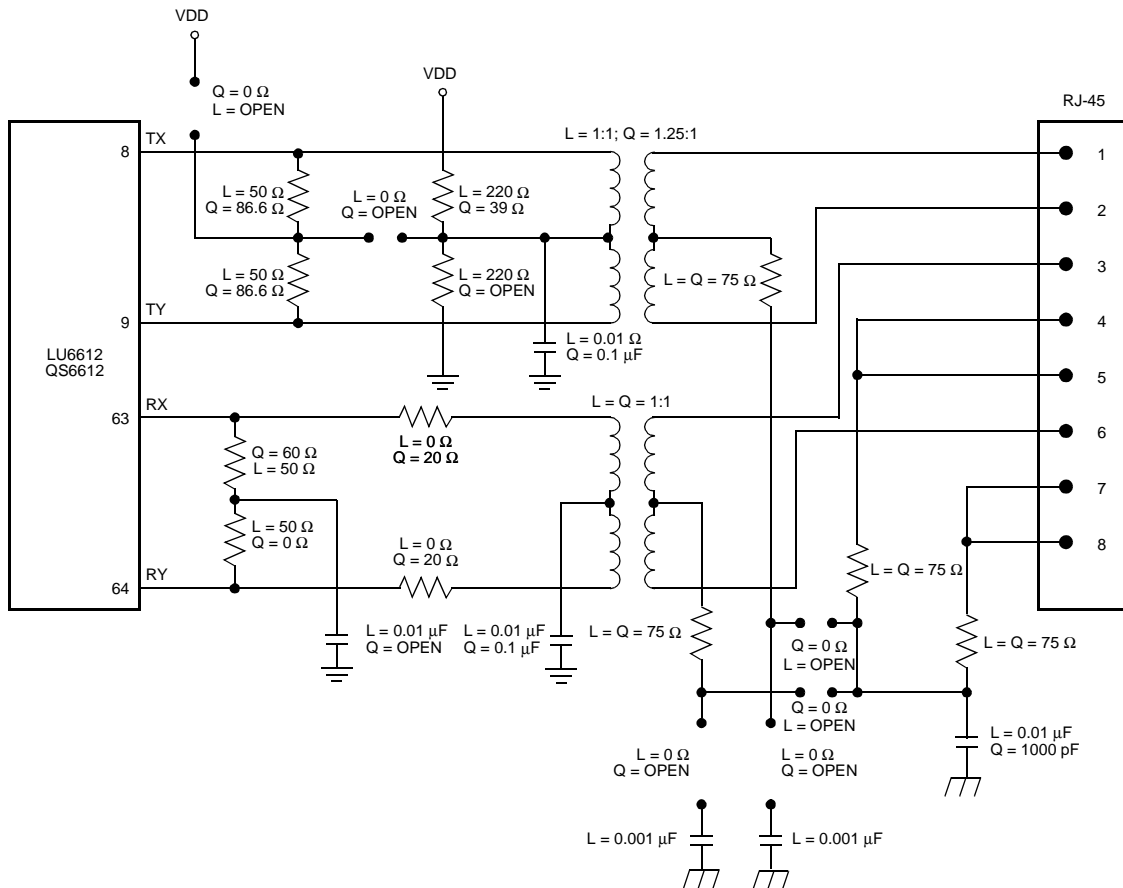
Description (continued)



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Figure 3. Typical Twisted-Pair (TP) Interface

Description (continued)



Key:

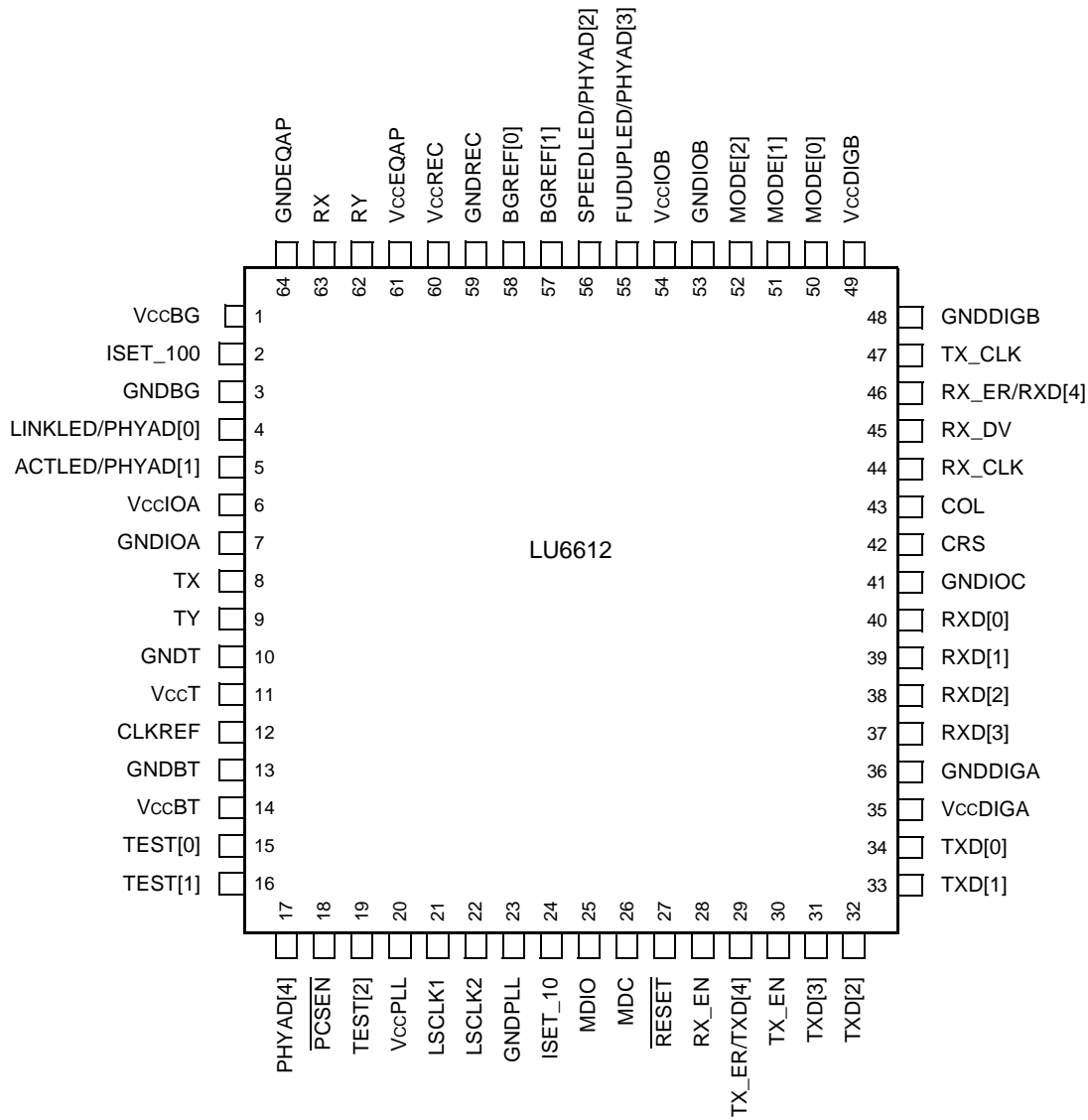
L = Lucent's LU6612.

Q = Quality Semiconductor Inc. QS6612.

Figure 4. Onboard Universal Twisted-Pair Interface Circuit to Interchange Lucent and Quality Semiconductor Inc. Parts

5-5433j

Pin Information



5-5866.r2

Figure 5. LU6612 Pinout



Pin Information (continued)

Pin Descriptions

Table 1. MII/Serial Interface Pins (17)

Signal	Type	Pin	Description
COL	O	43	<b>Collision Detect.</b> This signal signifies in half-duplex mode that a collision has occurred on the network. COL is asserted high whenever there is transmit and receive activity on the UTP media. COL is the logical AND of TX_EN and receive activity, and is an asynchronous output. When SERIAL_SEL (register 30, bit 1) is high and in 10Base-T mode, this signal indicates the jabber timer has expired. This signal is held low in full-duplex mode.
CRS	O	42	<b>Carrier Sense.</b> When CRS_SEL (register 29, bit 10) is low, CRS is asserted high when either the transmit or receive is nonidle. This signal remains asserted throughout a collision condition. When CRS_SEL (register 29, bit 10) is high, CRS is asserted on receive activity only.
RX_CLK	O	44	<b>Receive Clock.</b> 25 MHz clock output in 100 Mbps mode, 2.5 MHz output in 10 Mbps nibble mode, 10 MHz in 10 Mbps serial mode. RX_CLK has a worst-case 45/55 duty cycle. RX_CLK provides the timing reference for the transfer of RX_DV, RXD, and RX_ER signals.
RXD[3:0]	O	37:40	<b>Receive Data.</b> 4-bit parallel data outputs that are synchronous to the falling edge of RX_CLK. When RX_ER is asserted high in 100 Mbps mode, an error code will be presented on RXD[3:0] where appropriate. The codes are as follows: <ul style="list-style-type: none"> <li>■ Packet errors: ERROR_CODES = 2h;</li> <li>■ Link errors: ERROR_CODES = 3h (Packet and link error codes will only be repeated if registers [29.9] and [29.8] are enabled.);</li> <li>■ Premature end errors: ERROR_CODES = 4h;</li> <li>■ Code errors: ERROR_CODES = 5h.</li> </ul> When SERIAL_SEL (register 30, bit 1) is active-high and 10 Mbps mode is selected, RXD[0] is used for data output and RXD[3:1] are 3-stated.
RX_DV	O	45	<b>Receive Data Valid.</b> When this pin is high, it indicates the LU6612 is recovering and decoding valid nibbles on RXD[3:0], and the data is synchronous with RX_CLK. RX_DV is synchronous with RX_CLK. This pin is not used in serial 10 Mbps mode.
RX_ER/ RXD[4]	O	46	<b>Receive Error.</b> When high, RX_ER indicates the LU6612 has detected a coding error in the frame presently being transferred. RX_ER is synchronous with RX_CLK. When the encode/decode bypass (EDB) is selected through the MII management interface, this output serves as the RXD[4] output. This pin is only valid when LU6612 is in 100 Mbps mode.
TX_CLK	O	47	<b>Transmit Clock.</b> 25 MHz clock output in 100 Mbps mode, 2.5 MHz output in 10 Mbps MII mode, 10 MHz output in 10 Mbps serial mode. TX_CLK provides timing reference for the transfer of the TX_EN, TXD, and TX_ER signals. These signals are sampled on the rising edge of TX_CLK.
TXD[3:0]	I	31:34	<b>Transmit Data.</b> 4-bit parallel input synchronous with TX_CLK. When SERIAL_SEL (register 30, bit 1) is active-high and 10 Mbps mode is selected, only TXD[0] is valid.
TX_EN	I	30	<b>Transmit Enable.</b> When driven high, this signal indicates there is valid data on TXD[3:0]. TX_EN is synchronous with TX_CLK. When SERIAL_SEL (register 30, bit 1) is active-high and 10 Mbps mode is selected, this pin indicates there is valid data on TXD[0].

Pin Information (continued)

Table 1. MII/Serial Interface Pins (17) (continued)

Signal	Type	Pin	Description
TX_ER/ TXD[4]	I	29	<b>Transmit Coding Error.</b> When driven high, this signal causes the encoder to intentionally corrupt the byte being transmitted across the MII (00100 will be transmitted). When the encoder/decoder bypass bit is set, this input serves as the TXD[4] input. When in 10 Mbits/s mode and SERIAL_SEL (register 30, bit 1) is active-high, this pin is ignored.
RX_EN	I	28	<b>Receive Enable.</b> When this pin is high, the outputs (RXD[3:0], RX_ER, RX_CLK, RX_DV) are enabled. This pin has an internal 100 kΩ pull-up resistor.

Table 2. MII Management Pins (2)

Signal	Type	Pin	Description
MDC	I	26	<b>Management Data Clock.</b> This is the timing reference for the transfer of data on the MDIO signal. This signal may be asynchronous to RX_CLK and TX_CLK. The standard clock rate is 2.5 MHz, the maximum clock rate is 12.5 MHz. When running MDC above 6.25 MHz, MDC must be synchronous with LSCLK and have a setup time of 15 ns and a hold time of 5 ns with respect to LSCLK.
MDIO	IO	25	<b>Management Data Input/Output.</b> This I/O is used to transfer control and status information between LU6612 and the station management. Control information is driven by the station management synchronous with MDC. Status information is driven by the LU6612 synchronous with MDC.

Table 3. 10/100 Mbits/s Twisted-Pair (TP) Interface Pins (4)

Signal	Type	Pin	Description
RX	I	63	<b>Received Data.</b> Positive differential received 125 Mbaud MLT3 or 10 Mbaud Manchester data from magnetics.
RY	I	62	<b>Received Data.</b> Negative differential received 125 Mbaud MLT3 or 10 Mbaud Manchester data from magnetics.
TX	O	8	<b>Transmit Data.</b> Positive differential transmit 125 Mbaud MLT3 or 10 Mbaud Manchester data to magnetics.
TY	O	9	<b>Transmit Data.</b> Negative differential transmit 125 Mbaud MLT3 or 10 Mbaud Manchester data to magnetics.

**Pin Information** (continued)

**Table 4. Ground and Power Pins (21)**

Signal	Type	Pin	Description
VccIOA	PWR	6	Digital +5 V power supply for I/O
GNDIOA	PWR	7	Digital ground for I/O
VccIOB	PWR	54	Digital +5 V power supply for I/O
GNDIOB	PWR	53	Digital ground for I/O
GNDIOC	PWR	41	Digital ground for I/O
VccDIGA	PWR	35	Digital +5 V power supply for logic
GNDDIGA	PWR	36	Digital ground for logic
VccDIGB	PWR	49	Digital +5 V power supply for logic
GNDDIGB	PWR	48	Digital ground for logic
VccREC	PWR	60	Digital +5 V power supply for clock recovery circuit
GNDREC	PWR	59	Digital ground for clock recovery circuit
VccPLL	PWR	20	Analog +5 V power supply for 10 MHz and 100 MHz PLL clock synthesizer
GNDPLL	PWR	23	Analog ground for 10 MHz and 100 MHz PLL clock synthesizer
VccT	PWR	11	Analog +5 V power supply for transmitter
GNDT	PWR	10	Analog ground for transmitter
VccEQAP	PWR	61	Analog +5 V power supply for equalizer and adaptation circuit
GNDEQAP	PWR	64	Analog ground for adaptation circuit.
VccBG	PWR	1	Analog +5 V power supply for band-gap circuit
GNDBG	PWR	3	Analog ground band-gap circuit
VccBT	PWR	14	Analog +5 V power supply for 10Base-T transmitter
GNDBT	PWR	13	Analog ground for 10Base-T transmitter

**Table 5. Miscellaneous Pins (20)**

Signal	Type*	Pin	Description
LSCLK1	I	21	<b>Local Symbol Clock.</b> 25 MHz clock, $\pm 100$ ppm, 40%—60% duty cycle. This input is connected to one terminal of a 25 MHz crystal or an external 25 MHz clock source.
LSCLK2	O	22	<b>Local Symbol Clock.</b> 25 MHz crystal feedback. This output is connected to the other terminal of a 25 MHz crystal or an external 25 MHz. If LSCLK1 is driven from an external clock source, LSCLK2 is left unconnected.
LINKLED/ PHYAD[0]	I/O	4	<b>Link LED.</b> This pin indicates good link status. At powerup/reset, this pin is sampled as input and to set the PHYAD[0] bit. If pulled high through a resistor, this pin will set PHYAD[0] to a high or if pulled low through a resistor, will set PHYAD[0] to a zero. When this pin is pulled high the LED output will be active-low, when pulled low the LED output will be active-high.
ACTLED/ PHYAD[1]	I/O	5	<b>Activity LED.</b> This pin indicates transmit/receive activity. At powerup/reset, this pin is sampled as input to set the PHYAD[1] bit. If pulled high through a resistor, this pin will set PHYAD[1] to a high or if pulled low through a resistor, will set PHYAD[1] to a zero. When this pin is pulled high the LED output will be active-low, when pulled low the LED output will be active-high.

\* ↑ indicates there is an internal pull-up; ↓ indicates there is an internal pull-down.

Pin Information (continued)

Table 5. Miscellaneous Pins (20) (continued)

Signal	Type*	Pin	Description
SPEED-LED/ PHYAD[2]	I/O	56	<b>Speed LED.</b> This pin indicates the operating speed of LU6612: <ul style="list-style-type: none"> <li>■ LED is active when in 100 Mbps/s operation.</li> <li>■ LED is not active when in 10 Mbps/s operation.</li> </ul> At powerup/reset, this pin is sampled as input and to set the PHYAD[2] bit. If pulled high through a resistor, this pin will set PHYAD[2] to a high or if pulled low through a resistor, will set PHYAD[2] to a zero. When this pin is pulled high, the LED output will be active-low, when pulled low, the LED output will be active-high.
FUDU- PLED/ PHYAD[3]	I/O	55	<b>Full-Duplex LED.</b> This pin indicates the operating mode of LU6612 and is only valid when link is up: <ul style="list-style-type: none"> <li>■ LED is active when in full-duplex mode of operation.</li> <li>■ LED is not active when in half-duplex mode of operation.</li> </ul> At powerup/reset, this pin is sampled as an input to set the PHYAD[3] bit. If pulled high through a resistor, this pin will set PHYAD[3] to a high or if pulled low through a resistor, will set PHYAD[3] to a zero. When this pin is pulled high, the LED output will be active-low, when pulled low, the LED output will be active-high.
PHYAD[4]	↑	17	<b>PHYAD[4].</b> At powerup/reset, this pin is sampled as an input to set the PHYAD[4] bit. If pulled high through a resistor, this pin will set PHYAD[4] to a high or if pulled low through a resistor, will set PHYAD[4] to a zero. This pin has an internal 100 kΩ pull-up resistor.
MODE[2:0]	↑	52:50	<b>Mode Selection.</b> These pins carry encoded signals that are latched into the LU6612 upon powerup/reset and define specific modes of operation: half/full duplex, autonegotiation enabled/disabled, and transceiver isolation. Refer to Table 20 for the various modes and how various registers are affected. Pins [52:50] have internal 100 kΩ pull-ups. If left floating, LU6612 will default to all capable, autonegotiation enabled mode.
TEST[0]	↑	15	<b>Test Enable Pin for Factory Testing.</b> This pin has an internal 100 kΩ pull-down resistor. The pin can be either left floating or tied down.
TEST[2:1]	↓	19, 16	<b>Test Enable Pin for Factory Testing.</b> These two pins have internal 50 kΩ pull-down resistors. These pins can either be left floating or tied low.
CLKREF	I	12	<b>Clock Reference.</b> Connect this pin to a 1 nF ± 10% capacitor to ground.
RESET	I	27	<b>Full Chip Reset (Active-Low).</b> Reset is an active-low signal. Reset must be asserted low for at least five LSCLK cycles. The LU6612 will come out of reset after 400 μs. LSCLK1 must remain running during reset.
BGREF[1:0]	I	57:58	<b>Band-Gap Reference.</b> Connect these pins to a 24.9 kΩ ± 1% resistor to ground. The parasitic load capacitance should be less than 15 pF.
ISET_100	I	2	<b>Current Set 100 Mbps/s.</b> An external reference resistor (24.9 kΩ) is placed from this pin to ground to set the 100 Mbps/s TP driver transmit output level.
ISET_10	I	24	<b>Current Set 10 Mbps/s.</b> An external reference resistor (22.1 kΩ) is placed from this pin to ground to set the 10 Mbps/s TP driver transmit output level.
PCSEN	↑	18	<b>PCS Enable (Active-Low).</b> When this pin is active-low, the encoded 5-bit symbols appear on RXD[4:0] and TXD[4:0]. When this pin high, 4-bit data appears on RXD[3:0] and TXD[3:0]. When PCSEN is low, LU6612 bypasses the 4B5B encoder/decoder, the align function, the scrambler/descrambler, and does not detect and generate J/K and R/T code groups at the start or end of frame. This pin has an internal 100 kΩ pull-up.

\* ↑ indicates there is an internal pull-up; ↓ indicates there is an internal pull-down.

## MII Station Management

### Basic Operations

The primary function of station management is to transfer control and status information about the LU6612 to a management entity. This function is accomplished by the MDC clock input, which has a maximum frequency of 12.5 MHz, along with the MDIO pin. The management interface (MII) uses MDC and MDIO to physically transport information between the PHY and the station management entity.

A specific set of registers and their contents (described in Table 8) defines the nature of the information transferred across this interface. Frames transmitted on the MII management interface will have the frame structure shown in Table 6. The order of bit transmission is from left to right. Note that reading and writing of the management register must be completed without interruption.

### MII Management Frames

The fields and format for management frames are described in the following tables.

**Table 6. MII Management Frame Fields and Format**

Read/Write (R/W)	Pre	ST	OP	PHYADD	REGAD	TA	DATA	Idle
R	1 . . . 1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDDDD	Z
W	1 . . . 1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDDDD	Z

**Table 7. MII Management Frame Descriptions**

Field	Description
Pre	<b>Preamble.</b> The preamble is a series of 32 1s. The LU6612 will accept frames with no preamble. This is indicated by a 1 in register 1, bit 6.
ST	<b>Start of Frame.</b> The start of frame is indicated by a 01 pattern.
OP	<b>Operation Code.</b> The operation code for a read transaction is 10. The operation code for a write transaction is 01.
PHYADD	<b>PHY Address.</b> The PHY address is 5 bits, allowing for 32 unique addresses. The first PHY address bit transmitted and received is the MSB of the address. A station management entity, which is attached to multiple PHY entities, must have prior knowledge of the appropriate PHY address for each entity. The address 00000 is the broadcast address. This address will produce a match regardless of the local address.
REGAD	<b>Register Address.</b> The register address is 5 bits, allowing for 32 unique registers within each PHY. The first register address bit transmitted and received is the MSB of the address.
TA	<b>Turnaround.</b> The turnaround time is a 2-bit time spacing between the register address field and the data field of a frame to avoid drive contention on MDIO during a read transaction. During a write to the LU6612, these bits are driven to a 10 by the station. During a read, the MDIO is not driven during the first bit time and is driven to a 0 by the LU6612 during the second bit time.
DATA	<b>Data.</b> The data field is 16 bits. The first bit transmitted and received is bit 15 of the register being addressed.

**MII Station Management** (continued)

**Register Overview**

The MII management 16-bit register (MR) set is implemented as described in Table 8 below.

**Table 8. MII Management Registers (MR)**

Register Address	Symbol	Name	Default (Hex Code)
0	MR0	Control Register	3000
1	MR1	Status Register	7849
2	MR2	PHY Identifier Register 1	0180
3	MR3	PHY Identifier Register 2	7641
4	MR4	Autonegotiation Advertisement Register	01E1
5	MR5	Autonegotiation Link Partner Ability Register (Base_Page)	0000
5	MR5	Autonegotiation Link Partner Ability Register (Next_Page)	—
6	MR6	Autonegotiation Expansion Register	0000
7	MR7	Next-Page Transmit Register	0000
8—27	MR8—MR27	Reserved	0000
28	MR28	Device Specific Register 1	0000
29	MR29	Device Specific Register 2	1000
30	MR30	Device Specific Register 3	0000

## MII Station Management (continued)

This section provides a detailed discussion of each management register and its bit definitions.

**Table 9. MR0—Control Register Bit Descriptions**

Bit <sup>1</sup>	Type <sup>2</sup>	Description
0.15 (SW_RESET)	R/W	<b>Reset.</b> Setting this bit to a 1 will reset the LU6612. All registers will be set to their default state. This bit is self-clearing. The default is 0.
0.14 (LOOPBACK)	R/W	<b>Loopback.</b> When this bit is set to 1, no data transmission will take place on the media. Any receive data will be ignored. The loopback signal path will contain all circuitry up to, but not including, the PMD. The autonegotiation must be turned off, before loopback can be initiated, transmit data can be started 2 ms after loopback is initiated. The default value is a 0.
0.13 (SPEED100)	R/W	<b>Speed Selection.</b> The value of this bit reflects the current speed of operation (1 = 100 Mbits/s; 0 = 10 Mbits/s). This bit will only affect operating speed when the autonegotiation enable bit (register 0, bit 12) is disabled (0). This bit is ignored when autonegotiation is enabled (register 0, bit 12). The bit is set high when MODE[2:0] is 010 or 011 or 100. The default is 1.
0.12 (NWAY_ENA)	R/W	<b>Autonegotiation Enable.</b> The autonegotiation process will be enabled by setting this bit to a 1. This bit overrides SPEED100 bit (register 0, bit 13) and FULL_DUP bit (register 0, bit 8). This bit is set high when MODE[2:0] is 100 or 111. Autonegotiation must be disabled before loopback can be initiated. The default state is a 1.
0.11 (PWRDN)	R/W	<b>Powerdown.</b> The LU6612 may be placed in a low-power state by setting this bit to a 1, both the 10 Mbits/s transceiver and the 100 Mbits/s transceiver will be powered down. While in the powerdown state, the LU6612 will respond to management transactions. The default state is a 0.
0.10 (ISOLATE)	R/W	<b>Isolate.</b> When this bit is set to a 1, the MII outputs will be brought to the high-impedance state. The default state is a 0.
0.9 (REDONWAY)	R/W	<b>Restart Autonegotiation.</b> Normally, the autonegotiation process is started at powerup. The process may be restarted by setting this bit to a 1. The default state is a 0. The NWAYDONE bit (register 1, bit 5) is reset when this bit goes to a 1. This bit is self-cleared when autonegotiation restarts.
0.8 (FULL_DUP)	R/W	<b>Duplex Mode.</b> This bit reflects the mode of operation (1 = full duplex; 0 = half duplex). This bit is ignored when the autonegotiation enable bit (register 0, bit 12) is enabled. The default state is a 0. This bit is set as a 1 during powerup/reset, when MODE[2:0] is 001 or 011.
0.7 (COLTST)	R/W	<b>Collision Test.</b> When this bit is set to a 1, the LU6612 will assert the COL signal in response to TX_EN. This bit should only be set when in loopback mode.
0.6:0	NA	<b>Reserved.</b> All bits will read 0.

1. Note that the format for the pin descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.

2. R = read, W = write, NA = not applicable.

MII Station Management (continued)

Table 10. MR1—Status Register Bit Descriptions

Bit <sup>1</sup>	Type <sup>2</sup>	Description
1.15 (T4ABLE)	R	<b>100Base-T4 Ability.</b> This bit will always be a 0. 0: Not able 1: Able
1.14 (TXFULDUP)	R	<b>100Base-TX Full-Duplex Ability.</b> This bit will always be a 1. 0: Not able 1: Able
1.13 (TXHAFDUP)	R	<b>100Base-TX Half-Duplex Ability.</b> This bit will always be a 1. 0: Not able 1: Able
1.12 (ENFULDUP)	R	<b>10Base-T Full-Duplex Ability.</b> This bit will always be a 1. 0: Not able 1: Able
1.11 (ENHAFDUP)	R	<b>10Base-T Half-Duplex Ability.</b> This bit will always be a 1. 0: Not able 1: Able
1.10:7	R	<b>Reserved.</b> All bits will read as a 0.
1.6 (NO_PA_OK)	R	<b>Suppress Preamble.</b> This bit is set to a 1, indicating that the LU6612 accepts management frames with the preamble suppressed. (This function is not supported by QS6611.)
1.5 (NWAYDONE)	R	<b>Autonegotiation Complete.</b> When this bit is a 1, it indicates the autonegotiation process has been completed. The contents of registers MR4, MR5, MR6, and MR7 are now valid. The default value is a 0. This bit is reset when autonegotiation is started.
1.4 (REM_FLT)	R	<b>Remote Fault.</b> When this bit is a 1, it indicates a remote fault has been detected. This bit will remain set until cleared by reading the register. The default is a 0.
1.3 (NWAYABLE)	R	<b>Autonegotiation Ability.</b> When this bit is a 1, it indicates the ability to perform autonegotiation. The value of this bit is always a 1.
1.2 (LSTAT_OK)	R	<b>Link Status.</b> When this bit is a 1, it indicates a valid link has been established. This bit has a latching function: a link failure will cause the bit to clear and stay cleared until it has been read via the management interface.
1.1 (JABBER)	R	<b>Jabber Detect.</b> This bit will be a 1 whenever a jabber condition is detected. It will remain set until it is read, and the jabber condition no longer exists.
1.0 (EXT_ABLE)	R	<b>Extended Capability.</b> This bit indicates that the LU6612 supports the extended register set (MR2 and beyond). It will always read a 1.

1. Note that the format for the pin descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.

2. R = read.



## MII Station Management (continued)

**Table 11. MR2, 3—PHY Identifier Registers (1 and 2) Bit Descriptions**

Bit <sup>1</sup>	Type <sup>2</sup>	Description
2.15:0 (OUI[3:18])	R	<b>Organizationally Unique Identifier.</b> The third through the 24th bits of the OUI assigned to the PHY manufacturer by the <i>IEEE</i> are to be placed in bits 2.15:0 and 3.15:10. The value for bits 15:0 of register 2 is 0180h.
3.15:10 (OUI[19:24])	R	<b>Organizationally Unique Identifier.</b> The remaining 6 bits of the OUI. The value for bits 15:10 of register 3 is 1Dh.
3.9:4 (MODEL[5:0])	R	<b>Model Number.</b> 6-bit model number of the device. The model number is 12 decimal.
3.3:0 (VERSION[3:0])	R	<b>Revision Number.</b> The value of the present revision number. The value is 0001b for the first version.

1. Note that the format for the pin descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.

2. R = read.

**Table 12. MR4—Autonegotiation Advertisement Register Bit Descriptions**

Bit <sup>1</sup>	Type <sup>2</sup>	Description
4.15 (NEXT_PAGE)	R/W	<b>Next Page.</b> The next page function is activated by setting this bit to a 1. This will allow the exchange of arbitrary pieces of data. Data is carried by optional next pages of information. (This function is not supported by QS6611.)
4.14 (ACK)	R/W	<b>Acknowledge.</b> This bit is written to a logic zero and ignored on read.
4.13 (REM_FAULT)	R/W	<b>Remote Fault.</b> When set to 1, the LU6612 indicates to the link partner a remote fault condition.
4.12:10 (PAUSE)	R/W	<b>Pause.</b> When set to 1, indicates that the LU6612 wishes to exchange flow control information with its link partner.
4.9 (100BASET4)	R/W	<b>100Base-T4.</b> This bit should always be set to a 0.
4.8 (100BASET_FD)	R/W	<b>100Base-TX Full Duplex.</b> If written to 1, autonegotiation will advertise that the LU6612 is capable of 100Base-TX full-duplex operation. This bit is set high when MODE[2:0] is 111.
4.7 (100BASETX)	R/W	<b>100Base-TX.</b> If written to 1, autonegotiation will advertise that the LU6612 is capable of 100Base-TX operation.
4.6 (10BASET_FD)	R/W	<b>10Base-T Full Duplex.</b> If written to 1, autonegotiation will advertise that the LU6612 is capable of 10Base-T full-duplex operation. This bit is set high when MODE[2:0] is 111.
4.5 (10BASET)	R/W	<b>10Base-T.</b> If written to 1, autonegotiation will advertise that the LU6612 is capable of 10Base-T operation. This bit is set high when MODE[2:0] is 111.
4.4:0 (SELECT)	R/W	<b>Selector Field.</b> Reset with the value 00001 for <i>IEEE</i> 802.3.

1. Note that the format for the pin descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.

2. R = read, W = write.

MII Station Management (continued)

Table 13. MR5—Autonegotiation Link Partner (LP) Ability Register Bit Descriptions (Base\_Page)

Bit <sup>1</sup>	Type <sup>2</sup>	Description
5.15 (LP_NEXT_PAGE)	R	<b>Link Partner Next Page.</b> When this bit is set to 1, it indicates that the link partner wishes to engage in next page exchange.
5.14 (LP_ACK)	R	<b>Link Partner Acknowledge.</b> When this bit is set to 1, it indicates that the link partner has successfully received at least three consecutive and consistent FLP bursts.
5.13 (LP_REM_FAULT)	R	<b>Link Partner Remote Fault.</b> When this bit is set to 1, it indicates that the link partner has a fault.
5.12:10	R	<b>Reserved.</b> These bits are reserved.
5.9 (LP_100BASET4)	R	<b>Link Partner 100Base-T4.</b> When this bit is set to 1, it indicates that link partner is capable of 100Base-T4 operation.
5.8 (LP_100BASET_FD)	R	<b>Link Partner 100Base-TX Full Duplex.</b> When this bit is set to 1, it indicates that link partner is capable of 100Base-TX full-duplex operation.
5.7 (LP_100BASETX)	R	<b>Link Partner 100Base-TX.</b> When this bit is set to 1, it indicates that link partner is capable of 100Base-TX operation.
5.6 (LP_10BASET_FD)	R	<b>Link Partner 10Base-T Full Duplex.</b> When this bit is set to 1, it indicates that link partner is capable of 10Base-T full-duplex operation.
5.5 (LP_10BASET)	R	<b>Link Partner 10Base-T.</b> When this bit is set to 1, it indicates that link partner is capable of 10Base-T operation.
5.4:0 (LP_SELECT)	R	<b>Selector Field.</b> This field contains the type of message sent by the link partner. For <i>IEEE</i> 802.3 compliant link partners, this field should read 00001.

1. Note that the format for the pin descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.

2. R = read.

Table 14. MR5—Autonegotiation Link Partner (LP) Ability Register Bit Descriptions (Next\_Page)

Bit <sup>1</sup>	Type <sup>2</sup>	Description
5.15 (LP_NEXT_PAGE)	R	<b>Next Page.</b> When this bit is set to a logic 0, it indicates that this is the last page to be transmitted. A logic 1 indicates that additional pages will follow.
5.14 (LP_ACK)	R	<b>Acknowledge.</b> When this bit is set to a logic 1, it indicates that the link partner has successfully received its partner's link code word.
5.13 (LP_MES_PAGE)	R	<b>Message Page.</b> This bit is used by the Next_Page function to differentiate a Message Page (logic one) from an unformatted page (logic zero).
5.12 (LP_ACK2)	R	<b>Acknowledge 2.</b> This bit is used by Next_Page function to indicate that a device has the ability to comply with the message (logic one) or not (logic zero).
5.11 (LP_TOGGLE)	R	<b>Toggle.</b> This bit is used by the arbitration function to ensure synchronization with the link partner during next page exchange. Logic 0 indicates that the previous value of the transmitted link code word was logic 1. Logic 1 indicates that the previous value of the transmitted link code word was logic 0.
5.10:0 (MCF)	R	<b>Message/Unformatted Code Field.</b> With these 11 bits, there are 2048 possible messages. Message code field definitions are described in annex 28C of the <i>IEEE</i> 802.3u standard.

1. Note that the format for the pin descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.

2. R = read.

## MII Station Management (continued)

**Table 15. MR6—Autonegotiation Expansion Register Bit Descriptions**

Bit <sup>1</sup>	Type <sup>2</sup>	Description
6.15:5	R	<b>Reserved.</b>
6.4 (PAR_DET_FAULT)	R/LH	<b>Parallel Detection Fault.</b> When this bit is set to 1, it indicates that a fault has been detected in the parallel detection function. This fault is due to more than one technology detecting concurrent link conditions. This bit can only be cleared by reading this register.
6.3 (LP_NEXT_PAGE_ABLE)	R	<b>Link Partner Next Page Able.</b> When this bit is set to 1, it indicates that the link partner supports the next page function.
6.2 (NEXT_PAGE_ABLE)	R	<b>Next Page Able.</b> This bit is set to 1, indicating that this device supports the next page function.
6.1 (PAGE_REC)	R/LH	<b>Page Received.</b> When this bit is set to 1, it indicates that a next page has been received.
6.0 (LP_NWAY_ABLE)	R	<b>Link Partner Autonegotiation Capable.</b> When this bit is set to 1, it indicates that the link partner is autonegotiation capable.

1. Note that the format for the pin descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.

2. R = read, LH = latched high.

**Table 16. MR7—Next\_Page Transmit Register Bit Descriptions**

Bit <sup>1</sup>	Type <sup>2</sup>	Description
7.15 (NEXT_PAGE)	R/W	<b>Next Page.</b> This bit indicates whether or not this is the last next page to be transmitted. When this bit is 0, it indicates that this is the last page. When this bit is 1, it indicates there is an additional next page.
7.14 (ACK)	R	<b>Acknowledge.</b> This bit is the acknowledge bit from the link code word.
7.13 (MESSAGE)	R/W	<b>Message Page.</b> This bit is used to differentiate a message page from an unformatted page. When this bit is 0, it indicates an unformatted page. When this bit is 1, it indicates a formatted page.
7.12 (ACK2)	R/W	<b>Acknowledge 2.</b> This bit is used by the next page function to indicate that a device has the ability to comply with the message. Acknowledge 2 will be set as follows: <ul style="list-style-type: none"> <li>■ When this bit is 0, it indicates the device cannot comply with the message.</li> <li>■ When this bit is 1, it indicates the device will comply with the message.</li> </ul>
7.11 (TOGGLE)	R	<b>Toggle.</b> This bit is used by the arbitration function to ensure synchronization with the link partner during next page exchange. This bit will always take the opposite value of the toggle bit in the previously exchanged link code word: <ul style="list-style-type: none"> <li>■ If the bit is a logic 0, the previous value of the transmitted link code word was a logic 1.</li> <li>■ If the bit is a 1, the previous value of the transmitted link code word was a 0.</li> </ul> The initial value of the toggle bit in the first next page transmitted is the inverse of the value of bit 11 in the base link code word and, therefore, may assume a value of 1 or 0.
7.10:0 (MCF)	R/W	<b>Message/Unformatted Code Field.</b> With these 11 bits, there are 2048 possible messages. Message code field definitions are described in annex 28C of the <i>IEEE 802.3u</i> standard.

1. Note that the format for the pin descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.

2. R = read, W = write.

MII Station Management (continued)

Table 17. MR28—Device-Specific Register 1 (Status Register) Bit Descriptions

Bit <sup>1</sup>	Type <sup>2</sup>	Description
28.15:9 (R28[15:9])	R	<b>Unused.</b> Read as 0.
28.8 (BAD_FRM)	R/LH	<b>Bad Frame.</b> If this bit is a 1, it indicates a packet has been received without an SFD. This bit is only valid in 10 Mb/s mode.  This bit is latching high and will only clear after it has been read or the device has been reset. The default is 0.
28.7 (CODE)	R/LH	<b>Code Violation.</b> When this bit is a 1, it indicates a Manchester code violation has occurred. The error code will be output on the RXD lines. Refer to Table 1 for a detailed description of the RXD pin error codes. This bit is only valid in 10 Mb/s mode.  This bit is latching high and will only clear after it has been read or the device has been reset. The default is 0.
28.6 (APS)	R	<b>Autopolarity Status.</b> When register 30, bit 3 is set and this bit is a 1, it indicates the LU6612 has detected and corrected a polarity reversal on the twisted pair.  If the APF_EN bit (register 30, bit 3) is set, the reversal will be corrected inside the LU6612. This bit is not valid in 100 Mb/s operation. The default is 0.
28.5 (DISCON)	R/LH	<b>Disconnect.</b> If this bit is a 1, it indicates a disconnect. This bit will latch high until read. This bit is only valid in 100 Mb/s mode. The default is 0.
28.4 (UNLOCKED)	R/LH	<b>Unlocked.</b> Indicates that the TX scrambler lost lock. This bit will latch high until read. This bit is only valid in 100 Mb/s mode. The default is 0.
28.3 (RXERR_ST)	R/LH	<b>RX Error Status.</b> Indicates a false carrier. This bit will latch high until read. This bit is only valid in 100 Mb/s mode. The default is 0.
28.2 (FRC_JAM)	R/LH	<b>Force Jam.</b> This bit will latch high until read. This bit is only valid in 100 Mb/s mode. The default is 0.
28.1 (LNK100UP)	R	<b>Link Up 100.</b> This bit, when set to a 1, indicates a 100 Mb/s transceiver is up and operational. The default is 0.
28.0 (LNK10UP)	R	<b>Link Up 10.</b> This bit, when set to a 1, indicates a 10 Mb/s transceiver is up and operational. The default is 0.

1. Note that the format for the pin descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.

2. R = read, LH = latched high.

## MII Station Management (continued)

Table 18. MR29—Device-Specific Register 2 (100 Mbps/s Control) Bit Descriptions

Bit <sup>1</sup>	Type <sup>2</sup>	Description
29.15 (LOCALRST)	R/W	<b>Management Reset.</b> This is the local management reset bit. Writing a logic 1 to this bit will cause the lower 16 registers and registers 28 and 29 to be reset to their default values. This bit is self-clearing. The default is 0.
29.14 (RST1)	R/W	<b>Generic Reset 1.</b> This register is used for manufacture test only. The default is 0.
29.13 (RST2)	R/W	<b>Generic Reset 2.</b> This register is used for manufacture test only. The default is 0.
29.12 (100OFF)	R/W	<b>100 Mbps/s Transmitter Off.</b> When this bit is set to 0, it forces RX low and RY high. This bit defaults to 1.
29.11	R/W	<b>Reserved.</b> Program to zero.
29.10 (CRS_SEL)	R/W	<b>Carrier Sense Select.</b> CRS will be asserted on receive only when this bit is set to a 1. If this bit is set to logic 0, CRS will be asserted on receive or transmit. The default is 0.
29.9 (LINK_ERR)	R/W	<b>Link Error Indication.</b> When this bit is a 1, a link error code will be reported on RXD[3:0] of the LU6612 when RX_ER is asserted on the MII. The specific error codes are listed in the RXD pin description. If it is 0, it will disable this function. The default is 0.
29.8 (PKT_ERR)	R/W	<b>Packet Error Indication Enable.</b> When this bit is a 1, a packet error code, which indicates that the scrambler is not locked, will be reported on RXD[3:0] of the LU6612 when RX_ER is asserted on the MII. When this bit is 0, it will disable this function. The default is 0.
29.7 (RESERVED)	R/W	<b>Reserved.</b> This bit must remain as a zero. The default is 0.
29.6 (EDB)	R/W	<b>Encoder/Decoder Bypass.</b> When this bit is set to 1, the 4B/5B encoder and 5B/4B decoder function will be disabled. The default is a zero. At powerup/reset, if PCSEN is strapped low, then this bit is set to a 1. The default is 0.
29.5 (SAB)	R/W	<b>Symbol Aligner Bypass.</b> When this bit is set to 1, the aligner function will be disabled. The default is 0.
29.4 (SDB)	R/W	<b>Scrambler/Descrambler Bypass.</b> When this bit is set to 1, the scrambling/descrambling functions will be disabled. The default is a zero. At powerup/reset, if PCSEN is strapped low, then this bit is set to a 1. The default is 0.
29.3 (CARIN_EN)	R/W	<b>Carrier Integrity Enable.</b> When this bit is set to a 1, carrier integrity is enabled. (This function is not supported by QS6611.) The default is 0.
29.2 (JAM_COL)	R/W	<b>Jam Enable.</b> When this bit is a 1, it enables JAM associated with carrier integrity to be ORed with COL. The default is 0.
29.1 (RESERVED)	R/W	<b>Reserved.</b> This bit must remain as a zero. The default is 0.
29.0 (RESERVED)	R/W	<b>Reserved.</b> This bit must remain as a zero. The default is 0.

1. Note that the format for the pin descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.

2. R = read, W = write.

MII Station Management (continued)

Table 19. MR30—Device-Specific Register 3 (10 Mbits/s Control) Bit Descriptions

Bit <sup>1</sup>	Type <sup>2</sup>	Description
30.15:6 (R30[15:6])	R/W	<b>Unused.</b> Read as 0.
30.5 (HBT_EN)	R/W	<b>Heartbeat Enable.</b> When this bit is a 1, the heartbeat function will be enabled. Valid in 10 Mbits/s mode only. The default is 0.
30.4 (ELL_EN)	R/W	<b>Extended Line Length Enable.</b> When this bit is a 1, the receive squelch levels are reduced from a nominal 435 mV to 350 mV, allowing reception of signals with a lower amplitude. Valid in 10 Mbits/s mode only. The default is 0.
30.3 (APF_EN)	R/W	<b>Autopolarity Function Enable.</b> When this bit is a 1 and the LU6612 is in 10 Mbits/s mode, the autopolarity function will determine if the TP link is wired with a polarity reversal. If there is a polarity reversal, the LU6612 will assert the APS bit (register 28, bit 6) and correct the polarity reversal. If this bit is a 0 and the device is in 10 Mbits/s mode, the reversal will not be corrected. The default is 0.
30.2 (REF_SEL)	R/W	<b>Reference Select.</b> When this bit is a 1, the external 10 MHz reference of pin REF10 is used for phase alignment. This bit defaults to a 0.
30.1 (SERIAL_SEL)	R/W	<b>Serial Select.</b> When this bit is set to a 1, 10 Mbits/s serial mode will be selected. When the LU6612 is in 100 Mbits/s mode, this bit will be ignored. The default is 0.
30.0 (ENA_NO_LP)	R/W	<b>No Link Partner Mode.</b> Setting this bit to a 1 will allow 10 Mbits/s operation with link pulses disabled. If the LU6612 is configured for 100 Mbits/s operation, setting this bit will not affect operation. The default is 0.

- Note that the format for the pin descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.
- R = read, W = write.

## MODE Selection

LU6612 can be forced to operate in specific operating modes. This is achieved by configuring the MODE pins to the appropriate values at powerup/reset. The strapping options of the MODE pins are latched on reset to set the default values of various registers. The values can be modified by writing into the registers. The MODE[2:0] pins have 100 kΩ internal pull-ups. If MODE[2:0] are left floating, LU6612 will default to all capable, autonegotiation enabled mode.

The different modes of operation of LU6612 and the register bits affected are presented in the following table.

**Table 20. Operation Modes of LU6612**

MODE [2:0]	Definition	Register.Bit						
		0.8	0.10	0.12	0.13	4.5	4.6	4.8
000	10Base-T, half-duplex with autonegotiation disabled	0	0	0	0	1	0	1
001	10Base-T, full-duplex with autonegotiation disabled	1	0	0	0	1	1	1
010	100Base-TX, half-duplex with autonegotiation disabled	0	0	0	1	0	0	1
011	100Base-TX, full-duplex with autonegotiation disabled	1	0	0	1	0	0	1
100	Advertise 100Base-TX, half-duplex autonegotiation enabled	0	0	1	1	0	0	0
101	Reserved	—	—	—	—	—	—	—
110	Isolate MII	0	1	0	1	1	1	0
111	All capable, autonegotiation enabled	0	0	1	1	1	1	1

**Table 21. LU6612 Crystal Specifications**

Parameter	Requirement
Type	Quartz Fundamental Mode
Frequency	25 MHz
Stability	±25 ppm, 0—70 °C
Shunt Capacitor	7 pF
Load Capacitor	20 pF
Series Resistance	<30 Ω

## Absolute Maximum Ratings (T<sub>A</sub> = 25 °C)

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

**Table 22. Absolute Maximum Ratings**

Parameter	Symbol	Min	Max	Unit
Ambient Operating Temperature	T <sub>A</sub>	0	70	°C
Storage Temperature	T <sub>stg</sub>	-40	125	°C
Voltage on Any Pin with Respect to Ground	—	-0.5	V <sub>DD</sub> + 0.5	V
Maximum Supply Voltage	—	—	5.5	V

**Table 23. Operating Conditions**

Parameter	Symbol	Min	Typ*	Max	Unit
Operating Supply Voltage	—	4.75	5.0	5.25	V
Power Dissipation:					
100 Mbits/s TX	P <sub>D</sub>	—	1.4	1.6	W
10 Mbits/s	P <sub>D</sub>	—	1.0	1.35	W
Autonegotiating	P <sub>D</sub>	—	1.0	—	mW

\* Typical power dissipations are specified at 5.0 V and 25 °C. This is the power dissipated by the LU6612 transmitting over 100 meters of cable.

## Electrical Characteristics

The following specifications apply for V<sub>DD</sub> = 5 V ± 5%.

**Table 24. dc Characteristics**

Parameter	Symbol	Min	Typ	Max	Unit
TTL Inputs:					
Input High Voltage	V <sub>IH</sub>	2.0	—	—	V
Input Low Voltage	V <sub>IL</sub>	—	—	0.8	V
Input High Current	I <sub>IH</sub>	—	—	50	μA
Input Low Current	I <sub>IL</sub>	—	—	-400	μA
Input Leakage Current	I <sub>L</sub>	—	—	50	μA
TTL Outputs:					
Output High Voltage	V <sub>OH</sub>	2.4	—	—	V
Output Low Voltage	V <sub>OL</sub>	—	—	0.45	V
Output Short-circuit Current	I <sub>sc</sub>	-15	—	-85	mA
10 Mbits/s Twisted Pair: Input Voltage	V <sub>DIFF</sub>	0.35	—	2.0	V
100 Mbits/s Twisted Pair: Input Voltage	V <sub>DIFF</sub>	—	—	1.5	V
10 Mbits/s Twisted Pair: Output Current	V <sub>DIFF</sub>	45	50	55	mA
100 Mbits/s Twisted Pair: Output Current	V <sub>DIFF</sub>	19	20	21	mA



## Timing Characteristics (Preliminary)

Table 25. MII Management Interface Timing (25 pF Load)

Name	Parameter	Min	Typ	Max	Unit
t1	MDIO Valid to Rising Edge of MDC (setup)	10	—	—	ns
t2	Rising Edge of MDC to MDIO Invalid (hold)	10	—	—	ns
t3	MDC Falling Edge to MDIO Valid (prop. delay)	0	—	40	ns
t4	MDC High*	—	200	—	ns
t5	MDC Low*	40	200	—	ns
t6	MDC Period*	80	400	—	ns

\* When operating MDC above 6.25 MHz, MDC must be synchronous with LSCLK and have a setup time of 15 ns and a hold time of 5 ns, with respect to LSCLK.

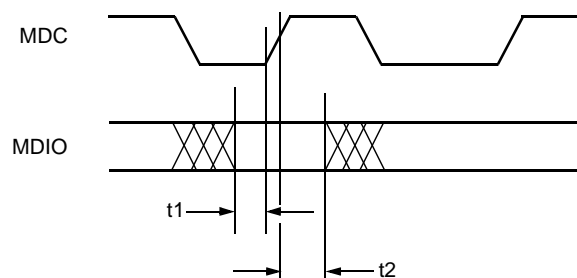


Figure 6. MDIO Input Timing

5-4959(F).a

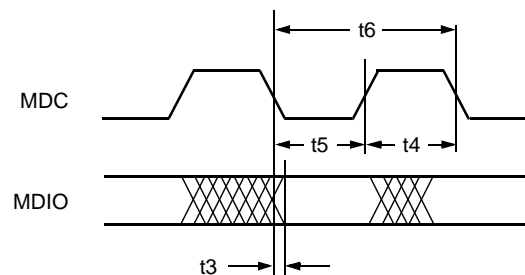
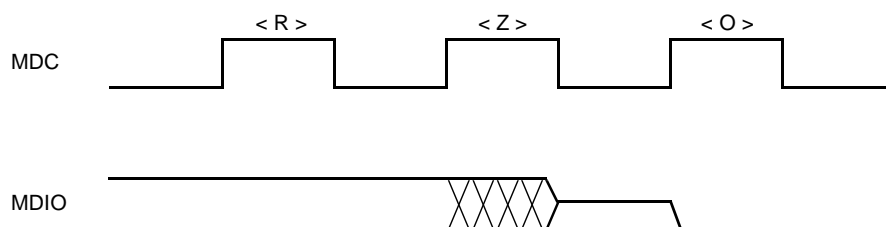


Figure 7. MDIO Output Timing

5-4960(F).c



5-5312(F).r1

Note: MDIO turnaround (TA) time is a 2-bit time spacing between the register address field, and the data field of a frame to avoid drive contention on MDIO during a read transaction. During a write to the LU6612, these bits are driven to a 10 by the station. During a read, the MDIO is not driven during the first bit time and is driven to a 0 by the LU6612 during the second bit time.

Figure 8. MDIO During TA (Turnaround) of a Read Transaction

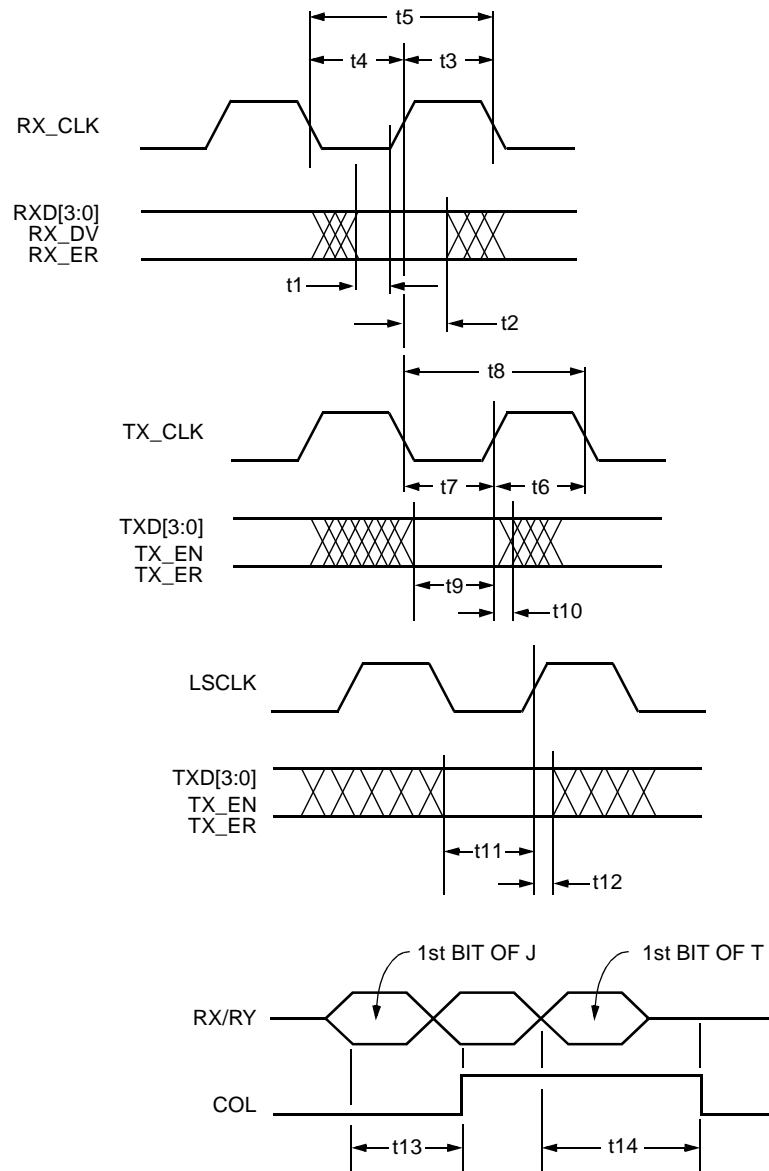
**Timing Characteristics (Preliminary)** (continued)

**Table 26. MII Data Timing (25 pF Load)**

Name	Parameter	Min	Typ	Max	Unit
t1	RXD[3:0], RX_ER, RX_DV, Valid to RX_CLK High	10/100	—	—	ns
t2	RX_CLK High to RXD[3:0], RX_DV, RX_ER Invalid	10/100	—	—	ns
t3	RX_CLK High	14/180	—	26/220	ns
t4	RX_CLK Low	14/180	—	26/220	ns
t5	RX_CLK Period	—	40	—	ns
t6	TX_CLK High	14/180	—	26/220	ns
t7	TX_CLK Low	14/180	—	26/220	ns
t8	TX_CLK Period	—	40	—	ns
t9	TXD[3:0], TX_EN, TX_ER, Setup to TX_CLK	15/140	—	—	ns
t10	TXD[3:0], TX_EN, TX_ER, Hold to TX_CLK	0/0	—	—	ns
t11	TXD[3:0], TX_EN, TX_ER Setup to LSCLK*	10	—	—	ns
t12	TXD[3:0], TX_EN, TX_ER, Hold to LSCLK*	0	—	—	ns
t13	First Bit of J on RX/RX While Transmitting Data to COL Assert (half-duplex mode)	—	—	170	ns
t14	First Bit of T Received on RX/RX While Transmitting to COL Deasserted (half-duplex mode)	—	—	210	ns

\* 100 Mbits/s only.

Timing Characteristics (Preliminary) (continued)



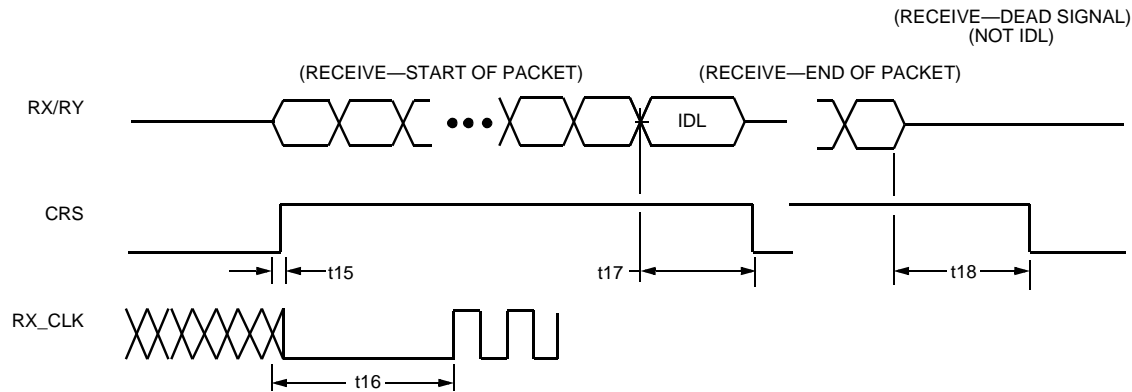
5-5432(F).cr1

Figure 9. MII Timing Requirements for LU6612

Timing Characteristics (Preliminary) (continued)

Table 27. Serial 10 Mbps/s Timing for RX/RX, CRS, and RX\_CLK

Name	Parameter	Min	Max	Unit
t15	RX/RX Activity to CRS Assertion	40	500	ns
t16	RX/RX Activity to RX_CLK Valid	800	2300	ns
t17	IDL to CRS Deassertion	200	550	ns
t18	Dead Signal to CRS Deassertion	400	1000	ns

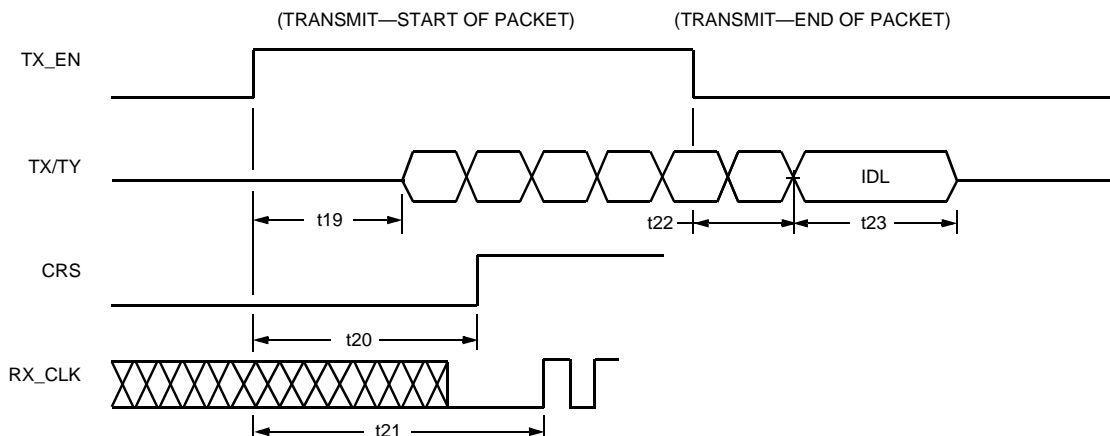


5-5293(F).mr1

Figure 10. Serial 10 Mbps/s Timing for RX/RX, CRS, and RX\_CLK

Table 28. Serial 10 Mbps/s Timing for TX\_EN, TX/TX, CRS, and RX\_CLK

Name	Parameter	Min	Max	Unit
t19	TX_EN Asserted to Transmit Pair Activity	50	400	ns
t20	TX_EN Asserted to CRS Asserted Due to Internal Loopback	5	1900	ns
t21	TX_EN Asserted to RX_CLK Valid Due to Internal Loopback	1000	1700	ns
t22	TX_EN Deasserted to IDL Transmission	50	300	ns
t23	IDL Pulse Width	250	350	ns



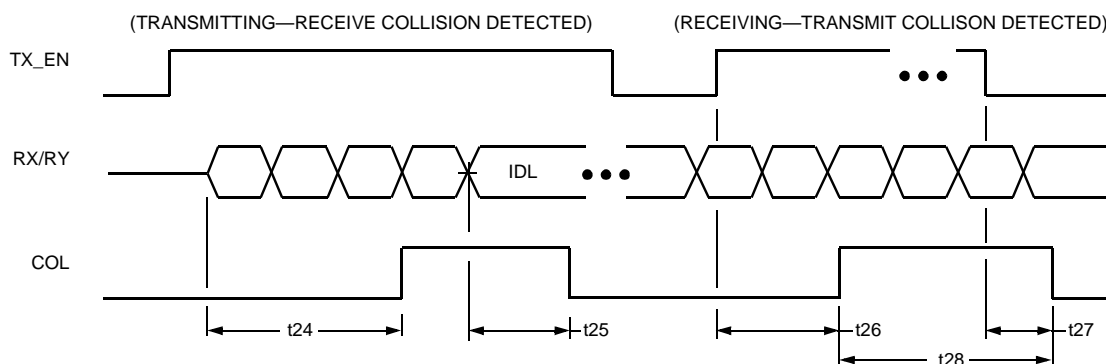
5-5293(F).nr1

Figure 11. Serial 10 Mbps/s Timing for TX\_EN, TX/TX, CRS, and RX\_CLK

Timing Characteristics (Preliminary) (continued)

Table 29. Serial 10 Mbps/s Timing for TX\_EN, RX/RX, and COL

Name	Parameter	Min	Max	Unit
t24	Time to Assert COL; LU6612 Is Transmitting; Receive Activity Starts	40	400	ns
t25	Time to Deassert COL; LU6612 Is Transmitting; Receive Activity Ceases	300	900	ns
t26	Time to Assert COL; LU6612 Is Receiving; Transmit Activity Starts	5	400	ns
t27	Time to Deassert COL; LU6612 Is Receiving; Transmit Activity Ceases	5	900	ns
t28	COL Pulse Width	100	—	ns



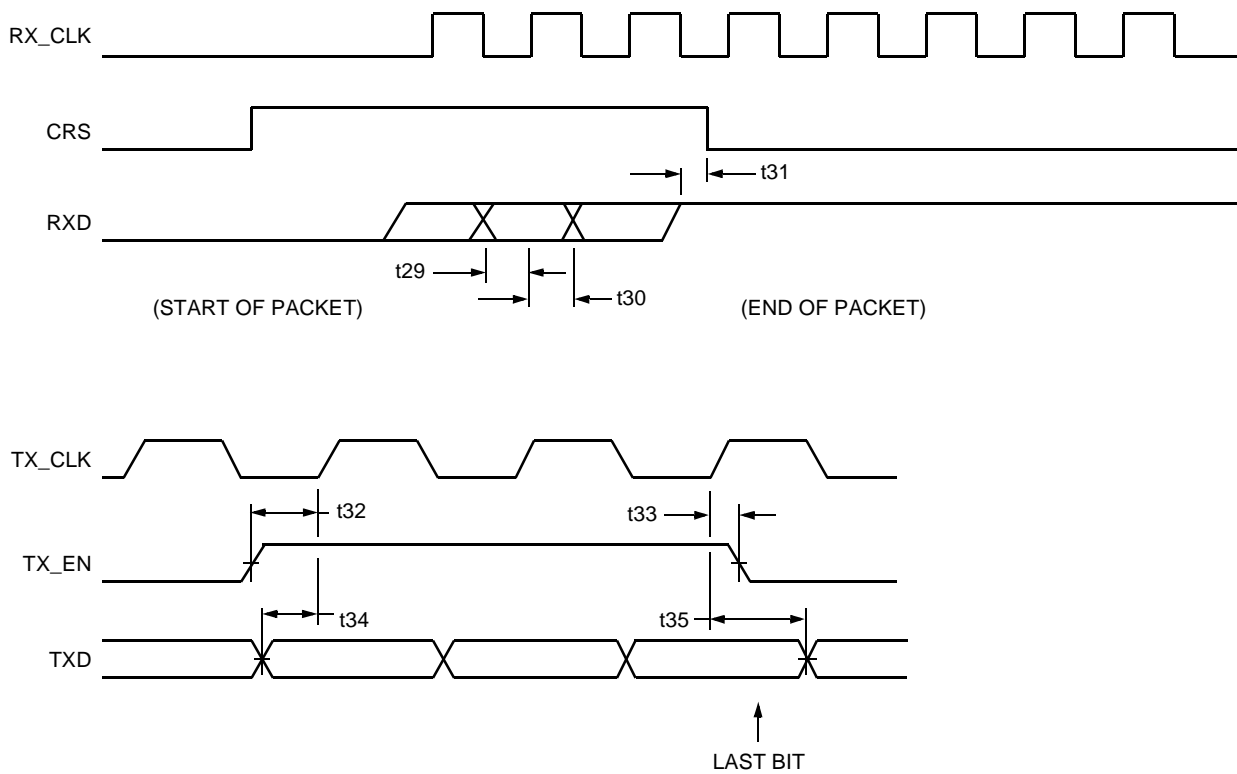
5-5293(F).1

Figure 12. Serial 10 Mbps/s Timing for TX\_EN, RX/RX, and COL

Timing Characteristics (Preliminary) (continued)

Table 30. Serial 10 Mbps/s Timing for RX\_CLK, CRS, RXD, TX\_CLK, TX\_EN, and TXD (25 pF Load)

Name	Parameter	Min	Max	Unit
t29	RXD Setup Before RX_CLK Rising Edge	30	—	ns
t30	RXD Held Past RX_CLK Edge	30	—	ns
t31	RX_CLK Low to CRS Deassertion (at end of received packet)	40	—	ns
t32	TX_EN Setup Before TX_CLK Rising Edge	30	—	ns
t33	TX_EN Held Past TX_CLK Rising Edge	0	—	ns
t34	TXD Setup Before TX_CLK Rising Edge	30	—	ns
t35	TXD Held Past TX_CLK Rising Edge	0	—	ns



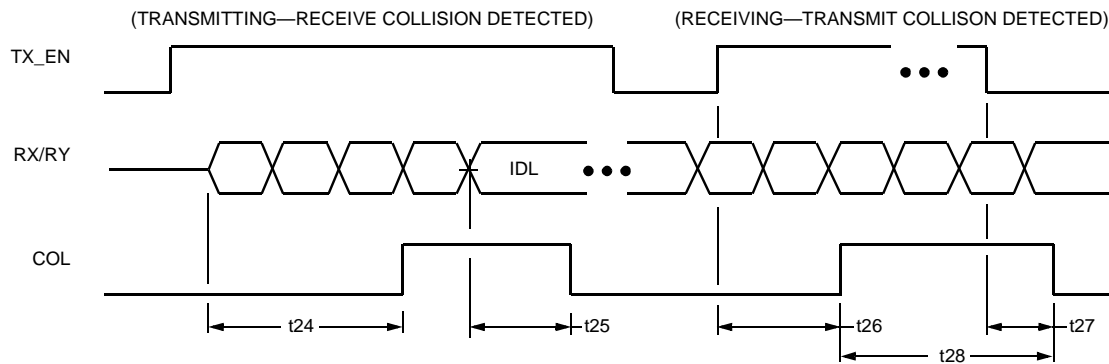
5-2736(F).d

Figure 13. Serial 10 Mbps/s Timing for RX\_CLK, CRS, RXD, TX\_CLK, TX\_EN, and TXD

Timing Characteristics (Preliminary) (continued)

Table 31. Serial 10 Mbps/s Timing for RX\_CLK and TX\_CLK (25 pF Load)

Name	Parameter	Min	Max	Unit
t36	RX_CLK Low Pulse Width	45	55	ns
t37	RX_CLK High Pulse Width	45	55	ns
t38	TX_CLK Low Pulse Width	45	55	ns
t39	TX_CLK High Pulse Width	45	55	ns



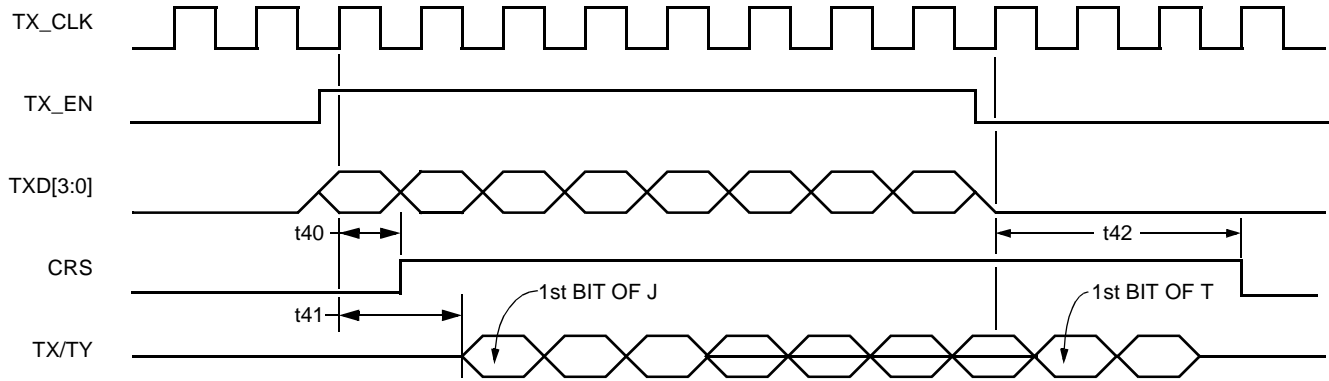
5-2737(F).dr1

Figure 14. Serial 10 Mbps/s Timing Diagram for RX\_CLK and TX\_CLK

**Timing Characteristics (Preliminary)** (continued)

**Table 32. 100 Mb/s MII Transmit Timing**

Name	Parameter	Min	Max	Unit
t40	Rising Edge of TX_CLK Following TX_EN Assertion to CRS Assertion	—	40	ns
t41	Rising Edge of TX_CLK Following TX_EN Assertion to TX/TY	—	60	ns
t42	Rising Edge of TX_CLK Following TX_EN Deassertion to CRS Deassertion	—	40	ns



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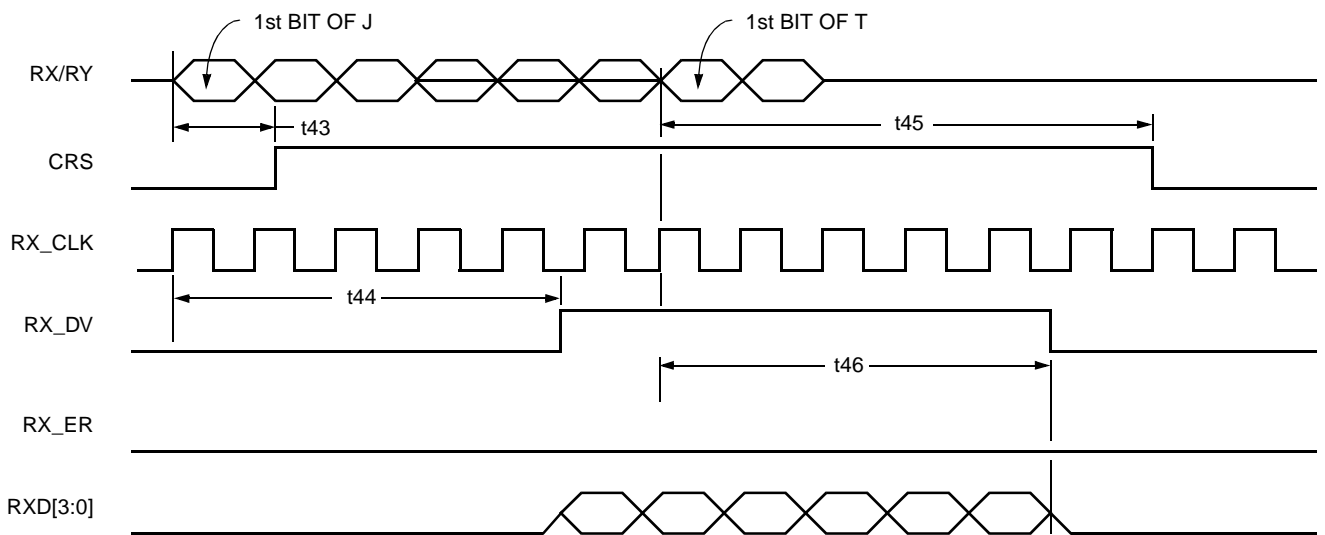
**Figure 15. 100 Mb/s MII Transmit Timing**



Timing Characteristics (Preliminary) (continued)

Table 33. 100 Mbits/s MII Receive Timing

Name	Parameter	Min	Max	Unit
t43	RX/RX 1st Bit of J Receive Activity to CRS Asserted	—	170	ns
t44	RX/RX Receive Activity to Receive Data Valid	—	210	ns
t45	RX/RX Receive Activity Cease (1st bit of T) to CRS Deasserted	—	210	ns
t46	RX/RX Receive Activity Cease (1st bit of T) to Receive Data Not Valid	—	210	ns



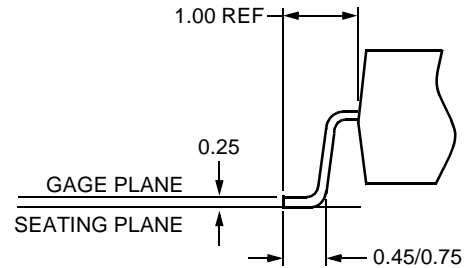
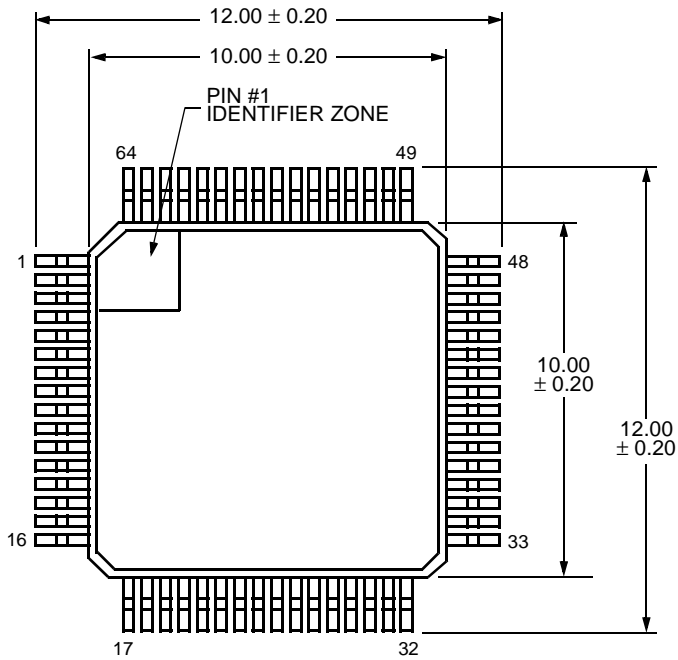
5-3747(F).er1

Figure 16. 100 Mbits/s MII Receive Timing

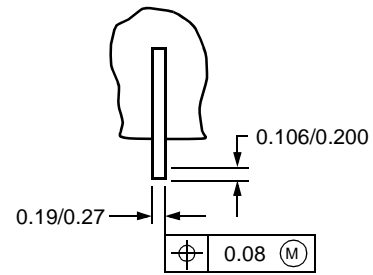
## Outline Diagram

### 64-Pin TQFP

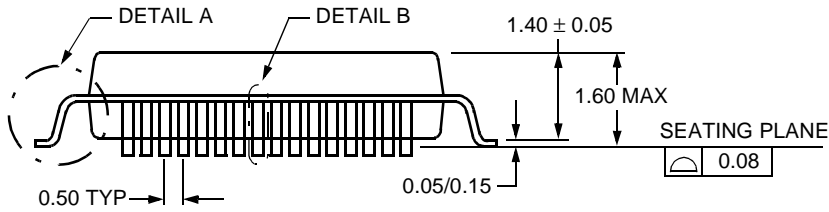
Dimensions are in millimeters.



DETAIL A



DETAIL B



5-3080r5

## Technical Document Types

The following descriptions pertain to the types of individual product data sheets.

Data sheets provide a definition of the particular integrated circuit device by detailing its full electrical and physical specifications. They are intended to be the basic source of information for designers of new systems and to provide data for users requiring information on equipment troubleshooting, training, incoming inspection, equipment testing, and system design modification.

A data sheet is classified according to the following criteria:

**Advance Data Sheet:** An advance data sheet presents the device's proposed design architecture. It lists target specifications but may not have complete parameter values and is subject to change.

**Preliminary Data Sheet:** Preliminary data sheets describe the characteristics of initial prototypes.

**Data Sheet:** When a data sheet has the specifications of a product in full production and has complete parameter values, it is considered final and is classified as a data sheet.

## Ordering Information

Device Code	Comcode	Package	Temperature
LU6612-T64-DB	108160680	64-Pin TQFP	0 °C to 70 °C

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