HIGH PERFORMANCE SERIAL INTERFACE CIRCUITS S2042/S2043

FEATURES

- Functionally compliant with ANSI X3T11 Fibre Channel physical and transmission protocol standards
- S2042 transmitter incorporates phase-locked loop (PLL) providing clock synthesis from low-speed reference
- S2043 receiver PLL configured for clock and data recovery
- 1062, 531 and 266 Mb/s operation
- 10- or 20-bit parallel TTL compatible interface
- 1 watt typical power dissipation for chipset
- +3.3/+5V power supply
- Low-jitter serial PECL compatible interface
- Lock detect
- Local loopback
- 10mm x 10mm 52 PQFP package
- Fibre Channel framing performed by receiver
- Continuous downstream clocking from receiver
- TTL compatible outputs possible with +5V I/O power supply

APPLICATIONS

High-speed data communications

- Supercomputer/Mainframe
- Workstation
- Switched networks
- Proprietary extended backplanes
- Mass storage devices/RAID drives

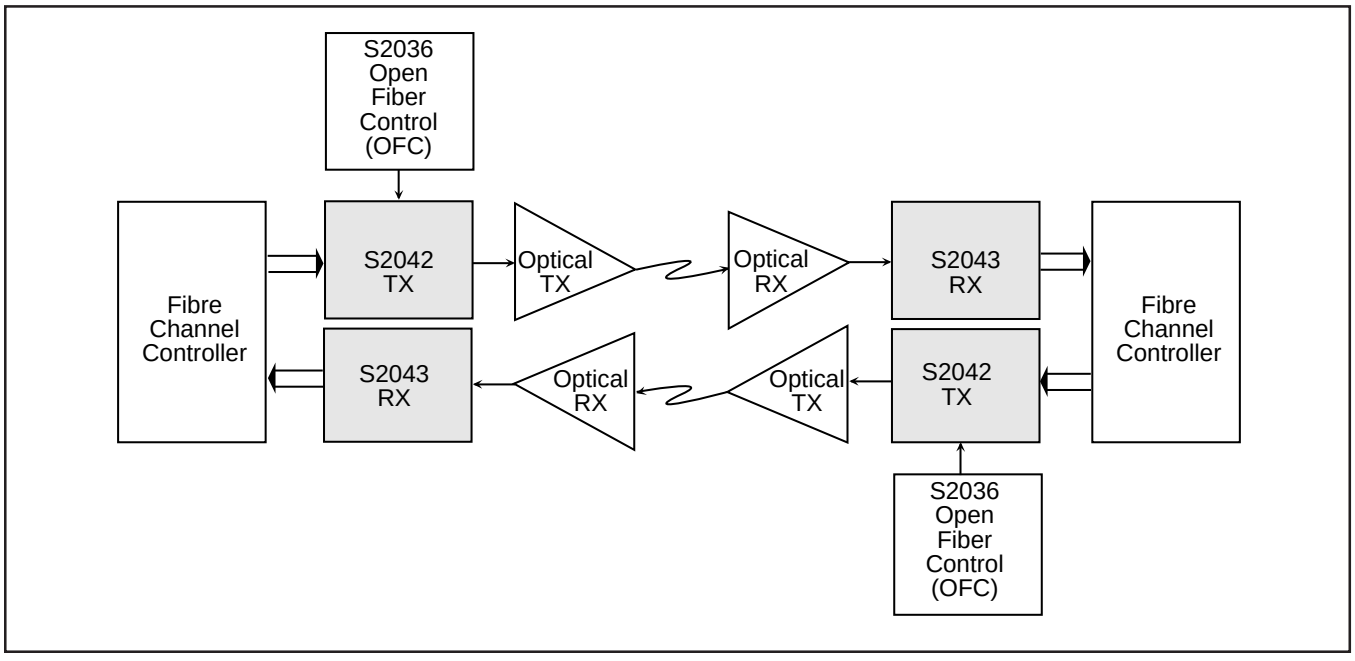
GENERAL DESCRIPTION

The S2042 and S2043 transmitter and receiver pair are designed to perform high-speed serial data transmission over fiber optic or coaxial cable interfaces conforming to the requirements of the ANSI X3T11 Fibre Channel specification. The chipset is selectable to 1062, 531 or 266 Mbit/s data rates with associated 10- or 20-bit data word.

The chipset performs parallel-to-serial and serial-to-parallel conversion and framing for block-encoded data. The S2042 on-chip PLL synthesizes the high-speed clock from a low-speed reference. The S2043 on-chip PLL synchronizes directly to incoming digital signals to receive the data stream. The transmitter and receiver each support differential PECL-compatible I/O for fiber optic component interfaces, to minimize crosstalk and maximize data integrity. Local loopback allows for system diagnostics. The TTL I/O section can operate from either a +3.3V or a +5V power supply. With a 3.3V power supply the chipset dissipates only 1W typically.

Figure 1 shows a typical network configuration incorporating the chipset. The chipset is compatible with AMCC's S2036 Open Fiber Control (OFC) device.

Figure 1. System Block Diagram



OVERVIEW

The S2042 transmitter and S2043 receiver provide serialization and deserialization functions for block-encoded data to implement a Fibre Channel interface. Operation of the S2042/S2043 chips is straightforward, as depicted in Figure 2. The sequence of operations is as follows:

Transmitter

1. 10/20-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver

1. Clock and data recovery from serial input
2. Serial-to-parallel conversion
3. Frame detection
4. 10/20-bit parallel output

The 10/20-bit parallel data handled by the S2042 and S2043 devices should be from a DC-balanced encoding scheme, such as the 8B/10B transmission code, in which information to be transmitted is encoded 8 bits at a time into 10-bit transmission characters.

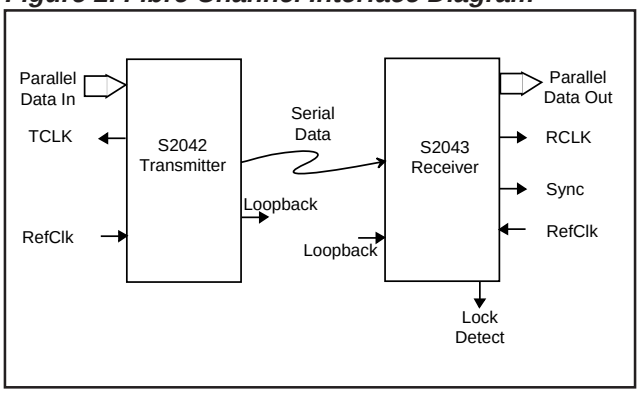
Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figure 5.

A lock detect feature is provided on the receiver, which indicates that the PLL is locked (synchronized) to the reference clock or the data stream.

Loopback

Local loopback is supported by the chipset, and provides a capability for performing offline testing of the interface to ensure the integrity of the serial channel before enabling the transmission medium. It also allows for system diagnostics.

Figure 2. Fibre Channel Interface Diagram

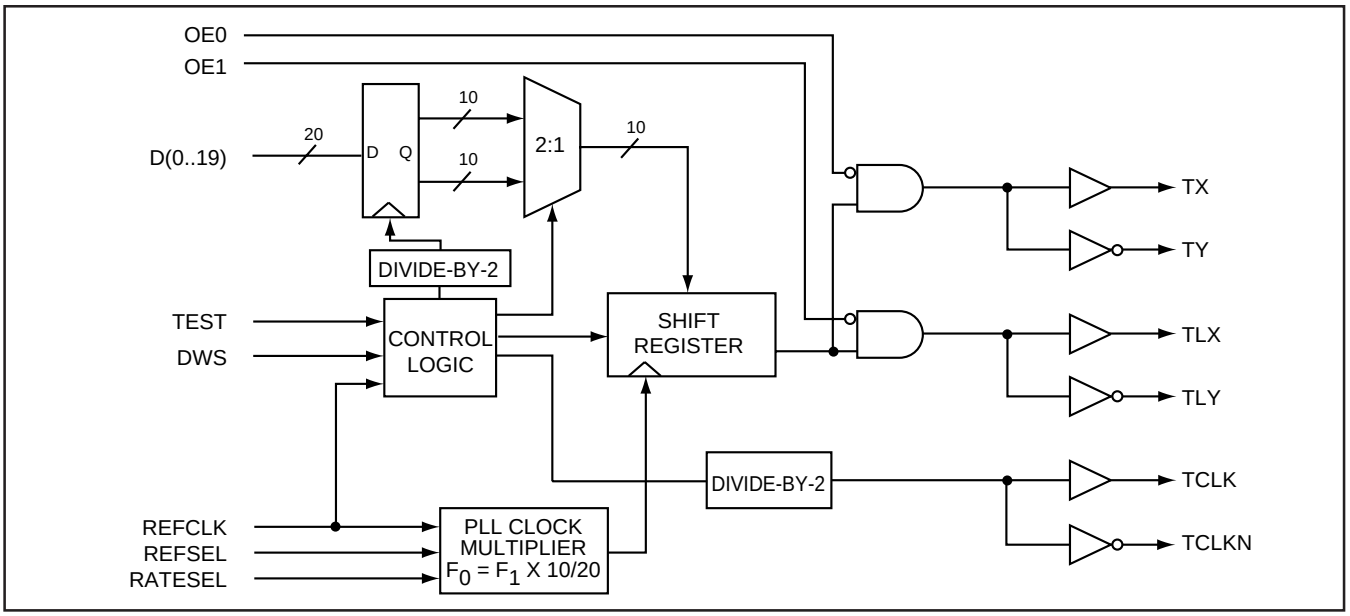


S2042 TRANSMITTER FUNCTIONAL DESCRIPTION

The S2042 transmitter accepts parallel input data and serializes it for transmission over fiber optic or coaxial cable media. The chip is fully compatible with the ANSI X3T11 Fibre Channel standard, and supports the Fibre Channel standard's data rates of 1062, 531 and 266 Mbit/sec.

The parallel input data word can be either 10 bits or 20 bits wide, depending upon DWS pin selection. A block diagram showing the basic chip operation is shown in Figure 3.

Figure 3. S2042 Functional Block Diagram



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Parallel/Serial Conversion

The parallel-to-serial converter takes in 10-bit or 20-bit wide data from the input latch and converts it to a serial data stream. Parallel data is latched into the transmitter on the positive going edge of REFCLK. The data is then clocked synchronous to the clock synthesis unit serial clock into the serial output shift register. The shift register is clocked by the internally generated bit clock which is 10 times the REFCLK input frequency. The state of the serial outputs is controlled by the output enable pins, OE0 and OE1. D10 is transmitted first in 10-bit mode. D0 is transmitted first in 20-bit mode. Table 2 shows the mapping of the parallel data to the 8B/10B codes.

10-Bit/20-Bit Mode

The S2042 operates with either 10-bit or 20-bit parallel data inputs. Word width is selectable via the DWS pin. In 10-bit mode, D10–D19 are used and D0–D9 are ignored.

Reference Clock Input

The reference clock input (REFCLK) must be supplied with a single-ended AC coupled crystal clock source with 100 PPM tolerance to assure that the transmitted data meets the Fibre Channel frequency limits. The internal serial clock is frequency locked to the reference clock. The word rate clock (TCLK, TCLKN) output frequency is determined by the selected operating speed and word width. Refer to Table 1 for TCLK/TCLKN clock frequencies.

Table 1. Transmitter Operating Modes

RATESEL	DWS	REFSEL	Data Rate (Mbits/sec)	Word Width (Bits)	Reference Clock Frequency (MHz)	TCLK/TCLKN Frequency (MHz)
0	1	1	1062.5	10	106.25	53.125
0	0	0	1062.5	20	53.125	53.125
1	1	1	531.25	10	53.125	53.125
1	0	0	531.25	20	26.5625	26.5625
Open	1	1	265.625	10	26.5625	26.5625

Table 2. Data Mapping to 8b/10b Alphabetic Representation

	First Data Byte										Second Data Byte									
TX[00:19] or RX[00:19]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
8b/10b alphabetic representation	a	b	c	d	e	i	f	g	h	j	a	b	c	d	e	i	f	g	h	j

↑ First bit transmitted in 20-bit mode ↑ First bit transmitted in 10-bit mode

Figure 4. S2043 Functional Block Diagram

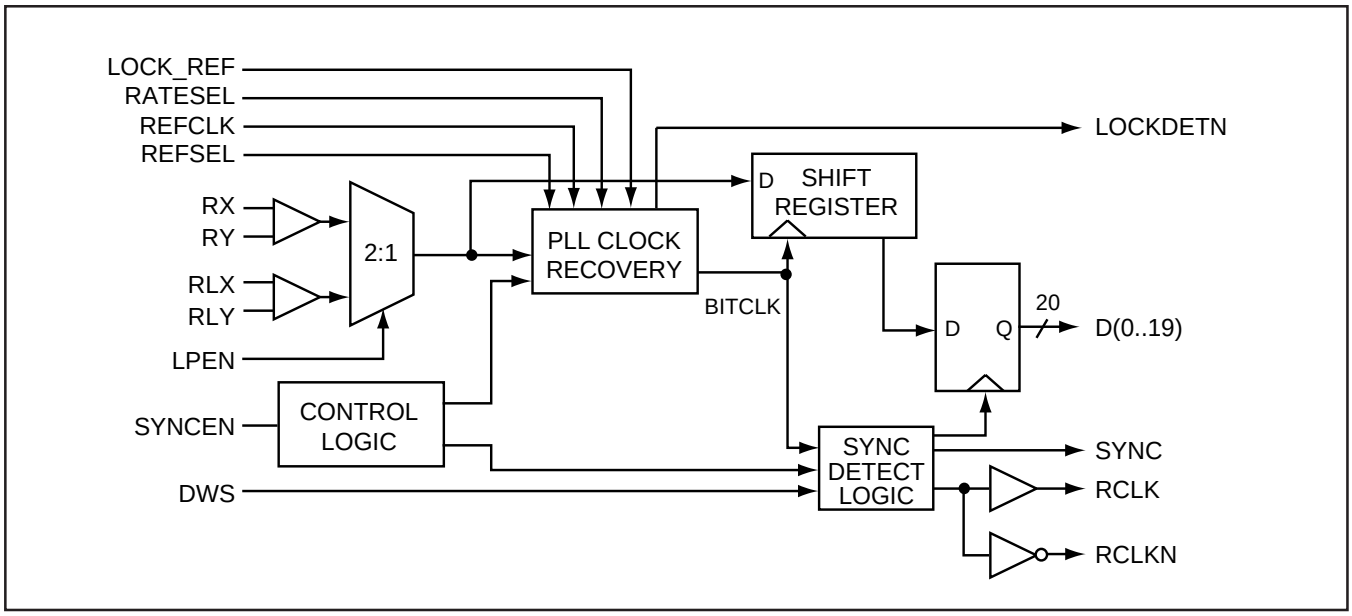


Figure 5. Functional Waveform

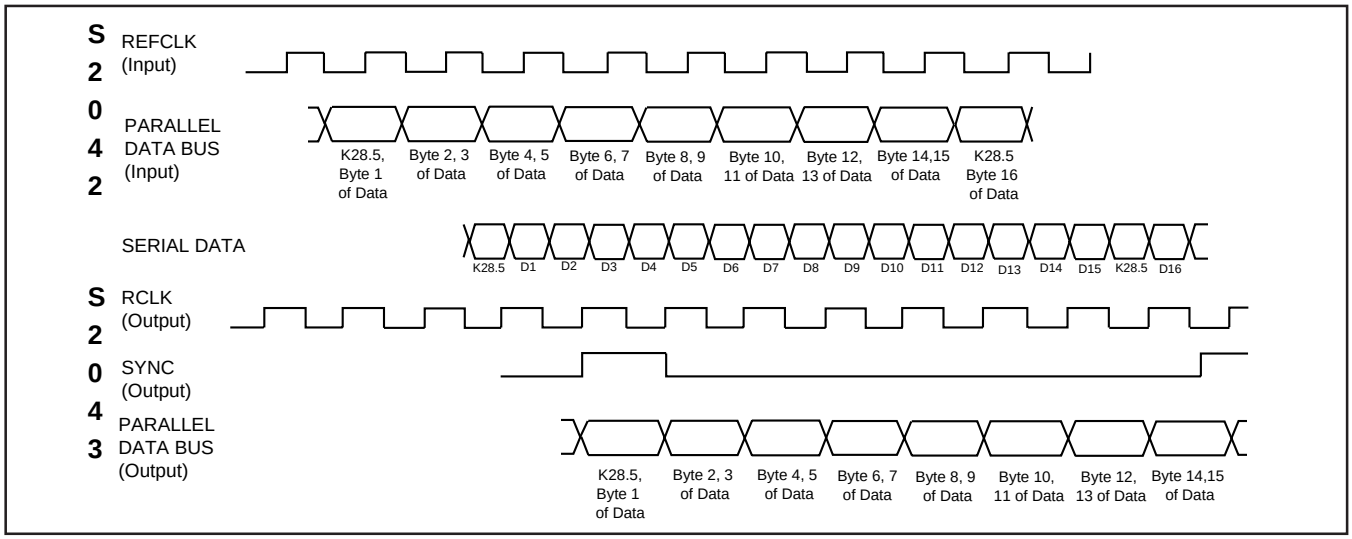


Table 3. Data Mapping to 8b/10b Alphabetic Representation

	First Data Byte										Second Data Byte									
TX[00:19] or RX[00:19]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
8b/10b alphabetic representation	a	b	c	d	e	i	f	g	h	j	a	b	c	d	e	i	f	g	h	j

↑ First bit received in 20-bit mode ↑ First bit received in 10-bit mode

S2043 RECEIVER FUNCTIONAL DESCRIPTION

The S2043 receiver is designed to implement the ANSI X3T11 Fibre Channel specification receiver functions. A block diagram showing the basic chip function is provided in Figure 4.

Whenever a signal is present, the S2043 attempts to achieve synchronization on both bit and transmission-word boundaries of the received encoded bit stream. Received data from the incoming bit stream is provided on the device's parallel data outputs.

The S2043 accepts serial encoded data from a fiber optic or coaxial cable interface. The serial input stream is the result of the serialization of 8B/10B encoded data by an FC compatible transmitter. Clock recovery is performed on-chip, with the output data presented to the Fibre Channel transmission layer as 10- or 20-bit parallel data. The chip is programmable to operate at the Fibre Channel specified operating frequencies of 1062, 531 and 266 Mbit/s.

Serial/Parallel Conversion

Serial data is received on the RX, RY pins. The PLL clock recovery circuit will lock to the data stream if the clock to be recovered is within ±100 PPM of the internally generated bit rate clock. The recovered clock is used to retime the input data stream. The data is then clocked into the serial to parallel output registers on the low going edge of RCLK. In 1062 Mbit/sec, 10-bit mode, data is clocked out on the falling edge of RCLK and RCLKN.The parallel data out can be either 10 or 20 bits wide determined by the state of the DWS pin. The word clock (RCLK) is synchronized to the incoming data stream word boundary by the detection of the fiber channel K28.5 synchronization pattern (0011111010, positive running disparity).

10-Bit/20-Bit Mode

The S2043 will operate with either 10-bit or 20-bit parallel data outputs. This option is selectable via the DWS pin. See Table 4. In 10-bit mode, D10-D19 are used and D0-D9 are driven to the logic high state.

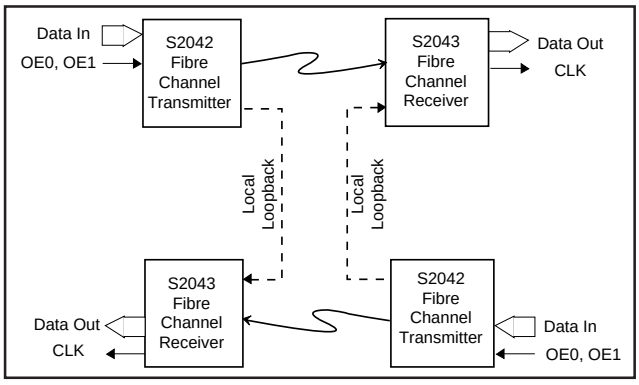
Reference Clock Input

The reference clock input must be supplied with a single-ended AC coupled crystal clock source at ±100 PPM tolerance. See Table 4 for reference clock frequencies.

Framing

The S2043 provides SYNC character recognition and data word alignment of the TTL level compatible output data bus. In systems where the SYNC detect function is undesired, a LOW on the SYNCEN input disables the SYNC function and the data will be "un-framed".

Figure 6. Loopback Interface Diagram



When framing is disabled by low SYNCEN, the S2043 simply achieves bit synchronization within 250 bit times and begins to deliver parallel output data words whenever it has received full transmission words. No attempt is made to synchronize on any particular incoming character. The SYNCEN input should be static during operation (i.e. connected to VCC or GND). The S2043 will not maintain the existing byte synchronization when SYNCEN transitions from the active to inactive state.

The SYNC output signal will go high whenever a K28.5 character (positive disparity) is present on the parallel data outputs. The SYNC output signal will be low at all other times. This is true whether the S2043 is operating in 10-bit mode or in 20-bit mode. In 20-bit mode, the K28.5 byte will always be placed in the MSB (D0-D9). In 10-bit mode, the K28.5 will be clocked with the RCLKN output.

Lock Detect

The S2043 lock detect function indicates the state of the phase-locked loop (PLL) clock recovery unit. The PLL will indicate lock within 250 bit times after the start of receiving serial data inputs. If the serial data inputs have an instantaneous phase jump (from a serial switch, for example) the PLL will not indicate an out-of-lock state, but will recover the correct phase alignment within 250 bit times. If a run length of 64 bits is exceeded, or if the transition density is less than 12%, the loop will be declared out of lock and will attempt to re-acquire bit synchronization. When lock is lost, the PLL will shift from the serial input data to the reference clock, so that correct frequency downstream clocking will be maintained.

In any transfer of PLL control from the serial data to the reference clock, the RCLK/RCLKN output remains phase continuous and glitch free, assuring the integrity of downstream clocking.

Table 4. Receiver Operating Modes

RATESEL	DWS	REFSEL	Data Rate (Mbits/sec)	Word Width (Bits)	Reference Clock Frequency (MHz)	RCLK/RCLKN Frequency (MHz)
0	1	1	1062.5	10	106.25	53.125
0	0	0	1062.5	20	53.125	53.125
1	1	1	531.25	10	53.125	53.125
1	0	0	531.25	20	26.5625	26.5625
Open	1	1	265.625	10	26.5625	26.5625

Start-Up Procedure

The clock recovery PLL requires an initilization procedure to correctly achieve lock on the serial data inputs. At power-up or loss of lock, the PLL must first acquire frequency lock to the local reference clock. This can be accomplished in three ways: 1) The –LOCK_REF pin can be connected to a 10 ms reset signal to initialize the PLL. 2) By guaranteeing that no data is seen at the serial data inputs for a minimum of 10 ms upon power-up. 3) The S2043 can be put into the loopback mode and the loopback outputs of the S2042 must be quiescent for a minimum of 10 ms after power-up.

Other Operating Modes

Loopback

Local loopback requires a S2042 and a S2043 as shown in the Figure 6. When enabled, serial data from the S2042 transmitter is sent to the S2043 receiver, where the clock is extracted and the data is deserialized. The parallel data is then sent to the subsystem for verification. This loopback mode provides the capability to perform offline testing of the interface to guarantee the integrity of the serial channel before enabling the transmission medium. It also allows system diagnostics.

Operating Frequency Range

The S2042 and S2043 are optimized for operation at the Fibre Channel rates of 266, 531 and 1062 Mbit/s. Operation at other than Fibre channel rates is possible if the rate falls within ±10% of the nominal rate. REFCLK must be selected to be within 100 ppm of the desired byte or word clock rate.

Test Modes

The TEST pin on the S2042 and the SYNCEN pin on the S2043 provide a PLL bypass mode that can be used for operating the digital area of the chip. In this mode, clock signals are input through the reference clock pins. This can be used for testing the device during the manufacturing process or during an off-line self-test. Sync detection is always enabled in test mode.

S2042 Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	TTL	I	50 49 48 47 44 43 42 41 38 37 36 35 31 30 29 28 25 24 23 22	Accepts parallel input data. Data is clocked in on the rising edge of REFCLK. In 20-bit mode, D0 is transmitted first. In 10-bit mode, D10-19 are used, D0-D9 are ignored, and D10 is transmitted first.
TEST	Static Multi-Level TTL	I	20	Multilevel input used for factory testing. When not connected, REFCLK replaces the internal bit clock to facilitate factory testing. In normal use, this input is wired to ground.
DWS	TTL	I	19	The level on this pin selects the parallel data bus width. When LOW, a 20-bit parallel bus width is selected, and D(0-19) are active. When HIGH, a 10-bit parallel data bus is selected, D(10-19) are active and D(0-9) are not used. (See Table 1.) A rising edge will reset the part (used for test).
REFCLK	PECL	I	16	(Externally capacitively coupled.) A crystal-controlled reference clock for the PLL clock multiplier. The frequency of REFCLK is set by the REFSEL pin. (See Table 1.)
TCLK TCLKN	Diff. TTL	O	12 11	Differential TTL word rate clock true and complement. See Table 1 for frequency.
TY TX	Diff. PECL	O	9 8	Differential PECL outputs that transmit the serial data and drive 75W or 50W termination to Vcc-2V. Enabled by OE0. TX is the positive output, and TY is the negative output.
TLX TLY	Diff. PECL	O	5 4	Differential PECL outputs that are functionally equivalent to TX and TY. They are intended to be used for loopback testing. Enabled by OE1.

S2042 Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
OE0	Static TTL	I	2	Active low output-enable control for TX/TY outputs. TX/TY will go to the logic low state when disabled.
OE1	TTL	I	1	Active low output-enable control for TLX/TLY outputs. TLX/TLY will go to the logic low state when disabled.
REFSEL	Static Multi-TTL	I	18	Multilevel input used to select the reference clock frequency. (See Table 1.)
RATESEL	TTL	I	15	Multilevel input used to select the operating speed of the transmitter. (See Table 1.)
ECLVCC	+3.3V	–	21, 39, 45	Core +3.3V
TTLGND	GND	–	14	TTL Ground
TTLVCC	+3.3V/ +5V	–	17	TTL Power Supply (+5V if TTL)
ECLIOVCC	+3.3V	–	3, 10	PECL I/O Power Supply
ECLIOVEE	GND	–	6, 7	PECL I/O Power Supply
AVCC	+3.3V	–	27, 32	Analog Power Supply
AVEE	GND	–	26, 33	Analog Ground
ECLVEE	GND	–	13, 34, 40, 46, 51, 52	Core Ground

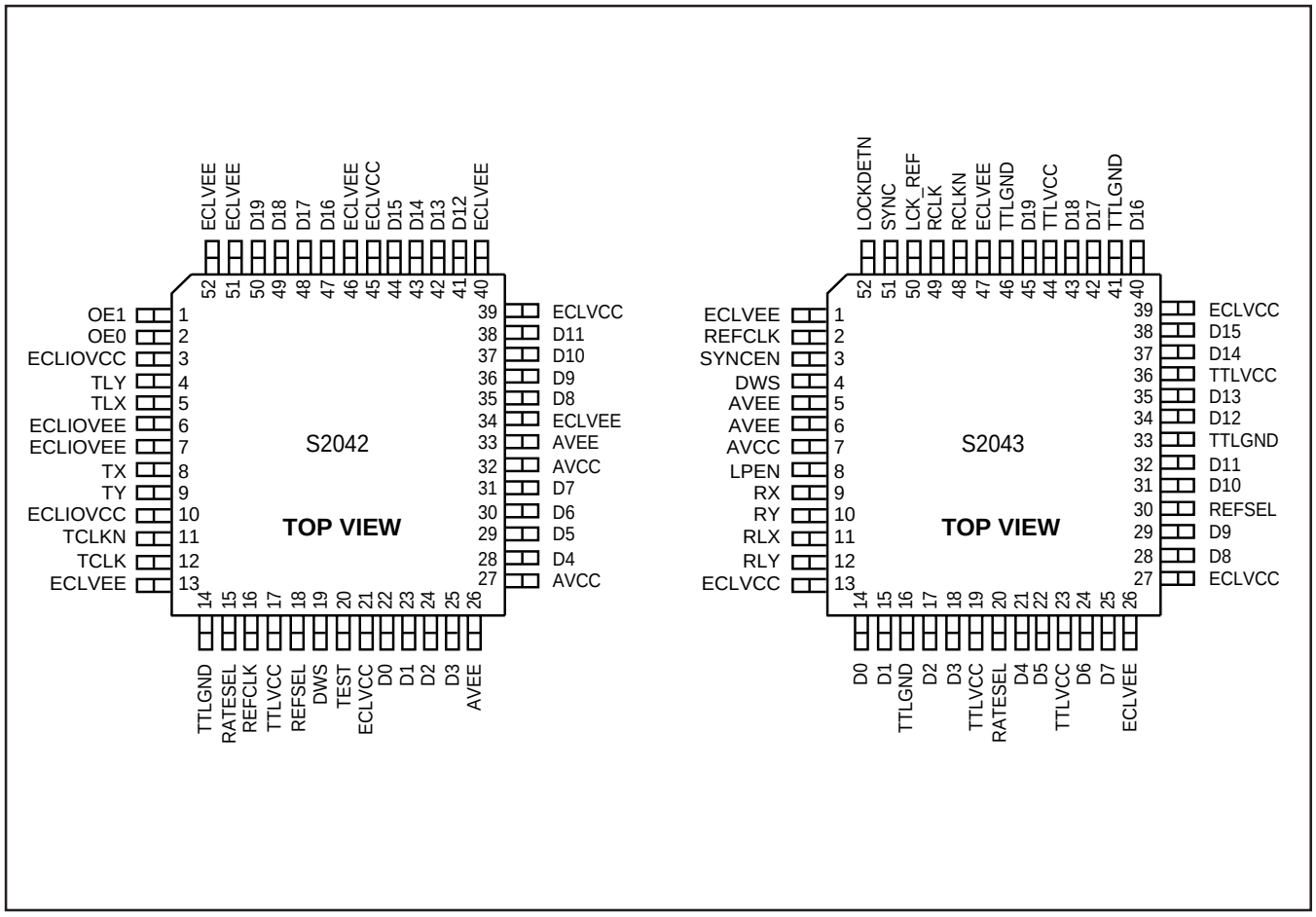
S2043 Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	TTL	O	45 43 42 40 38 37 35 34 32 31 29 28 25 24 22 21 18 17 15 14	Parallel data outputs. The width of the parallel data bus is selected by the state of the DWS pin. Parallel data on this bus is clocked out on the falling edge of RCLK in 20-bit mode and on both the falling edges of RCLK and RCLKN in 1062.5 Mbit/sec, 10-bit mode. In 20-bit mode, D0 is the first bit received. In 10-bit mode, D10-D19 are used and D0-D9 are driven to the high state. In 10-bit mode, D10 is the first bit received.
LOCKDETN	TTL	O	52	When LOW, LOCKDETN indicates that the PLL is locked to the incoming data stream. When HIGH, it provides a system flag indicating that the PLL is locked to the local reference clock.
LPEN	TTL	I	8	When HIGH, LPEN selects the loopback differential serial input pins. When LOW, LPEN selects RX and RY (normal operation).
DWS	Static TTL	I	4	The level on this pin selects the parallel data bus width. When LOW, a 20-bit parallel bus width is selected, and D(0-19) are active. When HIGH, a 10-bit parallel data bus is selected, D(10-19) are active and D(0-9) will go HIGH. (See Table 4.) A rising edge will reset the internal counters (used for test).
RCLK RCLKN	Diff. TTL	O	49 48	Parallel data is clocked out on the falling edge of RCLK/RCLKN (see Timing Diagrams in Figures 15-18). After a sync word is detected, the period of the current RCLK and RCLKN is stretched to align with the word boundary. (See Table 4 for frequency.)
REFCLK	Analog	I	2	(Externally capacitively coupled.) A free-running crystal-controlled reference clock for the PLL clock multiplier. The frequency of REFCLK is set by the REFSEL pin. (See Table 4.)
SYNC	TTL	O	51	Upon detection of a valid sync symbol, this output goes high for one RCLK period. When sync is active, the sync symbol shall be present on the parallel data bus bits D0-D9 in 20-bit mode and D10-D19 in 10-bit mode.
RLX RLY	Diff. PECL	I	11 12	(Externally capacitively coupled.) The serial loopback data inputs. RLX is the positive input, and RLY is the negative input.
RX RY	Diff. PECL	I	9 10	(Externally capacitively coupled.) The received serial data inputs. RX is the positive input, and RY is the negative input.

S2043 Pin Assignment and Descriptions (Continued)

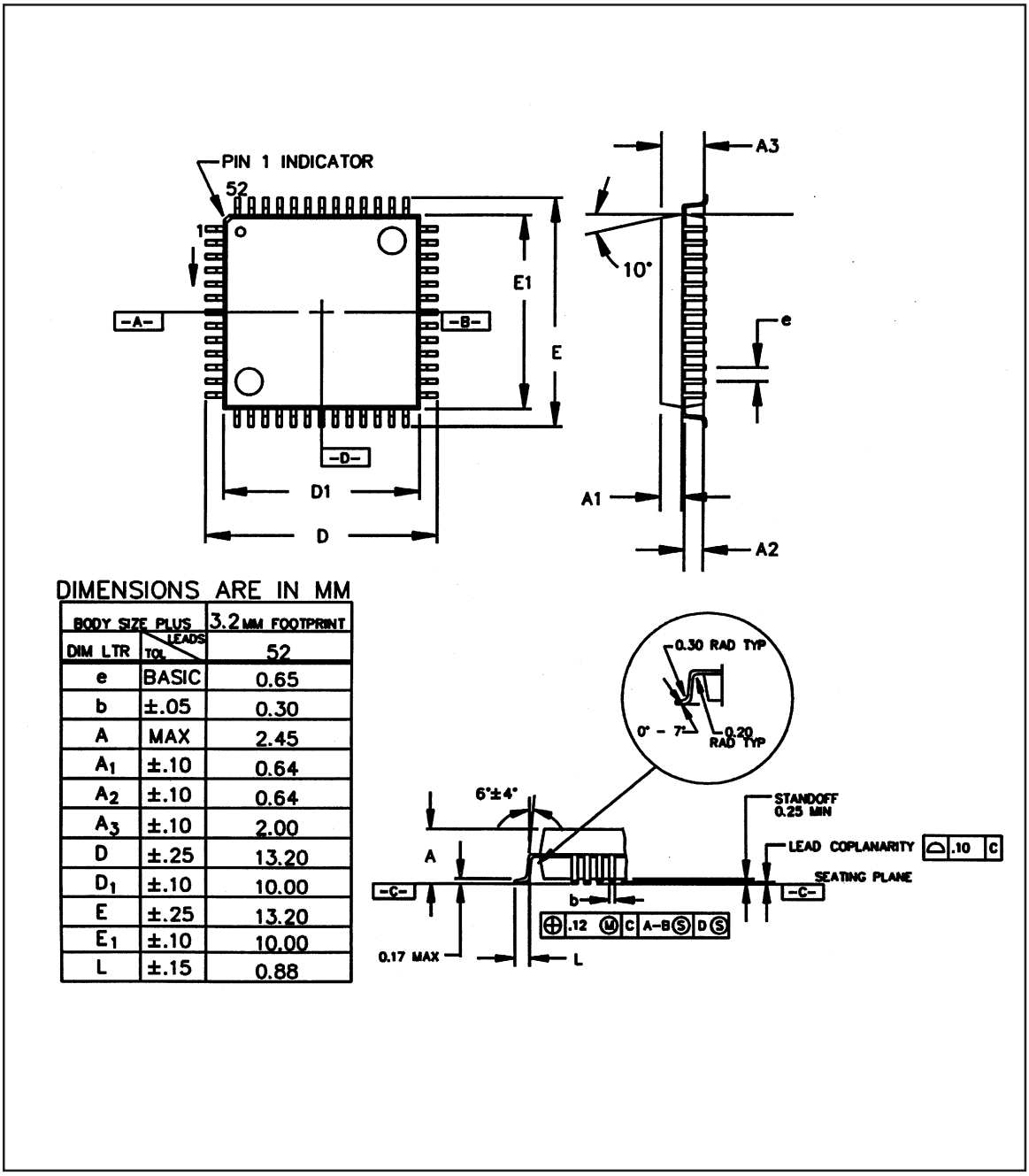
Pin Name	Level	I/O	Pin #	Description
SYNCEN	Static Multi-Level TTL	I	3	(Multilevel.) When HIGH, enables sync detection. Detection of the sync pattern (K28.5:0011111010, positive running disparity) will enable the word boundary for the data to follow. When open (not connected), REFCLK replaces internal bit clock to facilitate factory testing. In this mode of operation, sync detection is always enabled. When LOW, data is treated as unframed data.
REFSEL	Static Multi-Level TTL	I	30	(Multilevel.) Input used to select the reference clock frequency. (See Table 4.)
RATESEL	Static Multi-Level TTL	I	20	(Multilevel.) Input used to select the operating speed of the receiver. (See Table 4.)
LOCK_REF	TTL	I	50	When LOW, forces the PLL to lock to the REFCLK input and ignore the serial data inputs.
ECLVCC	+3.3V	–	13, 27, 39	Core Power Supply
TTLGND	GND	–	16, 33, 41, 46	TTL Ground
TTLVCC	+3.3V/ +5V	–	19, 23, 36, 44	TTL Power Supply (+5V if TTL)
AVCC	+3.3V	–	7	Analog Power Supply
AVEE	GND	–	5, 6	Analog Ground
ECLVEE	GND	–	1, 26, 47	Core Ground

Figure 7. 52 PQFP Pinouts



TTLVCC= +5V or +3.3V
AVCC= +3.3V
ECLVCC= +3.3V
ECLIOVCC = +3.3V
ECLIOVEE = 0V
TTLGND= 0V
ECLVEE= 0V
AVEE= 0V

Figure 8. 52 PQFP Package



DIMENSIONS ARE IN MM

BODY SIZE PLUS LEADS / DIM LTR	TOL	3.2 MM FOOTPRINT 52
e	BASIC	0.65
b	±.05	0.30
A	MAX	2.45
A_1	±.10	0.64
A_2	±.10	0.64
A_3	±.10	2.00
D	±.25	13.20
D_1	±.10	10.00
E	±.25	13.20
E_1	±.10	10.00
L	±.15	0.88

Absolute Maximum Ratings

PARAMETER	MIN	TYP	MAX	UNIT
Case Temperature under Bias	-55		125	°C
Junction Temperature under Bias	-55		150	°C
Storage Temperature	-65		150	°C
Voltage on VCC with Repect to GND	-0.5		+7.0	V
Voltage on any TTL Input Pin	-0.5		+5.5V	V
Voltage on any PECL Input Pin	0		VCC	V
TTL Output Sink Current			8	mA
TTL Output Source Current			8	mA
High Speed PECL Output Source Current			50	mA
Static Discharge Voltage		500		V

Recommended Operating Conditions

PARAMETER	MIN	TYP	MAX	UNIT
Ambient Temperature under Bias	0		70	°C
Junction Temperature under Bias			130	°C
Voltage on TTLVCC with Respect to GND 5V Operation 3.3V Operation	 4.75 3.13	 5.0 3.3	 5.25 3.47	 V V
Voltage on any TTL Input Pin	0		TTLVCC	V
Voltage on ECLVCC with respect to GND	3.13	3.3	3.47	V
Voltage on any PECL Input Pin	ECLVCC -2.0V		ECLVCC	V

Reference Clock Requirements

Parameters	Description	Min	Max	Units	Conditions
FT	Frequency Tolerance S2042	-100	+100	ppm	—
FT	Frequency Tolerance S2043	-100	+100	ppm	—
TD_{1-2}	Symmetry	40	60	%	Duty Cycle at 50% pt.
T_{RCR}, T_{RCF}	REFCLK Rise and Fall Time	—	2	ns	20 – 80%
—	Random Jitter			ps	Peak-to-Peak

S2042 DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage (TTL) – 3.3V Power Supply – 3.3V Power Supply – 5V Power Supply	 2.1 2.2 2.7			 V V V	 V_{CC} = min, I_{OH} = -2.4mA V_{CC} = min, I_{OH} = -.1mA V_{CC} = min, I_{OH} = -1mA
V_{OL}	Output LOW Voltage (TTL) – 3.3V Power Supply – 5V Power Supply			 .5 .5	 V V	 V_{CC} = min, I_{OL} = 2.4mA V_{CC} = min, I_{OL} = 4mA
V_{IH}	Input HIGH Voltage (TTL)	2.0	—	5.5	V	$I_H \leq$ 1mA at V_{IH} = 5.5V
V_{IL}	Input LOW Voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH Current (TTL)	—	—	50	µA	V_{IN} = 2.4V
I_{IL}	Input LOW Current (TTL)	-500	—	-50	µA	V_{IN} = 0.5V
I_{CC}	Supply Current		123	160	mA	Outputs open, V_{CC} = V_{CC} max
P_D	Power Dissipation		.406	.554	W	Outputs open, V_{CC} = V_{CC} max
ΔV_{INCLK}	Single-ended REFCLK input swing	440	—	1300	mV	AC coupled
ΔV_{OUT}	Serial Output Voltage Swing	600	—	1600	mV	50Ω to V_{CC} -2.0V

S2043 DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage (TTL) – 3.3V Power Supply – 3.3V Power Supply – 5V Power Supply	 2.1 2.2 2.7			 V V V	 V_{CC} = min, I_{OH} = -2.4mA V_{CC} = min, I_{OH} = -.1mA V_{CC} = min, I_{OH} = -1mA
V_{OL}	Output LOW Voltage (TTL) – 3.3V Power Supply – 5V Power Supply			 .5 .5	 V V	 V_{CC} = min, I_{OL} = 2.4mA V_{CC} = min, I_{OL} = 8mA
V_{IH}	Input HIGH Voltage (TTL)	2.0	—	5.5	V	$I_H \leq$ 1mA at V_{IH} = 5.5V
V_{IL}	Input LOW Voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH Current (TTL)	—	—	50	µA	V_{IN} = 2.4V
I_{IL}	Input LOW Current (TTL)	-500	—	-50	µA	V_{IN} = 0.5V
I_{CC}	Supply Current – 10-Bit Mode – 20-Bit Mode		 187 194	 256 267	 mA mA	 Outputs open, V_{CC} = V_{CC} max Outputs open, V_{CC} = V_{CC} max
P_D	Power Dissipation – 3.3V Supply, 10-Bit Mode – 3.3V Supply, 20-Bit Mode – 5V Supply, 10-Bit Mode – 5V Supply, 20-Bit Mode		 .617 .640 .728 .778	 .887 .925 1.08 1.142	 W W W W	 Outputs open, V_{CC} = V_{CC} max Outputs open, V_{CC} = V_{CC} max Outputs open, V_{CC} = V_{CC} max Outputs open, V_{CC} = V_{CC} max
ΔV_{INCLK}	Single-ended REFCLK input swing	440	—	1300	mV	AC coupled
V_{DIFF}	Min. differential input voltage swing for differential PECL inputs	100		1300	mV	

Table 5. AC Characteristics

Parameters	Description	Min	Max	Units	Conditions
T_1	REFCLK to TCLK	1.0	4.0	ns	—
T_2	Data setup w.r.t. REFCLK	1.0	—	ns	—
T_3	Data hold w.r.t. REFCLK	2.0	—	ns	—
T_4	Data setup w.r.t. TCLK	5		ns	
T_5	Data hold w.r.t. TCLK	1		ns	
T_{CR} , T_{CF}	TCLK rise and fall time	—	5.0	ns	10% to 90%, tested on a sample basis.
T_{SDR} , T_{SDF}	Serial data rise and fall	—	300	ps	20% to 80%, tested on a sample basis.
T_6	TCLK to TCLKN Skew	—	1	ns	Tested on a sample basis.
T_{DC}	TCLK, TCLKN Duty Cycle	40	60	%	—
Transmitter Output Jitter Allocation					
T_JRMS	Serial data output random jitter (RMS)	—	20	ps	RMS, tested on a sample basis. Measured with 1010 pattern.
T_{DJ}	Serial data output deterministic jitter (p-p)	—	100	ps	Peak-to-peak, tested on a sample basis. Measured with IDLE pattern.

Note: All AC measurements are made from the reference voltage level of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V). All TTL AC measurements are assumed to have the output load of 10pF.

Table 6. S2043 Receiver Timing

Parameters	Description	Min	Max	Units	Conditions
T_3	RCLK to RCLKN skew	—	1	ns	Tested on a sample basis.
T_4	Data set-up time	3.0	—	ns	1062 Mbit/sec, 10-bit mode.
T_5	Data hold time	1.5	—	ns	1062 Mbit/sec, 10-bit mode.
T_6	Data set-up time	2.5	—	ns	1062, 531 Mbit/sec, 20-bit mode. 531, 266 Mbit/sec, 20-bit mode.
T_7	Data hold time	7.5	—	ns	1062, 531 Mbit/sec, 20-bit mode. 531, 266 Mbit/sec, 20-bit mode.
T_{RCR} , T_{RCF}	RCLK rise and fall time	—	5.0	ns	10% to 90%, tested on a sample basis.
T_{DR} , T_{DF}	Data Output rise and fall time	—	5.0	ns	10% to 90%, tested on a sample basis.
T_{SDR} , T_{SDF}	Serial data input rise and fall	—	300	ps	20% to 80%.
T_{LOCK}	Data acquisition lock time @ <1.0625Gb/s	—	2.4	µs	8B/10B IDLE pattern sample basis
Duty Cycle	RCLK/RCLKN Duty Cycle	40%	60%		
Input Jitter Tolerance	Input data eye opening allocation at receiver input for BER ≤1E–12	30%	—	bit time	As specified in Fibre Channel FC–PH standard eye diagram jitter mask.

Note: All AC measurements are made from the reference voltage level of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V). All TTL AC measurements are assumed to have the output load of 10pF.

Figure 9. Transmitter Timing Diagram (531, 266 Mbits/sec, 10-bit mode)

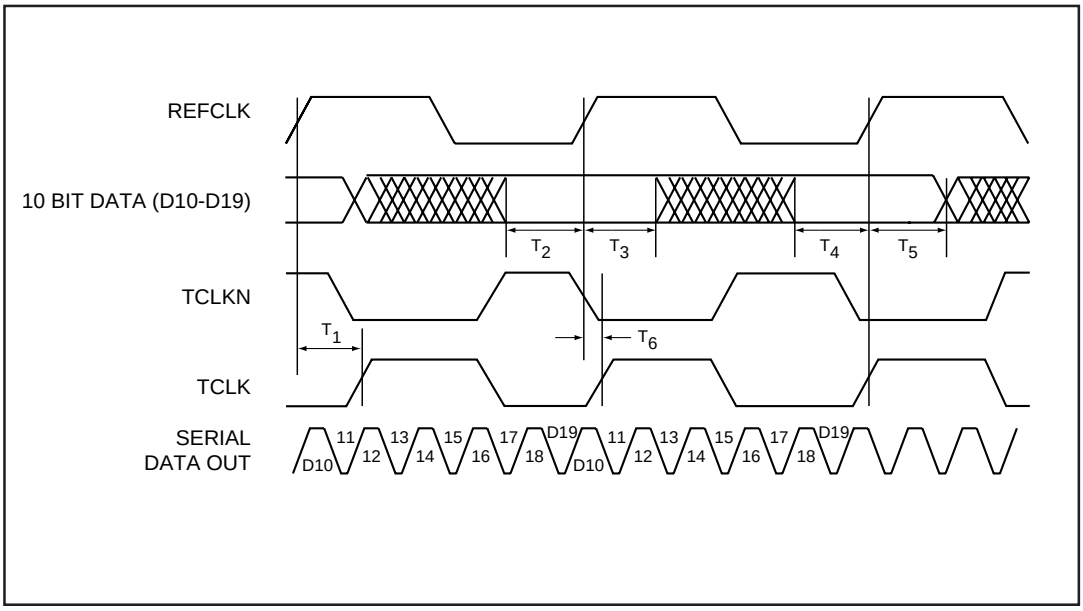


Figure 10. Transmitter Timing Diagram (531, 266 Mbits/sec, 20-bit mode)

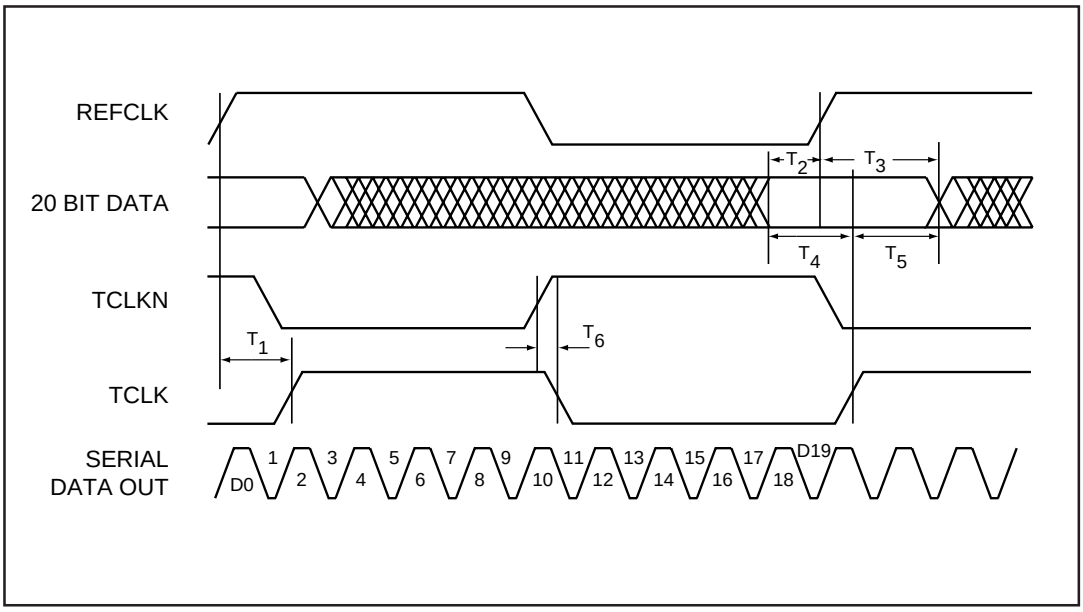


Figure 11. Transmitter Timing Diagram (1062 Mbits/sec, 10-bit mode)

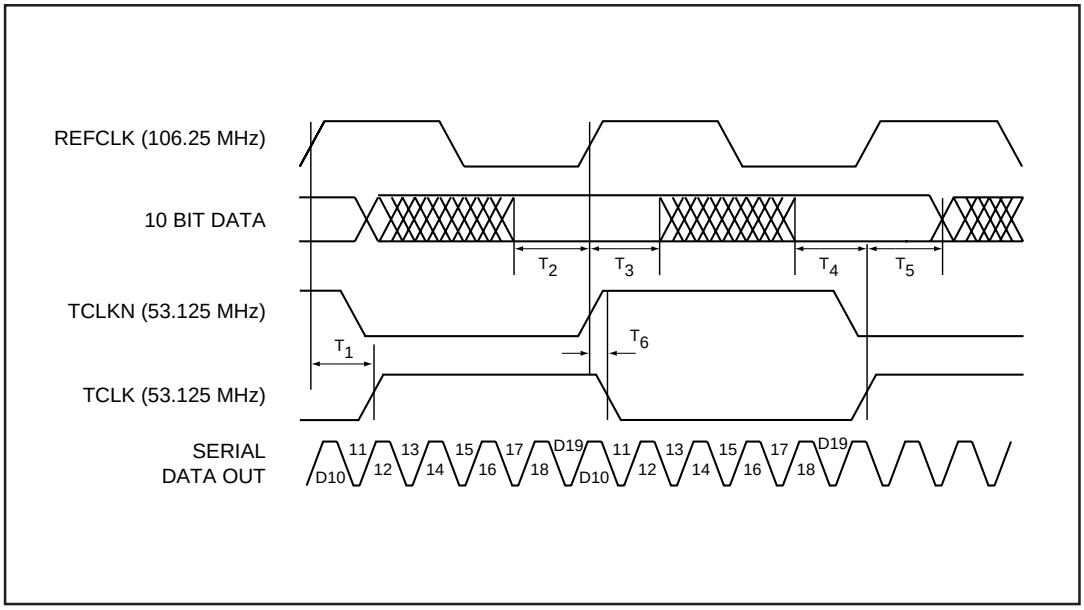


Figure 12. Transmitter Timing Diagram (1062 Mbits/sec, 20-bit mode)

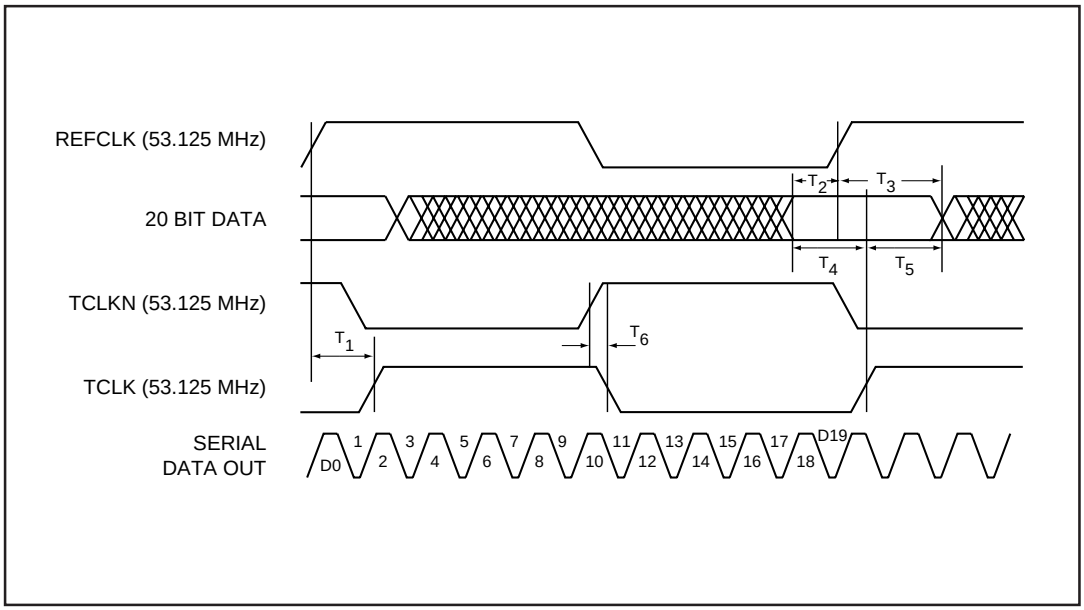


Figure 13. Receiver Timing Diagram (531, 266 Mbits/sec, 10-bit mode)

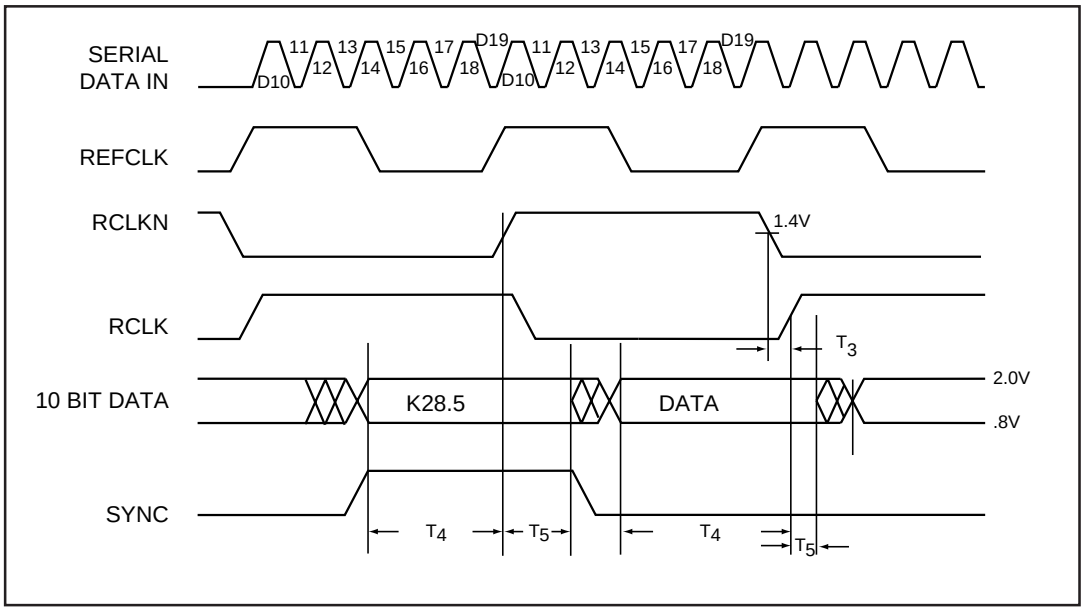


Figure 14. Receiver Timing Diagram (531 Mbits/sec, 20-bit mode)

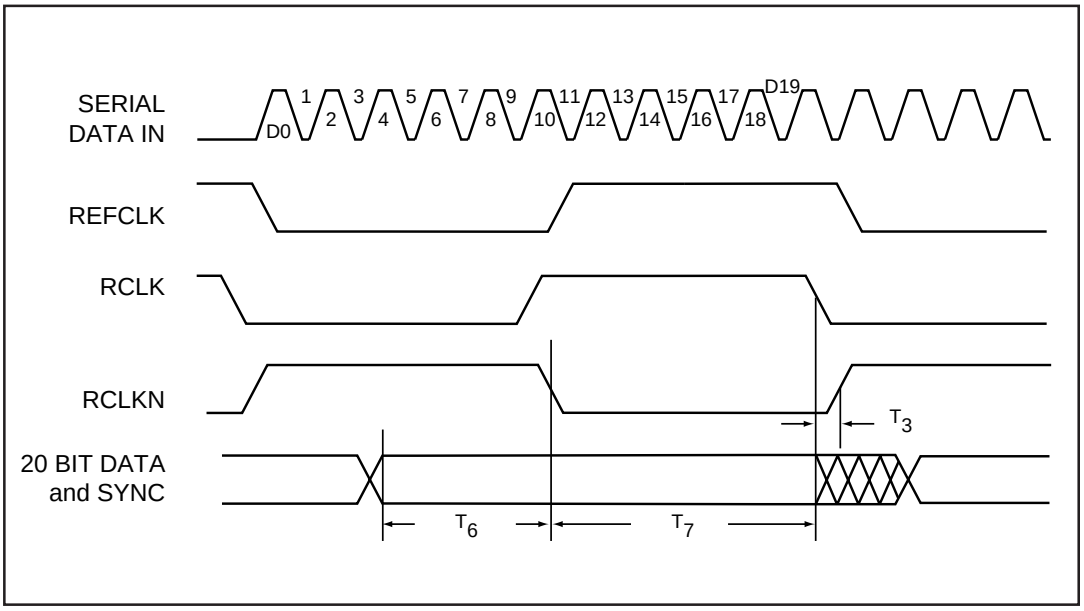


Figure 15. Receiver Timing Diagram (1062 Mbits/sec, 10-bit mode)

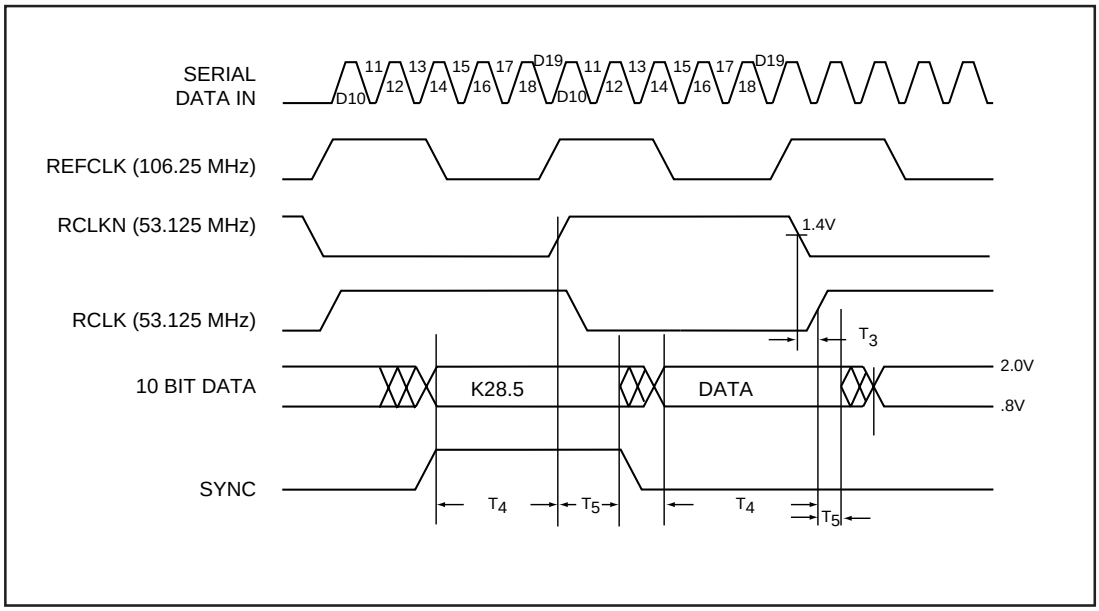


Figure 16. Receiver Timing Diagram (1062 Mbits/sec, 20-bit mode)

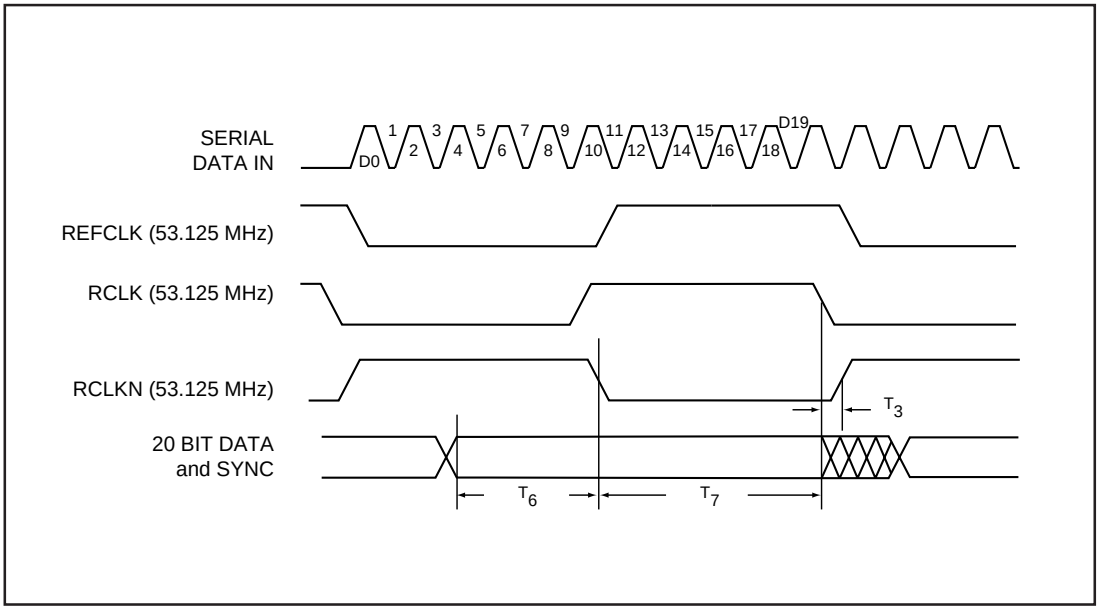


Figure 17. Serial Input Rise and Fall Time

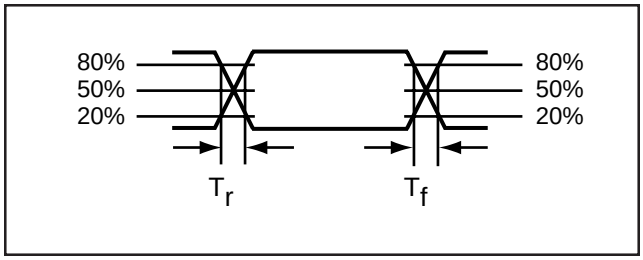


Figure 18. Serial Output Load

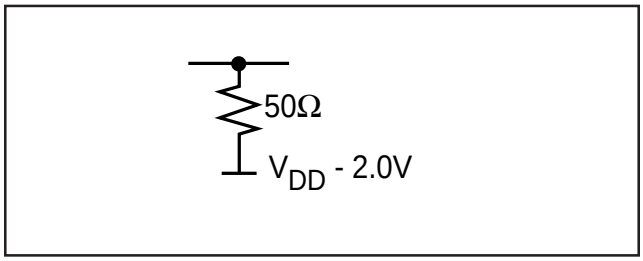


Figure 19.TTL Input and Output Rise and Fall Time

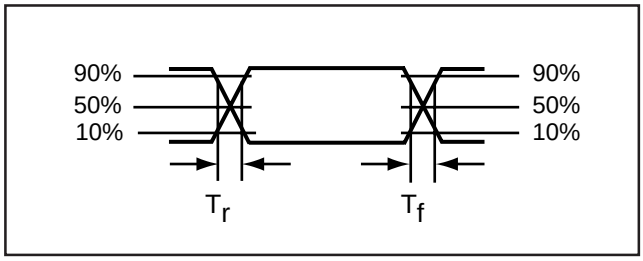
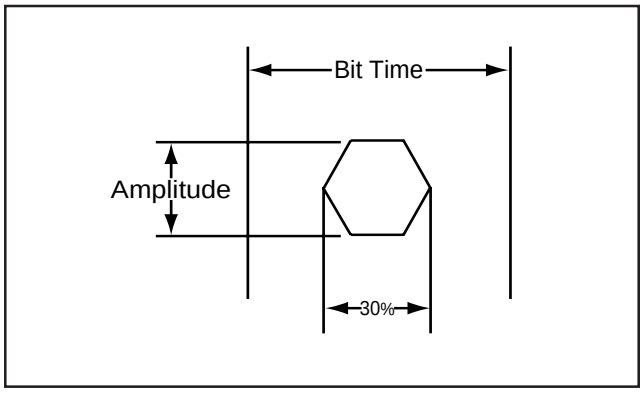


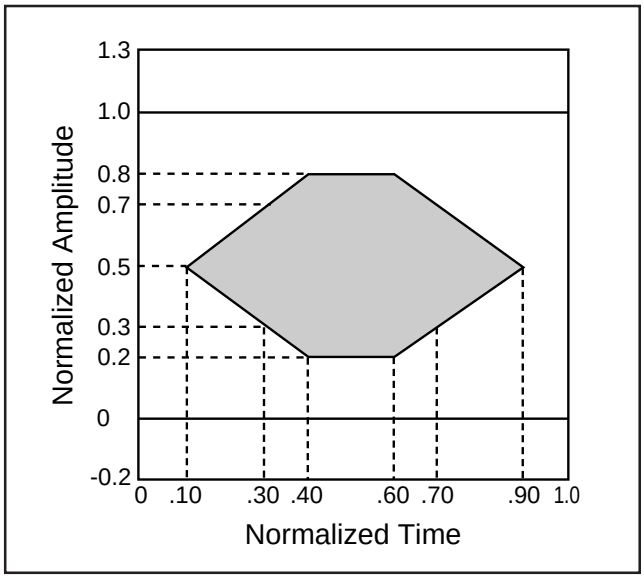
Figure 20. Receiver Input Eye Diagram Jitter Mask



ACQUISITION TIME

With the input eye diagram shown in Figure 21, the S2043 will recover data with a 10^{-9} BER within 50 bit times after an instantaneous phase shift of the incoming data.

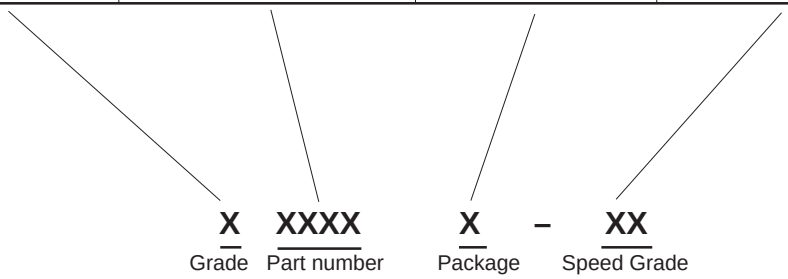
Figure 21. Acquisition Time Eye Diagram



Ordering Information

GRADE	TRANSMITTER	PACKAGE	SPEED GRADE
S – commercial	2042	B – 52 PQFP	10 – 1062, 531, 266 Mbit/s

GRADE	RECEIVER	PACKAGE	SPEED GRADE
S – commercial	2043	B – 52 PQFP	10 – 1062, 531, 266 Mbit/s



Example: S2042B-05 — S2042 in a 52 PQFP package operating at 531 or 266 Mbit/sec rates.

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