Advance Information

Low Voltage 1:18 Clock Distribution Chip

MPC940

LOW VOLTAGE 1:18 CLOCK DISTRIBUTION CHIP

The MPC940 is a 1:18 low voltage clock distribution chip. The device features the capability to select either a differential LVPECL or an LVTTL/LVCMOS compatible input. The 18 outputs are LVCMOS or LVTTL compatible and feature the drive strength to drive 50Ω series or parallel terminated transmission lines. With output–to–output skews of 150ps, the MPC940 is ideal as a clock distribution chip for the most demanding of synchronous systems. For a similar product with a larger number of outputs, please consult the MPC941 data sheet.

- LVPECL or LVCMOS/LVTTL Clock Input
- 150ps Maximum Targeted Output–to–Output Skew
- Drives Up to 36 Independent Clock Lines
- Maximum Output Frequency of 250MHz
- 32–Lead TQFP Packaging
- 3.3V V_{CC} Supply Voltage

FA SUFFIX
32–LEAD TQFP PACKAGE
CASE 873A–02

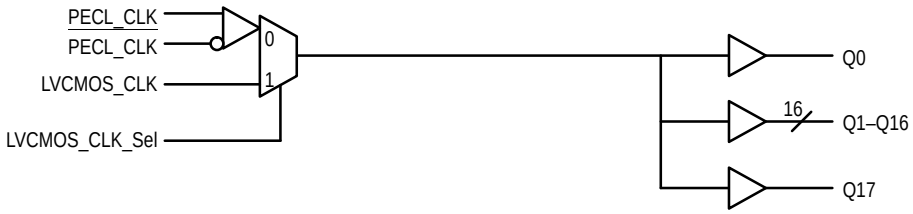
With a low output impedance (≈20Ω), in both the HIGH and LOW logic states, the output buffers of the MPC940 are ideal for driving series terminated transmission lines. More specifically, each of the 18 MPC940 outputs can drive two series terminated 50Ω transmission lines. With this capability, the MPC940 has an effective fanout of 1:36 in applications where each line drives a single load. With this level of fanout, the MPC940 provides enough copies of low skew clocks for most high performance synchronous systems.

The differential LVPECL inputs of the MPC940 allow the device to interface directly with a LVPECL fanout buffer like the MC100EP111 to build very wide clock fanout trees or to couple to a high frequency clock source. The LVCMOS/LVTTL input provides a more standard interface for applications requiring only a single clock distribution chip at relatively low frequencies. In addition, the two clock sources can be used to provide for a test clock interface as well as the primary system clock. A logic HIGH on the LVCMOS_CLK_Sel pin will select the TTL level clock input.

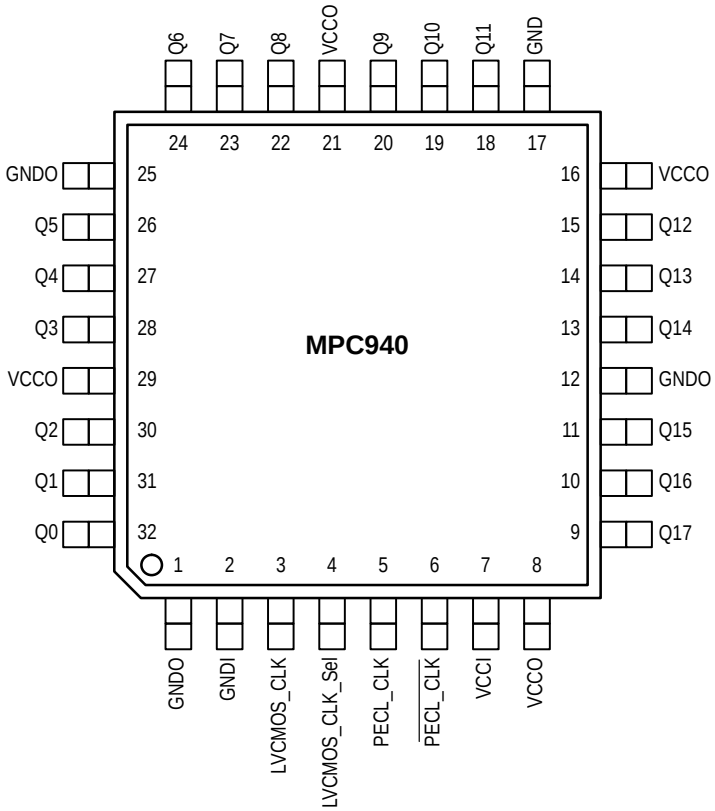
The MPC940 is fully 3.3V compatible. The 32–lead TQFP package was chosen to optimize performance, board space and cost of the device. The 32–lead TQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

LOGIC DIAGRAM



Pinout: 32–Lead TQFP (Top View)



FUNCTION TABLE

LVCMOS_CLK_Sel	Input
0	PECL_CLK
1	LVCMOS_CLK

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	3.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	PECL_CLK Other	2.135 2.0		2.42 3.60	V	
V_{IL}	Input LOW Voltage	PECL_CLK Other	1.49		1.825 0.8	V	
V_{PP}	Peak–to–Peak Input Voltage	PECL_CLK	300		1000	mV	
V_{CMR}	Common Mode Range	PECL_CLK	V_{CC}–2.0		V_{CC}–0.6	V	
V_{OH}	Output HIGH Voltage		2.5			V	I_{OH} = –16mA, Note 1.
V_{OL}	Output LOW Voltage				0.5	V	I_{OH} = 16mA, Note 1.
I_{IN}	Input Current				±100	µA	
C_{IN}	Input Capacitance				4	pF	
C_{pd}	Power Dissipation Capacitance			8		pF	Per Output
I_{CC}	Maximum Quiescent Supply Current	I_{CCL} I_{CCH}		70 140		mA	

1. The MPC940 outputs can drive series or parallel terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge.

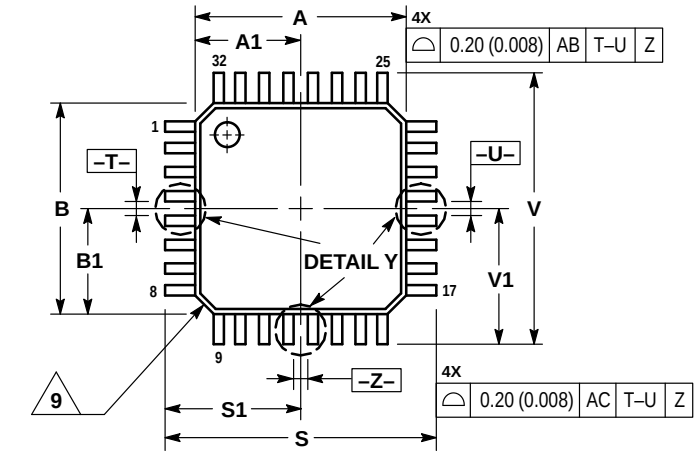
AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

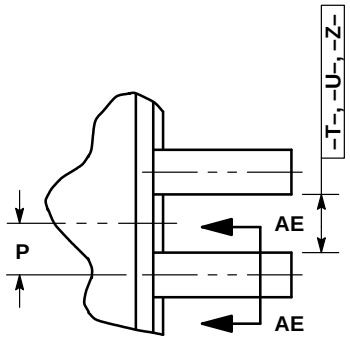
Symbol	Characteristic		Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency			250		MHz	Note 1.
t_{pd}	Propagation Delay	PECL_CLK to Q TTL_CLK to Q		1.7 2.0		ns	Note 1.
$t_{sk(o)}$	Output–to–Output Skew				150	ps	Note 1.
$t_{sk(pr)}$	Part–to–Part Skew	PECL_CLK to Q TTL_CLK to Q		800 800		ps	Notes 2., 3.
t_{pwo}	Output Pulse Width		45		55	p%	Note 1., Measured at V_{CC}/2
t_r, t_f	Output Rise/Fall Time		0.20		1.0	ns	0.8V to 2.0V

1. Driving 50Ω transmission lines
2. Part–to–part skew at a given temperature and voltage
3. Final specification limits will be determined from matrix lot material. 800ps is the “best estimate” based on initial material and experience with previous products.

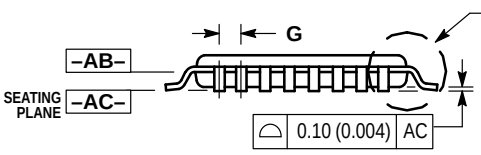
OUTLINE DIMENSIONS

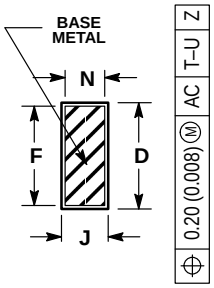
FA SUFFIX
TQFP PACKAGE
CASE 873A–02
ISSUE A



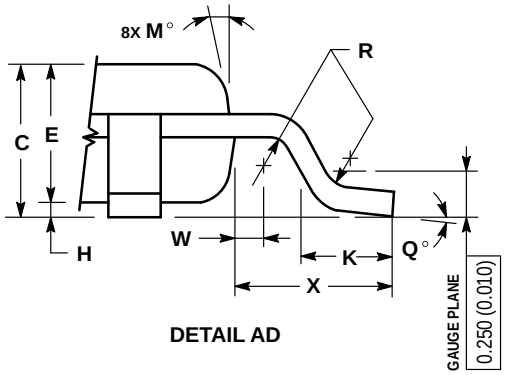


DETAIL Y





SECTION AE–AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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