Features

PEX 8547 General Features

- o 48-lane PCI Express switch
- Three configurable ports (x1, x2, x4, x8, x16)
- o Integrated SerDes
- o 37.5mm x 37.5mm, 736 pin PBGA package
- o Typical Power: 4.9 Watts

PEX 8547 Key Features

- o Standards Compliant
- PCI Express Base Specification, r1.1
- High Performance
 - Packet Cut Through
 - Packet Latency of 110ns (x16 to x16)
 - Non-blocking Switch Fabric
 - Full Line rate
- Flexible Configuration
 - Three configurable ports
 - Flexible lane width/port x1, x2, x4, x8, 16
 - Configurable with strapping pins, EEPROM, Host software or I²C
- Lane and polarity reversal
- o PCI Express Power Management
- Link power management states: L0, L0s, L1, L2/L3 Ready, and L3
- Device states: D0 and D3hot
- INTA and FATAL ERROR signal support
- Port Status bits and GPO available
- o Quality of Service (QoS)
 - Eight Traffic Classes per port
 - Round Robin and Weighted RR port arbitration
- Reliability, Availability, Serviceability (RAS)
 - Error reporting in addition to Advanced Error Reporting support of PCI Express
 - Per port performance monitoring
 - Average packet size, number of packets, CRC errors
 - JTAG boundary scan



PEX 8547

PCI ExpressTM Switch for Graphics Fan-Out

Multi-Purpose, Feature Rich PCI Express* ExpressLane™ Switch

The ExpressLane **PEX 8547** device offers PCI Express **switching** capability conforming to the latest revision of the PCI Express Base specification (r1.1). This device enables users to add scalable high bandwidth, **non-blocking** interconnects to high-end graphics applications. The PEX 8547 is designed to support graphics or data aggregation while supporting **peer-to-peer** traffic for high resolution graphics applications.

High Performance

The ExpressLane PEX 8547 architecture supports packet **cut-through with a latency of 110ns (x16 to x16).** This, combined with large packet memory (**256 to 1024 byte maximum payload size**) and nonblocking internal switch architecture, provide full line rate on its ports for performance hungry applications such as storage servers or storage switch fabrics.

Low Packet Latency

The PEX 8547 supports packet cut-through with a latency of 110ns between symmetric (x16) ingress and egress ports. The low latency enables many applications to achieve high throughput and performance. In addition to low latency, the device supports a packet payload size of up to 1024 bytes, enabling the user to achieve even higher throughput.

Low Power with Granular SerDes Control

The ExpressLane PEX 8547 provides **low power** capability that is fully compliant with the PCI Express power management specification.

Interoperability

The ExpressLane PEX 8547 is designed to be fully compliant with the PCI-SIG specification. Additionally, it supports auto-negotiation, lane reversal, and polarity reversal.

Configuration Flexibility

The ExpressLane PEX 8547 provides several ways to configure its operations. The device can be configured through strapping pins, I²C interface, CPU configuration cycles, or an optional serial EEPROM. This allows for easy debug during the development phase, performance monitoring during the operation phase, and driver or software upgrade.

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Fully Compliant Power Management

For applications that require power management, the ExpressLane PEX 8547 device supports both link (L0, L0s, L1, L2/L3 Ready, and L3) and device (D0 and D3hot) power management states, in compliance with the PCI Express power management specification.

SerDes Power and Signal Management

The ExpressLane PEX 8547 supports **software control** of the SerDes outputs to allow optimization of power and signal strength in a system. The PLX SerDes implementation supports four levels of power – off, low, typical and high. The SerDes block also supports loopback modes and advanced reporting of error conditions, which enables efficient debug and management of the entire system.

Applications

Targeted at high-end graphics applications, the PEX 8547 supports **host-centric** as well as **peer-to-peer** traffic patterns.

Host-Centric Graphics Fan-out Switch

In a graphics fan-out application (see Figure 1), the PEX 8547 drives a dual-output display. The PEX 8547 will fan out to two Graphics Modules (shown as GPUs in the Figures) via the two x16 downstream ports while the x16 upstream port links to the Root Complex. Each graphics

module drives its own monitor. Increasing memory and bandwidth requirements have put a strain on local GPU memory. The PEX 8547 allows for highly efficient data transfers over the PCI Express bus, allowing the Graphics Module to utilize the system memory and render it as if it were local graphics memory. In a fan-out application such as this one, the traffic patterns are hostcentric, with each Graphics Module driving its own output.



Figure 1. Dual Graphics Fan-Out

Dual Graphics with Peer-to-Peer Communication

High resolution 3D graphics applications can take full advantage of the PEX 8547 three port configuration. Applications such as high-resolution gaming, high resolution scientific use, and image processing can benefit from the performance of the PEX 8547 switch.

Figure 2 illustrates the use of the device in a high resolution gaming application where two Graphics Modules drive a single monitor for the ultimate gaming experience. The upstream x16 port links to the Root Complex and the two downstream ports connect to the Graphics Modules. The peer-to-peer support of the PEX 8547 allows the two Graphics Modules to communicate with each other for maximum performance.

In this example, the two Graphics Modules divide the screen into a

checkerboard pattern. In Figure 2, the screen is divided into white frames and blue frames, with one GPU managing the white frames and the other managing the blue frames. This mode of operation is referred to as Supertiling, and is generally the most efficient because it evenly divides the processing and graphics rendering workload across the two Graphics Modules. This usage model calls for heavy peerto-peer communication between the two Graphics Modules.



The PEX 8547 can also support dual-graphics solutions running in scissor, or alternate frame-rate modes. In each of these modes, the processing and graphics rendering workload is shared by the Graphics Modules, and therefore requires a great amount of peer-to-peer communication between the Graphics Modules to monitor each other's progress and execution.

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Development Tools

PLX is offering hardware and software tools (PEX 8547 RDK) to enable rapid customer design activity. These tools are bundled in a Rapid Development Kit (RDK). The RDK consists of hardware, hardware documentation and a Software Development Kit (SDK).



Figure 3. PEX 8547 RDK

The PEX 8547 RDK board can be installed on a motherboard or used as a riser card. The PEX 8547 RDK can be used to test and validate customer software. Additionally, it can be used as an evaluation vehicle for PEX 8547 features and benefits. The PEX 8547 RDK features three x16 ports (one upstream, two downstream).

SDK

The SDK tool set includes:

- GUI to use and configure the device
- Linux and Windows drivers
- C/C++ Source code, Objects, libraries
- User's Guides, Application examples, Tutorials





PLX Technology, Inc. 870 Maude Ave. Sunnyvale, CA 94085 USA Tel: 1-800-759-3735 Tel: 1-408-774-9060 Fax: 1-408-774-2169 Email: info@plxtech.com Web Site: www.plxtech.com

Product Ordering Information

Part Number	Description
PEX 8547-AA25BC G	48-Lane, 3-Port PCI Express Switch, Pb-Free
PEX 8547-AA RDK	PEX 8547 Rapid Development Kit w/ x16 Edge Connector
Breakout Board-88	Breakout Board w/ x16 Edge Connector for additional fan-out to two slots (x8, x8)
Breakout Board-844	Breakout Board w/ x16 Edge Connector for additional fan-out to three slots (x8, x4, x4)

Please visit the PLX Web site at http://www.plxtech.com or contact PLX sales at 408-774-9060 for sampling.

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