NEC

DATA SHEET

MOS INTEGRATED CIRCUIT

μPD70236A

V53A™
16-BIT MICROPROCESSOR

DESCRIPTION

The μPD70236A (V53A) is a 16-bit CMOS microprocessor that is software-compatible with the μPD70136A (V33A™).

The μPD70236A is based on the μPD70236 (V53™) with the only difference being its CPU, which is equivalent to that of the μPD70136A, instead of that of the μPD70136 (V33™).

The μPD70236A has a variety of on-chip peripheral LSI functions, enabling the creation of high-performance, very compact, low-power consumption, and high-reliability application systems.

Functions are described in detail in the following User's Manuals, which should be read before starting design work.

- **V53A User's Manual: U10108E**
- **16-Bit V Series™ User's Manual – Instructions: IEU-804***

(*: Document No. of Japanese version)

FEATURES

- High-performance 16-bit CPU (software-compatible with V33A)
  - 16M-byte memory space and 64K-byte I/O space
  - Software-compatible with V20™, V30™, V40™, and V50™ native modes
  - Dynamic bus sizing function
- On-chip standard peripheral LSI functions. . . TCU, SCU, DMAU, CG, WCU, REFU, BAU, ICU
- Allows connection of μPD72291 floating-point operation coprocessor.
- Standby functions. . . HALT mode
  STOP mode
- Maximum operating frequency: 20 MHz (with 40 MHz supplied externally)
- Operating temperature range: –40 to +85 °C
- Low voltage: V_{DD} = 2.7 V to 3.6 V (Max. 10 MHz)
- Small package versions available (20 x 20 mm fine-pitch QFP, 14 x 14 mm fine-pitch TQFP)
- Low current consumption

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The information in this document is subject to change without notice.

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Printed in Japan

The mark * shows revised points.

APPLICATIONS

- OA equipment (personal computers, word processors, etc.)
- Various control equipment (robot control, communications control, etc.)

ORDERING INFORMATION

	Part Number	Package	Max. Operating Frequency (MHz)
	μPD70236AGD-10-5BB	120-pin plastic QFP (28 x 28 mm)	10
	μPD70236AGD-12-5BB	120-pin plastic QFP (28 x 28 mm)	12.5
	μPD70236AGD-16-5BB	120-pin plastic QFP (28 x 28 mm)	16
	μPD70236AGD-20-5BB	120-pin plastic QFP (28 x 28 mm)	20
	μPD70236AGJ-10-3EB	120-pin plastic QFP (Fine pitch)(20 x 20 mm)	10
	μPD70236AGJ-12-3EB	120-pin plastic QFP (Fine pitch)(20 x 20 mm)	12.5
	μPD70236AGJ-16-3EB	120-pin plastic QFP (Fine pitch)(20 x 20 mm)	16
	μPD70236AGJ-20-3EB	120-pin plastic QFP (Fine pitch)(20 x 20 mm)	20
*	μPD70236AGC-10-9EV	120-pin plastic TQFP (Fine pitch) (14 x 14 mm)	10
*	μPD70236AGC-12-9EV	120-pin plastic TQFP (Fine pitch) (14 x 14 mm)	12.5
*	μPD70236AGC-16-9EV	120-pin plastic TQFP (Fine pitch) (14 x 14 mm)	16
*	μPD70236AGC-20-9EV	120-pin plastic TQFP (Fine pitch) (14 x 14 mm)	20
	μPD70236ARB-10	132-pin ceramic PGA	10
	μPD70236ARB-12	132-pin ceramic PGA	12.5
	μPD70236ARB-16	132-pin ceramic PGA	16
	μPD70236ARB-20	132-pin ceramic PGA	20

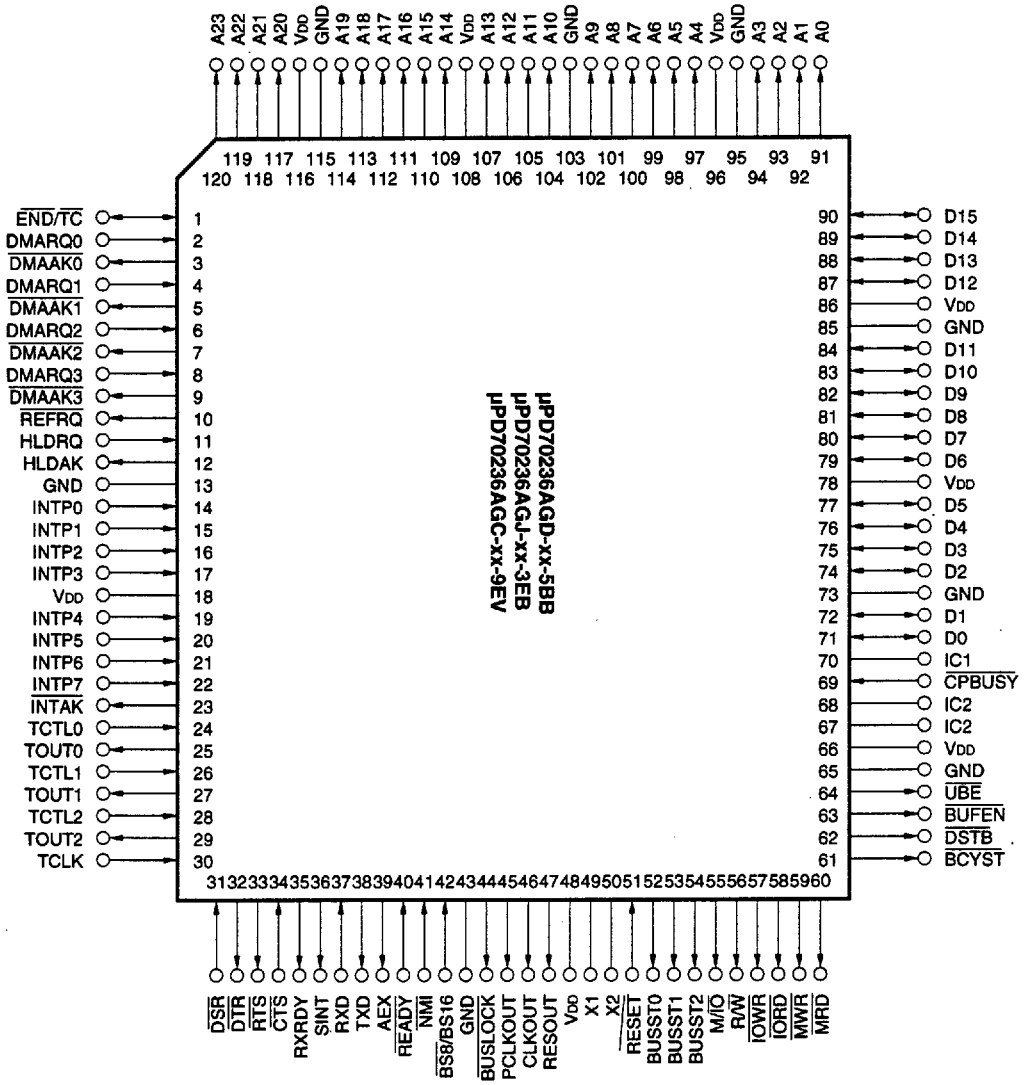
DIFFERENCES BETWEEN μPD70236A AND μPD70236

Parameter \ Part Number			V53A						V53				
			μPD70236A						μPD70236(A)		μPD70236		
			-10	-12	-16		-20		-10	-12	-10	-12	-16
Supply voltage: V_{DD} = 5 V ±10%	Operating temperature range: T_A [°C]		–40 to +85		–10 to +70	–40 to +85	–10 to +70		–40 to +85		–10 to +70		
	Operating frequency: f_x [MHz]Note 1		10	12.5	16		20		10	12.5	10	12.5	16
	Delay time (example): t_{DKA} [ns]	MAX.	35	30	20	30	20		45				40
		MIN.	2		3	2	3		5				
	Supply current: I_{DD} [mA]Note 2	Operating	f_x x 3.9 + 3						f_x x 10 + 20				
		HALT	1.0						20				
		STOP	0.005						1.0				
Supply voltage: V_{DD} = 3.6 to 4.5 V	Operating temperature range: T_A [°C]				–40 to +85								
	Operating frequency: f_x [MHz]Note 1				12.5		16						
	Delay time (example): t_{DKA} [ns]Note 1				35								
	Supply current: I_{DD} [mA]Note 2	Operating			f_x x 2.9 + 2								
		HALT			0.8								
		STOP			0.004								
Supply voltage : V_{DD} = 2.7 to 3.6 V	Operating temperature range: T_A [°C]				–40 to +85								
	Operating frequency: f_x [MHz]Note 1				8		10						
	Delay time (example): t_{DKA} [ns]Note 1				45								
	Supply current: I_{DD} [mA]Note 2	Operating			f_x x 2.2 + 2								
		HALT			0.6								
		STOP			0.003								
I/O recovery cycle			2 clocks						6 clocks				
Standby control register oscillation stabilization time			$2^{15}/f_{XX}$ to $2^{18}/f_{XX}$						$2^{18}/f_{XX}$ to $2^{21}/f_{XX}$				
External clock X1 input with X2 open			Possible						Not possible				
SCU transmission control by $\overline{CTS}$			External circuit unnecessary						External circuit necessary				
120-pin plastic QFP (fine-pitch) (20 x 20 mm)			Provided						Not provided				*
120-pin plastic TQFP (fine-pitch) (14 x 14 mm)			Provided						Not provided				*

Notes 1. MAX value
2. TYP value

PIN CONFIGURATION

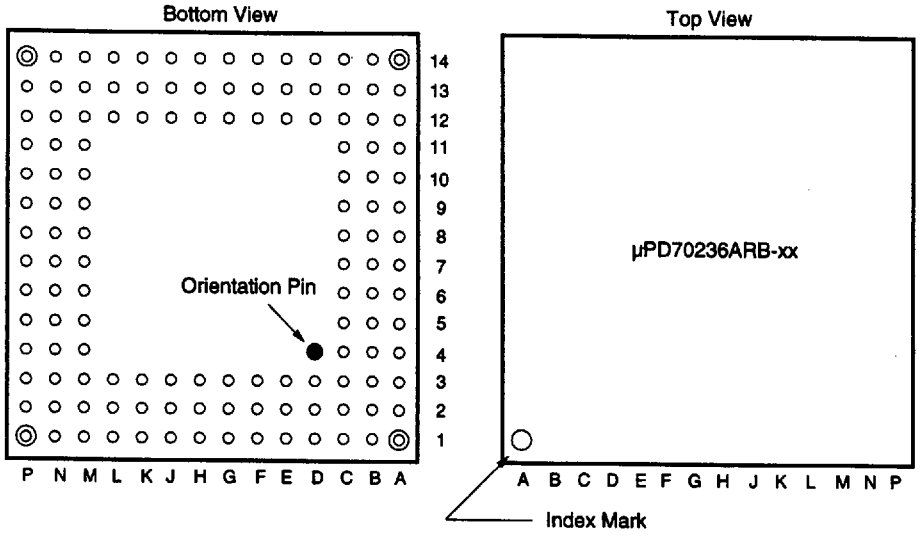
120-pin plastic QFP (28 x 28 mm) (Top View)
120-pin plastic QFP (Fine Pitch) (20 x 20 mm) (Top View)
120-pin plastic TQFP (Fine Pitch) (14 x 14 mm) (Top View)



IC: Internally Connected

Cautions 1. IC1: Leave open.
2. IC2: Connect to the ground.

132-pin ceramic PGA

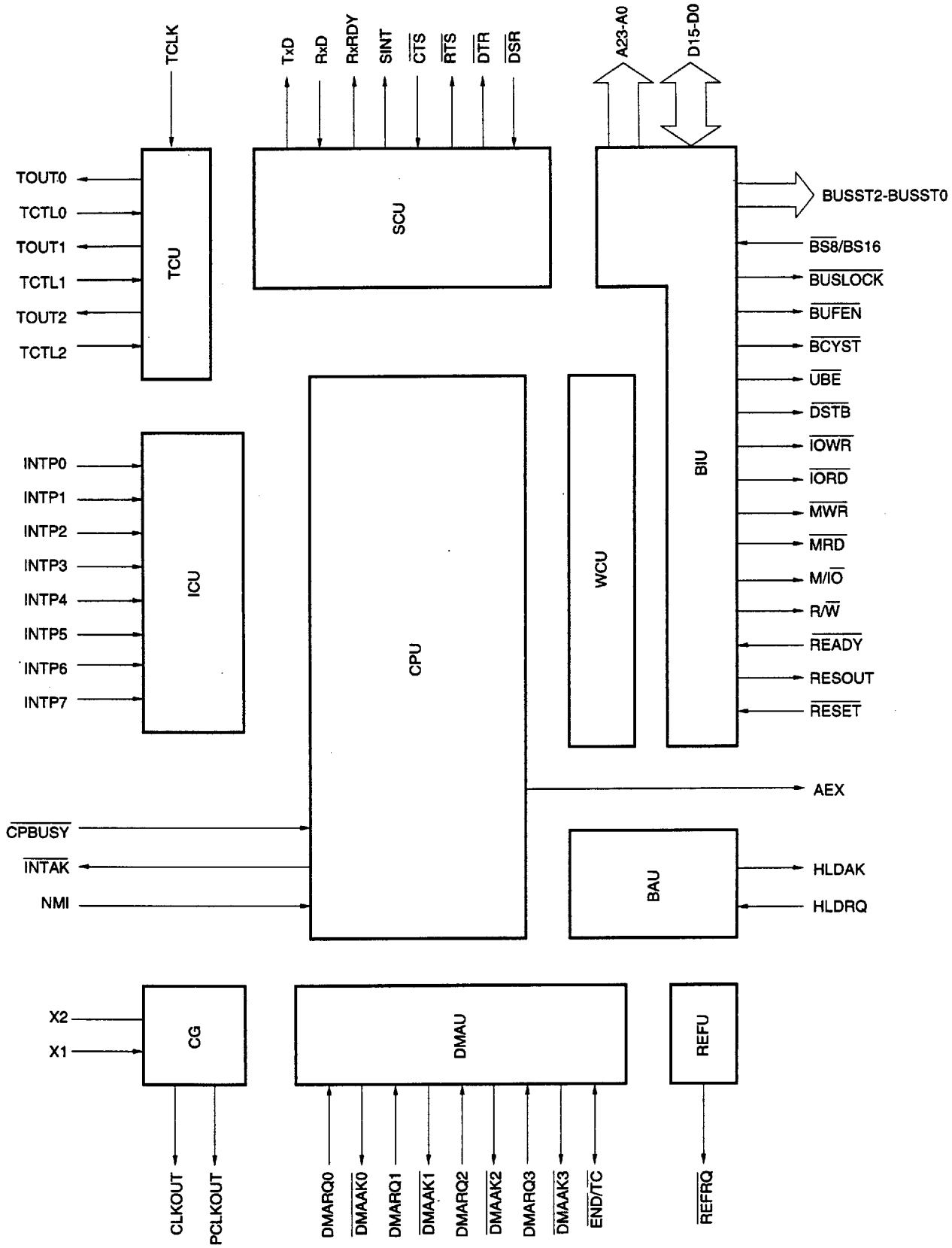


Remark The orientation pin is not included in the pin count.

No.	Name	No.	Name	No.	Name	No.	Name	No.	Name	No.	Name
A1	A22	B9	A9	D3	DMARQ0	H1	INTP2	L13	GND	N7	$\overline{\text{BUSLOCK}}$
A2	A20	B10	A5	D12	D14	H2	INTP3	L14	IC2	N8	RESOUT
A3	GND	B11	GND	D13	IC1	H3	V_{DD}	M1	TOUT0	N9	X2
A4	A19	B12	A2	D14	D11	H12	GND	M2	TCTL2	N10	BUSST0
A5	A16	B13	IC1	E1	HLDRQ	H13	D2	M3	TCLK	N11	R/$\overline{\text{W}}$
A6	A14	B14	D12	E2	$\overline{\text{DMAAK3}}$	H14	D3	M4	$\overline{\text{DTR}}$	N12	$\overline{\text{IORD}}$
A7	A12	C1	$\overline{\text{DMAAK2}}$	E3	$\overline{\text{DMARQ2}}$	J1	INTP4	M5	RxRDY	N13	$\overline{\text{BCYST}}$
A8	A11	C2	$\overline{\text{DMAAK0}}$	E12	V_{DD}	J2	INTP5	M6	AEX	N14	$\overline{\text{UBE}}$
A9	NC	C3	IC1	E13	D10	J3	INTP7	M7	GND	P1	$\overline{\text{DSR}}$
A10	A8	C4	A23	E14	D8	J12	IC1	M8	V_{DD}	P2	$\overline{\text{CTS}}$
A11	A6	C5	IC1	F1	NC	J13	D1	M9	BUSST1	P3	SINT
A12	A4	C6	A18	F2	HLDAK	J14	NC	M10	IC1	P4	TxD
A13	A3	C7	V_{DD}	F3	$\overline{\text{REFRQ}}$	K1	INTP6	M11	$\overline{\text{MRD}}$	P5	$\overline{\text{READY}}$
A14	A0	C8	GND	F12	D9	K2	$\overline{\text{INTAK}}$	M12	IC1	P6	$\overline{\text{BS8}}$/BS16
B1	DMARQ1	C9	A7	F13	D7	K3	TCTL1	M13	$\overline{\text{BUFEN}}$	P7	PCLKOUT
B2	$\overline{\text{END}}$/$\overline{\text{TC}}$	C10	V_{DD}	F14	D6	K12	V_{DD}	M14	IC2	P8	CLKOUT
B3	A21	C11	A1	G1	INTP1	K13	$\overline{\text{CPBUSY}}$	N1	TOUT1	P9	X1
B4	V_{DD}	C12	D15	G2	INTP0	K14	D0	N2	IC1	P10	$\overline{\text{RESET}}$
B5	A17	C13	D13	G3	GND	L1	TCTL0	N3	$\overline{\text{RTS}}$	P11	BUSST2
B6	A15	C14	GND	G12	V_{DD}	L2	IC1	N4	IC1	P12	M/$\overline{\text{IO}}$
B7	A13	D1	DMARQ3	G13	D5	L3	TOUT2	N5	RxD	P13	$\overline{\text{IOWR}}$
B8	A10	D2	$\overline{\text{DMAAK1}}$	G14	D4	L12	$\overline{\text{DSTB}}$	N6	$\overline{\text{NMI}}$	P14	$\overline{\text{MWR}}$

Cautions 1. **IC1: Leave open.**
2. **IC2: Connect to the ground.**

INTERNAL BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

1.1 LIST OF PIN FUNCTIONS

*

Pin Name	Input/Output	Function	Recommended Connections of Unused Pins
A23 to A0	3-state output	Address bus	Leave open.
D15 to D0	3-state input/ output	Data bus	
$\overline{UBE}$	3-state output	Data bus upper byte enable	
R/$\overline{W}$	3-state output	Read/write selection	
M/$\overline{IO}$	3-state output	Memory/(I/O) selection	
BUSST2 to BUSST0	3-state output	Bus status	
$\overline{BCYST}$	3-state output	Bus cycle start	
$\overline{DSTB}$	3-state output	Data strobe	
$\overline{MRD}$	3-state output	Memory read	
$\overline{MWR}$	3-state output	Memory write	
$\overline{IORD}$	3-state output	I/O read	
$\overline{IOWR}$	3-state output	I/O write	
$\overline{BUFEN}$	3-state output	Buffer enable	
$\overline{BUSLOCK}$	Output	Bus lock indication	
$\overline{READY}$	Input	Bus cycle end	Connect to GND through resistor.
$\overline{BS8}$/BS16	Input	Data bus width specification	Connect to V_{DD} or GND through resistor.
AEX	Output	Address extension mode indication	Leave open.
$\overline{REFRQ}$	Output	Refresh request	
HLDRQ	Input	Bus hold request	Connect to GND through resistor.
HLDAK	Output	Bus hold enable	Leave open.
$\overline{NMI}$	Input	Non-maskable interrupt request	Connect to V_{DD} through resistor.
$\overline{CPBUSY}$	Input	Co-processor busy	Connect to GND through resistor.
$\overline{RESET}$	Input	Reset	—
RESOUT	Output	System reset output	Leave open.
X2, X1	Input	Crystal/external clock	—
CLKOUT	Output	System clock output	Leave open.
PCLKOUT	Output	External I/O clock output	
TCLK	Input	Timer clock	Connect to V_{DD} or GND through resistor.
TCTL0 toTCTL2	Input	Timer control	
TOUT0 to TOUT2	Output	Timer output	Leave open.
INTP0 to INTP7	Input	Maskable interrupt request	Connect to GND through resistor.
$\overline{INTAK}$	Output	Interrupt acknowledge	Leave open.
TxD	Output	Serial transmit data	
RxD	Input	Serial receive data	Connect to GND through resistor.
RxRDY	Output	Serial receive enable	Leave open.
SINT	Output	Serial interrupt request	
$\overline{RTS}$	Output	Request to send	

Pin Name	Input/Output	Function	Recommended Connections of Unused Pins
$\overline{CTS}$	Input	Clear to send	Connect to V_{DD} or GND through resistor.
$\overline{DTR}$	Output	Data terminal ready	Leave open.
$\overline{DSR}$	Input	Data set ready	Connect to V_{DD} or GND through resistor.
DMARQ0 to DMARQ3	Input	DMA request	Connect to GND through resistor.
$\overline{DMAAK0}$ to $\overline{DMAAK3}$	Output	DMA acknowledge	Leave open.
$\overline{END}/\overline{TC}$	Input/output	DMA service forced termination input/ DMA service completion output	Connect individually to V_{DD} through resistor.
V_{DD}	—	Positive power supply pin	—
GND	—	Ground potential pin	—
IC1	—	Internally connected pin	Leave open.
IC2	—	Intenally connected pin	Connect to GND.

1.2 PIN STATES IN SPECIFIC STATES

The state of each pin in specific states (bus hold, standby mode, reset, DMA cascade) is shown below.

Table 1-1 Pin States in Specific States (1/2)

Pin Name	Input/Output	Bus Latch Note 1	Specific States				Asynchronous Input with Respect to CLKOUT
			Bus Hold	Standby Mode	Reset	DMA Cascade	
A23 to A0	3-state output	Yes	Hi-Z	L	Hi-Z	Hi-Z	
D15 to D0	3-state input/ output	Yes	Hi-Z	**Note 2**	Hi-Z	Hi-Z	
$\overline{UBE}$	3-state output	Yes	Hi-Z	H	Hi-Z	Hi-Z	
R/$\overline{W}$	3-state output	Yes	Hi-Z	L	Hi-Z	H	
M/$\overline{IO}$	3-state output	Yes	Hi-Z	L	Hi-Z	H	
BUSST2 to BUSST0	3-state output	Yes	Hi-Z	**Note 8**	Hi-Z	H	
$\overline{BCYST}$	3-state output	Yes	Hi-Z	**Note 3**	Hi-Z	Hi-Z	
$\overline{DSTB}$	3-state output	Yes	Hi-Z	H	Hi-Z	Hi-Z	
$\overline{MRD}$	3-state output	Yes	Hi-Z	H	Hi-Z	Hi-Z	
$\overline{MWR}$	3-state output	Yes	Hi-Z	H	Hi-Z	Hi-Z	
$\overline{IORD}$	3-state output	Yes	Hi-Z	H	Hi-Z	Hi-Z	
$\overline{IOWR}$	3-state output	Yes	Hi-Z	H	Hi-Z	Hi-Z	
$\overline{BUFEN}$	3-state output	Yes	Hi-Z	H	Hi-Z	Hi-Z	
$\overline{BUSLOCK}$	Output	No	**Note 4**	**Note 4**	H	H	
$\overline{READY}$	Input	No	—	—	—	—	Not possible
$\overline{BS8}$/BS16	Input	No	—	—	—	—	Not possible
AEX	Output	No	**Note 5**	**Note 5**	H/L	**Note 5**	
$\overline{REFRQ}$	Output	No	H	**Note 6**	H	H	
HLDRQ	Input	No	—	—	—	—	Possible
HLDAK	Output	No	H	H/L	L	L	
$\overline{NMI}$	Input	No	—	—	—	—	Possible
$\overline{CPBUSY}$	Input	No	—	—	—	—	Possible
$\overline{RESET}$	Input	No	—	—	—	—	Possible
RESOUT	Output	No	L	L	H	L	
X2, X1	Input	No	—	—	—	—	
CLKOUT	Output	No	Not fixed	**Note 7**	Not fixed	Not fixed	
PCLKOUT	Output	No	Not fixed	**Note 7**	Not fixed	Not fixed	
TCLK	Input	No	—	—	—	—	Possible
TCTL0 to TCTL2	Input	No	—	—	—	—	Possible
TOUT0 to TOUT2	Output	No	Not fixed	Not fixed	Not fixed	Not fixed	
INTP0 to INTP7	Input	No	—	—	—	—	Possible
$\overline{INTAK}$	Output	No	H	H	H	H	

Table 1-1 Pin States in Specific States (2/2)

Pin Name	Input/Output	Bus Latch[Note 1]	Specific States				Asynchronous Input with Respect to CLKOUT
			Bus Hold	Standby Mode	Reset	DMA Cascade	
TxD	Output	No	Not fixed	Not fixed	H	Not fixed	
RxD	Input	No	—	—	—	—	Possible
RxRDY	Output	No	Not fixed	Not fixed	H	Not fixed	
SINT	Output	No	Not fixed	Not fixed	L	Not fixed	
$\overline{RTS}$	Output	No	Not fixed	Not fixed	H	Not fixed	
$\overline{CTS}$	Input	No	—	—	—	—	Possible
$\overline{DTR}$	Output	No	Not fixed	Not fixed	H	Not fixed	
$\overline{DSR}$	Input	No	—	—	—	—	Possible
DMARQ0 to DMARQ3	Input	No	—	—	—	—	Possible
$\overline{DMAAK0}$ to $\overline{DMAAK3}$	Output	No	H	Not fixed	H	Not fixed	
$\overline{END}/\overline{TC}$	Input/output	No	Hi-Z	Not fixed	Hi-Z	Not fixed	Not possible
V_{DD}	—	No	—	—	—	—	
GND	—	No	—	—	—	—	
IC2, IC1	—	No	—	—	—	—	

Notes 1. Yes : Latch incorporated.
No : Latch not incorporated.
See **Fig. 1-1 Latch Configuration Diagram.**
When pins that incorporate a latch become Hi-Z, they retain their pre-Hi-Z state until driven from off-chip. Therefore, these pins need not be pulled high or low.
Also, drive capacity of the latch inversion current (I_{ILH}, I_{ILL}) or greater is required in order to invert the pin level from off-chip in the Hi-Z state.

* Immediately after power is applied, the latch level becomes undefined. Therefore, if your application requires a specific level immediately after power is applied to a latch-contained pin, connect a pull-up or pull-down resistor as required.

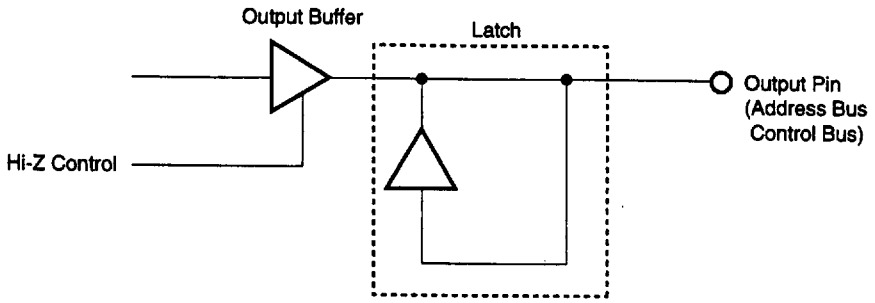
2. Undefined during the first 2 clock cycles of the halt acknowledge cycle, and Hi-Z thereafter.
3. Low during the first clock cycle of the halt acknowledge cycle, and high thereafter.
4. Low in either of the following cases, otherwise high:
- Execution of an instruction with a BUSLOCK prefix in a hold.
- Execution of a HALT instruction with a BUSLOCK prefix.

5. High in address extension mode, low in non-extension mode.
6. Not fixed in HALT mode and high in STOP mode.
7. Not fixed in HALT mode and low in STOP mode.
8. BUSST2 → Outputs low level.
BUSST1, BUSST0 → Output high level.

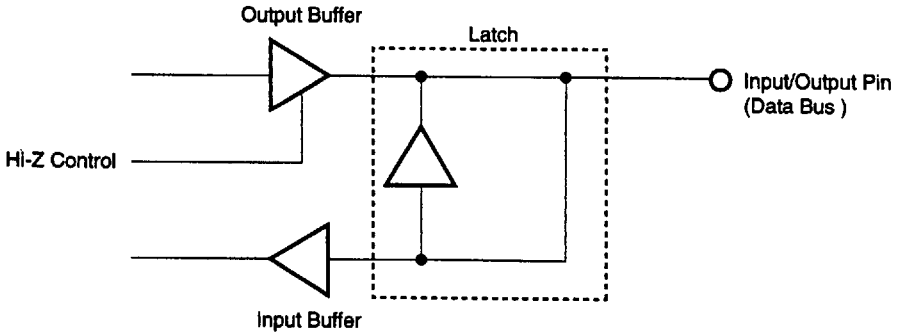
Remarks 1. H: High level,
L: Low level,
H/L: High level or low level,
Hi-Z: High-impedance,
Not fixed: outputs the valid values
2. "Standby mode" refers to either the HALT mode or STOP mode (see **13. STANDBY FUNCTIONS**).

Fig. 1-1 Latch Configuration Diagram

Output pin



Input/output pin



1.3 TYPES OF BUS CYCLES

Bus cycles initiated by the μPD70236A on the external bus are of 18 types, according to the following combinations of signals.

M/$\overline{IO}$	R/$\overline{W}$	BUSST2	BUSST1	BUSST0	Bus Cycle
0	1	0	0	0	Interrupt acknowledge cycle (from SLAVE)
0	1	1	0	0	Interrupt acknowledge cycle (from ICU)
0	1	0	0	1	External I/O read cycle
0	1	1	0	1	Internal I/O read cycle
0	0	0	0	1	External I/O write cycle
0	0	1	0	1	Internal I/O write cycle
0	1	0	1	0	Coprocessor read cycle
0	0	0	1	0	Coprocessor write cycle
0	0	0	1	1	Halt acknowledge cycle
1	1	0	0	0	Instruction fetch cycle
1	1	1	0	0	Refresh cycle
1	1	0	0	1	CPU memory read cycle
1	1	1	0	1	DMA read transfer cycle
1	0	0	0	1	CPU memory write cycle
1	0	1	0	1	DMA write transfer cycle
1	1	0	1	0	Coprocessor memory read cycle
1	0	0	1	0	Coprocessor memory write cycle
1	1	1	1	1	DMA cascade

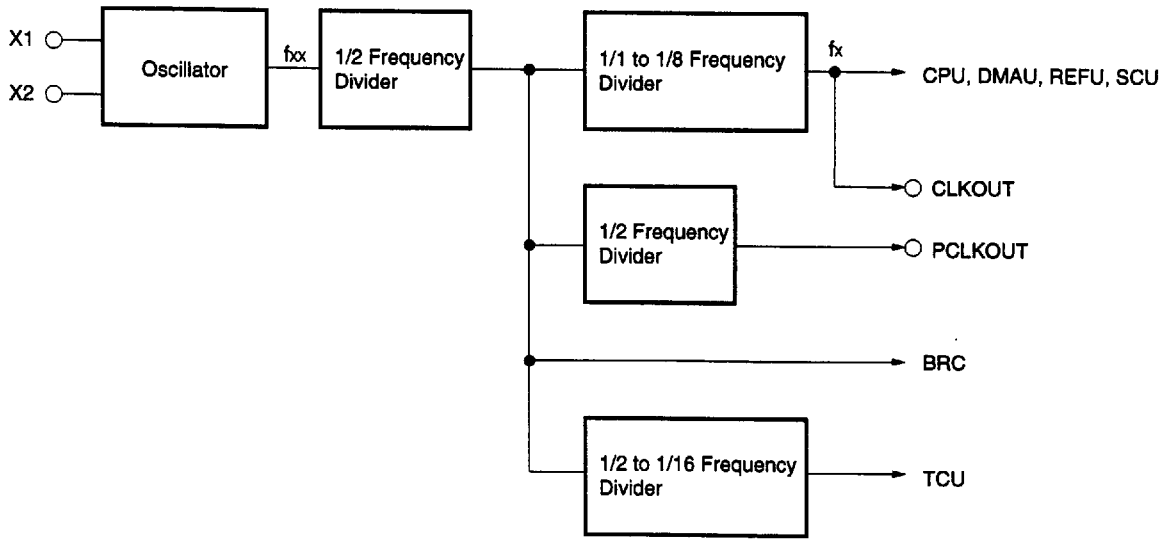
2. BLOCK CONFIGURATION

2.1 CPU

The CPU has the same functions as the μPD70136A(V33A), and has an instruction set that is upward compatible with the native mode of the V20, V30, V40 and V50. The address space can be expanded to 16M bytes.

2.2 CG (CLOCK GENERATOR)

This block generates a clock with 1/2, 1/4, 1/8 or 1/16 the frequency of the crystal and oscillator connected to the X1 and X2 pins, and supplies this clock as the CPU operating clock and also outputs it off-chip via the CLKOUT pin. In addition, this block outputs a clock with a fixed frequency 1/4 that of the oscillator frequency to the PCLKOUT pin.



2.3 BIU (BUS INTERFACE UNIT)

The BIU block controls the address bus, data bus and control bus pins. These buses are used in the CPU, DMAU and REFU blocks.

2.4 BAU (BUS ARBITRATION UNIT)

The BAU performs arbitration for μPD70236A internal bus mastership. The priority order for bus mastership is as follows:

CPU with BUSLOCK > Highest-priority REFU > DMAU > HLDRQ > Normal CPU > Lowest-priority REFU

2.5 WCU (WAIT CONTROL UNIT)

The WCU has the function of automatic insertion of 0 to 7 wait states in a memory cycle, I/O cycle, DMA cycle, or refresh cycle. 1M-byte memory space can be split into three, and 16M-byte space can be split into three.

2.6 REFU (REFRESH CONTROL UNIT)

The REFU supports DRAM refreshing by generating the 16-bit refresh address and the refresh signal ($\overline{\text{REFRQ}}$) which indicates a refresh cycle.

2.7 TCU (TIMER/COUNTER UNIT)

The TCU has equivalent functions to the μPD71054, and incorporates three 16-bit timer/counter channels.

2.8 SCU (SERIAL CONTROL UNIT)

The SCU incorporates a serial controller with equivalent functions to the μPD71051 with the exception of the synchronous mode, and supports the RS-232-C protocol.

This unit also incorporates a dedicated baud rate generator.

2.9 ICU (INTERRUPT CONTROL UNIT)

The ICU has equivalent functions to the μPD71059 with the exception of the CALL mode (8085 mode). It has 8-level external interrupt input pins, and also allows external interrupts to be extended by cascade connection.

2.10 DMAU (DMA CONTROL UNIT)

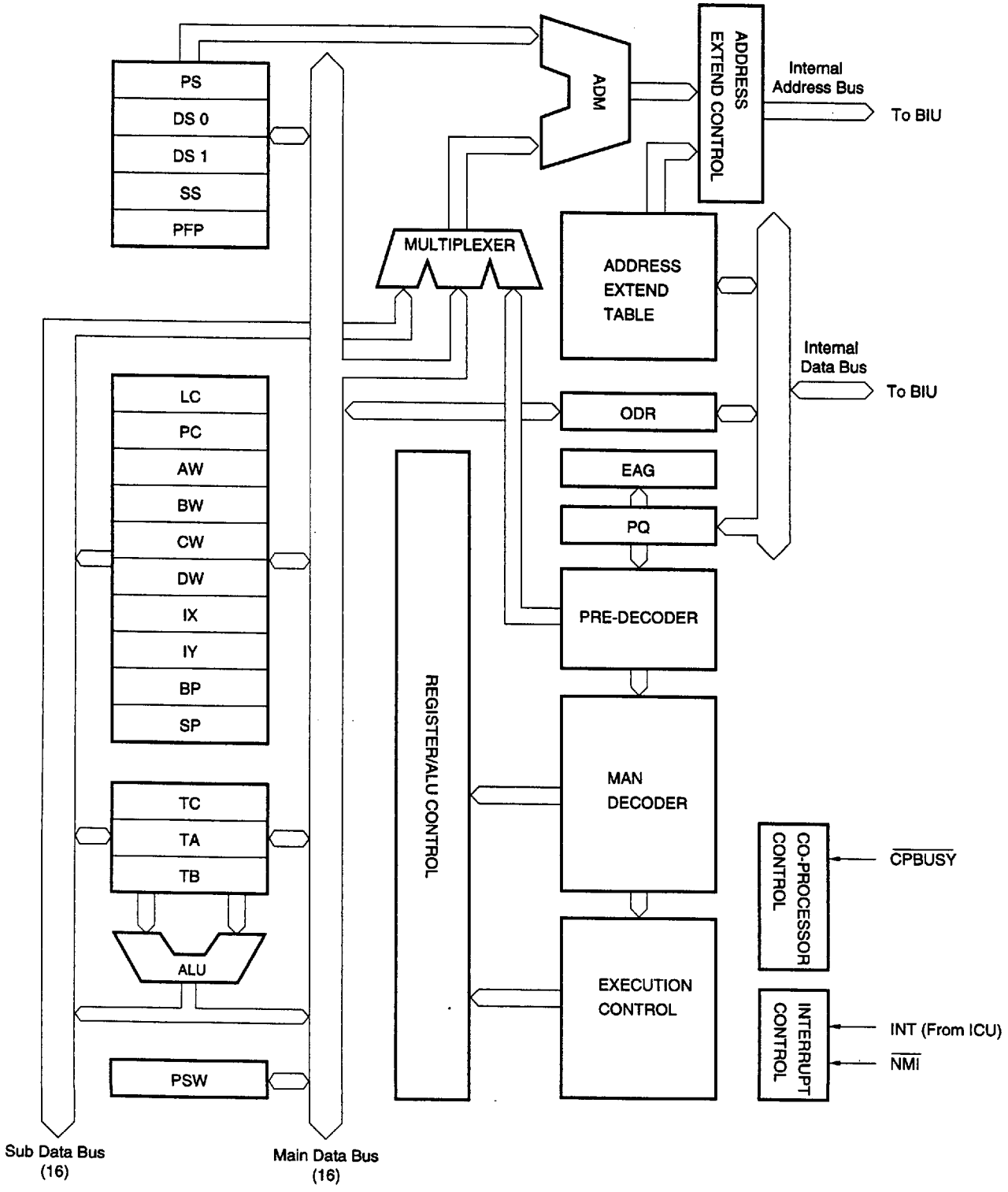
The DMAU has equivalent functions to the μPD71071 and μPD71037. Either operating mode can be selected by a setting in the system I/O area.

3. CPU

The CPU has equivalent functions to the μPD70136A. In hardware terms there are some changes in the relation between on-chip peripherals and use of bus, but in software terms the two are fully compatible.

The CPU internal block diagram is shown in Fig. 3-1.

Fig. 3-1 CPU Internal Block Diagram



3.1 REGISTER CONFIGURATION

3.1.1 PFP (Prefetch Pointer)

The prefetch pointer is a 16-bit binary counter which holds program memory address offset information.

The PFP is incremented each time an instruction byte is prefetched from program memory. It is also loaded with a new location each time a branch, call, return or break instruction is executed, in which case the contents of the PFP are the same as those of the PC (Program Counter).

The PFP is also always used as the PS (Program Segment) register.

3.1.2 PQ (Prefetch Queue)

The μPD70236 has an 8-byte instruction queue (FIFO) and can store up to 8 instruction code bytes to be prefetched.

The contents of the queue are cleared and an instruction in a new location is prefetched when a branch, call, return or break instruction is executed and when external interrupt servicing is performed.

Normally, the μPD70236A performs a prefetch when there is a space of one word (two bytes) or more in the queue.

If the average instruction time of consecutively executed instructions exceeds to a certain extent the number of clock cycles required to prefetch the operation codes of the individual instructions, when execution of one instruction ends, the next operation code which the EXU can execute is prepared in the queue and the fetch time from external memory is excluded from the instruction execution time. As a result, processing speed can be increased over that of a CPU which performs fetching and execution instruction by instruction.

The effectiveness of the queue decreases in proportion to the number of instructions for which the queue is cleared as in the execution of branch instructions as mentioned above, and when there are successive instructions with a short execution time, etc.

3.1.3 ODR (Operand Data Register)

The ODR has independent upper byte and lower byte read/ write capability for byte access purposes. A write operation is terminated by transferring data to the ODR, and a read operation is terminated by confirming that data has been transferred from the external data bus to the ODR.

3.1.4 Segment Registers (PS, SS, DS0, DS1)

The μPD70236A divides memory addresses into 64K-byte logical segments; the start address of each segment is specified by a segment register, and the offset from the start address is specified by a different register or an effective address.

There are four segment registers, as shown below.

Segment Register	Default Offset
PS (Program Segment)	PFP
SS (Stack Segment)	SP, effective address
DS0 (Data Segment 0)	IX, effective address
DS1 (Data Segment 1)	IY

The PS and PFP (Prefetch Pointer) pair and the DSI and IY pair are fixed.

The SS register is paired with the SP in normal stack manipulations, but represents the effective address offset when the BP register is selected as the base register.

The DS0 register is used together with the IX register in block transfer processing, but represents the effective address offset in other general processing.

In addressing which uses the SS register as the segment register when the BP register is used as the base register, use of a segment override prefix instruction (PS:, DS0:, DS1:) allows the other 3 segment registers to be used for segment selection.

3.1.5 ADM (Address Modifier)

The ADM (Address Modifier) performs physical address generation (addition of segment register and PFP or DP) and PFP (Prefetch Pointer) incrementing.

3.1.6 General Registers (AW, BW, CW, DW)

General registers comprise four 16-bit registers. In addition to being used as a 16-bit register, each register can be divided into a high-order and low-order 8-bit unit, each accessible as an 8-bit register (AH, AL, BH, BL, CH, CL, DH, DL).

These registers are therefore used as 8- or 16-bit registers with a wide range of instructions including transfer instructions, arithmetic operation instructions, and logical operation instructions.

In addition, individual registers are used as the default register for specific instruction processing, as shown below.

- AW : Word multiplication/division, word input/output, translation, BCD rotation, data conversion
- AL : Byte multiplication/division, byte input/output, BCD rotation, data conversion
- AH : Byte multiplication/division
- BW : Translation
- CW : Loop control branch, repeat prefix
- CL : Shift instructions, rotate instructions, BCD operation
- DW : Word multiplication/division, indirect addressing input/output

3.1.7 Pointers (SP, BP) AND Index Registers (IX, IY)

These registers are used as the base pointer or index register in a memory access using based addressing, indexed addressing, based indexed addressing, etc.

They are also used with transfer, arithmetic operation, logical operation and other instructions in the same way as general registers, but in this case they cannot be used as 8-bit registers.

In addition, individual registers are used as the default register for specific instruction processing, as shown below.

- SP : Stack manipulation
- IX : Block transfers (source side), BCD string operations
- IY : Block transfers (destination side), BCD string operations

3.1.8 TA/TB (Temporary Register/Shifter A/B)

TA/TB are 16-bit temporary registers/shifters used with multiplication/division and shift/rotate instructions (including BCD rotation).

When a multiplication/division instruction is executed, TA and TB function together as a 32-bit temporary register/ shifter, whereas in shift/rotate instruction execution TB only functions as a 16-bit temporary register/shifter.

Both TA and TB allow independent upper byte and lower byte reading/writing to/from the internal bus.

TA/TB provide ALU input.

3.1.9 TC (Temporary Register C)

TC is a 16-bit temporary register used in multiplication/ division and other internal operations.

TC provides ALU input.

3.1.10 ALU (Arithmetic Logic Unit)

The ALU (Arithmetic Logic Unit) consists of a full adder and a logic unit, and performs arithmetic operations (addition/ subtraction/multiplication/division, increment/ decrement, complement operations) and logical operations (testing, AND, OR, XOR, and bit-wise testing, setting, clearing, and inversion).

3.1.11 PSW (Program Status Word)

The program status word is composed of 6 status flags and 3 control flags.

Status Flags

- V (Overflow)
- S (Sign)
- Z (Zero)
- AC (Auxiliary Carry)
- P (Parity)
- CY (Carry)

Control Flags

- DIR (Direction)
- IE (Interrupt Enable)
- BRK (Break)

When stack processing is performed, these flags are manipulated using the following word image:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1	1	1	1	V	DIR	IE	BRK	S	Z	0	AC	0	P	1	CY	PSW

The status flags are automatically set or reset according to the result (data value) of various instruction execution.

The CY flag can be directly set, reset or complemented by an instruction.

The control flags are set or reset by an instruction, and control CPU operation.

3.1.12 LC (Loop Counter)

The LC (Loop Counter) is a 16-bit register which counts loops in primitive block transfer or input/output instructions (MOVBK, OUTM, etc.) controlled by a repeat prefix instruction (REP, REPC, etc.) and shifts in multiple bit shift/rotate instructions.

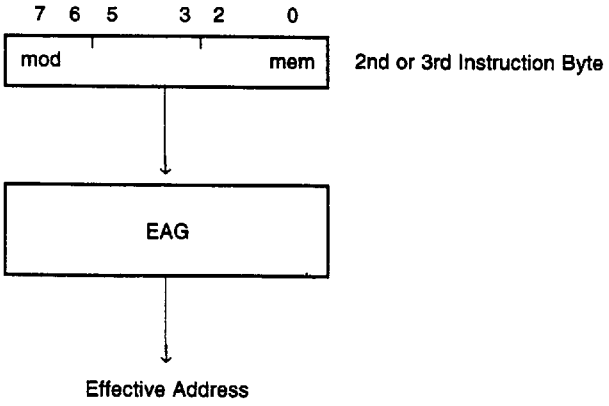
3.1.13 PC (Program Counter)

The program counter is a 16-bit binary counter which holds offset information for the program memory address on which execution is currently to be performed.

The PC is incremented each time the decoder fetches an instruction byte from the instruction queue. When a branch, call, return or break instruction is executed, the PC is loaded with a new location, and the contents of the PC are then the same as those of the PFP (Prefetch Pointer).

3.1.14 EAG (Effective Address Generator)

The EAG (Effective Address Generator) is a circuit which performs high-speed calculation of the effective address required when accessing memory. It completes the calculation in 2 clock cycles for all addressing modes.



The EAG takes in the byte (the 2nd or 3rd byte) in which the instruction operand is specified and, if a memory access is required, generates the control signal for the relevant register operation and calculates the effective address.

The EAG also initiates a bus cycle (memory read, etc.) as required.

3.2 MEMORY SPACE AND I/O SPACE

The μPD70236A provides a maximum 16M-byte memory space and a 64K-byte I/O space.

3.2.1 Memory Space

The μPD70236A has the 24 bits from A23 to A0 as address pins, and can use up to 16M bytes of memory space by means of the address space expansion function described later.

When the address space expansion function is not used, a 1M-byte memory space can be used by means of bits A19 to A0. In this case, the high-order 4 bits (A23 to A20) always output a low-level signal.

The address space expansion function is ignored in a DMA cycle, but since the DMAU contains a 24-bit length address register and a 16M-byte memory space can be used.

In a refresh cycle the refresh address is output using A15 to A0. In this case A23 to A16 output a low-level signal.

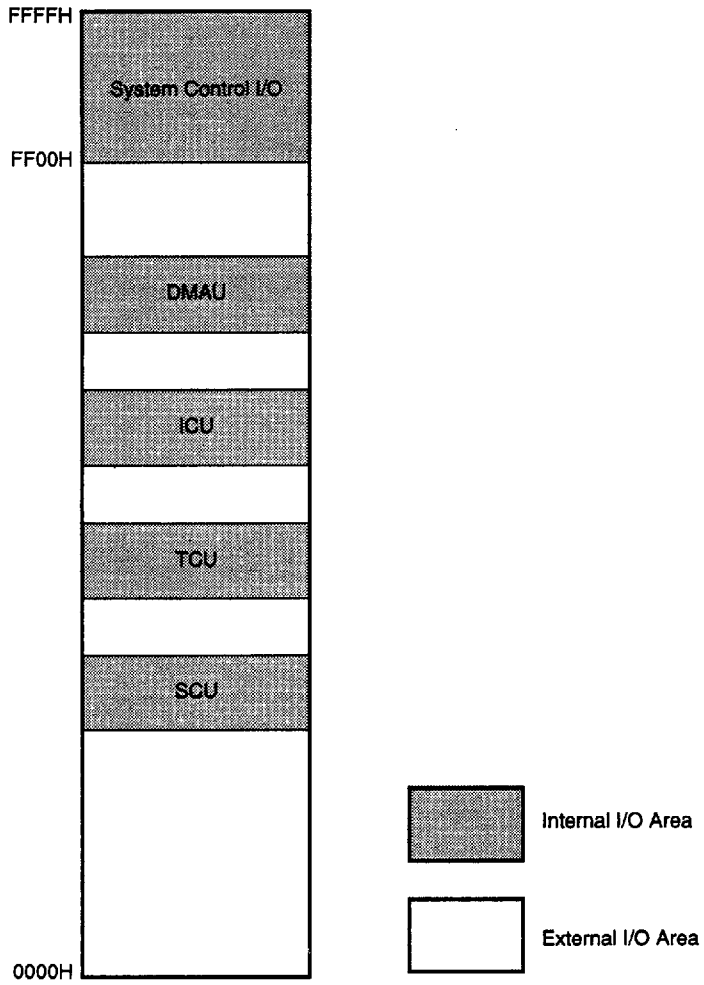
3.2.2 I/O Space

The μPD70236A supports a 64K-byte I/O space. Of this, the system I/O area (the high-order 256 bytes of the I/O space) are used as an internal I/O area, and cannot be mapped with external I/Os.

In an internal I/O access or external I/O access, the high-order 8 bits of the address (A23 to A16) always output a low-level signal.

Word type I/O accesses spanning the external I/O area and internal I/O area are prohibited.

Fig. 3-2 μPD70236A I/O Area



3.3 ADDRESS SPACE EXPANSION FUNCTION

3.3.1 Outline

The 20-bit address space is expanded to a 24-bit address space by EA (Effective Address) generation.

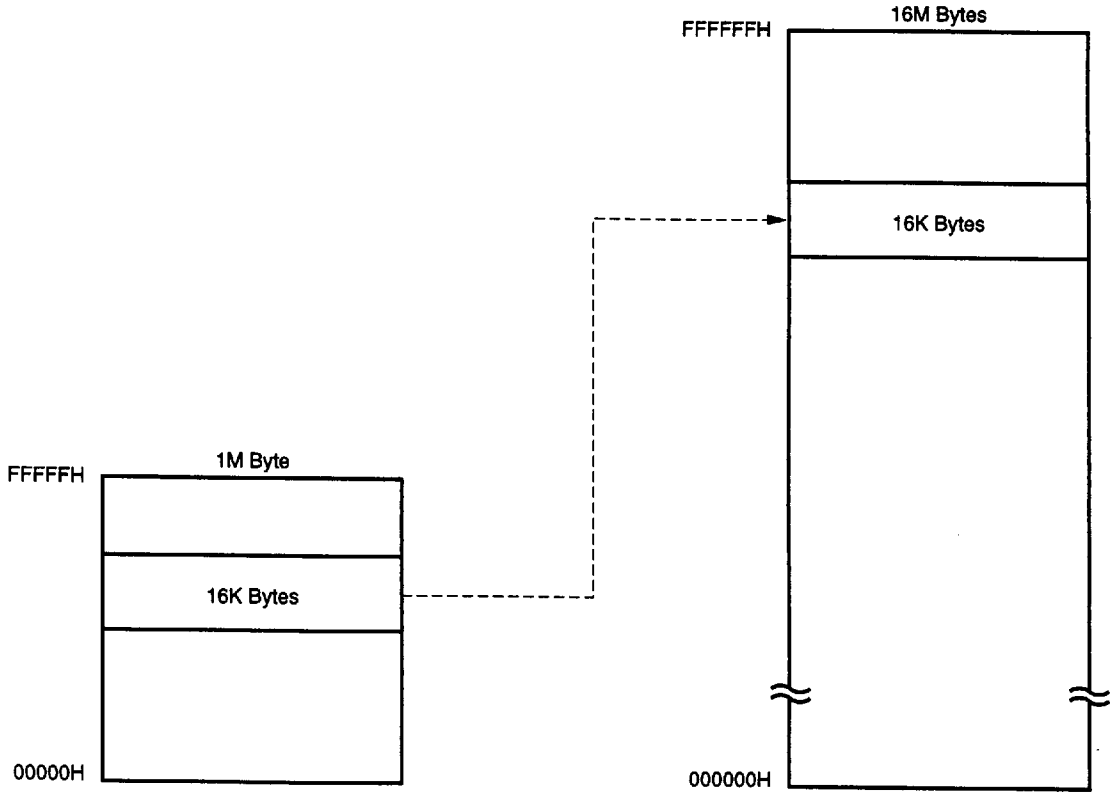
The expansion method used is address relocation.

The unit of relocation is a 16K-byte page, with expansion possible up to 16M bytes.

The expansion specification is performed by software.

When extended address mode has been set, the high-order 6 bits of a 20-bit address are extended to 10 bits by referencing a translation table, and a 24-bit extended address is generated.

When extended address mode is not set, the 20-bit physical address is output as it is, and the high-order 4 bits (A23 to A20) output a low-level signal.



3.3.2 Extended Address Mode Setting/Release

Setting and release of the extended address mode (XA mode) is performed by means of the following instructions:

BRKXA instruction
RETXA instruction

XA flag operations are as shown below.

Instruction	Operation	XA Mode
BRKXAn	Read vector n and branch. XA flag set to 1	Set
RETXAn	Read vector n and branch. XA flag reset to 0	Released

Remark The extended address mode and normal address mode are enabled from the branch destination address fetch cycle by means of BRKXA and RETXA instruction execution.

Whether or not the extended address mode is set can be ascertained by means of bit 0 (XA flag) of the XAM register (FF80H).

XAM (FF80H)

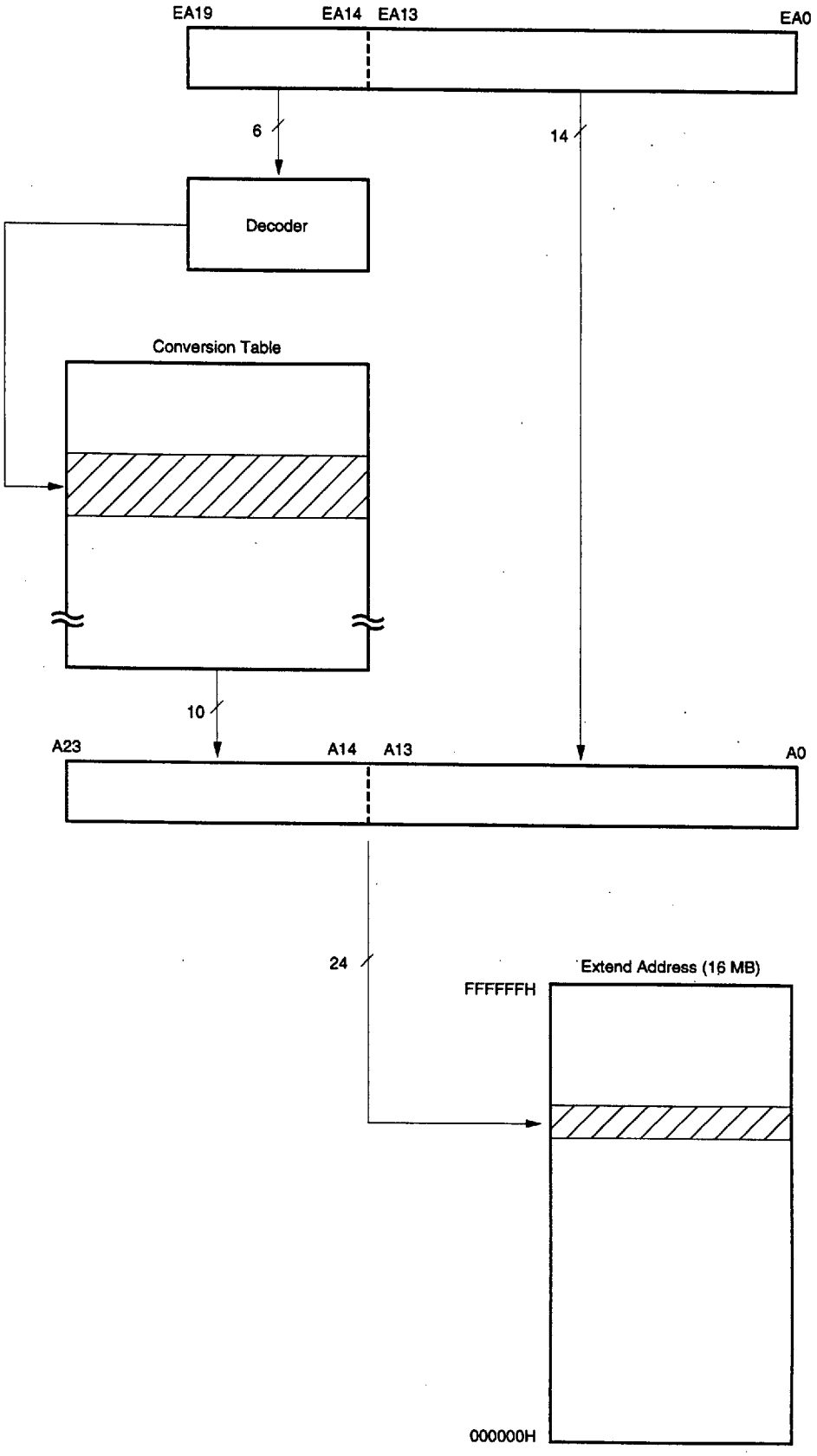
7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	XA

XA	Extended Address
0	Normal address mode (NA mode)
1	Extended address mode (XA mode)

Remark — : Undefined

The XA flag can be read only by the byte IN instruction. It is reset to 0 by reset input. It is set to 0 by reset input. A page register should not be accessed in extended address mode.

3.3.3 Address Conversion Method



3.3.4 Address Conversion Table

The high-order 6 bits of a 20-bit address generated by the address generator are input, one of 64 page registers (PGRs) is selected, and the low-order 10 bits of its contents are used as the high-order 10 bits of the extended address.

Page registers (PGRs) are allocated to addresses FF00H through FF7EH of the I/O space, and can be read/written to by a word IN/OUT instruction.

(1) Address conversion

A19	A18	A17	A16	A15	A14	Page Register to be selected	A19	A18	A17	A16	A15	A14	Page Register to be selected
0	0	0	0	0	0	PGR1	1	0	0	0	0	0	PGR33
0	0	0	0	0	1	PGR2	1	0	0	0	0	1	PGR34
0	0	0	0	1	0	PGR3	1	0	0	0	1	0	PGR35
0	0	0	0	1	1	PGR4	1	0	0	0	1	1	PGR36
0	0	0	1	0	0	PGR5	1	0	0	1	0	0	PGR37
0	0	0	1	0	1	PGR6	1	0	0	1	0	1	PGR38
0	0	0	1	1	0	PGR7	1	0	0	1	1	0	PGR39
0	0	0	1	1	1	PGR8	1	0	0	1	1	1	PGR40
0	0	1	0	0	0	PGR9	1	0	1	0	0	0	PGR41
0	0	1	0	0	1	PGR10	1	0	1	0	0	1	PGR42
0	0	1	0	1	0	PGR11	1	0	1	0	1	0	PGR43
0	0	1	0	1	1	PGR12	1	0	1	0	1	1	PGR44
0	0	1	1	0	0	PGR13	1	0	1	1	0	0	PGR45
0	0	1	1	0	1	PGR14	1	0	1	1	0	1	PGR46
0	0	1	1	1	0	PGR15	1	0	1	1	1	0	PGR47
0	0	1	1	1	1	PGR16	1	0	1	1	1	1	PGR48
0	1	0	0	0	0	PGR17	1	1	0	0	0	0	PGR49
0	1	0	0	0	1	PGR18	1	1	0	0	0	1	PGR50
0	1	0	0	1	0	PGR19	1	1	0	0	1	0	PGR51
0	1	0	0	1	1	PGR20	1	1	0	0	1	1	PGR52
0	1	0	1	0	0	PGR21	1	1	0	1	0	0	PGR53
0	1	0	1	0	1	PGR22	1	1	0	1	0	1	PGR54
0	1	0	1	1	0	PGR23	1	1	0	1	1	0	PGR55
0	1	0	1	1	1	PGR24	1	1	0	1	1	1	PGR56
0	1	1	0	0	0	PGR25	1	1	1	0	0	0	PGR57
0	1	1	0	0	1	PGR26	1	1	1	0	0	1	PGR58
0	1	1	0	1	0	PGR27	1	1	1	0	1	0	PGR59
0	1	1	0	1	1	PGR28	1	1	1	0	1	1	PGR60
0	1	1	1	0	0	PGR29	1	1	1	1	0	0	PGR61
0	1	1	1	0	1	PGR30	1	1	1	1	0	1	PGR62
0	1	1	1	1	0	PGR31	1	1	1	1	1	0	PGR63
0	1	1	1	1	1	PGR32	1	1	1	1	1	1	PGR64

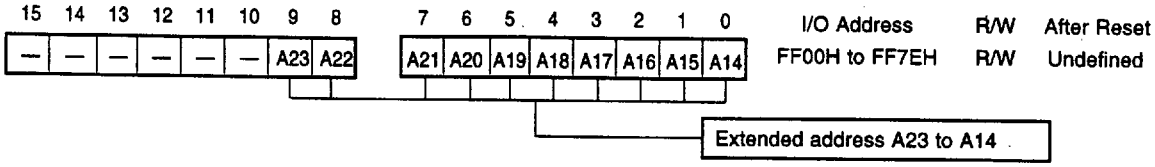
(2) Page registers (PGR1 to PGR64)

Page registers are accessed by the word IN and word OUT instructions.

Only the low-order 10 bits of a page register are valid (D9 to D0). The remaining high-order bits (D15 to D10) are read as 0 in a read, and ignored in a write. Reset input has no effect.

Page registers must not be accessed when extended address mode is set (XA = 1).

Page Register (PGR1 to PGR64)



I/O Address	Page Register	I/O Address	Page Register	I/O Address	Page Register
FF00	PGR1	FF2C	PGR23	FF58	PGR45
FF02	PGR2	FF2E	PGR24	FF5A	PGR46
FF04	PGR3	FF30	PGR25	FF5C	PGR47
FF06	PGR4	FF32	PGR26	FF5E	PGR48
FF08	PGR5	FF34	PGR27	FF60	PGR49
FF0A	PGR6	FF36	PGR28	FF62	PGR50
FF0C	PGR7	FF38	PGR29	FF64	PGR51
FF0E	PGR8	FF3A	PGR30	FF66	PGR52
FF10	PGR9	FF3C	PGR31	FF68	PGR53
FF12	PGR10	FF3E	PGR32	FF6A	PGR54
FF14	PGR11	FF40	PGR33	FF6C	PGR55
FF16	PGR12	FF42	PGR34	FF6E	PGR56
FF18	PGR13	FF44	PGR35	FF70	PGR57
FF1A	PGR14	FF46	PGR36	FF72	PGR58
FF1C	PGR15	FF48	PGR37	FF74	PGR59
FF1E	PGR16	FF4A	PGR38	FF76	PGR60
FF20	PGR17	FF4C	PGR39	FF78	PGR61
FF22	PGR18	FF4E	PGR40	FF7A	PGR62
FF 24	PGR19	FF50	PGR41	FF7C	PGR63
FF26	PGR20	FF52	PGR42	FF7E	PGR64
FF28	PGR21	FF54	PGR43		
FF2A	PGR22	FF56	PGR44		

Caution When accessing the page registers (PGR1 to PGR64), always make a word access to an even address.

3.4 DYNAMIC BUS SIZING FUNCTION

The data bus of the μPD70236A is 16 bits wide, but a dynamic bus sizing function is provided to enable connection to a system with an 8-bit data bus.

The bus sizing function is valid for both memory accesses and I/O accesses (external I/O only); when $\overline{BS8}$/BS16 is driven low, only the low-order 8 bits of the data bus are valid.

When a word access is made to an even-numbered address, after a normal 1st bus cycle a 2nd bus cycle is initiated and a read/write of the high-order 8-bit data is performed using D7 to D0.

Table 3-1 Data Accesses

$\overline{UBE}$	A0	Operation
0	0	16-bit access
0	1	Upper 8-bit access
1	0	Lower 8-bit access
1	1	2nd cycle with bus sizing

Table 3-2 Write Operation

Byte/Word	Address	A0	$\overline{UBE}$	Cycle	Non-Sizing ($\overline{BS8}$/BS16 = 1)		Sizing ($\overline{BS8}$/BS16 = 0)	
					D15 to D8	D7 to D0	D15 to D8	D7 to D0
Byte	Even	0	1	1st	Undefined	Lower byte	Undefined	Lower byte
	Odd	1	0	1st	Lower byte	Lower byte	Lower byte	Lower byte
Word	Even	0	0	1st	Upper byte	Lower byte	Upper byte	Lower byte
		1	1	2nd	No cycle	No cycle	Upper byte	Upper byte
	Odd	1	0	1st	Lower byte	Lower byte	Lower byte	Lower byte
		0	1	2nd	Lower byte	Upper byte	Lower byte	Upper byte

Table 3-3 Read Operation

Byte/Word	Address	A0	$\overline{UBE}$	Cycle	Non-Sizing ($\overline{BS8}$/BS16 = 1)		Sizing ($\overline{BS8}$/BS16 = 0)	
					D15 to D8	D7 to D0	D15 to D8	D7 to D0
Byte	Even	0	1	1st	—	Lower byte	—	Lower byte
	Odd	1	0	1st	Lower byte	—	—	Lower byte
Word	Even	0	0	1st	Upper byte	Lower byte	—	Lower byte
		1	1	2nd	No cycle	No cycle	—	Upper byte
	Odd	1	0	1st	Lower byte	—	—	Lower byte
		0	1	2nd	—	Upper byte	—	Upper byte

Table 3-4 Presence/absence of Bus Sizing and Sampling in Each Bus Cycle

Bus Cycle	Pins D0 to D15 Enabled Bus Size	Pins $\overline{BS8}$/BS16 Sampling
Interrupt acknowledge cycle (slave)	8 bits	No
Interrupt acknowledge cycle (ICU)	8 bits	No
External I/O read cycle	8/16 bits	Yes
Internal I/O read cycle	8/16 bits	No
External I/O write cycle	8/16 bits	Yes
Internal I/O write cycle	8/16 bits	No
Coprocessor read cycle	16 bits	No
Coprocessor write cycle	16 bits	No
Halt acknowledge cycle	Hi-Z (meaningless)	No
Instruction fetch cycle	8/16 bits	Yes
Refresh cycle	Hi-Z (meaningless)	No
CPU memory read cycle	8/16 bits	Yes
DMA read transfer cycle	Hi-Z (dependent on transfer I/O)	No
CPU memory write cycle	8/16 bits	Yes
DMA write transfer cycle	Hi-Z (dependent on transfer I/O)	No
Coprocessor memory read cycle	16 bits	Yes[Note]
Coprocessor memory write cycle	16 bits	Yes[Note]
DMA cascades	Hi-Z (meaningless)	No

Note Operation is not performed normally, when 8-bit bus size is specified.

3.5 INTERRUPT OPERATIONS

Broadly speaking, the μPD70236A uses two kinds of interrupts: Those resulting from an external interrupt request, and those resulting from software processing.

These can be further subdivided as shown below.

(1) External interrupts

(a) $\overline{\text{NMI}}$ input (non-maskable)

(b) ICU input (maskable)

(2) Software instructions

(a) Instruction processing result
- Divide error in DIV or DIVU instruction
- Memory boundary exceeded in CHKIND instruction
- Detection of undefined instruction
- Co-processor error
- Co-processor absent

(b) Conditional break instruction
- When V = 1 in BRKV instruction

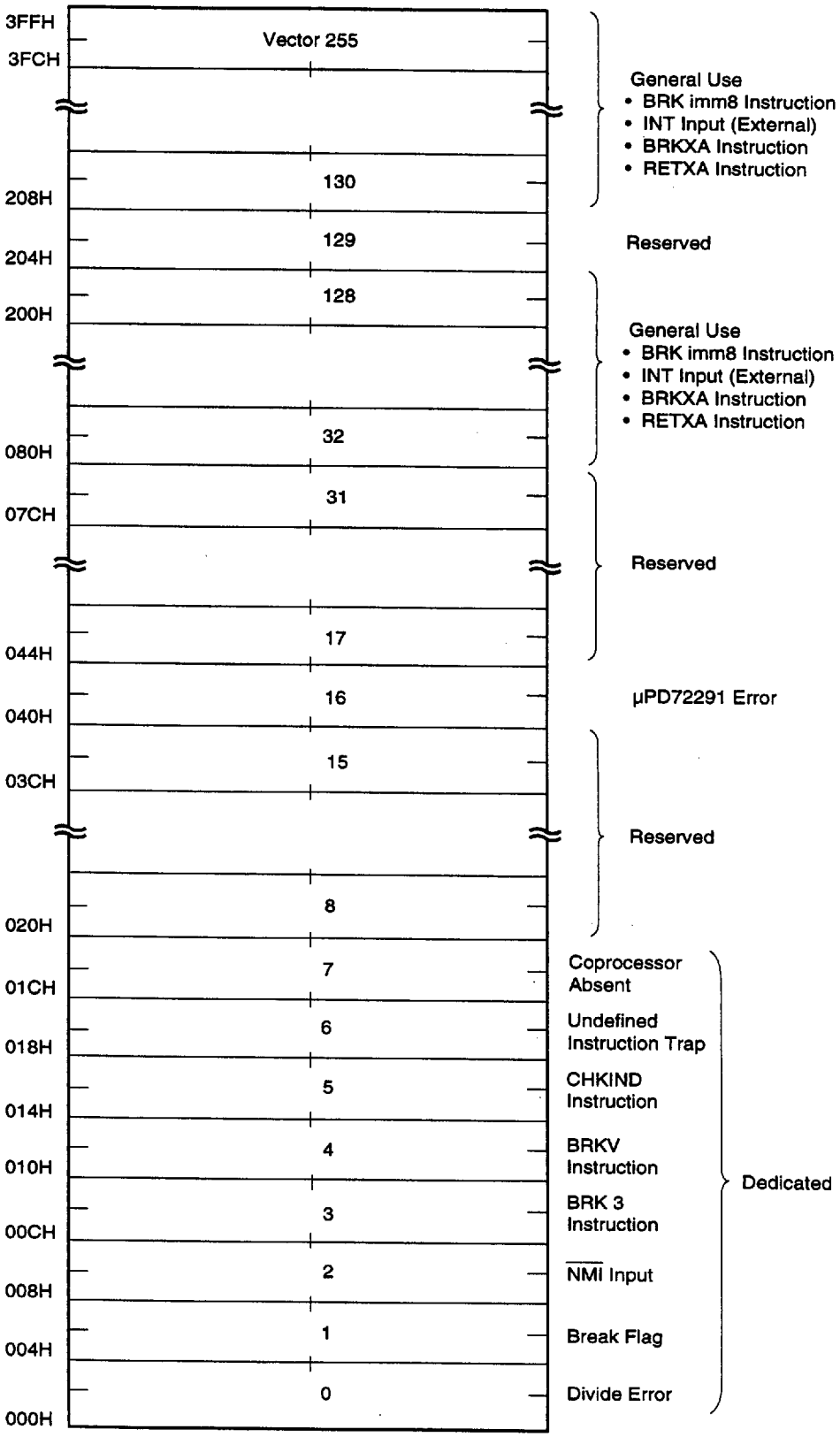
(c) Unconditional break instruction
- 1-byte break instruction BRK 3
- 2-byte break instruction BRK imm8

(d) Flag operation (single-step)
- BRK flag setting using stack manipulation

With any interrupt, a location in the previously provided interrupt vector table is selected automatically or according to the specification given on that occasion, and the start address of the interrupt routine is thus determined.

The interrupt vector table is shown in Fig. 3-3. This table is allocated to the 1024-byte memory area from 000H to 3FFH, and contains 256 vectors (using 4 bytes per vector).

Fig. 3-3 Interrupt Vector Table



Vectors 0 to 5 have specified uses, while vectors 6 to 31 are reserved and are not available for general use.

Vectors 32 to 255 are for general use, and can be used by a 2-byte break instruction and INT input.

Vectors 122 and 128 to130, however, have specified uses and are not available for general use.

Each vector consists of 4 bytes: The 2 bytes of the lower address are loaded into the PC as the offset, and the 2 bytes of the upper address are loaded into the PS register as the base.

Example Vector 0

003H	002H
001H	000H

PS← (003H, 002H)
PC← (001H, 000H)

The programmer initializes the contents of the vectors to be used at the start of the program based on this format. The basic steps involved in branching to an interrupt service routine are shown below.

TA← Lower vector (offset)
TC← Upper vector (segment base)
SP← SP – 2, (SP + 1, SP)← PSW
IE← 0, BRK← 0
SP← SP – 2, (SP + 1, SP)← PS
PS← TC
SP← SP – 2, (SP + 1, SP)← PC
PC← TA

Cautions

1. **With an interrupt generated by the following sources, the PC and PS values that indicate the start address of the instruction at which the interruput was applid are saved to the stack.**
   - **Non-defined operation code trap**
   - **Coprocessor absence interrupt**
   - **μPD72291 error interrupt**

   For interrupts which are generated from the sources other than above, the PC and PS values indicating the instruction next to the interrupted instruction are saved to the stack.
2. **In the NMI service routine, no other NMI interrupt is acknowledged until the RETI instruction is executed. However, in the NMI service routine, an NMI interrupt is acknowledged if the HALT instruction is executed and the standby mode is set. In this case, the standby mode is released and an NMI interrupt (vector 2) is generated.**

4. SYSTEM CONTROL I/O

The system control I/Os which control the entire μPD70236A are described below.
In the μPD70236A, addresses FF00H to FFFFH are reserved as the internal I/O area, onto which system control I/Os are mapped. When using the μPD70236A these I/Os must first be correctly initialized.

4.1 SYSTEM I/O AREA

The system I/O area occupies the most significant 256 bytes (FF00H to FFFFH) of the 64K-byte I/O space (0000H toFFFFH). The system I/O area has mapped onto it various registers required for μPD70236A initialization, and system control I/Os in the REFU and WCU.

The registers mapped onto the system I/O area and their major functions are outlined below.

(1) SCTL (System control register)
- 8-bit boundary/16-bit boundary switching for on- chip peripheral relocation addresses
- Switching of the on-chip DMAU between μPD71071 mode and μPD71037 mode
- Control of carry propagation from A15 to A16 in μPD71037 mode
- Control of carry propagation from A19 to A20 in μPD71037 mode
- SCU clock baud rate generator/TOUT switching

(2) OPSEL (On-chip peripheral selection register)
- On-chip I/O available/unavailable setting

(3) On-chip peripheral relocation registers (OPHA, DULA, IULA, TULA, SULA)
- On-chip I/O relocation address setting

(4) WMB0 (Programmable wait memory area setting register 0)
- 3-way partitioning of 16M-byte memory space on which automatic wait insertion is performed

(5) WMB1 (Programmable wait memory area setting register1)
- 3-way partitioning of 1M-byte memory space on which automatic wait insertion is performed

(6) WCY0 (Programmable wait cycles setting register 0)
- Setting of the number of automatically inserted waits in a 16M-byte upper memory space access

(7) WCY1 (Programmable wait cycles setting register 1)
- Setting of the number of automatically inserted waits in a 16M-byte middle or lower memory space access

(8) WCY2 (Programmable wait cycles setting register 2)
- Setting of the number of automatically inserted waits in a 1M-byte middle or lower memory space access

(9) WCY3 (Programmable wait cycles setting register 3)
- Setting of the number of automatically inserted waits in an external I/O cycle
- Setting of the number of automatically inserted waits in a 1M-byte upper memory space access

(10) WCY4 (Programmable wait cycles setting register 4)
- Setting of the number of automatically inserted waits in a DMA cycle
- Setting of the number of automatically inserted waits in a refresh cycle

(11) WAC (Programmable wait memory address control register)

- Setting of A23 to A20 of 1M-byte memory space on which automatic wait insertion is performed

For details of WMB0, WMB1, WCY0 to WCY4, and WAC, refer to 5 **"WCU (WAIT CONTROL UNIT)"**.

(12) RFC (Refresh control register)

- Refresh cycle usable/not usable setting
- Refresh bus width setting
- Refresh interval setting

For details of RFC, refer to **6 "REFU (REFRESH CONTROL UNIT)"**.

(13) SBCR (Standby control register)

- Selection of HALT mode/STOP mode by HALT instruction execution
- Setting of oscillation stabilization time in case of STOP mode release
- Internal clock frequency division setting

For details of SBCR, refer to **13 "STANDBY FUNCTIONS"**.

(14) TCKS (Timer clock selection register)

- Internal clock/TCLK selection for TCU clock
- TCU clock internal clock frequency division setting

(15) BADR (Bank address register)

- Sets bank register lower address A7 to A2 or A7 toA3 and A0.

(16) BSEL (Bank selection register)

- Sets the bank register selection channel.

For details of BADR and BSEL, refer to **10 "DMAU (DMA CONTROL UNIT)"**.

(17) BRC (Baud rate counter)

- SCU baud rate counter

(18) PGR1 to PGR64 (Page registers 1 to 64)

- 64-entry table for address extension

(19) XAM (Address extension mode register)

- Address extension flag

For details of PGR1 to PGR64 and XAM, refer to **3 "CPU"**.

Table 4-1 System I/O Area

I/O Address	Register Name	Operation
FFFFH	Reserved	—
FFFEH	SCTL	Read/write
FFFDH	OPSEL	Read/write
FFFCH	OPHA	Read/write
FFFBH	DULA	Read/write
FFFAH	IULA	Read/write
FFF9H	TULA	Read/write
FFF8H	SULA	Read/write
FFF7H	Reserved	—
FFF6H	WCY4	Read/write
FFF5H	WCY3	Read/write
FFF4H	WCY2	Read/write
FFF3H	WMB1	Read/write
FFF2H	REFC	Read/write
FFF1H	SBCR	Read/write
FFF0H	TCKS	Read/write
FFEFH to FFEEH	Reserved	—
FFEDH	WAC	Read/write
FFECH	WCY0	Read/write
FFEBH	WCY1	Read/write
FFEAH	WMB0	Read/write
FFE9H	BRC	Read/write
FFE8H	Reserved	—
FFE7H to FFE2H	Reserved	—
FFE1H	BADR	Read/write
FFE0H	BSEL	Read/write
FFDFH to FF81H	Reserved	—
FF80H	XAM	Read
FF7FH to FF00H	PGR64 to PGR1	Read/write

Caution **Make an access to this system I/O area as well as μPD70236A internal I/O using the IN/OUT instruction which is basically of the byte type. Word access is possible only for the registers in DMAU in the μPD71071 mode.**

4.2 SCTL (SYSTEM CONTROL REGISTER)

The SCTL register controls on-chip peripherals; its functions are described below.

(1) 8-bit boundary/16-bit boundary switching for on-chip peripheral relocation addresses ... IOAG

The μPD70236A has four I/Os as on-chip peripherals:

The DMAU, ICU, TCU and SCU, and the I/O addresses of these peripherals are set by means of the relocation register. At this time, it is determined whether the LSB A0 is fixed and location is on a 16-bit boundary, or whether the LSB is not fixed and location is on an 8-bit boundary.

(2) Switching of the on-chip DMAU between μPD71071 mode and μPD71037 mode ... DMAM

The DMAU has two modes, the μPD71071 mode and the μPD71037 mode, and this bit determines the mode in which the DMAU is used. This bit must be set without fail before the DMAU is used.

(3) Control of carry propagation from A15 to A16 in μPD71037 mode ... CE0

When the DMAU is used in the μPD71037 mode, this bit determines whether or not a carry is propagated from A15 to A16 of the DMA address.

(4) Control of carry propagation from A19 to A20 in μPD71037 mode .. CE1

When the DMAU is used in the μPD71037 mode, this bit determines whether or not a carry is propagated from A19 to A20 of the DMA address.

(5) SCU clock baud rate generator/TOUT1 switching ... SC

This bit determines whether the dedicated baud rate generator or the TOUT1 output of the TCU is used as the SCU send/receive clock.

Fig. 4-1 SCTL (System Control Register)

I/O Address FFFEH — SCTL

7	6	5	4	3	2	1	0
—	—	—	SC	CE1	CE0	DMAM	IOAG

IOAG	Function
0	Fixes on-chip I/O addresses as odd/even (16-bit boundary)
1	Makes on-chip I/O addresses consecutive (8-bit boundary)

DMAM	Function
0	Sets DMAU to μPD71071 mode
1	Sets DMAU to μPD71037 mode

CE0	Function
0	Carry not propagated to A16 in μPD71037 mode
1	Carry propagated to A16 in μPD71037 mode

CE1	Function
0	Carry not propagated to A20 in μPD71037 mode
1	Carry propagated to A20 in μPD71037 mode

SC	SCU Input Clock Specification
0	TOUT1 used for SCU input clock
1	Baud rate generator used for SCU input clock

4.3 OPSEL (ON-CHIP PERIPHERAL SELECTION REGISTER)

OPSEL has the following functions:

- On-chip DMAU available/unavailable setting
- On-chip ICU available/unavailable setting
- On-chip TCU available/unavailable setting
- On-chip SCU available/unavailable setting

The unavailable status means that programming is not possible for the relevant I/O area. In other words, before performing programming involving a peripheral, it must be set to the available status by using this register.

Fig. 4-2 OPSEL (On-Chip Peripheral Selection Register)

I/O Address FFFDH — OPSEL

7	6	5	4	3	2	1	0
—	—	—	—	SS	TS	IS	DS

DS	On-Chip DMAU Use Setting
0	On-chip DMAU unavailable
1	On-chip DMAU available

IS	On-Chip ICU Use Setting
0	On-chip ICU unavailable
1	On-chip ICU available

TS	On-Chip TCU Use Setting
0	On-chip TCU unavailable
1	On-chip TCU available

SS	On-Chip SCU Use Setting
0	On-chip SCU unavailable
1	On-chip SCU available

Caution Before setting or reading OPSEL, set the on-chip peripheral relocation registers (OPHA, DULA, IULA, TULA and SULA).

4.4 ON-CHIP PERIPHERAL RELOCATION REGISTERS (OPHA, DULA, IULA, TULA, SULA)

There are five on-chip I/O relocation registers: OPHA, DULA, IULA, TULA, SULA, which set the I/O address for the DMAU, ICU, TCU and SCU on-chip peripherals.

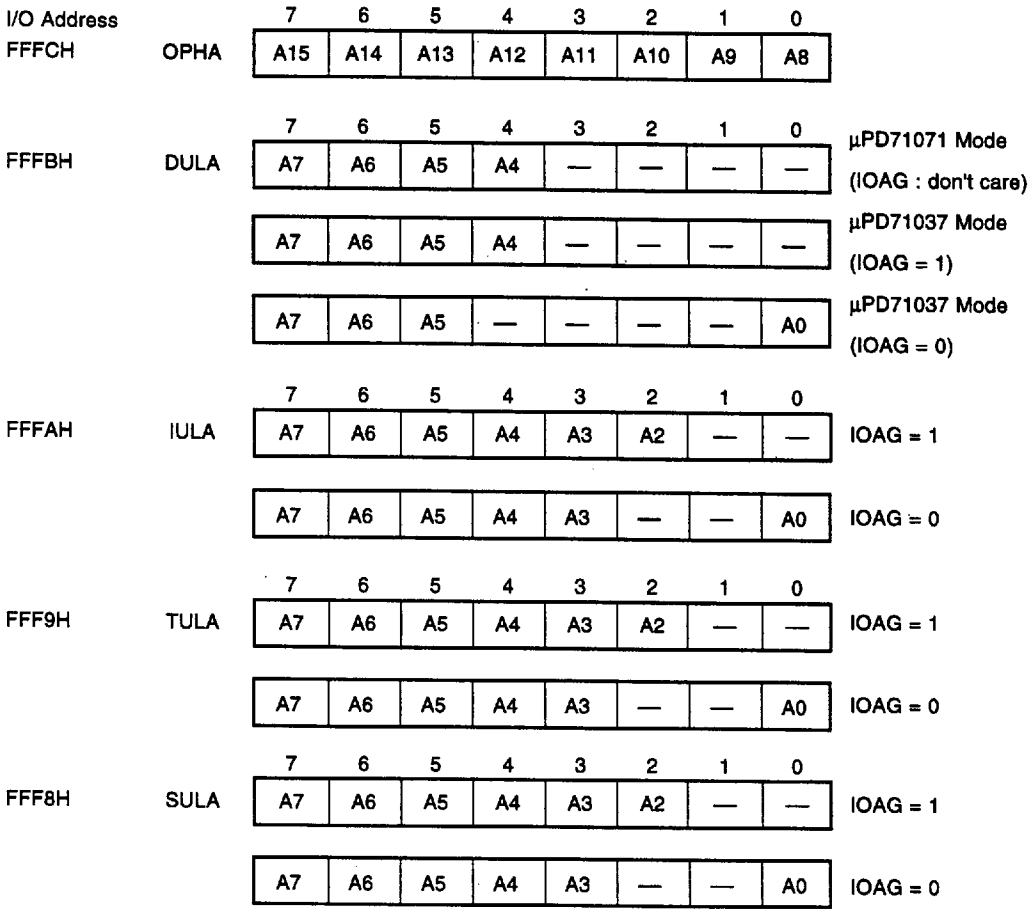
OPHA is common to these four peripherals, and sets the high-order 8 bits of each address. That is, these four peripherals are located in the I/O space within the 256 bytes set by the OPHA register. Next, the lower address of DULA, IULA, TULA or SULA specifies where in this 256- byte area the respective peripheral is located. The settable bits of the lower address vary depending on the value of the IOAG bit in the SCTL register described previously.

Fig. 4-3 shows the details of the on-chip peripheral relocation registers.

Cautions

1. **The DMAU occupies 16 bytes of the I/O area, and the ICU, TCU and SCU, 4 bytes each: Ensure that there is no mutual overlapping.**
2. **As mentioned earlier, accesses other than to the DMAU should be performed by means of a byte type IN/OUT instruction.**
3. **The on-chip peripheral I/O area and I/O space other than the system I/O area cannot be used as an external I/O area.**
4. **FFH should not be set in OPHA.**

Fig. 4-3 On-chip Peripheral Relocation Registers



4.5 TCKS (TIMER CLOCK SELECTION REGISTER)

The TCKS register specifies whether the clock supplied to the 3 counters (TCT#0 to TCT#2) in the TCU is input from the TCLK pin, or whether an internal clock is used (obtained by scaling the oscillator frequency of the crystal connected to the X1 and X2 pins).

Fig. 4-4 TCKS (Timer Clock Selection Register)

I/O Address FFF0H — TCKS

7	6	5	4	3	2	1	0
—	—	—	CS2	CS1	CS0	PS	

CS2	TCU Channel 2 Clock Selection
0	Internal clock used as TCU channel 2 clock
1	TCLK pin input used as TCU channel 2 clock

CS1	TCU Channel 1 Clock Selection
0	Internal clock used as TCU channel 1 clock
1	TCLK pin input used as TCU channel 1 clock

CS0	TCU Channel 0 Clock Selection
0	Internal clock used as TCU channel 0 clock
1	TCLK pin input used as TCU channel 0 clock

PS	Frequency Specification when Internal Clock is Used
0 0	Division ratio for oscillator frequency when internal clock is used = 1/4
0 1	Division ratio for oscillator frequency when internal clock is used = 1/8
1 0	Division ratio for oscillator frequency when internal clock is used = 1/16
1 1	Division ratio for oscillator frequency when internal clock is used = 1/32

4.6 BRC (BAUD RATE COUNTER)

The BRC is an SCU dedicated baud rate generator 8-bit dividing counter. It sets the frequency division ratio of the internal clock (fixed at 1/2 the oscillator frequency).

Fig. 4-5 BRC (Baud Rate Counter)

I/O Address FFE9H — BRC

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

The baud rate is calculated from the following expressions.

(1) When baud rate generator is used

$$\text{Baud rate} = \frac{\text{Oscillator frequency (Hz)}}{\text{BF x BRC set value}} \times \frac{1}{2}$$

Remark The relation between the BRC register and the BRC set value is as follows.

BRC Register	BRC Set Value
00H	2
01H	2
02H	2
03H	3
04H	4
:	:
FFH	255

(2) When TCU is used

$$\text{Baud rate} = \frac{\text{TCLK1 frequency (Hz)}}{\text{BF x TCT\#1 set value}}$$

Remark The BF (baud rate factor) is specified by the SMD register BF bit and takes the value of 16 or 64.

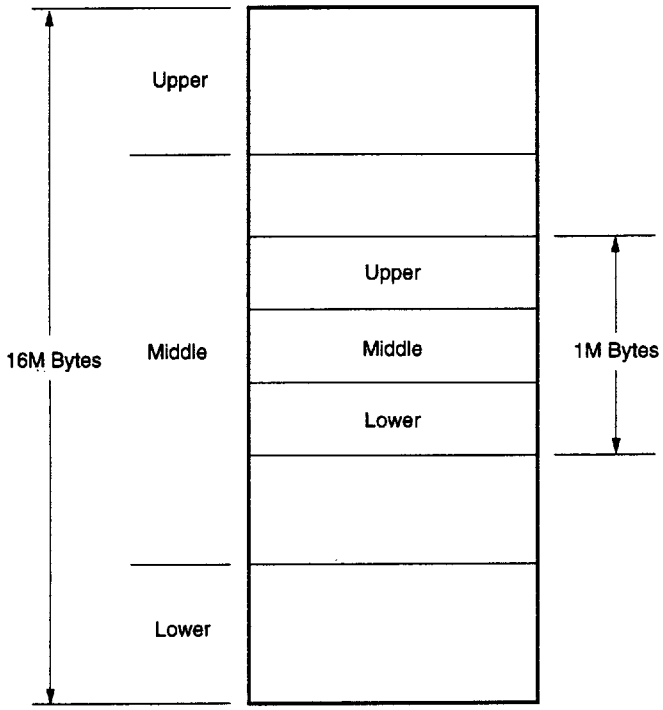
5. WCU (WAIT CONTROL UNIT)

The WCU has the function of automatically inserting a wait states(TW) equivalent to between 0 and 7 clock cycles in a CPU, DMAU or REFU bus cycle.

5.1 FEATURES

- Automatic setting of 0 to 7 waits in a CPU memory bus cycle
- 3-way partitioning capability for 16M-byte memory space
- 3-way partitioning capability for specific 1M-byte memory space
- Automatic setting of 0 to 7 waits in an external I/O cycle
- Automatic setting of 0 to 7 waits in an DMA cycle
- Automatic setting of 0 to 7 waits in a refresh cycle

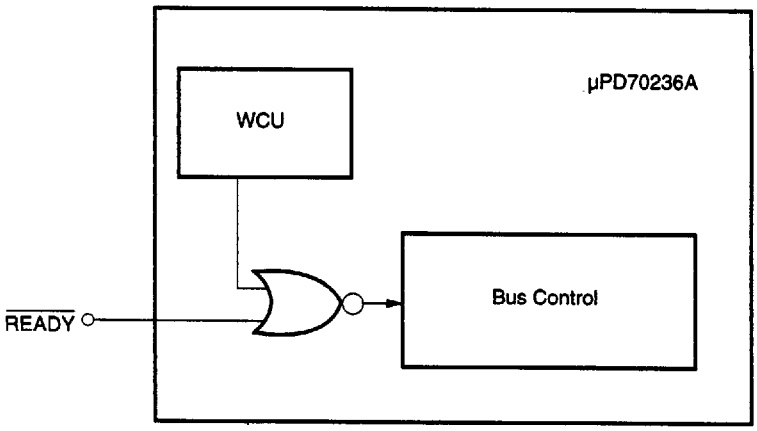
Fig. 5-1 Memory Space Partitioning



5.2 WCU AND $\overline{\text{READY}}$ PIN

If TW states of more than 0 to 7 clock cycles are required, the WCU can be used in conjunction with the $\overline{\text{READY}}$ signal. The TW conforming to the WCU set value and the TW resulting from $\overline{\text{READY}}$ control are inserted in logical sum form, so that the greater number of TWs are inserted.

Fig. 5-2 Relation between WCU and $\overline{\text{READY}}$ Pin



5.3 BUS CYCLES

$\overline{\text{READY}}$ pin sampling and programmable wait setting by WCU are shown for each bus cycle in the table below.

Bus Cycle	$\overline{\text{READY}}$ Pin Sampling	Programmable Wait Setting
External I/O read cycle	Enabled	Enabled[Note1]
External I/O write cycle	Enabled	
Interrupt acknowledge cycle (slave)	Enabled	
Interrupt acknowledge cycle (ICU)	Enabled	
Instruction fetch cycle	Enabled	Enabled (Area specifiable)
CPU memory read cycle	Enabled	
CPU memory write cycle	Enabled	
Coprocessor memory read cycle	Enabled	
Coprocessor memory write cycle	Enabled	
DMA read transfer cycle	Enabled	Enabled
DMA write transfer cycle	Enabled	
Refresh cycle	Enabled	Enabled
Internal I/O read cycle	—[Note 2]	Disabled
Internal I/O write cycle	—[Note 2]	Disabled
Coprocessor read cycle	Enabled	Disabled
Coprpcessor write cycle	Enabled	Disabled
Halt acknowledge cycle	—	Disabled
Cascade DMA cycle	—	Disabled

Notes
1. In case of the interrupt acknowledge cycle, 2 waits are set for 0-wait setting and 3 waits are set for 1-wait setting.
2. Accesses to registers PGR1 to PGR64 and XAM are carried out with 0 waits, however, in case of accesses to other registers, a 2-clock wait state is automatically inserted.

5.4 MEMORY/EXTERNAL I/O CYCLE

The memory space of the μPD70236A is 16M bytes; sometimes waits are not made necessary at the time of system configuration depending on the memory space, and inserting the same number of waits for the entire memory space is also related to decreased system performance. Consequently, provision has been made to enable the 16M- byte memory space to be divided into three, and for between 0 and 7 waits to be set for each area independently. In addition, any desired 1M-byte space within the 16M-byte space can be divided into three. The number of waits set here is valid for CPU instruction fetch cycles, operand access cycles, and external I/O access cycles.

Programmable wait control for memory/external I/O cycles is performed by the registers described below.

5.4.1 WMB0 (Programmable Wait Memory Area Setting Register 0)

WMB0 divides a 16M-byte memory space into 3 memory blocks:Lower, middle and upper. The lower block and upper block are set by the ELMB and EUMB fields, and the middle block is the area between these two.

Fig. 5-3 WMB0 Register

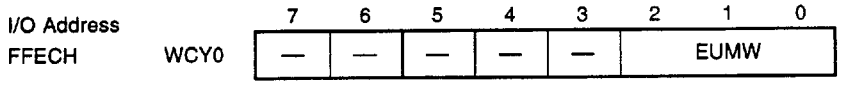
I/O Address		7	6	5	4	3	2	1	0
FFEAH	WMB0	—	ELMB			—	EUMB		

ELMB,EUMB	16M-Byte Memory Space Lower & Upper Memory Block Size
0 0 0	1M bytes
0 0 1	2M bytes
0 1 0	3M bytes
0 1 1	4M bytes
1 0 0	5M bytes
1 0 1	6M bytes
1 1 0	7M bytes
1 1 1	8M bytes

5.4.2 WCY0 (Programmable Wait Cycles Setting Register 0)

WCY0 sets the number of wait cycles, between 0 and 7, for the upper memory block of the 16M-byte space set by WMB0.

Fig. 5-4 WCY0 Register

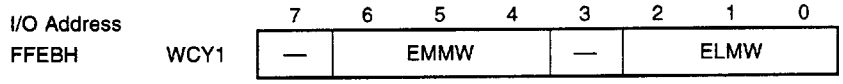


EUMW	Wait Insertion Specification for Access to Upper Memory Block in 16M-Byte Space
0 0 0	No waits automatically inserted
0 0 1	1 wait automatically inserted
0 1 0	2 waits automatically inserted
0 1 1	3 waits automatically inserted
1 0 0	4 waits automatically inserted
1 0 1	5 waits automatically inserted
1 1 0	6 waits automatically inserted
1 1 1	7 waits automatically inserted

5.4.3 WCY1 (Programmable Wait Cycles Setting Register 1)

WCY1 sets the number of wait cycles, between 0 and 7, for the middle and lower memory block of the 16M byte space set by WMB0.

Fig. 5-5 WCY1 Register



EMMW, ELMW	Wait Insertion Specification for Access to Middle & Lower Memory Block in 16M-Byte Space
0 0 0	No waits automatically inserted
0 0 1	1 wait automatically inserted
0 1 0	2 waits automatically inserted
0 1 1	3 waits automatically inserted
1 0 0	4 waits automatically inserted
1 0 1	5 waits automatically inserted
1 1 0	6 waits automatically inserted
1 1 1	7 waits automatically inserted

5.4.4 WMB1 (Programmable Wait Memory Area Setting Register 1)

WMB1 divides a 1M-byte memory space into 3 memory blocks: Lower, middle and upper. The lower block and upper block are set by the ELMB and EUMB fields, and the middle block is the area between these two.

Fig. 5-6 WMB1 Register

I/O Address FFF3H — WMB1

7	6	5	4	3	2	1	0
—	LMB			—	UMB		

LMB, UMB	1M-Byte Memory Space Lower & Upper Memory Block Size
0 0 0	32K bytes
0 0 1	64K bytes
0 1 0	96K bytes
0 1 1	128K bytes
1 0 0	192K bytes
1 0 1	256K bytes
1 1 0	384K bytes
1 1 1	512K bytes

5.4.5 WAC (Programmable Wait Memory Address Control Register)

WAC sets the high-order 4-bit address of the 16M-byte memory space, and determines the 1M-byte memory space set by WMB1.

Fig. 5-7 WAC Register

I/O Address FFEDH — WAC

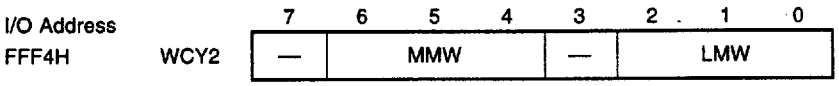
7	6	5	4	3	2	1	0
—	—	—	—	UWA			

UWA3 to UWA0 : High-order 4 bits which specify the 1M-byte memory space for which automatic wait setting is possible.

5.4.6 WCY2 (Programmable Wait Cycles Setting Register 2)

WCY2 sets the number of wait cycles, between 0 and 7, for the middle and lower memory blocks of the 1M-byte space set by WMB1.

Fig. 5-8 WCY2 Register



MMW, LMW	Wait Insertion Specification for Access to Middle & Lower Memory Blocks in 1M-Byte Space
0 0 0	No waits automatically inserted
0 0 1	1 wait automatically inserted
0 1 0	2 waits automatically inserted
0 1 1	3 waits automatically inserted
1 0 0	4 waits automatically inserted
1 0 1	5 waits automatically inserted
1 1 0	6 waits automatically inserted
1 1 1	7 waits automatically inserted

5.4.7 WCY3 (Programmable Wait Cycles Setting Register 3)

WCY3 sets the number of wait cycles, between 0 and 7, for the upper memory block of the 1M-byte space set by WMB1, or an I/O bus cycle.

Caution This setting is ignored in an internal I/O area read/write cycle. It is valid in an interrupt acknowledge cycle.

Fig. 5-9 WCY3 Register

I/O Address FFF5H — WCY3

7	6	5	4	3	2	1	0
—	IOW			—	UMW		

IOW	Wait Insertion Specification for External I/O Cycle	Wait Insertion Specification for Interrupt Acknowledge Cycle
0 0 0	No waits automatically inserted	2 waits automatically inserted
0 0 1	1 wait automatically inserted	3 waits automatically inserted
0 1 0	2 waits automatically inserted	2 waits automatically inserted
0 1 1	3 waits automatically inserted	3 waits automatically inserted
1 0 0	4 waits automatically inserted	4 waits automatically inserted
1 0 1	5 waits automatically inserted	5 waits automatically inserted
1 1 0	6 waits automatically inserted	6 waits automatically inserted
1 1 1	7 waits automatically inserted	7 waits automatically inserted

UMW	Wait Insertion Specification for Access to Upper Memory Block in 1M-Byte Space
0 0 0	No waits automatically inserted
0 0 1	1 wait automatically inserted
0 1 0	2 waits automatically inserted
0 1 1	3 waits automatically inserted
1 0 0	4 waits automatically inserted
1 0 1	5 waits automatically inserted
1 1 0	6 waits automatically inserted
1 1 1	7 waits automatically inserted

5.5 DMA/REFRESH CYCLE

The number of waits for a DMA cycle or refresh cycle is set by the WCY4 register.

5.5.1 WCY4 (Programmable Wait Cycles Setting Register 4)

WCY4 sets the number of wait cycles, between 0 and 7, for a DMA cycle or refresh cycle. Memory space partitioning is invalid in a DMA cycle or refresh cycle.

Fig. 5-10 WCY4 Register

I/O Address		7	6	5	4	3	2	1	0
FFF6H	WCY4	—	DMAW			—	RFW		

DMAW	Wait Insertion Specification for DMA Cycle
0 0 0	No waits automatically inserted
0 0 1	1 wait automatically inserted
0 1 0	2 waits automatically inserted
0 1 1	3 waits automatically inserted
1 0 0	4 waits automatically inserted
1 0 1	5 waits automatically inserted
1 1 0	6 waits automatically inserted
1 1 1	7 waits automatically inserted

RFW	Wait Insertion Specification for Refresh Cycle
0 0 0	No waits automatically inserted
0 0 1	1 wait automatically inserted
0 1 0	2 waits automatically inserted
0 1 1	3 waits automatically inserted
1 0 0	4 waits automatically inserted
1 0 1	5 waits automatically inserted
1 1 0	6 waits automatically inserted
1 1 1	7 waits automatically inserted

6. REFU (REFRESH CONTROL UNIT)

The REFU generates refresh cycles required for external DRAM refresh operations. Refresh enabling/disabling and the refresh interval are set by the RFC register.

6.1 FEATURES

- Lowest-priority refreshing/highest-priority refreshing
- 7 refresh queues
- 16-bit refresh address
- 4 clocks/1 bus cycle

6.2 REFRESH ADDRESS

The address in A15 to A0 is output as the refresh address.Each refresh cycle the refresh address is incremented by 1 or 2, and the next refresh address is generated.

In a refresh cycle a low-level signal is output for the upper address (A23 to A16).

The refresh address is not affected by a reset. After powering on, the refresh address is undefined.

6.3 RFC (REFRESH CONTROL REGISTER)

The RFC register is mapped onto the system I/O area, and has the following functions:

(1) Refresh enabling/disabling

Refresh enabling/disabling is performed by the RFE bit. As the RFE bit is not initialized by a reset, refreshing may be enabled or disabled after powering on. Therefore, a refresh cycle may be initiated 144 (16 x 9) clock cycles after a power-on reset.

(2) Refresh interval

The refresh interval is set by the RTM bit. The optimum value for the refresh interval should be set for the individual system according to the following expression:

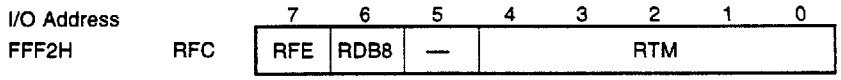
16 x Timer Factor (N) (Clock cycles)

The smallest set value for the refresh interval is N = 1, in a reset the value is initialized to N = 9.

(3) Address update control

Incrementing by 1 or by 2 of the refresh address is selected by the RDB8 bit.

Fig. 6-1 RFC (Refresh Control Register)



RFE	Refresh Enabling/Disabling
0	Refresh disabled
1	Refresh enabled

RDB8	Refresh Address Update Control
0	Refresh address incremented by 2 $\overline{UBE}$: Low-level output
1	Refresh address incremented by 1 $\overline{UBE}$: High for even address, low for odd address

RTM	Timer Factor Setting
0 0 0 0 0	N (Timer factor) = 1
0 0 0 0 1	N (Timer factor) = 2
0 0 0 1 0	N (Timer factor) = 3
0 0 0 1 1	N (Timer factor) = 4
0 0 1 0 0	N (Timer factor) = 5
0 0 1 0 1	N (Timer factor) = 6
:	:
1 1 1 1 0	N (Timer factor) = 31
1 1 1 1 1	N (Timer factor) = 32

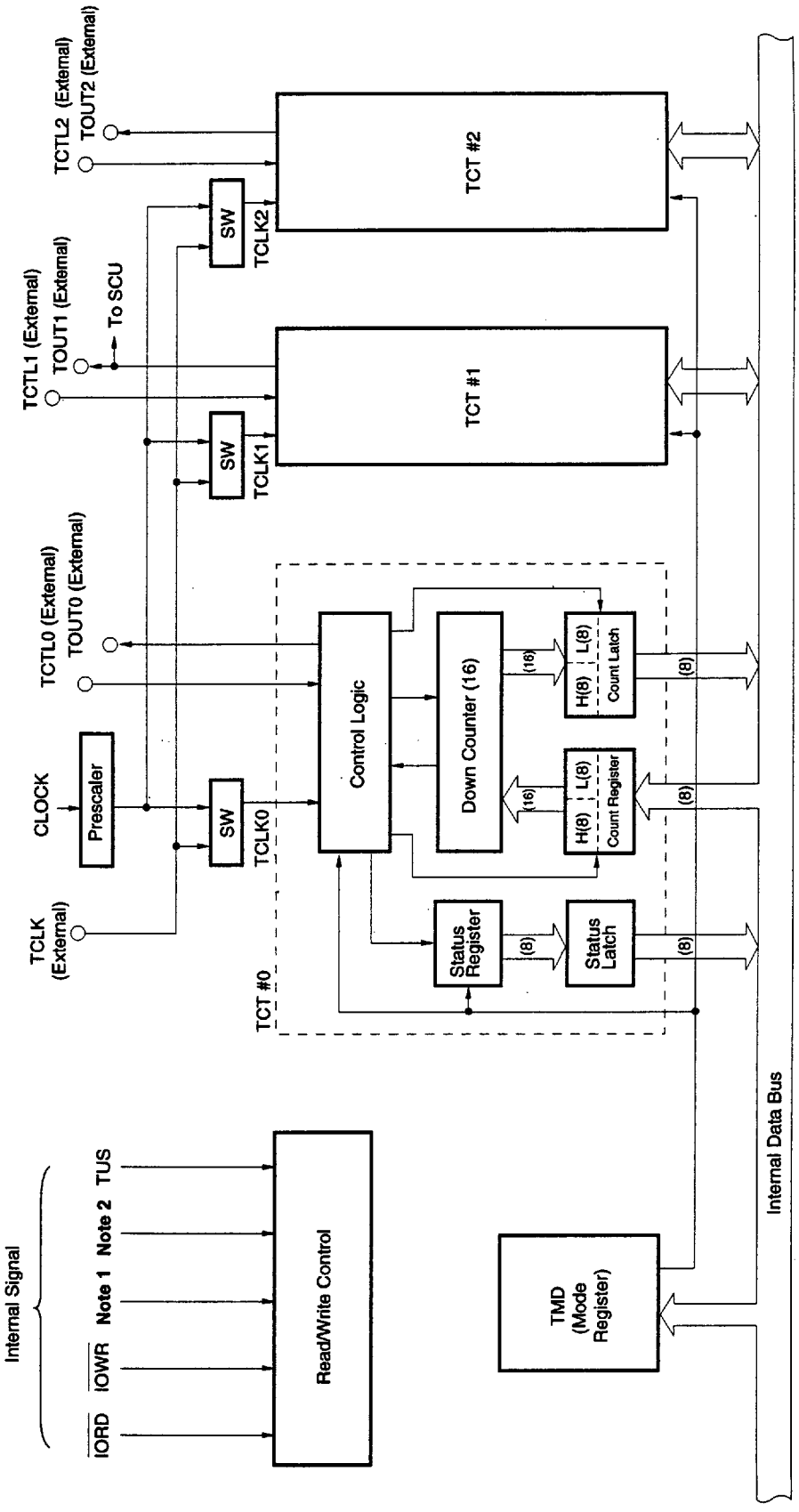
7. TCU (TIMER/COUNTER UNIT)

The TCU has 3 counters, and is functionally identical to the μPD71054.

7.1 FEATURES

- Three timer channels
- TOUT0 to TOUT2 pin outputs
- TCTL0 to TCTL2 pin inputs
- TCLK pin input
- TOUT1 usable as SCU clock
- Three 16-bit counters
- Six programmable count modes
- Binary/BCD count
- Multiple latch command
- Count latch command
- Internal/external input clock selectable
- 20 MHz operation capability (using μPD70236A-20)

7.2 TCU INTERNAL BLOCK DIAGRAM

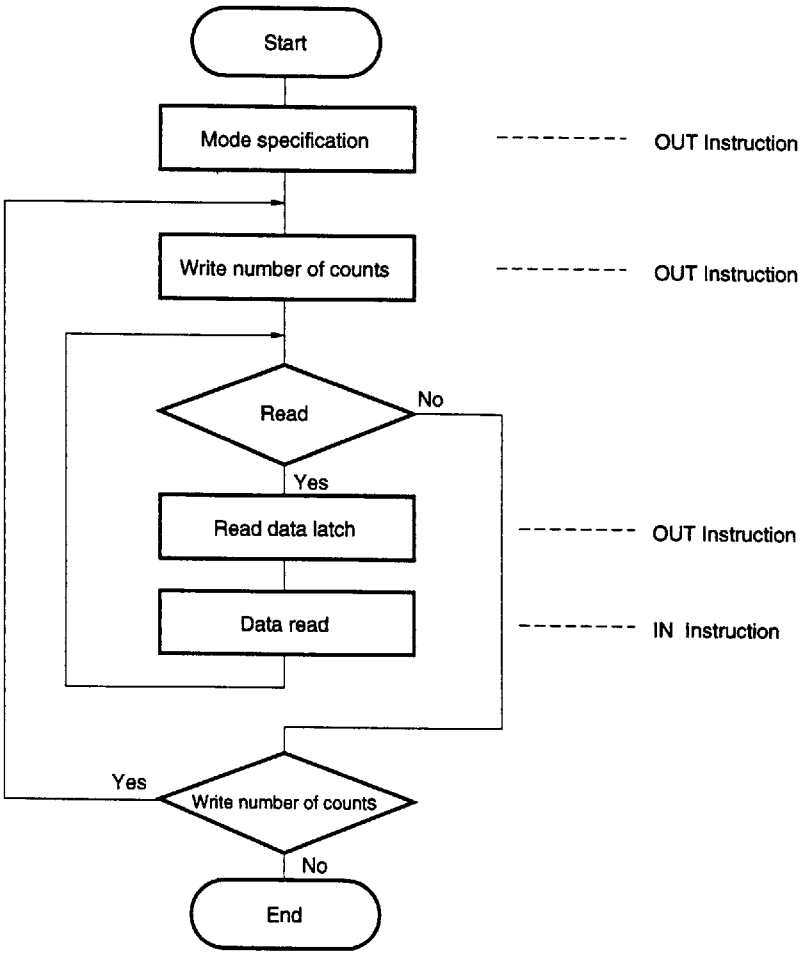


Notes 1. When IOAG of the SCTL register = 1, A0. When IOAG = 0, A1.
2. When IOAG of the SCTL register = 1, A1. When IOAG = 0, A2.

7.3 TCU OPERATING PROCEDURE

After powering on, the TCU is in an undefined state. When the TCU is used, therefore, the operating mode must be specified by programming the target counter. Once a counter has been programmed for a certain mode, operation continues in that mode until that counter has mode specification performed again. When the count value is written into the counter and this value is transferred to the down counter a new count is started. The current count data (counter value) and the status of the counter can be read during the count.

Fig. 7-1 Basic Operating Procedure



7.4 TCU REGISTERS AND COMMANDS

TCU register read/write command issuance is performed by I/O input/output instructions on an address set in the system I/O area, and the selection of registers etc., is performed by A1 and A0 (when IOAG of the SCTL register = 1) or A2 and A1 (when IOAG = 0).

Table 7-1 TCU Register/Command Addresses

A1/A2	A0/A1	Register/Command	Operation
0	0	TCT #0	Read/write
		TST 0	Read
0	1	TCT #1	Read/write
		TST 1	Read
1	0	TCT #2	Read/write
		TST 2	Read
1	1	TMD	write

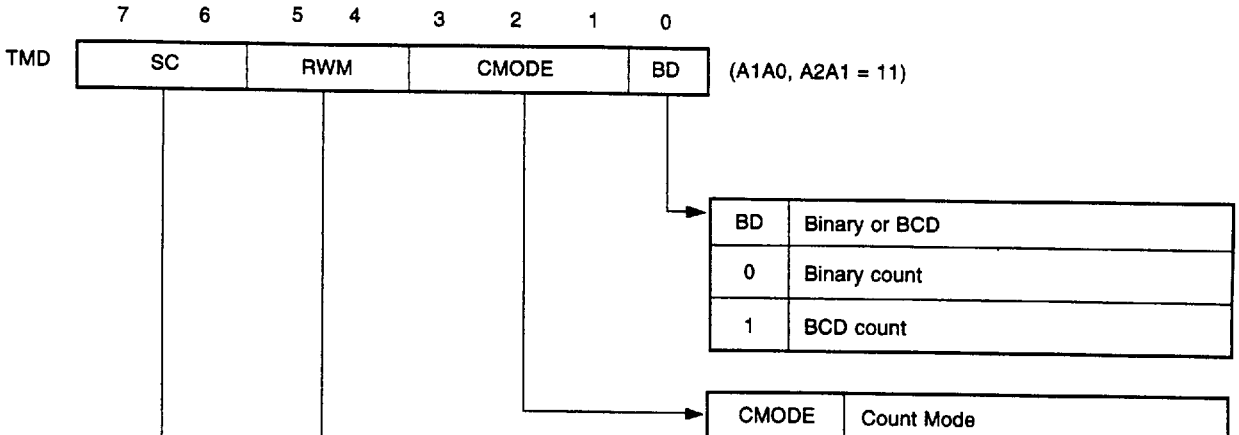
A write to the TMD is performed by setting the operating mode of individual counters in the TCU (count mode, binary/BCD, read/write mode) and issuing a command (count latch command, multiple latch command) to latch the counter value.

TCT#2 to TCT#0 are used to write the count value to and read the count data from individual counters. Normally, a count data read is performed after first latching the count data of the target counter by issuing a count latch command or a multiple latch command.

In a read of TST2 to TST0, the status information for the relevant counter is read. A status read is performed after first latching the status of the target counter with a multiple latch command.

When both the status and count data of a counter are latched, the first read obtains the status.

Fig. 7-2 Mode Word



BD	Binary or BCD
0	Binary count
1	BCD count

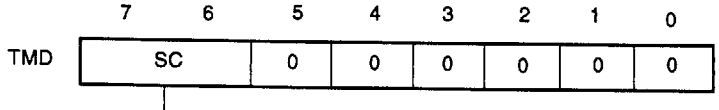
CMODE	Count Mode
000	Mode 0
001	Mode 1
x10	Mode 2
x11	Mode 3
100	Mode 4
101	Mode 5

RWM	Read/Write Mode
00	Count latch command
01	Lower byte
10	Upper byte
11	2 bytes in order: Lower, upper

SC	Counter Subject to Mode Setting
00	TCT #0
01	TCT #1
10	TCT #2
11	Multiple latch command

x : don't care

Fig. 7-3 Count Latch Command



SC	Counter Subject to Latch
00	TCT #0
01	TCT #1
10	TCT #2

Fig. 7-4 Multiple Latch Command

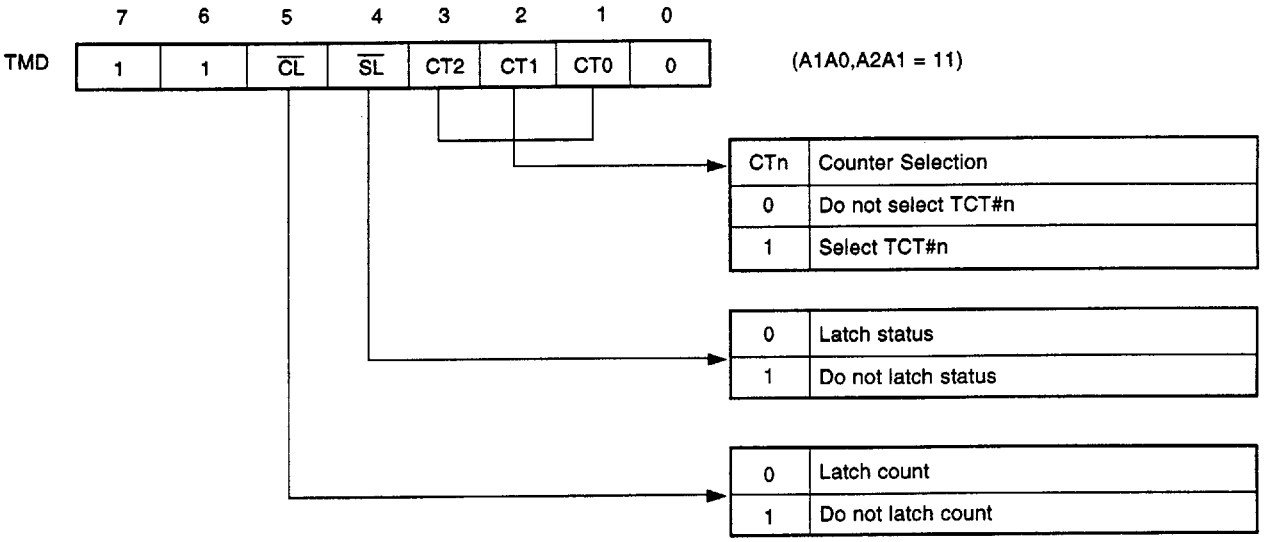
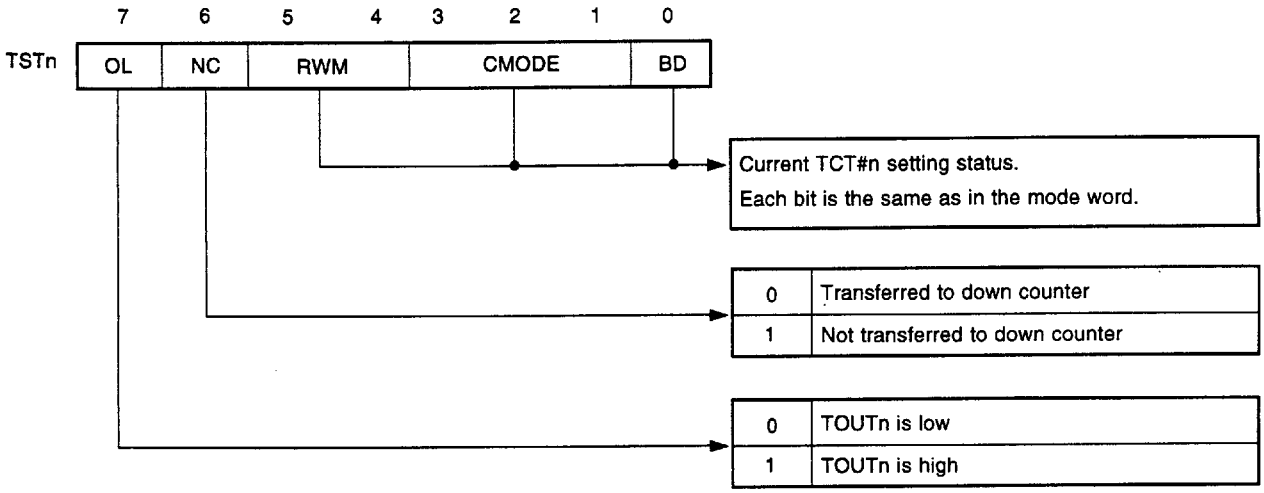


Fig. 7-5 Status



7.5 COUNT MODE

There are six count modes for each count.

(1) Mode 0: Output of end of count signal

When the specified count ends, the TOUT output changes from low to high.

(2) Mode 1: Control pin retriggerable one-shot

A low-level one-shot pulse of the specified length is output to TOUT. Can be retriggered by TCTL input.

(3) Mode 2: Rate generator

Dividing counter which periodically performs an operation whereby the TOUT output is driven low for the last clock cycle only of the specified count.

(4) Mode 3: Square wave generator

A similar scaling counter to that in mode 2, with a TOUT output low/high duty of approximately 50%.

(5) Mode 4: Software-triggered strobe

When the specified count ends, the TOUT output is driven low for one clock cycle only.

(6) Mode 5: Hardware-triggered strobe (retriggerable)

The same operation as mode 4, but started by TCTL input and retriggerable.

8. SCU (SERIAL CONTROL UNIT)

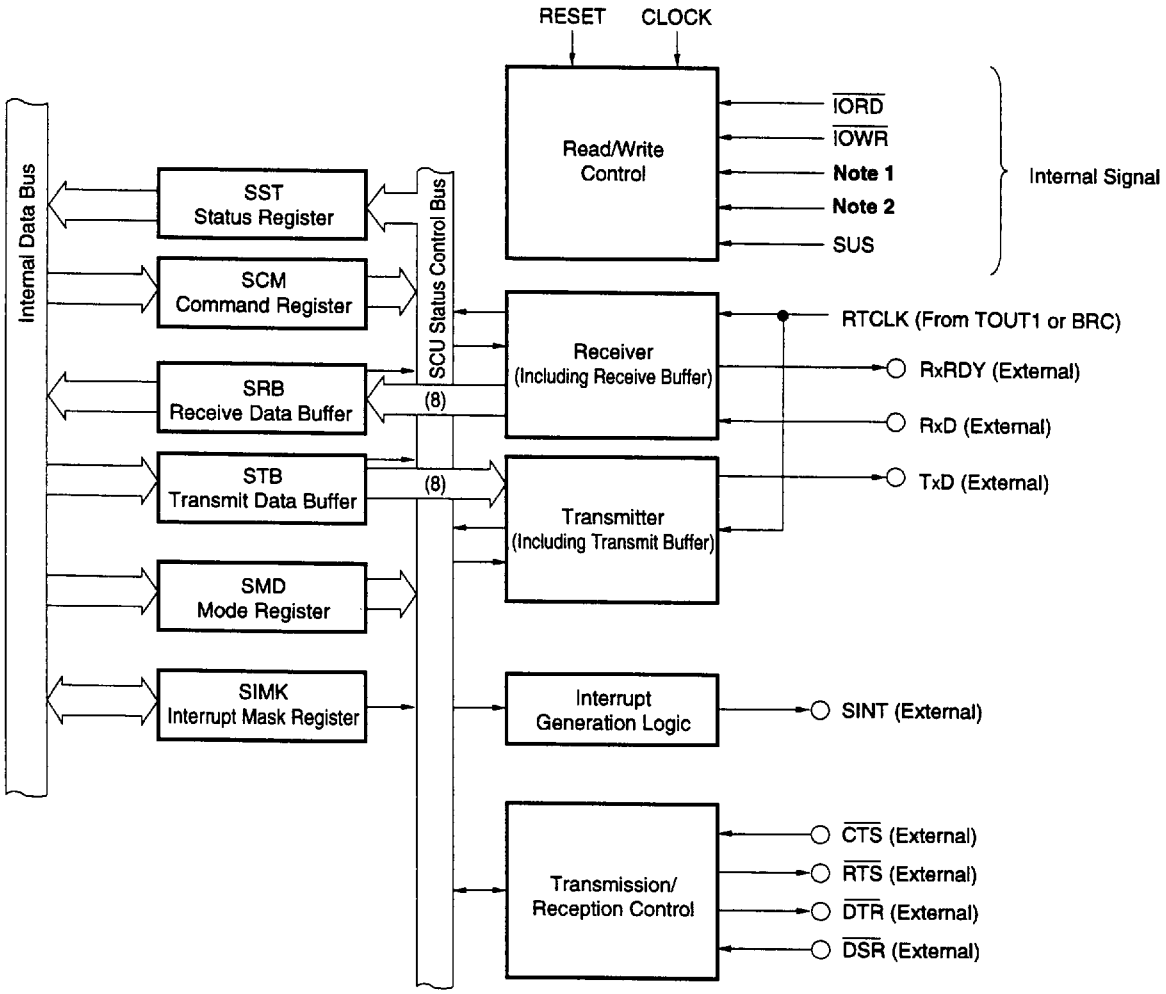
The SCU provides asynchronous serial communication functions.

The command system resembles that of the μPD71051, but what was the control word register in the μPD71051 has been divided into two: The SCM (serial command register) and SMD (serial mode register).

8.1 FEATURES

- RS-232-C protocol support (on-chip $\overline{RTS}$, $\overline{CTS}$, $\overline{DTR}$ and $\overline{DSR}$ pins)
- On-chip dedicated baud rate generator (using internal clock)
- Baud rate generator output or timer output selectable as transmit/receive clock
- Asynchronous only
- No input/output pin multiplexing
- Serial interrupt output (SINT)
- Clock rate: Baud rate x 16, baud rate x 64
- Baud rate: DC - 625 Kbps
- Character length: 7 or 8 bits
- Transmitted stop bits: 1 or 2 bits
- Break transmission
- Automatic break detection
- Full duplex double buffer system
- Parity addition/checking
- Error detection: Parity, overrun, framing

8.2 SCU INTERNAL BLOCK DIAGRAM

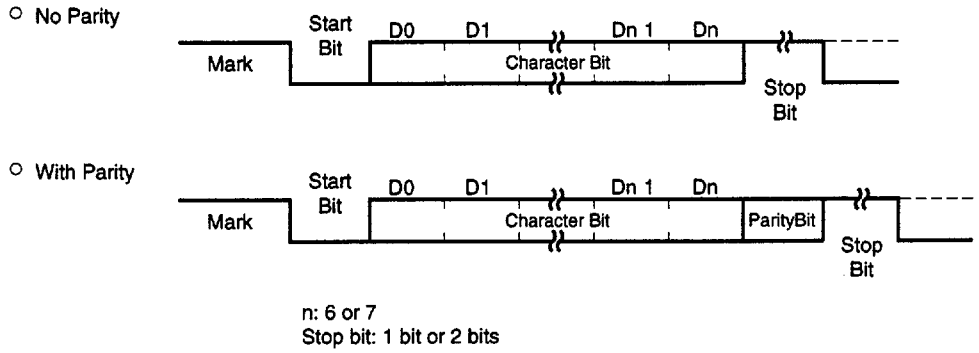


Notes 1. When IOAG of the SCTL register = 1, A0. When IOAG = 0, A1.
2. When IOAG of the SCTL register = 1, A1. When IOAG = 0, A2.

8.3 SERIAL DATA FORMAT

The serial data format handled by the SCU is shown in Fig. 8-1. The data which the CPU receives from the SCU and passes to the SCU comprises the character bit portion. The start bit, parity bit and stop bit(s) enclosing the character bits are control information required for serial communication, and are automatically added (in transmission) and deleted (in reception) by the SCU.

Fig. 8-1 Serial Data Format

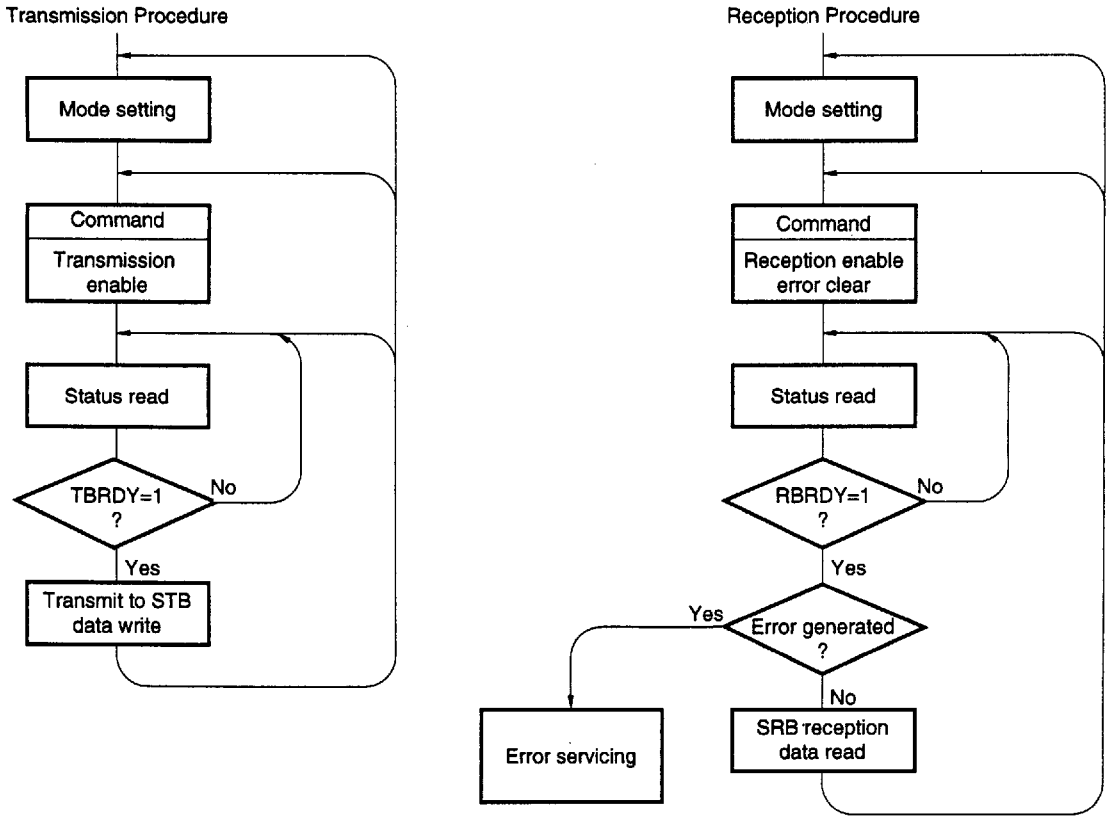


n: 6 or 7
Stop bit: 1 bit or 2 bits

8.4 SCU OPERATING PROCEDURE

The operating procedure for serial communication by the SCU is shown in Fig. 8-2.

Fig. 8-2 SCU Operating Procedure



For transmission, transmission is enabled, the status register is checked to confirm that the STB (transmit data buffer) is empty, then transmit data is written into the STB.

For reception, reception is enabled and at the same time the error flag in the status register is cleared. Then the status register is checked to confirm that there is receive data in the SRB (receive buffer), and the receive data is read from the SRB.

In Fig. 8-2, the status register is read and transmission/reception is performed while checking the TBRDY/RBRDY flags, but this can be performed using an interrupt, too.

8.5 SCU REGISTERS AND COMMANDS

SCU register read/write command issuance is performed by I/O input/output instructions on an address set in the system I/O area, and the selection of registers etc. is performed by A1 and A0 (when IOAG of the SCTL register = 1) or A2 and A1 (when IOAG = 0).

Table 8-1 SCU Register/Command Addresses

A1/A2	A0/A1	Register/Command	Operation
0	0	SRB	Read
		STB	Write
0	1	SST	Read
		SCM	Write
1	0	SMD	Write
1	1	SIMK	Read/write

SRB is the receive data buffer from which the CPU can read receive data.

STB is the transmit data buffer to which the CPU writes transmit data.

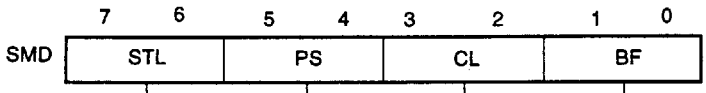
SST is the status register which indicates the communication status. It contains SRB and STB information and receive error information.

SCM is the command register which specifies transmission/reception enabling/disabling, error flag clearing, break transmission, and $\overline{\text{SRDY}}$ pin control.

SMD is the mode register which performs serial data setting. This register specifies the baud rate, character length, parity, and number of stop bits. When a 7-bit character length is selected, only the low-order 7 bits of SRB and STB are valid.

SIMK is the serial interrupt mask register which controls masking of interrupt requests generated by the SCU. When masking is performed, interrupts are no longer generated.

Fig. 8-3 SMD (Serial Mode Register)



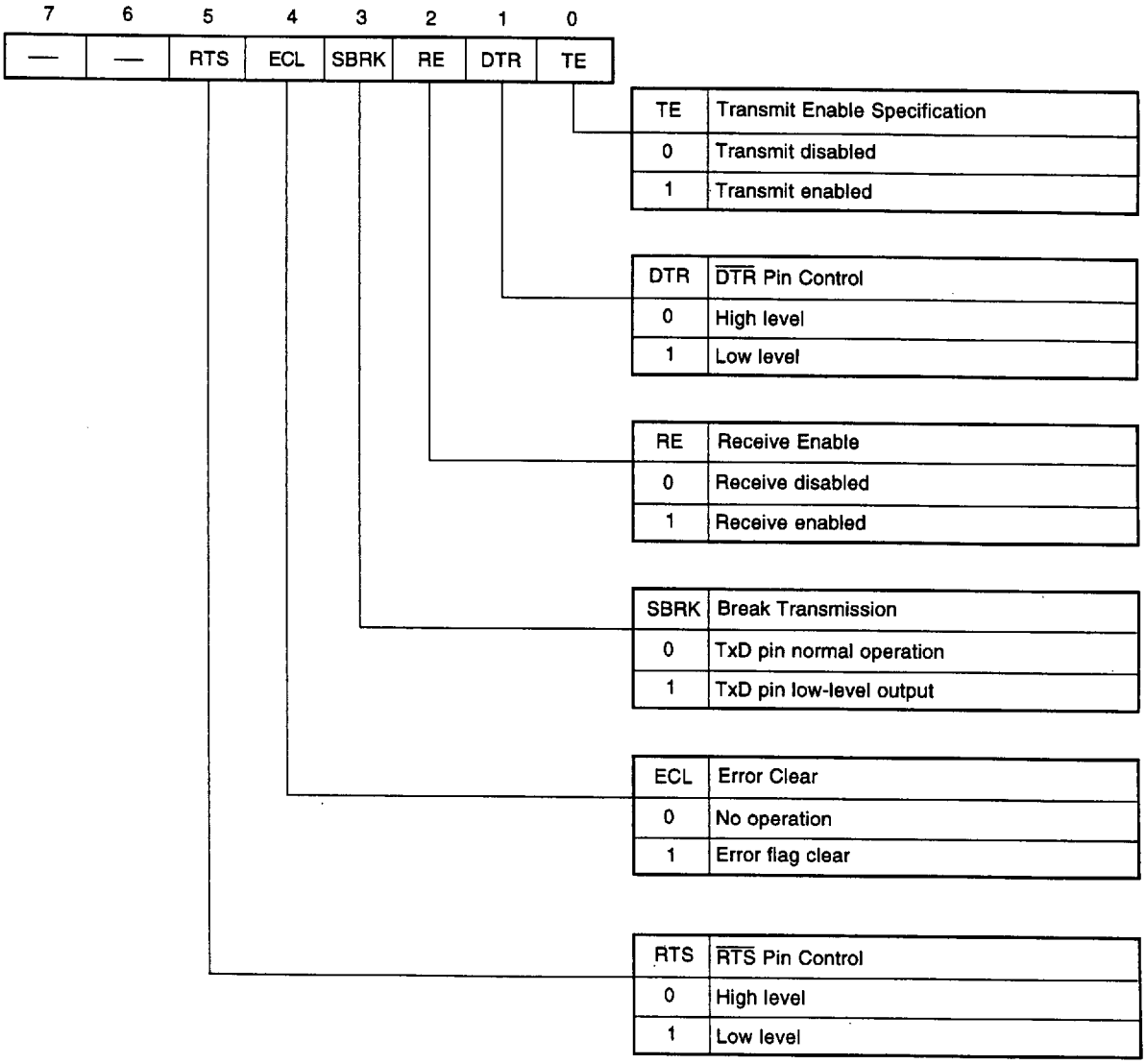
BF	Baud Rate
0 –	Setting prohibited
10	RTCLK frequency ÷ 16
11	RTCLK frequency ÷ 64

CL	Character Length
0 –	Setting prohibited
10	7 bits
11	8 bits

PS	Parity Selection
– 0	Parity disabled
01	Odd parity addition/check
11	Even parity addition/check

STL	Number of Stop Bits
– 0	Setting prohibited
01	1 bit
11	2 bits

Fig. 8-4 SCM (Serial Command Register)



TE	Transmit Enable Specification
0	Transmit disabled
1	Transmit enabled

DTR	$\overline{DTR}$ Pin Control
0	High level
1	Low level

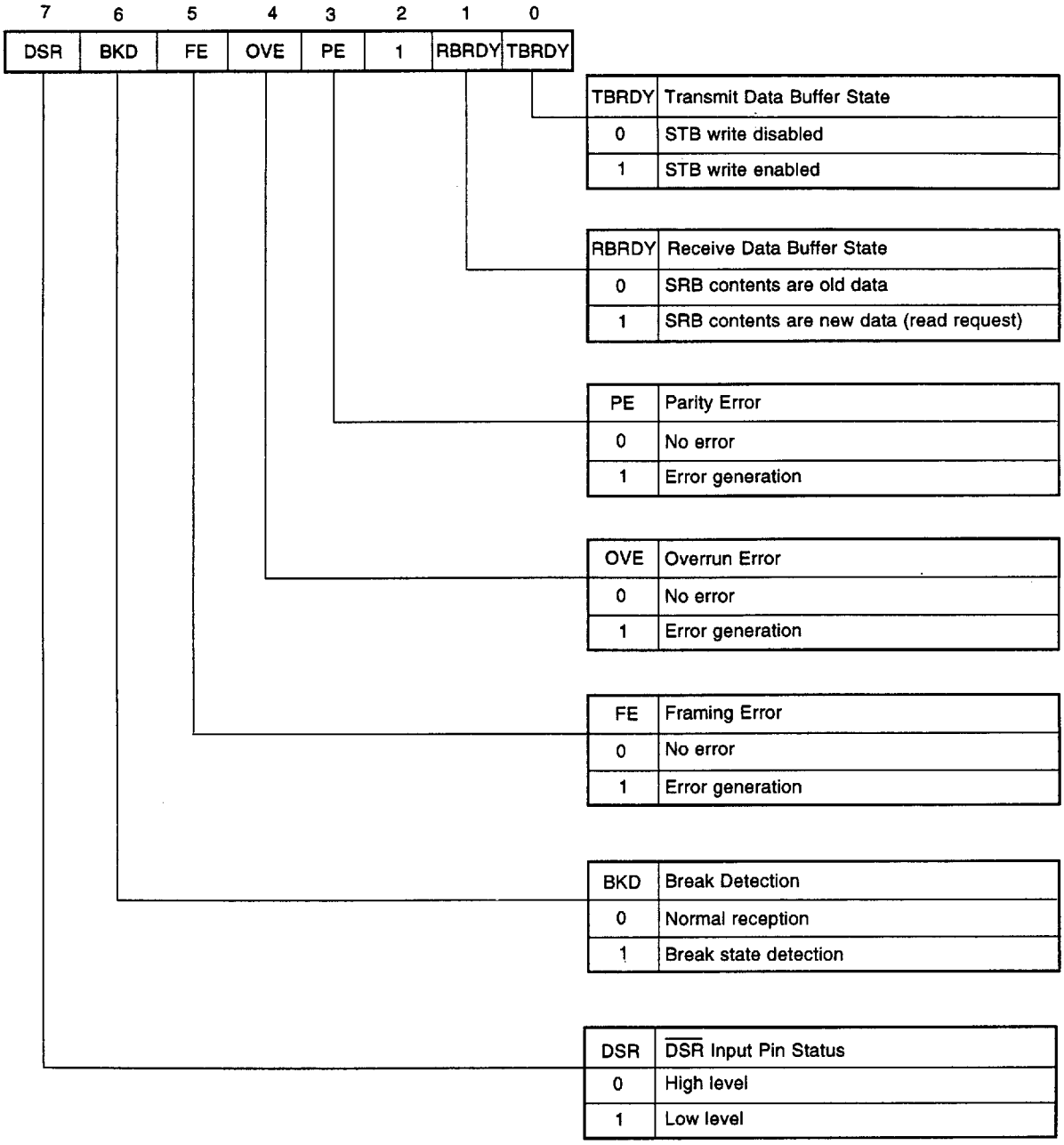
RE	Receive Enable
0	Receive disabled
1	Receive enabled

SBRK	Break Transmission
0	TxD pin normal operation
1	TxD pin low-level output

ECL	Error Clear
0	No operation
1	Error flag clear

RTS	$\overline{RTS}$ Pin Control
0	High level
1	Low level

Fig. 8-5 SST (Serial Status Register)



TBRDY	Transmit Data Buffer State
0	STB write disabled
1	STB write enabled

RBRDY	Receive Data Buffer State
0	SRB contents are old data
1	SRB contents are new data (read request)

PE	Parity Error
0	No error
1	Error generation

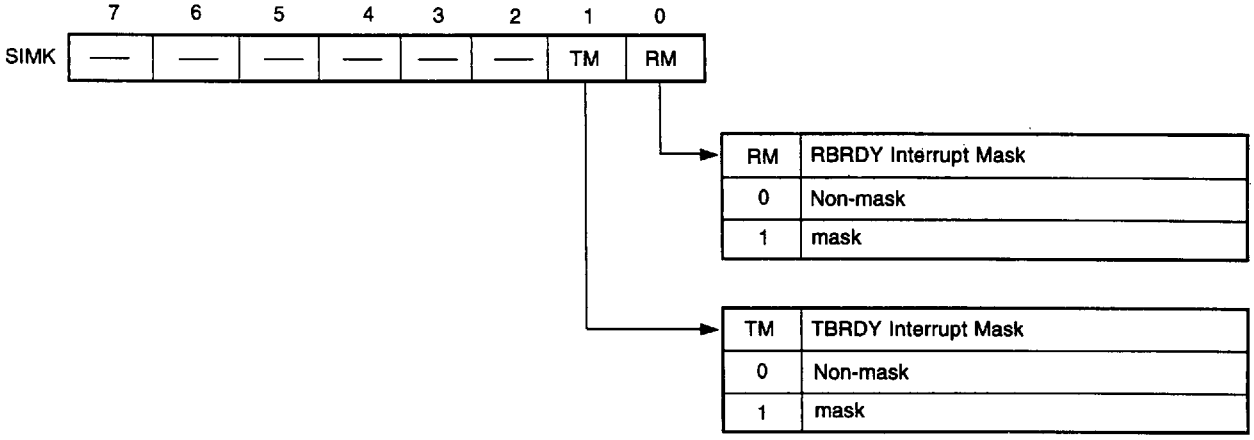
OVE	Overrun Error
0	No error
1	Error generation

FE	Framing Error
0	No error
1	Error generation

BKD	Break Detection
0	Normal reception
1	Break state detection

DSR	$\overline{\text{DSR}}$ Input Pin Status
0	High level
1	Low level

Fig. 8-6 SIMK (Serial Interrupt Mask Register)



9. ICU (INTERRUPT CONTROL UNIT)

The ICU arbitrates between up to 8 interrupt requests, and conveys one request to the CPU.

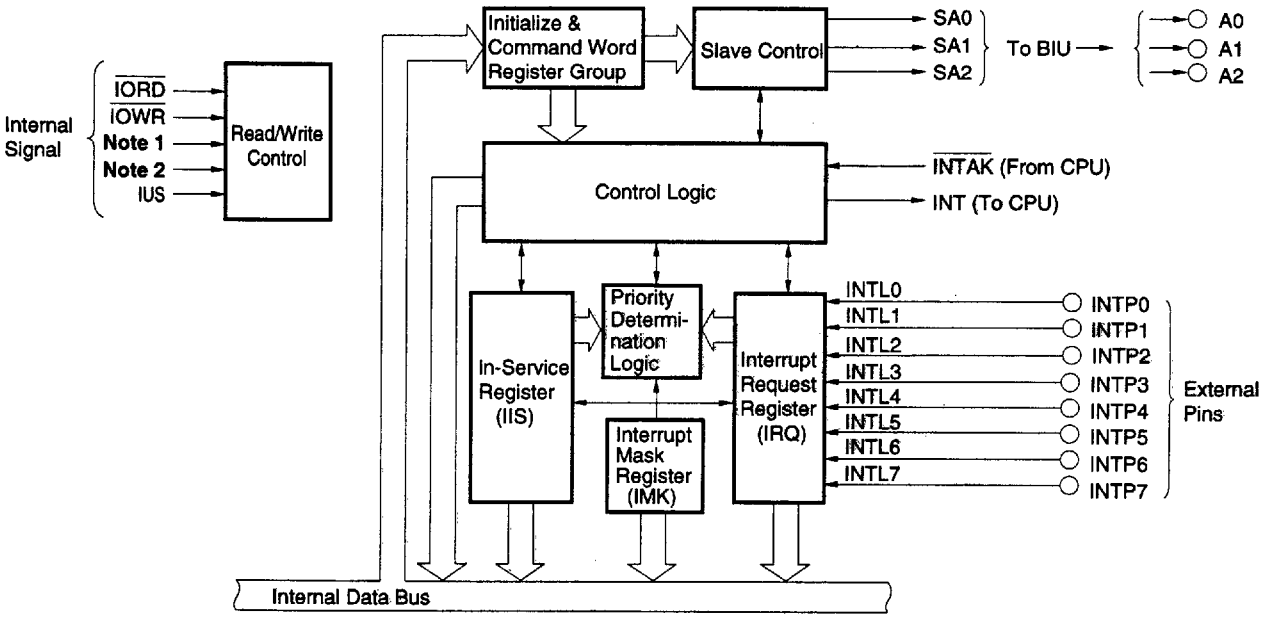
It is functionally the same as the μPD71059 with the CALL mode (8085 mode) and slave functions with cascading eliminated.

9.1 FEATURES

- μPD71059 equivalent
  - Channel expansion possible by cascade
  - Edge trigger/level trigger selectable
  - Individually maskable interrupt requests
  - Programmable interrupt request priority orders
  - Polling operation capability
- 8 interrupt request inputs (INTP0 to INTP7)
- 8 external input pins
- $\overline{\text{INTAK}}$ output pin

Caution The μPD70236A does not incorporate pull-up resistors in pins INTP0 to INTP7 to reduce power consumption when stopped. This is different from the μPD71059 and μPD70208/70216.

9.2 ICU INTERNAL BLOCK DIAGRAM

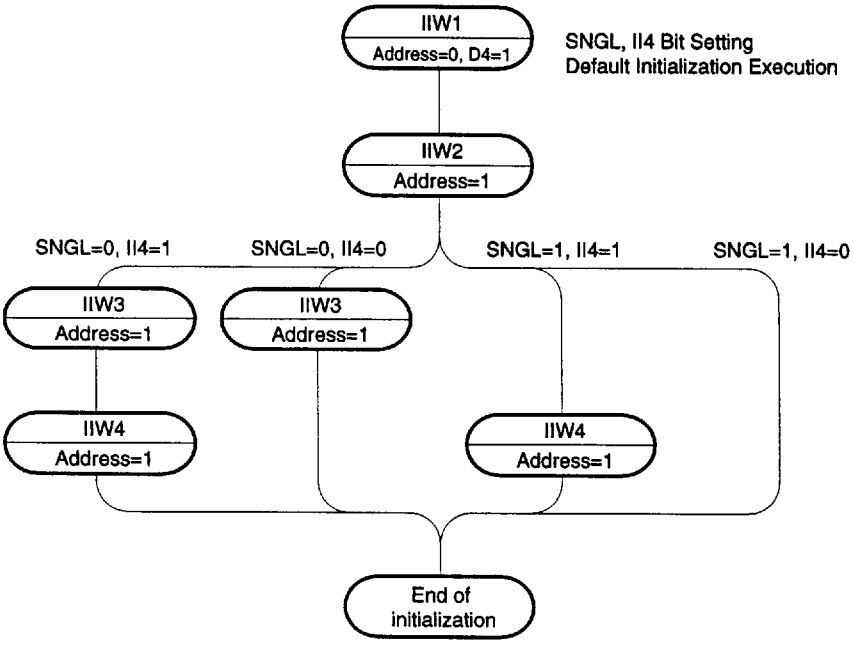


Notes 1. When IOAG of the SCTL register = 1, A0. When IOAG = 0, A1.
2. When IOAG of the SCTL register = 1, A1. When IOAG = 0, A2.

9.3 INTERRUPTS BY ICU

The ICU is always used when maskable interrupts are used in a μPD70236A system. The ICU must be initialized by execution of an initialization program before starting interrupt operations. There are four methods of initializing the ICU, following the initialization sequence shown in Fig. 9-1.

Fig. 9-1 ICU Initialization Sequence



Remark Address is A1 or A0.

When initialization is complete, the ICU arbitrates between requests coming in on the 8 interrupt request pinsINTL0 to INTL7, and transmits the highest-priority request to the CPU. At the end of the initiated interrupt service routine, the CPU issues an FI (Finish Interrupt) command to the ICU to report the end of interrupt servicing. The ICU ascertains the current interrupt service situation from the interrupt request signal and the FI command information from the CPU.

Commands from the CPU can be used to change interrupt request priorities, mask requests, read registers, conduct polling, and soon.

9.4 ICU REGISTERS

ICU register read/writing and command issuance is performed by I/O input/output instructions on an address set in the system I/O area, and the selection of registers, etc. is performed by A0 (when IOAG of the SCTL register = 1) or A1 (when IOAG = 0) (A1 when IOAG = 1 and A2 when IOAG = 0 may be either 0 or 1).

Table 9-1 Register/Command Addresses

	A0/A1	A1/A2	Other A0 (A1) Condition	Operation
Read	0	x (don't care)	IRQ set by IMD	CPU ← IRQ data
			IIS set by IMD	CPU ← IIS data
			Polling phase[Note]	CPU ← IPOL
	1		———	CPU ← IMKW
Write	0		D4 = 1	CPU → IIW1
			(D4 = 0) • (D3 = 0)	CPU → IPFW
			(D4 = 0) • (D3 = 1)	CPU → IMDW
	1		During initialization sequence	CPU → IIW2
				CPU → IIW3
				CPU → IIW4
			After initialization	CPU → IMKW

Note In the polling phase, polling data of IPOL is read with priority given to IRQ or IIS.

Initialization words IIW1 to IIW4 perform ICU initialization, check whether a μPD71059 is connected as a slave, and perform setting of the vector number to be sent to the CPU, the INTP pin input trigger, and so forth.

There are 3 command words: IMKW, IPFW, and IMDW.

IMKW sets interrupt request masking.

IPFW issues the FI (Finish Interrupt) command issued at the end of interrupt servicing and interrupt request priority change (rotation) commands.

IMDW specifies the register to be read (IRQ or IIS) by a register read when A1 = 0, directs the start of a polling operation, and so forth.

Fig. 9-2 ICU Initialization Words

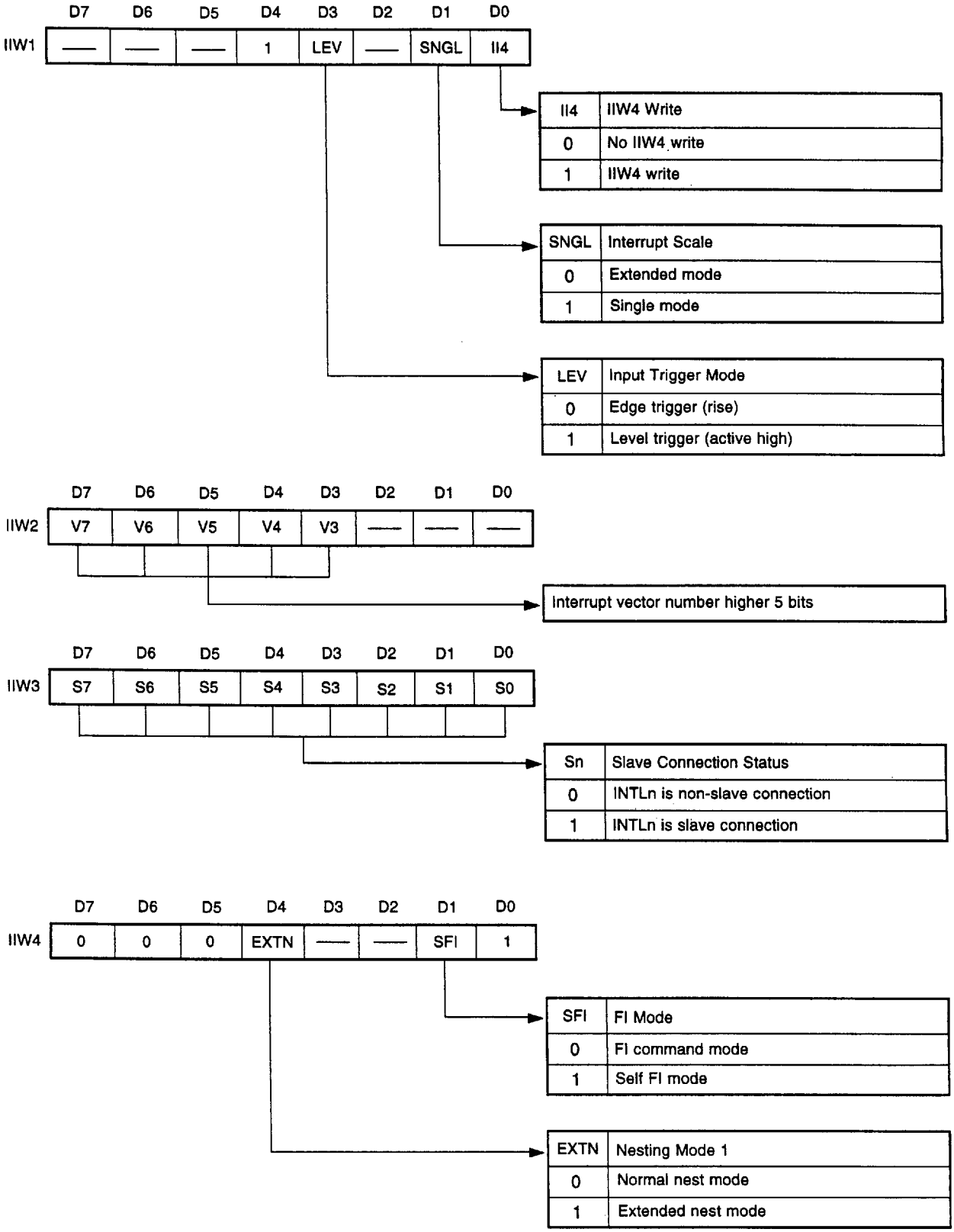
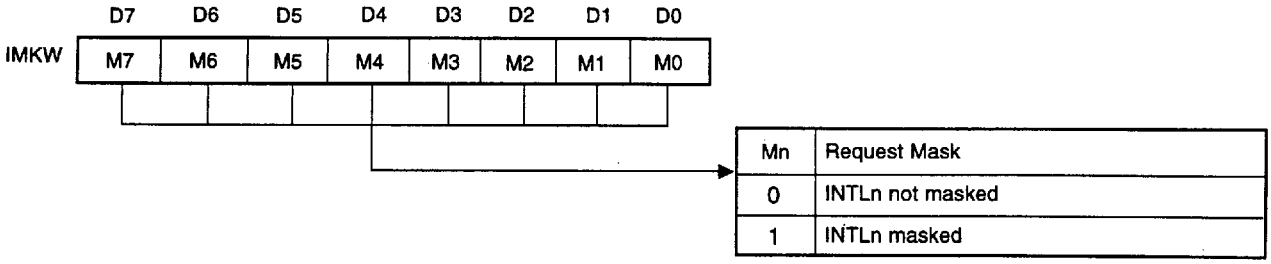
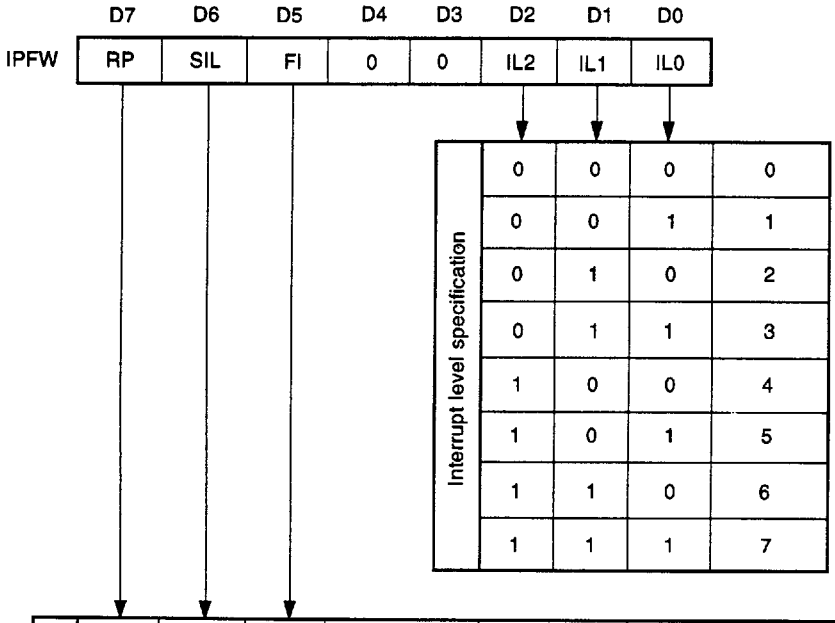


Fig. 9-3 ICU Command Words

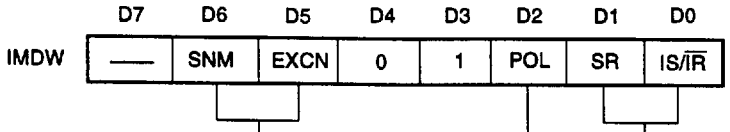


Mn	Request Mask
0	INTLn not masked
1	INTLn masked



Interrupt level specification				
	0	0	0	0
	0	0	1	1
	0	1	0	2
	0	1	1	3
	1	0	0	4
	1	0	1	5
	1	1	0	6
	1	1	1	7

Priority order rotation and FI command							
	0	0	1	FI command	No level specification	No rotation	Normal FI command
	1	0	1			Rotation	Normal rotation FI command
	0	1	1		Level specification	No rotation	Specified FI command
	1	1	1			Rotation	Specified rotation FI command
	0	1	0	Non-FI command		No rotation	No operation
	1	1	0			Rotation	Specified rotation command
	0	0	0		No level specification	No rotation	Self FI mode rotation reset
	1	0	0			Rotation	Self FI mode rotation set



SR	IS/IR	Read Register Selection
0	—	No operation
1	0	IRQ selection
1	1	IIS selection

POL	Polling
0	No operation
1	Polling command

SNM	EXCN	Nesting Mode 2
0	—	No operation
1	0	Exception nest mode release
1	1	Exception nest mode setting

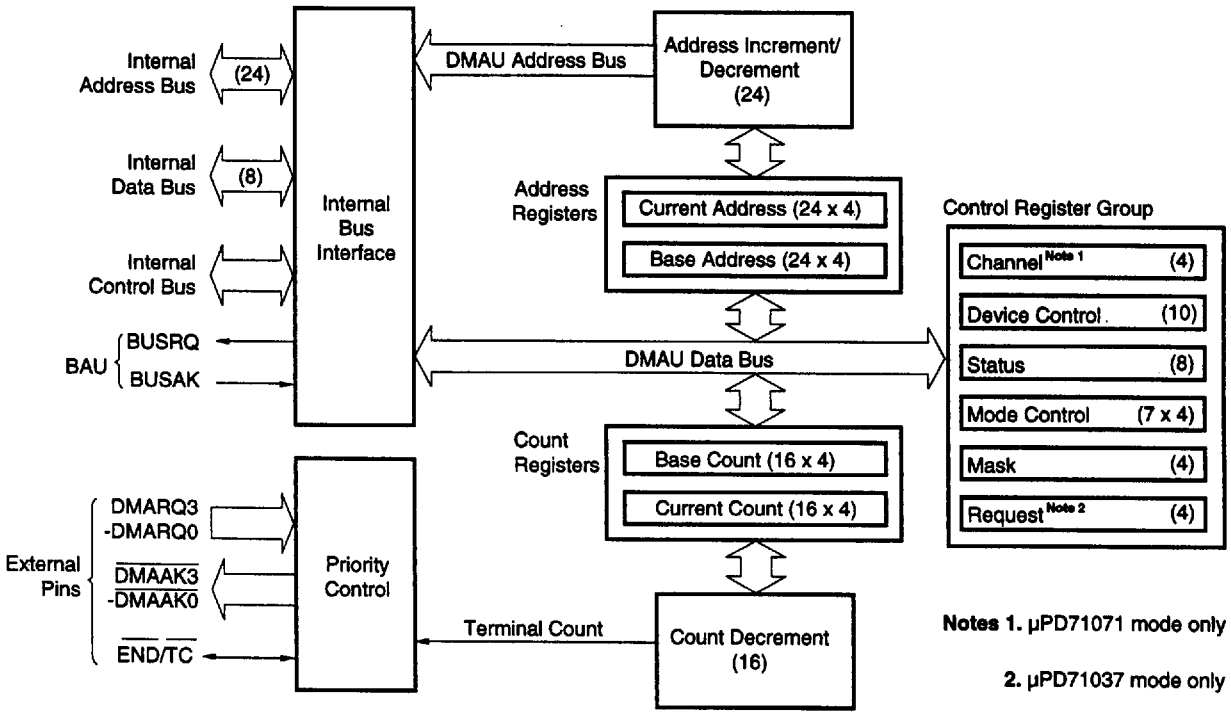
10. DMAU (DMA CONTROL UNIT)

The DMAU has four DMA channels, and provides the functions (subsets) of two LSIs: The μPD71071 and μPD71037.

10.1 FEATURES

- 2 operating modes (μPD71071 mode, μPD71037 mode)
- 24-bit length address register
- 16-bit length count register
- 4 independent DMA channels
- 4 clocks/1 bus cycle
- Byte transfer/word transfer selectable
- 3 transfer modes (settable per channel)
  Single transfer mode, demand transfer mode, block transfer mode
- 2 bus modes (Common to all channels; bus release mode only in μPD71037 mode)
  Bus release mode
  Bus hold mode
- DMA requests maskable on an individual channel basis
- Auto-initialization function
- Transfer address incrementing/decrementing
- 2 kinds of channel priority order (fixed priority/ rotating priority)
- $\overline{TC}$ output at the end of transfer
- Forced service termination by $\overline{END}$ input
- Cascading capability
- I/O-memory and memory-I/O transfer capability

10.2 DMAU INTERNAL BLOCK DIAGRAM



Notes 1. μPD71071 mode only

2. μPD71037 mode only

Remark The other four register groups function in both modes.

10.3 DIFFERENCES BETWEEN μPD71071 MODE AND μPD71071

With the exception of the functions shown below, the μPD71071 mode of DMAU is functionally identical to the μPD71071.

Table 10-1 Differences between μPD71071 Mode and μPD71071

Function	μPD71071 Mode	μPD71071
Software requests	No	Yes
Memory–to–memory transfers	No	Yes
DMARQ active level	High	High or low
DMAAK active level	Low	High or low
Bus cycle	4 clock cycles	4 or 3 clock cycles

10.4 DIFFERENCES BETWEEN μPD71037 MODE AND μPD71037

With the exception of the functions shown below, the μPD71037 mode of DMAU is functionally identical to the μPD71037.

Table 10-2 Differences between μPD71037 Mode and μPD71037

Function	μPD71037 Mode	μPD71037
Memory–to–memory transfers	No	Yes
DMARQ active level	High	High or low
DMAAK active level	Low	High or low
Bus cycle	4 clock cycles	3 or 2 clock cycles

10.5 DIFFERENCES BETWEEN μPD71037 MODE AND μPD71071 MODE

The differences between the μPD71037 mode and the μPD71071 mode are described below.

(1) Unit of transfer

In the μPD71071 mode either byte transfers or word transfers can be selected, whereas in the μPD71037 mode all transfers are byte transfers.

(2) Channel selection

Since there is no channel register in the μPD71037 mode, the channel is specified each time a command is issued. In the case of the mode control register, the channel is selected by part of the write data.

In the case of the address register and count register, the channel is selected by means of the I/O address to be accessed.

(3) Base/current register accesses

The address register and count register of each channel consist of a base register and current register. The target of the access varies depending on the mode as shown below.

(a) μPD71071 mode

Switching can be performed by means of the channel register as follows:

- For a read : Current register only
  For a write: Both base register and current register simultaneously
- For a read/write: Base register only

(b) μPD71037 mode

For a read : Current register only
For a write: Both base register and current register simultaneously

(4) Software DMA requests

The μPD71037 mode has a request register which is not provided in the μPD71071 mode, and this allows DMA requests to be generated by software.

(5) Bus mode

In the μPD71037 mode there is no bus mode selection, and operation is always in the μPD71071 mode bus release mode only.

(6) DMAU location addresses

In the μPD71071 mode, DMAU I/O addresses are always located consecutively, whereas in the μPD71037 mode it is possible to select consecutive addresses or to fix accesses to odd or even addresses by means of the SCTL register.

(7) Others

Basic commands are the same in both modes, but the μPD71071 mode has commands which are not provided in the μPD71037 mode, and vice versa. Also, there is no compatibility between the I/O addresses for individual commands in the μPD71071 mode and the μPD71037 mode. All commands in the μPD71037 mode must be executed by byte type IN/OUT instructions.

10.6 μPD71071 MODE

Setting the DMAM bit of the SCTL register in the system I/O area to "0" places the DMAU in the μPD71071 mode. The μPD71071 mode is also selected directly after a reset.

10.6.1 Commands in μPD71071 Mode

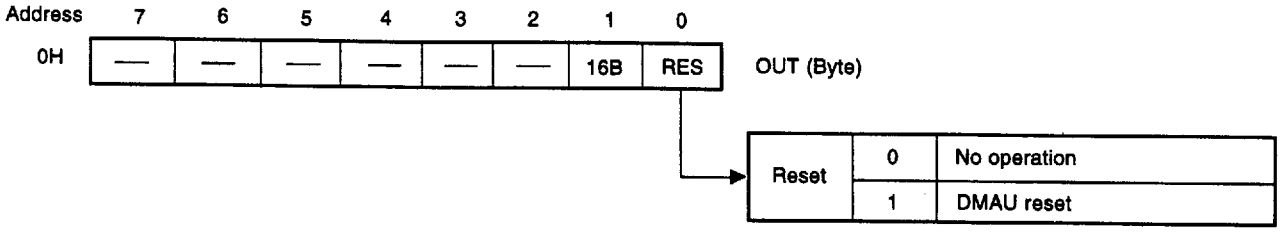
Issuance of commands to read/write DMAU registers is performed by I/O input/output instructions on an address set in the system I/O area, and command selection is performed by the 4 bits A3 to A0. A command address refers to the value of A3 to A0.

Table 10-3 DMAU Command Addresses (μPD71071 Mode)

Address	Operation	Command
0H	W(B)	Initialize (DICM)
1H	R(B)	Channel register read (DCH)
	W(B)	Channel register write (DCH)
2H	R/W	Count register read/write (DBC/DCC)
3H	R/W	
4H	R/W	Address register read/write (DBA/DCA)
5H	R/W	
6H	R/W (B)	
8H	R/W	Device control register read/write (DDC)
9H	R/W	
0AH	R/W (B)	Mode control register read/write (DMD)
0BH	R(B)	Status register read (DST)
0FH	R/W (B)	Mask register read/write (DMK)

Caution Commands followed by (B) should be performed by means of a byte IN/OUT instruction. Address and operation combinations not shown in this table are prohibited.

Fig. 10-1 Initialize Command Format



Remark In the μPD71071, either the 8-bit data bus or 16- bit data bus is selected by the 16B bit. However, in the μPD70236A, the 16-bit data bus is always set by the 16B bit whether it is 0 or 1.

Table 10-4 DMAU Register Initialization by Reset

Register Name	Initialization Contents
Address register	No change
Count register	No change
Channel register	7 6 5 4 3 2 1 0 — — — 0 0 0 0 1 (CH0 selection)
Mode countrol register	All bits cleared
Device countrol register	All bits cleared
Status register	All bits cleared
Mask register	All bits set (all channels masked)

Fig. 10-2 Channel Register Read Command Format

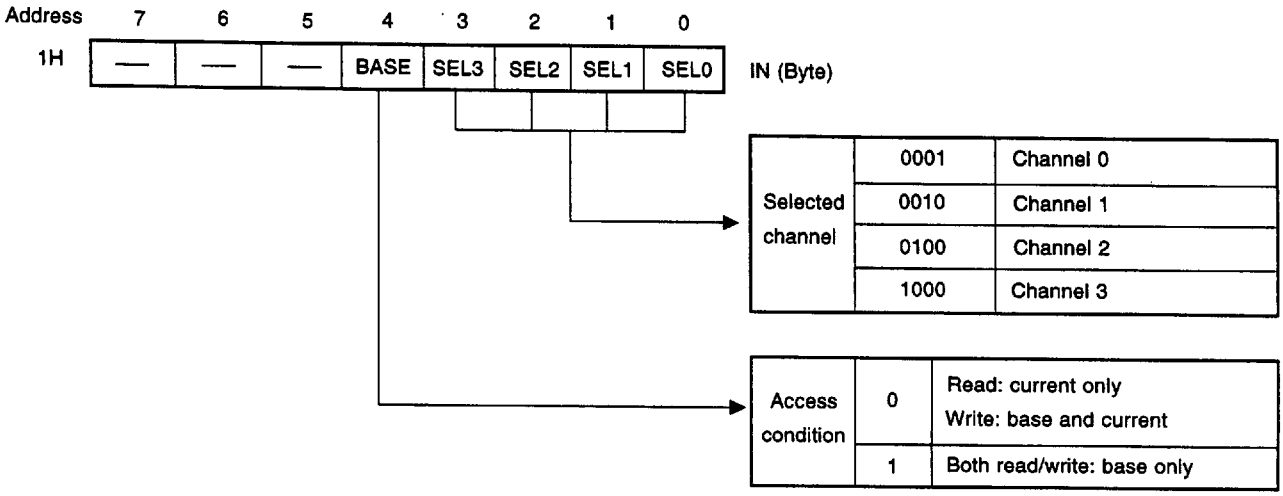


Fig. 10-3 Channel Register Write Command Format

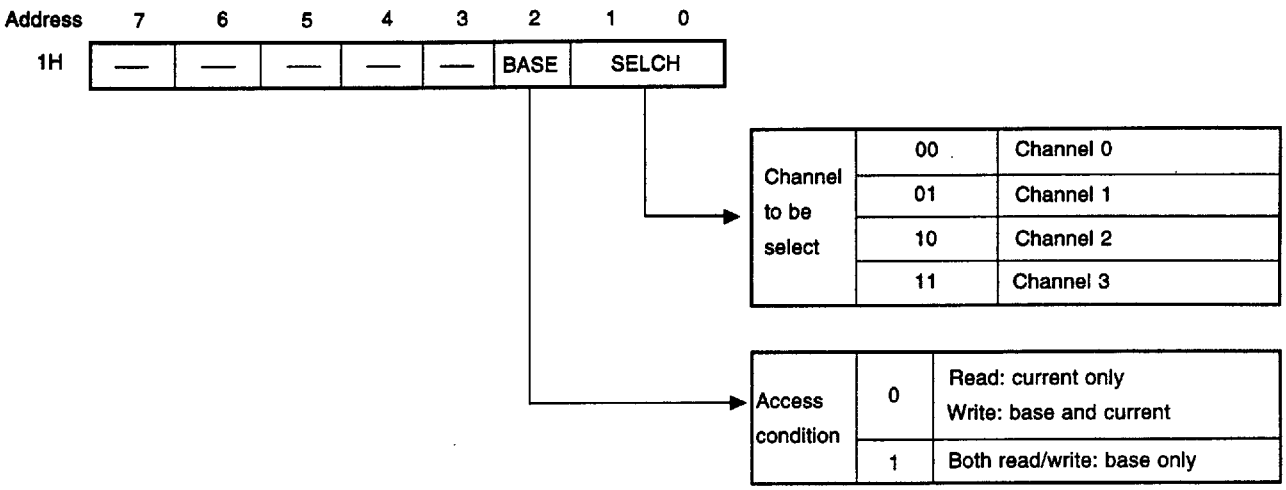


Fig. 10-4 Count Register Read/Write Command Format

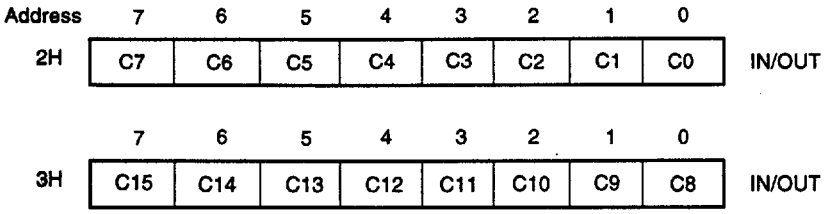


Fig. 10-5 Address Register Read/Write Command Format

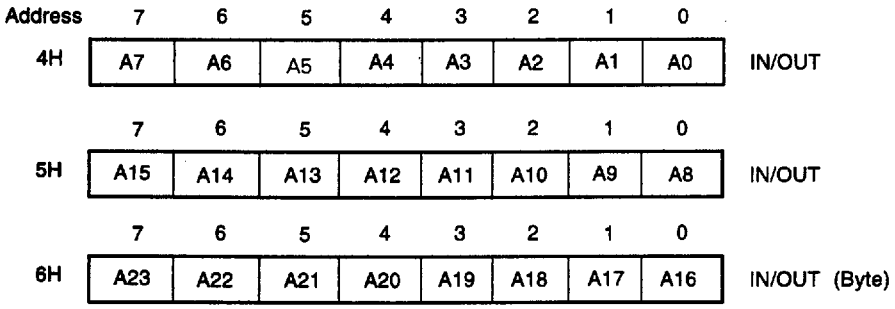


Fig. 10-6 Device Control Register Read/Write Command Format

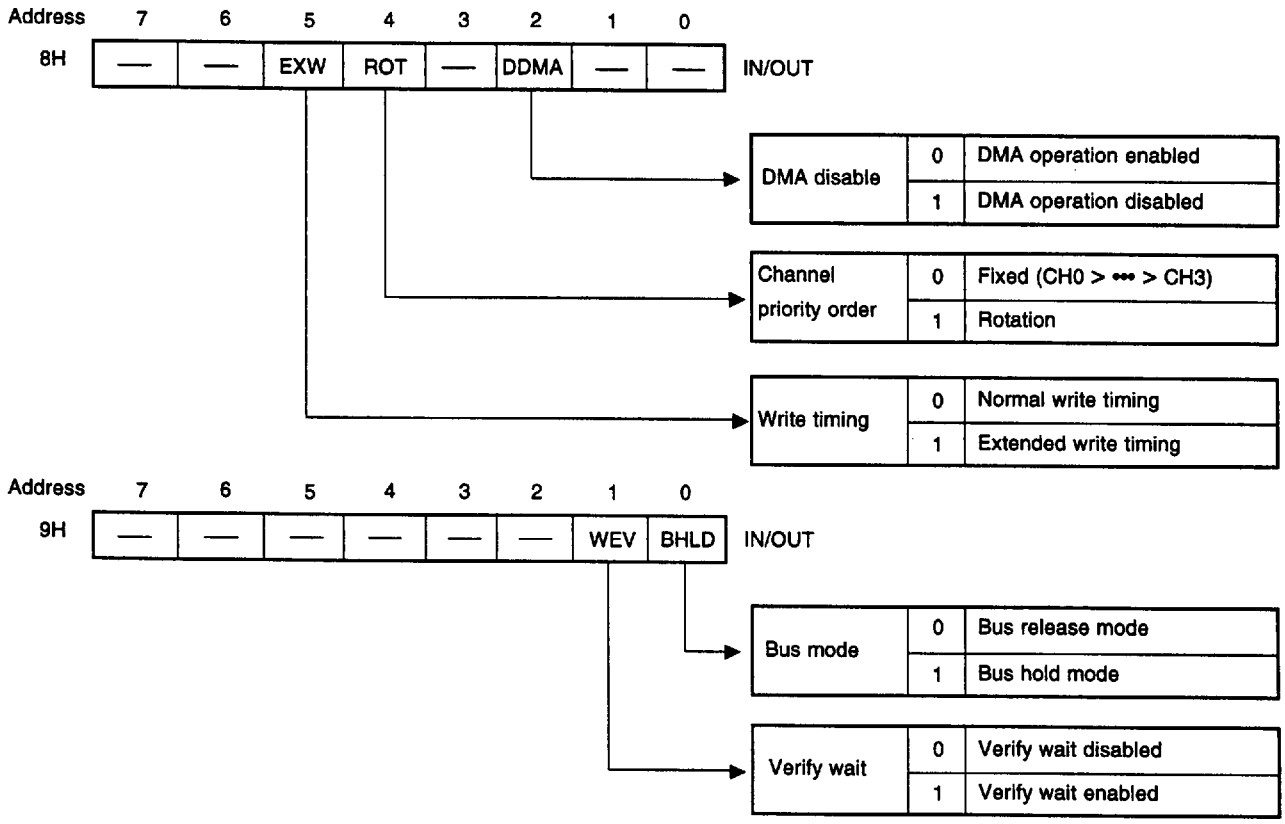


Fig. 10-7 Mode Control Register Read/Write Command Format

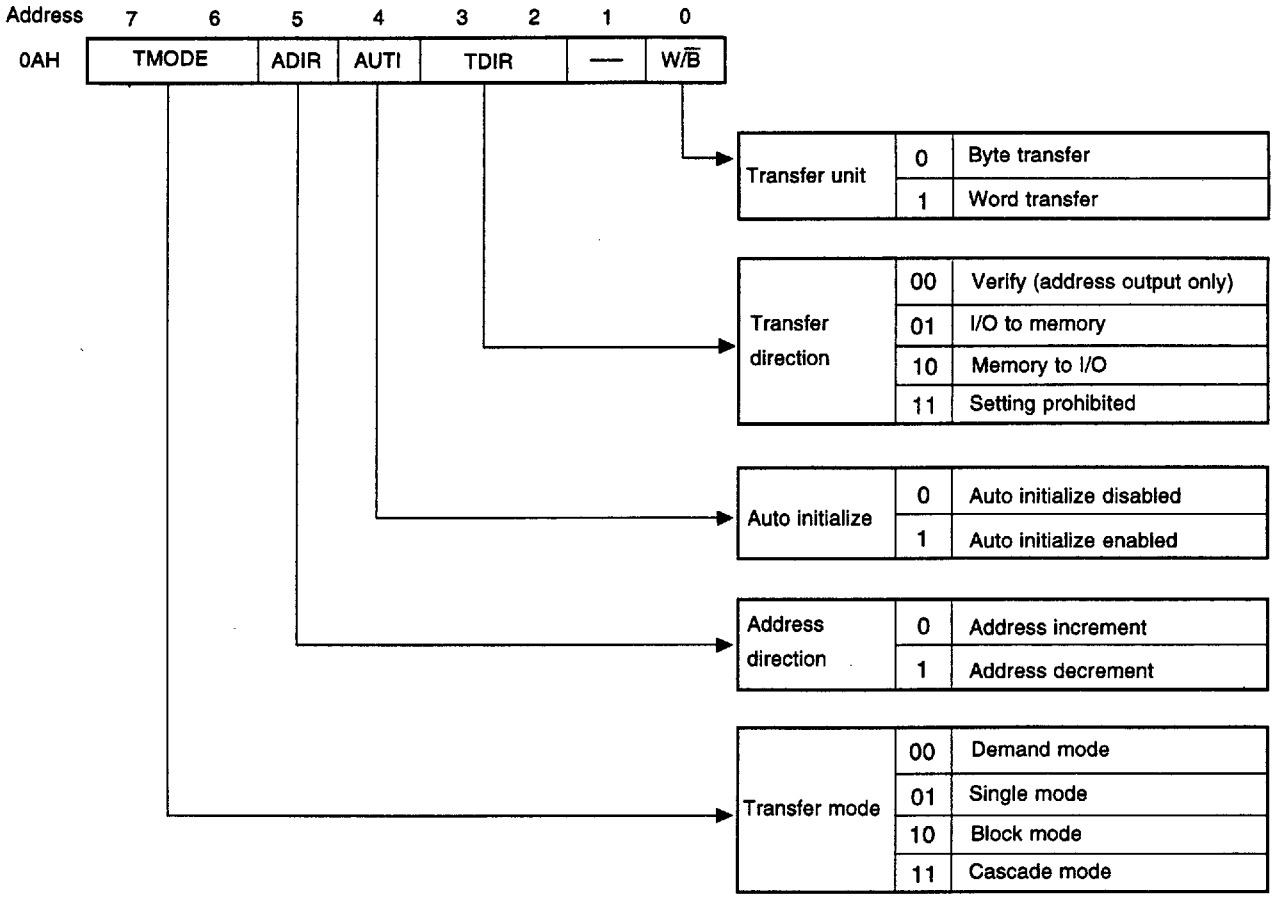


Fig. 10-8 Status Register Read Command Format

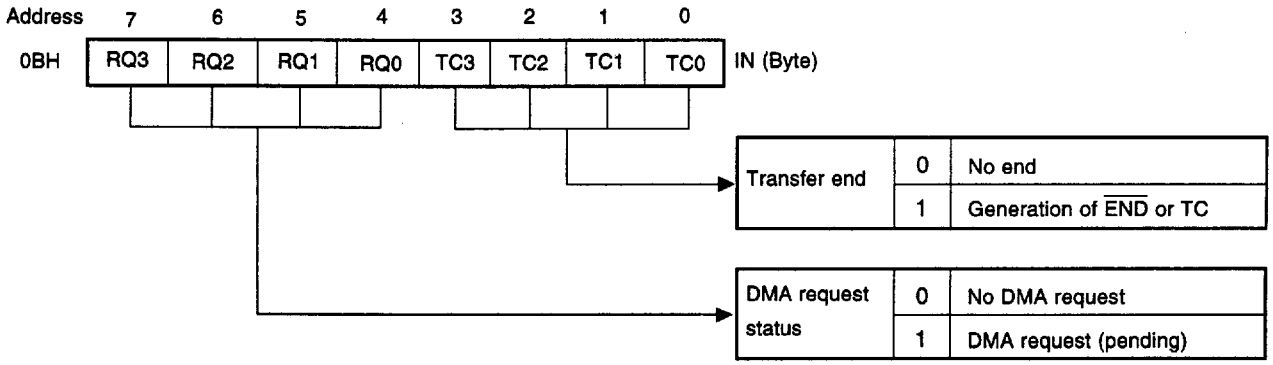
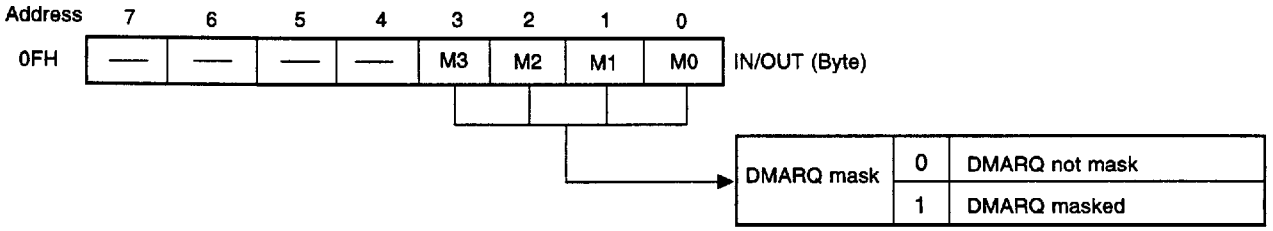


Fig. 10-9 Mask Register Read/Write Command Format



10.7 μPD71037 MODE

Setting the DMAM bit of the SCTL register in the system I/O area to "1" places the DMAU in the μPD71037 mode. The μPD71071 mode, not the μPD71037 mode, is selected directly after a reset.

10.7.1 List of μPD71037 Mode Commands

A3 A2 A1 A0	Operation	F/F	Command Name
0 channel[Note] 0	Read	0	Read current address register (lower byte)
		1	Read current address register (upper byte)
	Write	0	Write base & current address register (lower byte)
		1	Write base & current address register (upper byte)
0 channel[Note] 1	Read	0	Read current count register (lower byte)
		1	Read current count register (upper byte)
	Write	0	Write base & current count register (lower byte)
		1	Write base & current count register (upper byte)
1 0 0 0	Read		Read status register
	Write		Write command register
1 0 0 1	Write		Write request register
1 0 1 0	Write		Write single mask register
1 0 1 1	Write		Write mode register
1 1 0 0	Write		Clear byte pointer F/F
1 1 0 1	Write		Initialize
1 1 1 0	Write		Clear mask register
1 1 1 1	Write		Write all mask register

Note channel = 00: Channel 0 selected
channel = 01: Channel 1 selected
channel = 10: Channel 2 selected
channel = 11: Channel 3 selected

10.7.2 Commands In μPD71037 Mode

The detailed format of each control command is shown below. With the three commands Clear Byte Pointer F/F, Initialize, and Clear Mask Register, the write data has no significance and the value of the data in a byte type OUT instruction is immaterial.

Fig. 10-10 Read Status Register

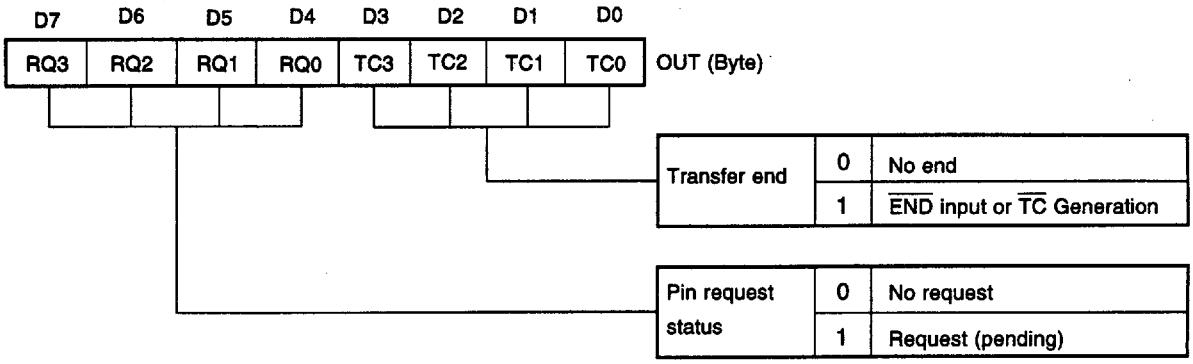


Fig. 10-11 Write Command Register

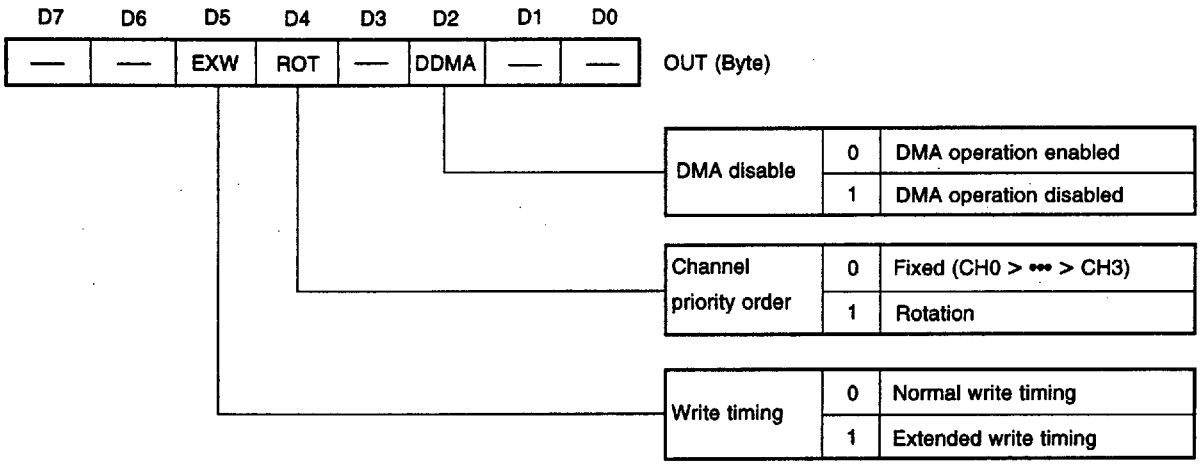


Fig. 10-12 Write Request Register

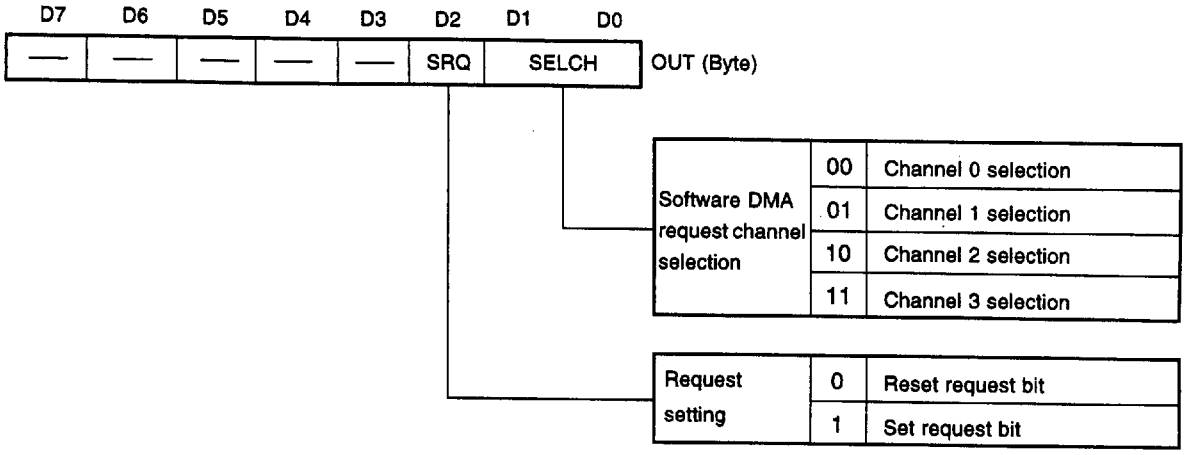


Fig. 10-13 Write Single Mask Register

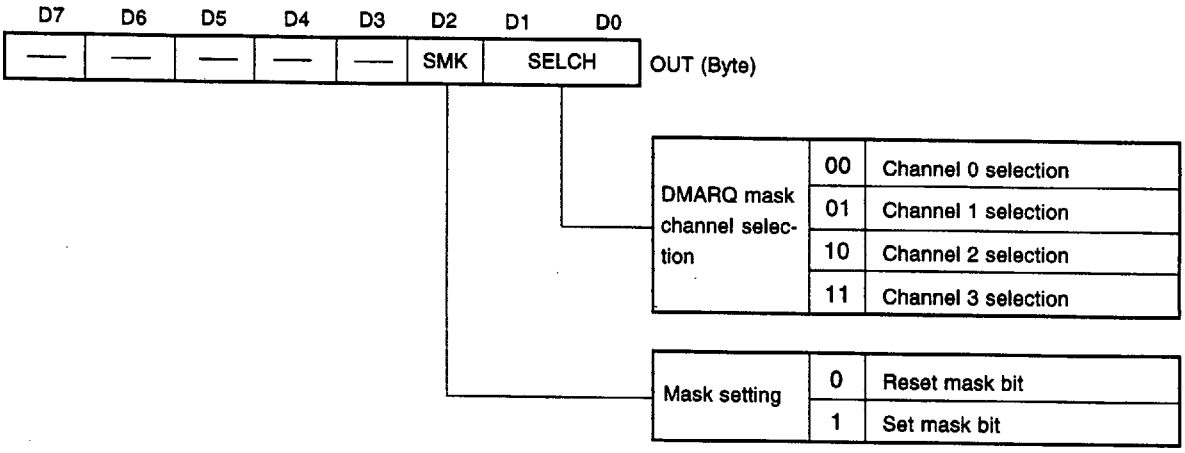


Fig. 10-14 Write All Mask Register

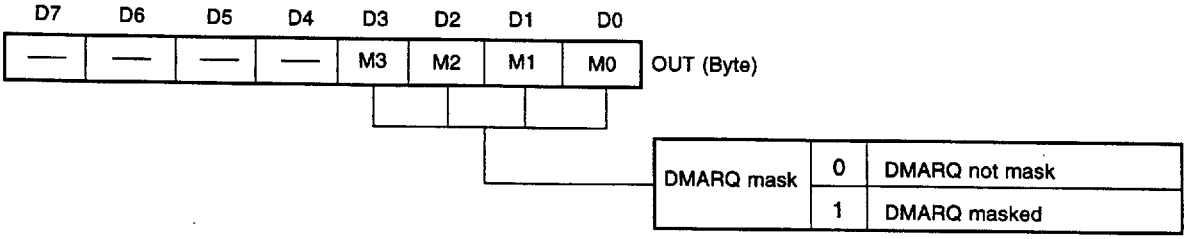
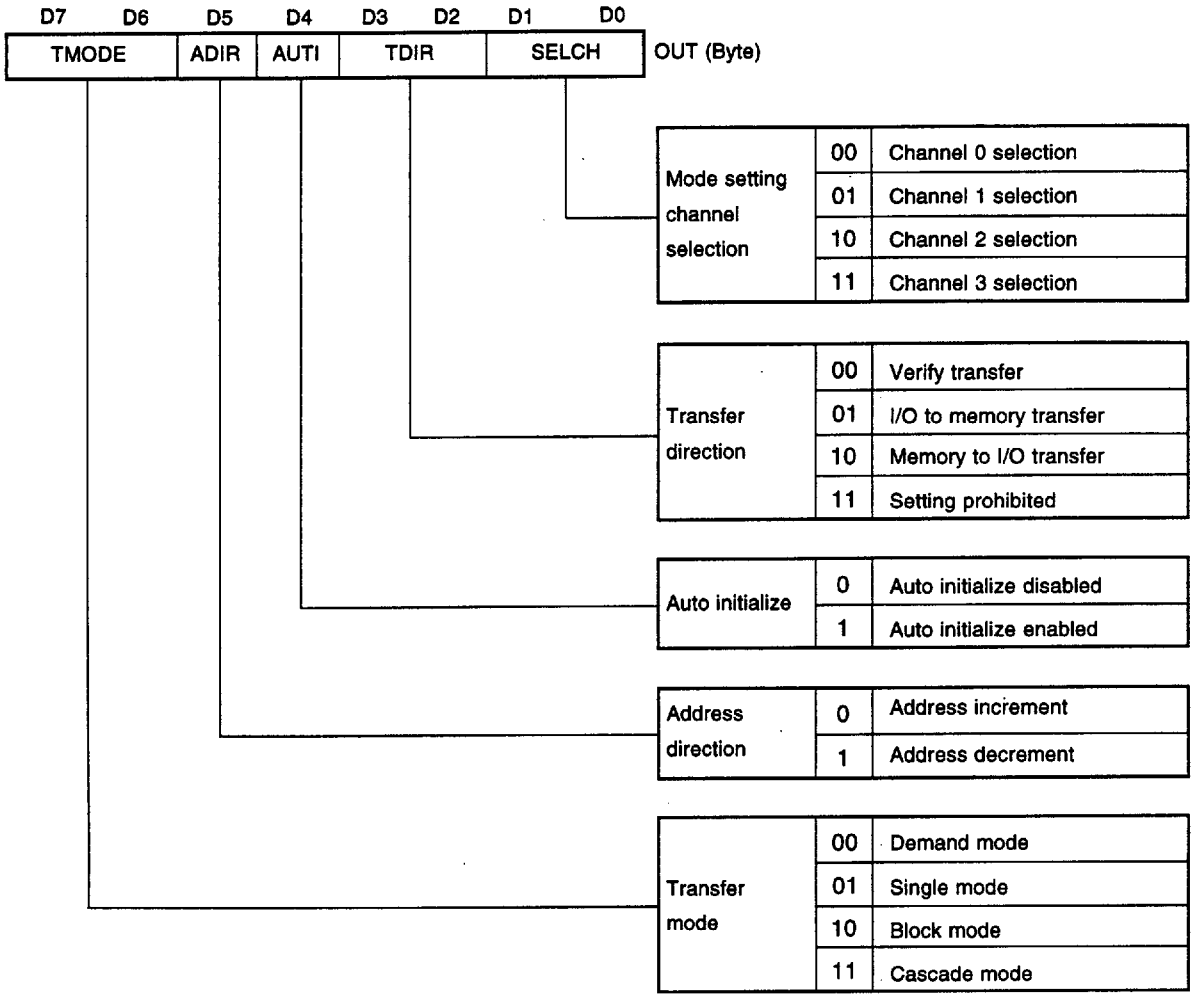


Fig. 10-15 Write Mode Register



10.7.3 Bank Registers

In the μPD71037 mode, the μPD70236A incorporates bank registers (BNKR3 to BNKR0) which set the extended DMA address A23 to A16 for channels 3 to 0. In the μPD71037 mode, the I/O address for reading/writing these registers is set by OPHA and BADR in the system I/O area. BADR is a relocatable register.

(1) Bank register I/O addresses

The high-order 8 bits (A15 to A8) of a bank register (BNKR3 to BNKR0) I/O address are set by OPHA, and the low-order 8 bits (A7 to A0) by BADR (the bank address register). As with other on-chip peripheral relocation registers, the settable bits vary depending on the value of the IOAG bit in SCTL.

Fig. 10-16 Bank Address Register

I/O Address: FFE1H BADR

7	6	5	4	3	2	1	0	
A7	A6	A5	A4	A3	A2	—	—	When IOAG = 0
A7	A6	A5	A4	A3	—	—	A0	When IOAG = 1

(2) Bank selection register

The I/O address of a bank register is determined by the address set by the OPHA and BADR registers, but in addition, the bank register selected by A1/A0 or A2/A1 is also programmable.

Fig. 10-17 Bank Selection Register

I/O Address: FFE0H BSEL

7	6	5	4	3	2	1	0
BNK3		BNK2		BNK1		BNK0	

BNK3, BNK2, BNK1, BNK0	Address Specification of Bank Registers (BNKR3 toBNKR0) of Channels 3, 2, 1, 0
00	A1 (A2) = 0, A0 (A1) = 0
01	A1 (A2) = 0, A0 (A1) = 1
10	A1 (A2) = 1, A0 (A1) = 0
11	A1 (A2) = 1, A0 (A1) = 1

(3) Bank register

Fig. 10-18 Bank Register

7	6	5	4	3	2	1	0
A23	A22	A21	A20	A19	A18	A17	A16

This register becomes undefined after using the μPD71071 mode. In the bank register, the use of DMAU is enabled by OPSEL in the system I/O area and the register exists in the I/O space only in the μPD71037 mode. It does not exist in the internal I/O space in the μPD71071 mode. However, both the BADR and BSEL registers exist in the system I/O space irrespective of the DMAU mode. The bank register uses the address register high-order 8 bits in the μPD71071 mode.

(4) Carry propagation control

Propagation of a carry from A15 to A16 or from A19 to A20 when the bank registers are used is controlled by the CE0 and CE1 bits in SCTL in the system I/O area.

CE0	Function
0	Carry not propagated into A16 in μPD71037 mode
1	Carry propagated into A16 in μPD71037 mode

CE1	Function
0	Carry not propagated into A20 in μPD71037 mode
1	Carry propagated into A20 in μPD71037 mode

11. μPD72291 FLOATING-POINT CO-PROCESSOR INTERFACE

The interface between the μPD72291 and the μPD70236A is described below.

11.1 SYSTEM CONFIGURATION EXAMPLE

An example of a system configuration with the μPD72291 connected to the μPD70236A is shown in Fig. 11-1.

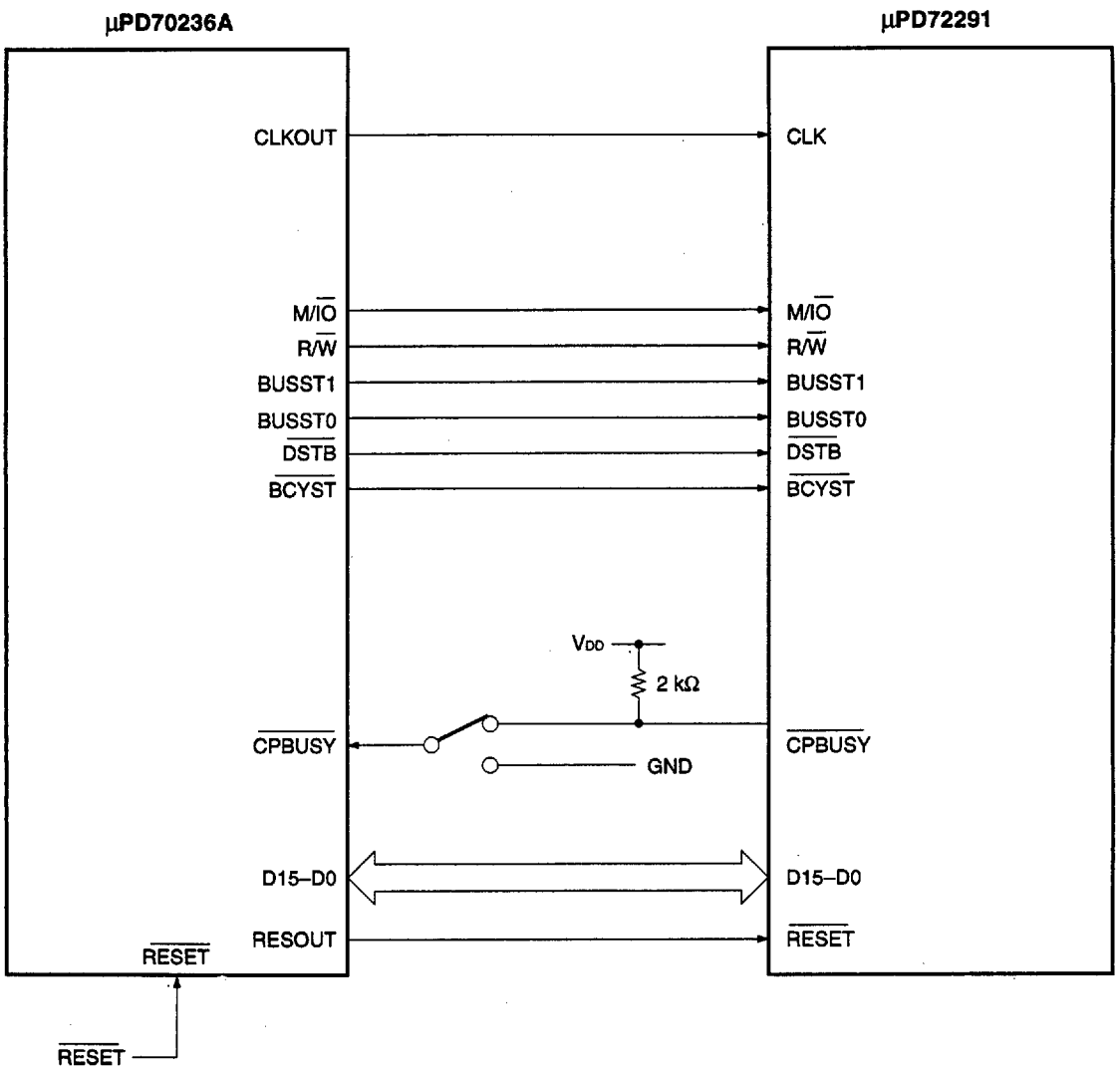
The μPD72291 and μPD70236A can be connected without the addition of external circuit.

μPD72291 input/output signals (CLK, $\overline{\text{RESET}}$, BUSST1, BUSST0, M/$\overline{\text{IO}}$, R/$\overline{\text{W}}$, $\overline{\text{DSTB}}$, D15 to D0) are directly connected to the μPD70236A. A CLKOUT signal shared with the μPD70236A should be input as the μPD72291 CLK pin.

The μPD72291 $\overline{\text{CPBUSY}}$ signal should be connected to the μPD70236A $\overline{\text{CPBUSY}}$ signal and pulled up to V_{DD} with a resistor (around 2kΩ).

When a μPD72291 socket only is provided and a μPD72291 is not connected, a switch is attached to the μPD70236A $\overline{\text{CPBUSY}}$ signal allowing it to be connected to GND. The μPD70236A samples the $\overline{\text{CPBUSY}}$ signal when a reset is performed and if the $\overline{\text{CPBUSY}}$ signal is low, a co-processor absent exception is generated when execution of a μPD72291 instruction is attempted.

Fig. 11-1 System Configuration Example



Cautions

1. **Ensure that the μPD70236A CPU CLKOUT signal is input to the μPD72291 CLK pins.**
2. **When connecting the μPD72291 to the μPD70236A, input the μPD72291 $\overline{\text{CPBUSY}}$ signal to the $\overline{\text{CPBUSY}}$ pin of the μPD70236A. When a μPD72291 socket only is provided and a μPD72291 is not connected, attach a switch to the μPD70236A $\overline{\text{CPBUSY}}$ signal and connect it to GND.**
3. **Connect the data bus line and control signal line between the μPD72291 and μPD70236A directly without an intermediate buffer, etc.**
4. **As the V53A and μPD72291 operate on the same clock, you should ensure that the V53A operating frequency does not exceed 16 MHz when a μPD72291 is connected.**

11.2 BUS CYCLES

This section describes co-processor-related bus cycles issued by the μPD70236A.

Bus cycles issued by the μPD70236A include co-processor- related bus cycles as well as those for memory or I/O accesses. Where data is to be transferred from and to is indicated by the bus status signals (M/$\overline{IO}$, R/$\overline{W}$, BUSST1, BUSST0). The relation between the bus status signals and bus cycles of μPD70236A is shown in Table 11-1.

Table 11-1 μPD70236A Bus Status Signals and Bus Cycles

M/$\overline{IO}$	R/$\overline{W}$	BUSST2	BUSST1	BUSST0	Bus Cycle	Data Transfer Direction
0	1	0	1	0	Co-processor read	COP → CPU
0	0				Co-processor write	CPU → COP
1	1				Co-processor memory read	Memory → COP
1	0				Co-processor memory write	COP → Memory

Remark COP: Co-processor

Caution **When executing the μPD72291 instructions, always place the memory operands at even addresses. Also specify the dynamic bus sizing as 16 bits. This is because the μPD72291 accesses 16-bit data in 1 bus cycle and therefore if the memory sized as 8 bits is specified as operand, a normal operation is not possible.**

(1) Co-processor read

This operation is used to read the status from the μPD72291 status word port (STWP). The address (A23 to A0) output by the μPD70236A has no meaning (the μPD70236A outputs 000008H). The data bus is driven by the μPD72291.

The bus cycle consists of 2 clock cycles.

(2) Co-processor write

This operation is used to write an instruction to the μPD72291 command word port (CMWP). The address (A23 to A0) output by the μPD70236A has no meaning (the μPD70236A outputs 000000H). The data bus is driven by the μPD70236A.

The bus cycle consists of 2 clock cycles.

(3) Co-processor memory read

This operation is used to transfer memory data to the μPD72291 source operand word port (SOPWP). The address (A23 to A0) output by the μPD70236A is the memory address. The data bus is driven by the memory.

The bus cycle consists of 3 clock cycles (the μPD70236A automatically extends the bus cycle by one clock cycle).

(4) Co-processor memory write

This operation is used to transfer an operation result to memory from the μPD72291 destination operand word port (DOPWP). The address (A23 to A0) output by the μPD70236A is the memory address. The data bus is driven by the μPD72291, not the μPD70236A.

The bus cycle consists of 3 clock cycles (the μPD70236A automatically extends the bus cycle by one clock cycle).

Remark STWP, CMWP, SOPWP, and DOPWP are on-chip μPD72291 ports.

12. RESET FUNCTION

The μPD70236A is reset when the $\overline{\text{RESET}}$ pin is input low at least 6 clock cycles before being returned to the high level.

12.1 CPU RESET OPERATION

When the CPU is reset, it is initialized as shown in Table 12-1, and instruction prefetching begins at address FFFF0H.

Table 12-1 CPU Reset

Target	Initial Value	Remarks
PFP	0000H	Start address: FFFF0H
PC	0000H	
PS	FFFFH	
SS	0000H	
DS0	0000H	
DS1	0000H	
PSW	Upper: 1 1 1 1 V=0 DIR=0 IE=0 BRK=0 Lower: S=0 Z=0 0 AC=0 0 P=0 0 CY=0	
Queue	Cleared	
XAM	7 6 5 4 3 2 1 0 — — — — — — — 0	XA flag: Normal address mode
PGR1 to PGR64	15 14 13 12 11 10 9 8 — — — — — — x x 7 6 5 4 3 2 1 0 x x x x x x x x	Page register: Undefined

Remark x: Retains state prior to reset.

12.2 ON-CHIP I/O RESET OPERATION

Some on-chip I/Os are also initialized by a reset: These are listed in Table 12-2. I/Os not listed in this table retain their pre-reset status, but their status is undefined after powering on.

Table 12-2 On-Chip I/O Reset (1/3)

(a) System I/O Area (1/2)

Target	Initial Value	Remarks
SCTL	7 6 5 4 3 2 1 0 — — — 0 0 0 0 0	• 16-bit boundary • μPD71071 mode selection • No carry is transferred to A16 in the μPD71037 mode • No carry is transferred to A20 in the μPD71037 mode • SCU input clock : TOUT1
OPSEL	7 6 5 4 3 2 1 0 — — — — 0 0 0 0	DMAU, ICU, TCU and SCU cannot be used
WCY0	7 6 5 4 3 2 1 0 — — — — — 1 1 1	Wait insertion when accessing upper memory block in 16M bytes : 7 waits
WCY1	7 6 5 4 3 2 1 0 — 1 1 1 — 1 1 1	Wait insertion when accessing middle and lower memory blocks in 16M bytes : 7 waits
WCY2	7 6 5 4 3 2 1 0 — 1 1 1 — 1 1 1	Wait insertion when accessing middle and lower memory blocks in 1M bytes : 7 waits
WCY3	7 6 5 4 3 2 1 0 — 1 1 1 — 1 1 1	• Wait insertion in external I/O access and interrupt acknowledge cycle : 7 waits • Wait insertion when accessing upper memory block in 1M bytes : 7 waits
WCY4	7 6 5 4 3 2 1 0 — 1 1 1 — 1 1 1	• Wait insertion in DMA cycle: 7 waits • Wait insertion in refresh cycle : 7 waits
WMB0	7 6 5 4 3 2 1 0 — 1 1 1 — 1 1 1	Size of upper and lower memory blocks in 16M-byte memory space : 8M bytes
WMB1	7 6 5 4 3 2 1 0 — 1 1 1 — 1 1 1	Size of upper and lower memory blocks in 1M-byte memory space : 512K bytes
WAC	7 6 5 4 3 2 1 0 — — — — 0 0 0 0	Address high-order 4 bits in 1M-byte memory area 16M-byte space : 0000

Table 12-2 On-Chip I/O Reset (2/3)

(a) System I/O Area (2/2)

Target	Initial Value	Remarks
TCKS	7 6 5 4 3 2 1 0 — — — 0 0 0 0 0	TCU clocks TCT#0 to TCT#2 are internal clocks of oscillator frequency divided by 4.
RFC	7 6 5 4 3 2 1 0 x 0 — 0 1 0 0 0	• Refresh enabled/disabled : undefined • Timer factor (N) = 9 • Increments refresh address by 2 • $\overline{UBE}$: low-level output
SBCR	7 6 5 4 3 2 1 0 — — — 0 0 0 0 0	• System enters HALT mode by execution of HALT instruction. • Oscillation stabilization time = 2^{18}/fxx • Internal clock frequency fx = fxx x 1/2
BRC	7 6 5 4 3 2 1 0 0 0 0 0 0 0 0 0	BRC set value = 2

(b) SCU

Target	Initial Value	Remarks
SMD	7 6 5 4 3 2 1 0 0 1 0 0 1 0 1 1	• Baud rate : x 64 • Character length : 7 bits • Parity: none • No. of stop bits : 1 bit
SCM	7 6 5 4 3 2 1 0 — — 0 0 0 0 0 0	• Send disabled • Receive disabled
SIMK	7 6 5 4 3 2 1 0 — — — — — — 1 1	• RBRDY interrupt : mask • TBRDY interrupt : mask
SST	7 6 5 4 3 2 1 0 x 0 0 0 0 1 0 0	• Send data buffer status : Non-Ready • Receive data buffer status : Non-Ready • Error : none • Break detection : none

Remarks x: Retains state prior to reset.
fxx: Oscillator frequency

Table 12-2 On-Chip I/O Reset (3/3)

(c) DMAU

Target	Initial Value	Remarks
DCH	7 6 5 4 3 2 1 0 — — — 0 0 0 0 1	• DMA channel 0 selection • Access condition : current only (read) base & current (write)
DMD	7 6 5 4 3 2 1 0 0 0 0 0 0 0 — 0	• Demand mode, address increment • Auto initialize disabled • Verify transfer, byte transfer
DDC	[High-Order] 7 6 5 4 3 2 1 0 — — — — — — 0 0	• Bus release mode • Wait state disabled in verify operation
	[Low-Order] 7 6 5 4 3 2 1 0 — — 0 0 — 0 — —	• DMA operation : enabled • Channel priority : fixed (CH0 > ... >CH3) • Write timing : normal write timing
DST	7 6 5 4 3 2 1 0 0 0 0 0 0 0 0 0	• Transfer end : no end • DMA request status : no request
DMK	7 6 5 4 3 2 1 0 — — — — 1 1 1 1	Entire channel DMA request mask

13. STANDBY FUNCTIONS

The μPD70236A is provided with two standby functions: Standby during program standby resulting from a HALT instruction, and standby during program execution resulting from switching the instruction cycle time.

13.1 FEATURES

(1) HALT mode

Execution of the HALT instruction stops the clock supplied to the CPU (except the HALT mode release circuit)

(2) STOP mode

Execution of the HALT instruction stops all clocks supplied to the CPU and internal I/Os.

The STOP mode should be used when a resonator is connected to the X1 and X2 pins.

(3) Variable instruction cycle time function

The internal system clock frequency can be specified as 1/2, 1/4, 1/8 or 1/16 of the oscillator frequency.

13.2 SBCR (STANDBY CONTROL REGISTER)

The μPD70236A's standby functions are controlled by the SBCR register in the system I/O area.

Fig. 13-1 SBCR (Standby Control Register)

I/O Address		7	6	5	4	3	2	1	0
FFF1H	SBCR	—	—	—	CLKC		WT		STOP

STOP	HALT Mode/STOP Mode Switchover
0	HALT mode entered by execution of HALT instruction
1	STOP mode entered by execution of HALT instruction

WT	Oscillation Stabilization Time Specification		
		fxx = 40 MHz	fxx = 32 MHz
00	Oscillation stabilization time = 2^{18}/fxx	6.55 ms	8.19 ms
01	Oscillation stabilization time = 2^{17}/fxx	3.27 ms	4.09 ms
10	Oscillation stabilization time = 2^{16}/fxx	1.63 ms	2.04 ms
11	Oscillation stabilization time = 2^{15}/fxx	0.81 ms	1.02 ms

CLKC	System Clock Frequency (fx) Specification
00	fx = fxx x 1/2
01	fx = fxx x 1/4
10	fx = fxx x 1/8
11	fx = fxx x 1/16

Remark fxx is the oscillator frequency.

14. INSTRUCTION SET

Table 14-1 Operand Types Legend

Identifier	Description
reg, reg'	8-/16-bit general register
reg8, reg8'	8-bit general register
reg16, reg16'	16-bit general register
dmem	8-/16-bit memory location
mem	8-/16-bit memory location
mem8	8-bit memory location
mem16	16-bit memory location
mem32	32-bit memory location
imm	Constant in range 0 to FFFFH
imm3	Constant in range 0 to 7
imm4	Constant in range 0 to FH
imm8	Constant in range 0 to FFH
imm16	Constant in range 0 to FFFFH
acc	AW or AL register
sreg	Segment register
src-table	Name of 256-byte conversion table
src-block	Name of block addressed by IX register
dst-block	Name of block addressed by IY register
near-proc	Procedure in current program segment
far-proc	Procedure in different program segment
near-label	Label in current program segment
short-label	Label in range -128 to +127 bytes from end of instruction
far-label	Label in different program segment
memptr16	Word containing offset of location in current program segment to which control is to be transferred
memptr32	Doubleword containing offset and segment base address of location in different program segment to which control is to be transferred
regptr16	16-bit general register containing offset of location in different program segment to which control is to be transferred
pop-value	Number of bytes to be removed from stack (0 to 64K, normally an even number)
fp-op	Immediate value for discrimination of external floating-point operation coprocessor operation code
R	Register set

Table 14-2 Operation Codes Legend

Identifier	Description
W	Byte/word specify bit (0: byte; 1: word). However, when s=1, the sign extension byte data becomes a 16-bit operand even when W=1
reg	Register field (000 to 111)
reg'	Register field (000 to 111) (Source-side register in instructions using two registers)
mem	Memory field (000 to 111)
mod	Mode field (00 to 10)
s	Sign extension specify bit (0: no sign extension, 1: sign extension)
X,XXX,YYY,ZZZ	Data for discrimination of external floating-point coprocessor, operation code

Table 14-3 Operand Description Legend

Identifier	Description
AW	Accumulator (16 bits)
AH	Accumulator (upper byte)
AL	Accumulator (lower byte)
BW	Register BW (16 bits)
CW	Register CW (16 bits)
CL	Register CW (lower byte)
DW	Register DW (16 bits)
BP	Base pointer (16 bits)
SP	Stack pointer (16 bits)
PC	Program counter (16 bits)
PSW	Program status word (16 bits)
IX	Index register (source) (16 bits)
IY	Index register (destination) (16 bits)
PS	Program segment register (16 bits)
SS	Stack segment register (16 bits)
DS0	Data segment 0 register (16 bits)
DS1	Data segment 1 register (16 bits)
AC	Auxiliary carry flag
CY	Carry flag
P	Parity flag
S	Sign flag
Z	Zero flag
DIR	Direction flag
IE	Interrupt enable flag
V	Overflow flag
BRK	Break flag
(...)	Contents of memory shown in ( )
disp	Displacement (8/16 bits)
ext-disp8	16 bits comprising sign extension on 8-bit displacement
temp	Temporary register (8/16/32 bits)
temp 1, 2	Temporary register (16 bits)
TA	Temporary register A (16 bits)
TB	Temporary register B (16 bits)
TC	Temporary register C (16 bits)
tmpcy	Temporary carry flag (1 bit)
seg	Immediate segment data (16 bits)
offset	Immediate offset data (16 bits)
←	Transfer direction
+	Addition
−	Subtraction
x	Multiplication
÷	Division
%	Modulo
∧	Logical product
∨	Logical sum
∀	Exclusive logical sum
xxH	2-digit hexadecimal number
xxxxH	4-digit hexadecimal number

Table 14-4 Flag Operation Legend

Identifier	Description
(Blank)	Not affected
0	Cleared to 0
1	Set to 1
x	Set or cleared depending upon result
U	Undefined
R	Previously saved value is restored

Table 14-5 Memory Addressing

mem \ mod	00	01	10
000	BW + IX	BW + IX + disp 8	BW + IX + disp 16
001	BW + IY	BW + IY + disp 8	BW + IY + disp 16
010	BP + IX	BP + IX + disp 8	BP + IX + disp 16
011	BP + IY	BP + IY + disp 8	BP + IY + disp 16
100	IX	IX + disp 8	IX + disp 16
101	IY	IY + disp 8	IY + disp 16
110	DIRECT ADDRESS	BP + disp 8	BP + disp 16
111	BW	BW + disp 8	BW + disp 16

Table 14-6 8/16-Bit General Register Selection

reg, reg'	W=0	W=1
000	AL	AW
001	CL	CW
010	DL	DW
011	BL	BW
100	AH	SP
101	CH	BP
110	DH	IX
111	BH	IY

Table 14-7 Segment Register Selection

sreg	
00	DS1
01	PS
10	SS
11	DS0

The instruction set is shown in tabular form in the following pages.

The number of clocks (cycles) indicated in the table represent the time required by the execution unit for executing instructions, and are based on the following conditions.

- The prefetch time, pre-decode time, and wait time to use the bus are not included.
- Memory access presumes a 0 wait period. In other words, one bus cycle corresponds to two clocks.
- I/O access presumes a 0 wait period.
- Primitive block transfer instructions and primitive I/O instructions include a repeat prefix.
- The number of clocks is for when 16 bits are specified with the bus sizing function. To specify 8 bits, set the bus cycle of word data for even addresses to twice the number of clocks.
- The values indicated are for the normal address mode.

The number of clocks of instructions with byte or word processing (instructions having W bit) is indicated in the following manner.

Left of slash (/): Value for byte processing (W = 0), or for word processing (W = 1) of even address.
Right of slash (/): Value for word processing of odd address (W = 1).

For the number of clocks for executing block transfer-related instructions, see **Table 14-8.**

* **Table 14-8 Number of Clock Cycles of Block Transfer-Related Instructions**

Instruction	Number of Clock Cycles			
	Byte Processing (W = 0)	Word Processing (W = 1)		
		Odd, Odd Address	Even, Even Address	Odd, Even Address
MOVBK	6 / rep (6)	10 / rep (10)	6 / rep (6)	8 / rep (8)
CMPBK	12 / rep – 1 (11)	16 / rep – 1 (15)	12 / rep – 1 (11)	14 / rep – 1 (13)
CMPM	10 / rep – 1 (9)	12 / rep – 1 (11)	10 / rep – 1 (9)	——
LDM	3 / rep + 2 (5)	5 / rep + 2 (7)	3 / rep + 2 (5)	——
STM	3 / rep (3)	5 / rep (5)	3 / rep (3)	——
INM	8 / rep (8)	14 / rep (14)	8 / rep (8)	Odd I/O address : 12 / rep (12) Odd memory address : 10 / rep (10)
OUTM	8 / rep – 2 (6)	14 / rep – 2 (12)	8 / rep – 2 (6)	Odd I/O address : 12 / rep – 2 (10) Odd memory address : 10 / rep – 2 (8)

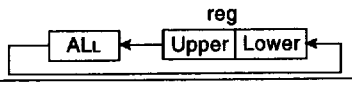
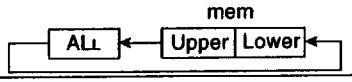
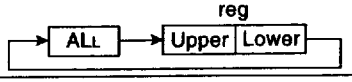
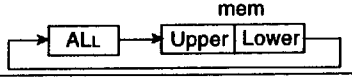
Remarks 1. Figure in parentheses apply to one-time only processing.
2. "/rep" indicates the number of repetitions. One execution is equivalent to one repetition.

Instruction Group	Mnemonic	Operand(s)	Operation Code 76543210	Operation Code 76543210	Bytes	Clock Cycles	Operation	Flags AC	CY	V	P	S	Z
Data transfer instructions	MOV	reg, reg'	1000101W	11 reg reg'	2	2	reg ← reg'						
		mem, reg	1000100W	mod reg mem	2-4	3/5	(mem) ← reg						
		reg, mem	1000101W	mod reg mem	2-4	5/7	reg ← (mem)						
		mem, imm	1100011W	mod 000 mem	3-6	3/5	(mem) ← imm						
		reg, imm	1011W reg		2-3	2	reg ← imm						
		acc, dmem	1010000W		3	5/7	If W=0: AL ← (dmem) If W=1: AH ← (dmem + 1), AL ← (dmem)						
		dmem, acc	1010001W		3	3/5	If W=0: (dmem) ←AL If W=1: (dmem + 1) ← AH, (dmem) ←AL						
		sreg, reg16	10001110	110 sreg reg	2	2	sreg ← reg16 sreg:SS, DS0, DS1						
		sreg, mem16	10001110	mod0 sreg mem	2-4	5/7	sreg ← (mem16) sreg:SS, DS0, DS1						
		reg16, sreg	10001100	110 sreg reg	2	2	reg16 ← sreg						
		mem16, sreg	10001100	mod0 sreg mem	2-4	3/5	(mem16) ← sreg						
		DS0, reg16, mem32	11000101	mod reg mem	2-4	10/14	reg16← (mem32) DS0 ← (mem32 + 2)						
		DS1, reg16, mem32	11000100	mod reg mem	2-4	10/14	reg16 ← (mem32) DS1 ← (mem32 + 2)						
		AH, PSW	10011111		1	2	AH ← S, Z, x, AC, x, P, x, CY						
		PSW, AH	10011110		1	2	S, Z, x, AC, x, P, x, CY← AH	x	x		x	x	x
	LDEA	reg16, mem16	10001101	mod reg mem	2-4	2	reg16 ←mem16						
	TRANS	src-table	11010111		1	5	AL← (BW + AL)						
	XCH	reg, reg'	1000011W	11 reg reg'	2	3	reg ↔ reg'						
		mem, reg reg, mem	1000011W	mod reg mem	2-4	8/12	(mem) ↔ reg						
		AW, reg16 reg16, AW	10010 reg		1	3	AW ↔ reg16						

Instruction Group	Mnemonic	Operand(s)	Operation Code 76543210	Operation Code 76543210	Bytes	Clock Cycles	Operation	Flags AC	CY	V	P	S	Z
Repeat prefixes	REPC		01100101		1	2	While CW ≠ 0, the following byte primitive block transfer instruction is executed and CW is decremented (–1). If there is a pending interrupt, it is serviced. If CY ≠ 1 the loop is exited.						
	REPNC		01100100		1	2	Same as above If CY ≠ 0 the loop is exited.						
	REP REPE REPZ		11110011		1	2	While CW ≠ 0, the following byte primitive block transfer instruction is executed and CW is decremented (–1). If there is a pending interrupt, it is serviced. If the primitive block transfer instruction is CMPBK or CMPM and Z ≠ 1 the loop is exited.						
	REPNE REPNZ		11110010		1	2	Same as above If Z ≠ 0 the loop is exited.						
Primitive block transfer instructions	MOVBK	dst-block, src-block	1010010W		1	See Table14-8	If W = 0: (IY) ← (IX) DIR = 0 : IX ← IX + 1, IY ← IY + 1 DIR = 1 : IX ← IX – 1, IY ← IY – 1 If W = 1: (IY + 1, IY) ← (IX + 1, IX) DIR = 0 : IX ← IX + 2, IY ← IY + 2 DIR = 1 : IX ← IX – 2, IY ← IY – 2						
	CMPBK	src-block, dst-block	1010011W		1	See Table14-8	If W = 0: (IX) – (IY) DIR = 0 : IX ← IX + 1, IY ← IY + 1 DIR = 1 : IX ← IX – 1, IY ← IY – 1 If W = 1: (IX + 1, IX) – (IY + 1, IY) DIR = 0 : IX ← IX + 2, IY ← IY + 2 DIR = 1 : IX ← IX – 2, IY ← IY – 2	x	x	x	x	x	x
	CMPM	dst-block	1010111W		1	See Table14-8	If W = 0: AL – (IY) DIR = 0 : IY ← IY + 1; DIR = 1 : IY ← IY – 1 If W = 1: AW – (IY + 1, IY) DIR = 0 : IY ← IY + 2; DIR = 1 : IY ← IY – 2	x	x	x	x	x	x
	LDM	src-block	1010110W		1	See Table14-8	If W = 0: AL ← (IX) DIR = 0 : IX ← IX + 1; DIR = 1 : IX ← IX – 1 If W = 1: AW ← (IX + 1, IX) DIR = 0 : IX + 2; DIR = 1 : IX ← IX – 2						
	STM	dst-block	1010101W		1	See Table14-8	If W = 0: (IY) ← AL DIR = 0 : IY ← IY + 1; DIR = 1 : IY ← IY – 1 If W = 1: (IY + 1, IY) ← AW DIR = 0 : IY ← IY + 2; DIR = 1 : IY ← IY – 2						

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles	Operation	Flags					
			76543210	76543210				AC	CY	V	P	S	Z
Bit field manipulation instructions	INS	reg8, reg8	00001111	00110001	3	37-69 /39-77	16-bit field ← AW						
			11 reg' reg										
		reg8, imm4	00001111	00111001	4	37-69 /39-77	16-bit field ← AW						
			11000 reg										
	EXT	reg8, reg8	00001111	00110011	3	29-61 /33-63	AW ← 16-bit field						
			11 reg' reg										
		reg8, imm4	00001111	00111011	4	29-61 /33-63	AW ← 16-bit field						
			11000 reg										
Input/output instructions	IN	acc, imm8	1110010W		2	5/7	If W = 0: AL ← (imm8) If W = 1: AH ← (imm8 + 1), AL ← (imm8)						
		acc, DW	1110110W		1	5/7	If W = 0: AL ← (DW) If W = 1: AH ← (DW + 1), AL ← (DW)						
	OUT	imm8, acc	1110011W		2	3/5	If W = 0: (imm8) ← AL If W = 1: (imm8 + 1) ← AH, (imm8) ← AL						
		DW, acc	1110111W		1	3/5	If W = 0: (DW) ← AL If W = 1: (DW + 1) ← AH, (DW) ← AL						
Primitive input/output instructions	INM	dst-block, DW	0110110W		1	See Table 14-8	If W = 0: (IY) ← (DW) DIR = 0 : IY ← IY + 1 ; DIR = 1 : IY ← IY − 1 If W = 1: (IY + 1, IY) ← (DW + 1, DW) DIR = 0 : IY ← IY + 2 ; DIR = 1 : IY ← IY − 2						
	OUTM	DW, src-block	0110111W		1	See Table 14-8	If W = 0: (DW) ← (IX) DIR = 0 : IX ← IX + 1 ; DIR = 1 : IX ← IX − 1 If W = 1: (DW + 1, DW) ← (IX + 1, IX) DIR = 0 : IX ← IX + 2 ; DIR = 1 : IX ← IX − 2						

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles	Operation	Flags					
			76543210	76543210				AC	CY	V	P	S	Z
Addition/subtraction instructions	ADD	reg, reg'	0000000 1 W	11 reg reg'	2	2	reg ← reg + reg'	x	x	x	x	x	x
		mem, reg	0000000 0 W	mod reg mem	2-4	7/11	(mem) ← (mem) + reg	x	x	x	x	x	x
		reg, mem	0000000 1 W	mod reg mem	2-4	6/8	reg ← reg + (mem)	x	x	x	x	x	x
		reg, imm	100000 s W	11000 reg	3-4	2	reg ← reg + imm	x	x	x	x	x	x
		mem, imm	100000 s W	mod000 mem	3-6	7/11	(mem) ← (mem) + imm	x	x	x	x	x	x
		acc, imm	0000010 W		2-3	2	If W = 0: AL ← AL + imm If W = 1: AW ← AW + imm	x	x	x	x	x	x
	ADDC	reg, reg'	0001001 W	11 reg reg'	2	2	reg ← reg + reg'+ CY	x	x	x	x	x	x
		mem, reg	0001000 W	mod reg mem	2-4	7/11	(mem) ← (mem) + reg + CY	x	x	x	x	x	x
		reg, mem	0001001 W	mod reg mem	2-4	6/8	reg ← reg + (mem) + CY	x	x	x	x	x	x
		reg, imm	100000 s W	11010 reg	3-4	2	reg ← reg + imm + CY	x	x	x	x	x	x
		mem, imm	100000 s W	mod010 mem	3-6	7/11	(mem) ← (mem) + imm + CY	x	x	x	x	x	x
		acc, imm	0001010 W		2-3	2	If W = 0: AL ← AL + imm + CY If W = 1: AW ← AW + imm + CY	x	x	x	x	x	x
	SUB	reg, reg'	0010101 W	11 reg reg'	2	2	reg ← reg – reg'	x	x	x	x	x	x
		mem, reg	0010100 W	mod reg mem	2-4	7/11	(mem) ← (mem) – reg	x	x	x	x	x	x
		reg, mem	0010101 W	mod reg mem	2-4	6/8	reg ← reg – (mem)	x	x	x	x	x	x
		reg, imm	100000 s W	11101 reg	3-4	2	reg ← reg – imm	x	x	x	x	x	x
		mem, imm	100000 s W	mod101 mem	3-6	7/11	(mem) ← (mem) – imm	x	x	x	x	x	x
		acc, imm	0010110 W		2-3	2	If W = 0: AL ← AL – imm If W = 1: AW ← AW – imm	x	x	x	x	x	x
	SUBC	reg, reg'	0001101 W	11 reg reg'	2	2	reg ← reg – reg'– CY	x	x	x	x	x	x
		mem, reg	0001100 W	mod reg mem	2-4	7/11	(mem) ← (mem) – reg – CY	x	x	x	x	x	x
		reg, mem	0001101 W	mod reg mem	2-4	6/8	reg ← reg – (mem) – CY	x	x	x	x	x	x
		reg, imm	100000 s W	11011 reg	3-4	2	reg ← reg – imm – CY	x	x	x	x	x	x
		mem, imm	100000 s W	mod011 mem	3-6	7/11	(mem) ← (mem) – imm – CY	x	x	x	x	x	x
		acc, imm	0001110 W		2-3	2	If W = 0: AL ← AL – imm – CY If W = 1: AW ← AW – imm– CY	x	x	x	x	x	x

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles	Operation	Flags					
			76543210	76543210				AC	CY	V	P	S	Z
BCD operation instructions	ADD4S		00001111	00100000	2	18 x n + 2	dst BCD string ← dst BCD string + src BCD string[Note]	U	x	U	U	U	x
	SUB4S		00001111	00100010	2	18 x n + 2	dst BCD string ← dst BCD string – src BCD string[Note]	U	x	U	U	U	x
	CMP4S		00001111	00100110	2	14 x n + 2	dst BCD string – src BCD string[Note]	U	x	U	U	U	x
	ROL4	reg8	00001111 11000 reg	00101000	3	9							
		mem8	00001111 mod000 mem	00101000	3-5	15							
	ROR4	reg8	00001111 11000 reg	00101010	3	13							
		mem8	00001111 mod000 mem	00101010	3-5	19							
Increment/decrement instructions	INC	reg8	11111110	11000 reg	2	2	reg8 ← reg8 + 1	x		x	x	x	x
		mem	1111111W	mod000 mem	2-4	7/11	(mem) ← (mem) + 1	x		x	x	x	x
		reg16	01000 reg		1	2	reg16 ← reg16 + 1	x		x	x	x	x
	DEC	reg8	11111110	11001 reg	2	2	reg8 ← reg8 – 1	x		x	x	x	x
		mem	1111111W	mod001 mem	2-4	7/11	(mem) ← (mem) – 1	x		x	x	x	x
		reg16	01001 reg		1	2	reg16 ← reg16 – 1	x		x	x	x	x

Remark n is half the number of BCD digits.

Note The number of BCD digits is given by the CL register: a value between 1 and 254 can be set.

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles	Operation	Flags					
			76543210	76543210				AC	CY	V	P	S	Z
Multiplication instructions	MULU	reg8	11110110	11100 reg	2	8	AW ← AL x reg8 AH = 0: CY ← 0, V ← 0 AH ≠ 0: CY ← 1, V ← 1	U	x	x	U	U	U
		mem8	11110110	mod100 mem	2-4	12	AW ← AL x (mem8) AH = 0: CY ← 0, V ← 0 AH ≠ 0: CY ← 1, V ← 1	U	x	x	U	U	U
		reg16	11110111	11100 reg	2	12	DW, AW ← AW x reg16 DW = 0: CY ← 0, V ← 0 DW ≠ 1: CY ← 1, V ← 1	U	x	x	U	U	U
		mem16	11110111	mod100 mem	2-4	16/18	DW, AW ← AW x (mem16) DW = 0: CY ← 0, V ← 0 DW ≠ 1: CY ←1, V ← 1	U	x	x	U	U	U
	MUL	reg8	11110110	11101 reg	2	8	AW ←AL x reg8 AH = AL sign extension: CY ← 0, V ← 0 AH ≠ AL sign extension: CY ← 1, V ← 1	U	x	x	U	U	U
		mem8	11110110	mod101 mem	2-4	12	AW ← AL x (mem8) AH = AL sign extension: CY ← 0, V ← 0 AH ≠ AL sign extension: CY ← 1, V ← 1	U	x	x	U	U	U
		reg16	11110111	11101 reg	2	12	DW, AW ← AW x reg16 DW = AW sign extension: CY ← 0, V ← 0 DW ≠ AW sign extension: CY ← 1, V ← 1	U	x	x	U	U	U
		mem16	11110111	mod101 mem	2-4	16/18	DW, AW ← AW x (mem16) DW = AW sign extension: CY ← 0, V ← 0 DW ≠ AW sign extension: CY ← 1, V ← 1	U	x	x	U	U	U
		reg16, (reg16',)[Note] imm8	01101011	11 reg reg'	3	12	reg16 ← reg16' x imm8 Product ≤ 16 bits : CY ← 0, V ← 0 Product > 16 bits : CY ← 1, V ← 1	U	x	x	U	U	U
		reg16, mem16, imm8	01101011	mod reg mem	3-5	16/18	reg16 ← (mem16) x imm8 Product ≤ 16 bits : CY ← 0, V ← 0 Product > 16 bits : CY ← 1, V ← 1	U	x	x	U	U	U
		reg16, (reg16',)[Note] imm16	01101001	11 reg reg'	4	12	reg16 ← reg16' x imm16 Product ≤ 16 bits : CY ← 0, V ← 0 Product > 16 bits : CY ← 1, V ← 1	U	x	x	U	U	U
		reg16, mem16, imm16	01101001	mod reg mem	4-6	16/18	reg16 ← (mem16) x imm16 Product ≤ 16 bits : CY ← 0, V ← 0 Product > 16 bits : CY ← 1, V ← 1	U	x	x	U	U	U

Note The 2nd operand can be omitted, in which case the same register as the 1st operand is taken as being specified.

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles	Operation	Flags					
			76543210	76543210				AC	CY	V	P	S	Z
Unsigned division instructions	DIVU	reg8	11110110	11110 reg	2	11	temp ← AW If temp ÷ reg8 ≤ FFH AH ← temp%reg8, AL ←temp ÷ reg8 If temp ÷ reg8 > FFH TA ← (001H, 000H), TC ← (003H, 002H) SP ← SP – 2, (SP + 1, SP) ← PSW, IE ← 0, BRK ← 0 SP ← SP – 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP – 2, (SP + 1, SP) ← PC[Note], PC ← TA	U	U	U	U	U	U
		mem8	11110110	mod110 mem	2-4	15	temp ← AW If temp ÷ (mem8) ≤ FFH AH ← temp%(mem8), AL ←temp ÷ (mem8) If temp ÷ (mem8) > FFH TA ← (001H, 000H), TC ← (003H, 002H) SP ← SP – 2, (SP + 1, SP) ← PSW, IE ← 0, BRK ← 0 SP ← SP – 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP – 2, (SP + 1, SP) ← PC[Note], PC ← TA	U	U	U	U	U	U
		reg16	11110111	11110 reg	2	19	temp ← DW, AW If temp ÷ reg16 ≤ FFFFH DW ← temp%reg16, AW ←temp ÷ reg16 If temp ÷ reg16 > FFFFH TA ← (001H, 000H), TC ← (003H, 002H) SP ← SP – 2, (SP + 1, SP) ← PSW, IE ← 0, BRK ← 0 SP ← SP – 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP – 2, (SP + 1, SP) ← PC[Note], PC ← TA	U	U	U	U	U	U
		mem16	11110111	mod110 mem	2-4	23/25	temp ← DW, AW If temp ÷ (mem16) ≤ FFFFH DW ← temp%(mem16), AW ←temp ÷ (mem16) If temp ÷ (mem16) > FFFFH TA ← (001H, 000H), TC ← (003H, 002H) SP ← SP – 2, (SP + 1, SP) ← PSW, IE ← 0, BRK ← 0 SP ← SP – 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP – 2, (SP + 1, SP) ← PC[Note], PC ← TA	U	U	U	U	U	U

Note Start address of DIVU instruction

Instruction Group	Mnemonic	Operand(s)	Operation Code 7 6 5 4 3 2 1 0	Operation Code 7 6 5 4 3 2 1 0	Bytes	Clock Cycles	Operation	Flags AC	CY	V	P	S	Z
Signed division instructions	DIV	reg8	1 1 1 1 0 1 1 0	1 1 1 1 1 reg	2	17	temp ← AW If temp + reg8 > 0 and temp + reg8 ≤ 7FH or temp + reg8 < 0 and temp + reg8 > 0 – 7FH –1 AH ← temp%reg8, AL ← temp + reg8 If temp + reg8 > 0 and temp + reg8 > 7FH or temp + reg8 < 0 and temp + reg8 ≤ 0 – 7FH –1 TA ← (001H, 000H), TC ← (003H, 002H) SP ← SP – 2, (SP + 1, SP) ← PSW, IE ← 0, BRK ← 0 SP ← SP – 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP – 2, (SP + 1, SP) ← PC[Note], PC ← TA	U	U	U	U	U	U
		mem8	1 1 1 1 0 1 1 0	mod 1 1 1 mem	2-4	20	temp ← AW If temp + (mem8) > 0 and temp + (mem8) ≤ 7FH or temp + (mem8) < 0 and temp + (mem8) > 0 – 7FH –1 AH ← temp%(mem8), AL ← temp +(mem8) If temp + (mem8) > 0 and temp + (mem8) > 7FH or temp + (mem8) < 0 and temp + (mem8) ≤ 0 – 7FH –1 TA ← (001H, 000H), TC ← (003H, 002H) SP ← SP – 2, (SP + 1, SP) ← PSW, IE ← 0, BRK ← 0 SP ← SP – 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP – 2, (SP + 1, SP) ← PC[Note], PC ← TA	U	U	U	U	U	U
		reg16	1 1 1 1 0 1 1 1	1 1 1 1 1 reg	2	24	temp ← DW, AW If temp + reg16 > 0 and temp + reg16 ≤ 7FFFH or temp + reg16 < 0 and temp + reg16 > 0 – 7FFFH –1 DW ← temp%reg16, AW ← temp + reg16 If temp + reg16 > 0 and temp + reg16 > 7FFFH or temp + reg16 < 0 and temp + reg16 ≤ 0 – 7FFFH –1 TA ← (001H, 000H), TC ← (003H, 002H) SP ← SP – 2, (SP + 1, SP) ← PSW, IE ← 0, BRK ← 0 SP ← SP – 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP – 2, (SP + 1, SP) ← PC[Note], PC ← TA	U	U	U	U	U	U
		mem16	1 1 1 1 0 1 1 1	mod 1 1 1 mem	2-4	28/30	temp ← DW, AW If temp + (mem16) > 0 and temp + (mem16) ≤ 7FFFH or temp + (mem16) < 0 and temp + (mem16) > 0 – 7FFFH –1 DW ← temp%(mem16), AW ← temp + (mem16) If temp + (mem16) > 0 and temp + (mem16) > 7FFFH or temp + (mem16) < 0 and temp + (mem16) ≤ 0 – 7FFFH –1 TA ← (001H, 000H), TC ← (003H, 002H) SP ← SP – 2, (SP + 1, SP) ← PSW, IE ← 0, BRK ← 0 SP ← SP – 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP – 2, (SP + 1, SP) ← PC[Note], PC ← TA	U	U	U	U	U	U

Note Start address of DIV instruction

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles	Operation	Flags					
			76543210	76543210				AC	CY	V	P	S	Z
BCD adjustment instructions	ADJBA		00110111		1	4	If AL ∧ 0FH > 9 or AC = 1: AL ← AL + 6 AH ← AH + 1, AC ← 1, CY ← AC, AL ← AL ∧ 0FH	x	x	U	U	U	U
	ADJ4A		00100111		1	2	If AL ∧ 0FH > 9 or AC = 1 AL ← AL + 6, AC ← 1 If AL > 9FH or CY = 1 AL ← AL + 60H, CY ← 1	x	x	U	x	x	x
	ADJBS		00111111		1	4	If AL ∧ 0FH > 9 or AC = 1 AL ← AL − 6, AH ← AH − 1 , AC← 1 CY ← AC, AL ← AL ∧ 0FH	x	x	U	U	U	U
	ADJ4S		00101111		1	2	If AL ∧ 0FH > 9 or AC = 1 AL ← AL − 6, AC ← 1 If AL > 9FH or CY = 1 AL ← AL − 60H, CY ← 1	x	x	U	x	x	x
Data conversion instructions	CVTBD		11010100	00001010	2	12	AH ← AL + 0AH, AL ← AL%0AH	U	U	U	x	x	x
	CVTDB		11010101	00001010	2	8	AL ← 0, AL ← AH × 0AH + AL	U	U	U	x	x	x
	CVTBW		10011000		1	2	If AL < 80H: AH ← 0, otherwise: AH ← FFH						
	CVTWL		10011001		1	2	If AW < 8000H: DW ← 0, otherwise: DW ← FFFFH						
Comparison instructions	CMP	reg, reg'	0011101W	11 reg reg'	2	2	reg − reg'	x	x	x	x	x	x
		mem, reg	0011100W	mod reg mem	2-4	6/8	(mem) − reg	x	x	x	x	x	x
		reg, mem	0011101W	mod reg mem	2-4	6/8	reg − (mem)	x	x	x	x	x	x
		reg, imm	100000sW	11111 reg	3-4	2	reg − imm	x	x	x	x	x	x
		mem, imm	100000sW	mod 111 mem	3-6	6/8	(mem) − imm	x	x	x	x	x	x
		acc, imm	0011110W		2-3	2	If W = 0: AL − imm If W = 1: AW − imm	x	x	x	x	x	x
Complement operation instructions	NOT	reg	1111011W	11010 reg	2	2	reg ← $\overline{\text{reg}}$						
		mem	1111011W	mod 010 mem	2-4	7/11	(mem) ← $\overline{(\text{mem})}$						
	NEG	reg	1111011W	11011 reg	2	2	reg ← $\overline{\text{reg}}$ + 1	x	x	x	x	x	x
		mem	1111011W	mod 011 mem	2-4	7/11	(mem) ← $\overline{(\text{mem})}$ + 1	x	x	x	x	x	x

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles	Operation	Flags					
			76543210	76543210				AC	CY	V	P	S	Z
Logical operation instructions	TEST	reg, reg'	1000010W	11 reg' reg	2	2	reg ∧ reg'	U	0	0	x	x	x
		mem, reg reg, mem	1000010W	mod reg mem	2-4	6/8	(mem) ∧ reg	U	0	0	x	x	x
		reg, imm	1111011W	11000 reg	3-4	2	reg ∧ imm	U	0	0	x	x	x
		mem, imm	1111011W	mod000 mem	3-6	6/8	(mem) ∧ imm	U	0	0	x	x	x
		acc, imm	1010100W		2-3	2	If W = 0: AL ∧ imm8 If W = 1: AW ∧ imm16	U	0	0	x	x	x
	AND	reg, reg'	0010001W	11 reg reg'	2	2	reg ← reg ∧ reg'	U	0	0	x	x	x
		mem, reg	0010000W	mod reg mem	2-4	7/11	(mem) ← (mem) ∧ reg	U	0	0	x	x	x
		reg, mem	0010001W	mod reg mem	2-4	6/8	reg ← reg ∧ (mem)	U	0	0	x	x	x
		reg, imm	1000000W	11100 reg	3-4	2	reg ← reg ∧ imm	U	0	0	x	x	x
		mem, imm	1000000W	mod100 mem	3-6	7/11	(mem) ← (mem) ∧ imm	U	0	0	x	x	x
		acc, imm	0010010W		2-3	2	If W = 0: AL ← AL ∧ imm8 If W = 1: AW ← AW ∧ imm16	U	0	0	x	x	x
	OR	reg, reg'	0000101W	11 reg reg'	2	2	reg ← reg ∨ reg'	U	0	0	x	x	x
		mem, reg	0000100W	mod reg mem	2-4	7/11	(mem) ← (mem) ∨ reg	U	0	0	x	x	x
		reg, mem	0000101W	mod reg mem	2-4	6/8	reg ← reg ∨ (mem)	U	0	0	x	x	x
		reg, imm	1000000W	11001 reg	3-4	2	reg ← reg ∨ imm	U	0	0	x	x	x
		mem, imm	1000000W	mod001 mem	3-6	7/11	(mem) ← (mem) ∨ imm	U	0	0	x	x	x
		acc, imm	0000110W		2-3	2	If W = 0: AL ← AL ∨ imm8 If W = 1: AW ← AW ∨ imm16	U	0	0	x	x	x
	XOR	reg, reg'	0011001W	11 reg reg'	2	2	reg ← reg ∀ reg'	U	0	0	x	x	x
		mem, reg	0011000W	mod reg mem	2-4	7/11	(mem) ← (mem) ∀ reg	U	0	0	x	x	x
		reg, mem	0011001W	mod reg mem	2-4	6/8	reg ← reg ∀ (mem)	U	0	0	x	x	x
		reg, imm	1000000W	11110 reg	3-4	2	reg ← reg ∀ imm	U	0	0	x	x	x
		mem, imm	1000000W	mod110 mem	3-6	7/11	(mem) ← (mem) ∀ imm	U	0	0	x	x	x
		acc, imm	0011010W		2-3	2	If W = 0: AL ← AL ∀ imm8 If W = 1: AW ← AW ∀ imm16	U	0	0	x	x	x

Instruction Group	Mnemonic	Operand(s)	Operation Code 76543210	Operation Code 76543210	Bytes	Clock Cycles	Operation	Flags AC	CY	V	P	S	Z
Bit manipulation instructions	TEST1	reg8, CL	00010000	11000 reg	3	4	reg8 bit NO.CL = 0 : Z ← 1 reg8 bit NO.CL = 1 : Z ← 0	U	0	0	U	U	x
		mem8, CL	0000	mod000 mem	3-5	8	(mem8) bit NO.CL = 0 : Z← 1 (mem8) bit NO.CL = 1 : Z← 0	U	0	0	U	U	x
		reg16, CL	0001	11000 mem	3	4	reg16 bit NO.CL = 0 : Z ← 1 reg16 bit NO.CL = 1 : Z ← 0	U	0	0	U	U	x
		mem16, CL	0001	mod000 mem	3-5	8/10	(mem16) bit NO.CL = 0 : Z← 1 (mem16) bit NO.CL = 1 : Z← 0	U	0	0	U	U	x
		reg8, imm3	1000	11000 reg	4	4	reg8 bit NO.imm3 = 0 : Z ← 1 reg8 bit NO.imm3 = 1 : Z ← 0	U	0	0	U	U	x
		mem8, imm3	1000	mod000 mem	4-6	8	(mem8) bit NO.imm3 = 0 : Z← 1 (mem8) bit NO.imm3 = 1 : Z← 0	U	0	0	U	U	x
		reg16, imm4	1001	11000 reg	4	4	reg16 bit NO.imm4 = 0 : Z ← 1 reg16 bit NO.imm4 = 1 : Z ← 0	U	0	0	U	U	x
		mem16, imm4	1001	mod000 mem	4-6	8/10	(mem16) bit NO.imm4 = 0 : Z← 1 (mem16) bit NO.imm4 = 1 : Z← 0	U	0	0	U	U	x
	NOT1	reg8, CL	0110	11000 reg	3	4	reg8 bit NO.CL← $\overline{\text{reg8 bit NO.CL}}$						
		mem8, CL	0110	mod000 mem	3-5	9	(mem8) bit NO.CL← $\overline{\text{(mem8) bit NO.CL}}$						
		reg16, CL	0111	11000 reg	3	4	reg16 bit NO.CL← $\overline{\text{reg16 bit NO.CL}}$						
		mem16, CL	0111	mod000 mem	3-5	9/13	(mem16) bit NO.CL← $\overline{\text{(mem16) bit NO.CL}}$						
		reg8, imm3	1110	11000 reg	4	4	reg8 bit NO.imm3← $\overline{\text{reg8 bit NO.imm3}}$						
		mem8, imm3	1110	mod000 mem	4-6	9	(mem8) bit NO.imm3← $\overline{\text{(mem8) bit NO.imm3}}$						
		reg16, imm4	1111	11000 reg	4	4	reg16 bit NO.imm4← $\overline{\text{reg16 bit NO.imm4}}$						
		mem16, imm4	1111	mod000 mem	4-6	9/13	(mem16) bit NO.imm4← $\overline{\text{(mem16) bit NO.imm4}}$						

2nd byte[Note] 3rd byte[Note]

Note 1st byte = 0FH

	NOT1	CY	11110101		1	2	CY← $\overline{\text{CY}}$		x				

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles	Operation	Flags					
			76543210	76543210				AC	CY	V	P	S	Z
Bit manipulation instructions	CLR1	reg8, CL	00010010	11000 reg	3	4	reg8 bit NO.CL ← 0						
		mem8, CL	0010	mod000 mem	3-5	9	(mem8) bit NO.CL ← 0						
		reg16, CL	0011	11000 mem	3	4	reg16 bit NO.CL ← 0						
		mem16, CL	0011	mod000 mem	3-5	9/13	(mem16) bit NO.CL ← 0						
		reg8, imm3	1010	11000 reg	4	4	reg8 bit NO.imm3 ← 0						
		mem8, imm3	1010	mod000 mem	4-6	9	(mem8) bit NO.imm3 ← 0						
		reg16, imm4	1011	11000 reg	4	4	reg16 bit NO.imm4 ← 0						
		mem16, imm4	1011	mod000 mem	4-6	9/13	(mem16) bit NO.imm4 ← 0						
	SET1	reg8, CL	0100	11000 reg	3	4	reg8 bit NO.CL ← 1						
		mem8, CL	0100	mod000 mem	3-5	9	(mem8) bit NO.CL ← 1						
		reg16, CL	0101	11000 reg	3	4	reg16 bit NO.CL ← 1						
		mem16, CL	0101	mod000 mem	3-5	9/13	(mem16) bit NO.CL ← 1						
		reg8, imm3	1100	11000 reg	4	4	reg8 bit NO.imm3 ← 1						
		mem8, imm3	1100	mod000 mem	4-6	9	(mem8) bit NO.imm3 ← 1						
		reg16, imm4	1101	11000 reg	4	4	reg16 bit NO.imm4 ← 1						
		mem16, imm4	1101	mod000 mem	4-6	9/13	(mem16) bit NO.imm4 ← 1						

2nd byte[Note] 3rd byte[Note]

Note 1st byte = 0FH

	CLR1	CY	11111000		1	2	CY ← 0		0				
		DIR	11111100		1	2	DIR ← 0						
	SET1	CY	11111001		1	2	CY ← 1		1				
		DIR	11111101		1	2	DIR ← 1						

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles	Operation	Flags					
			76543210	76543210				AC	CY	V	P	S	Z
Shift instructions	SHL	reg, 1	1101000W	11100 reg	2	2	CY ← reg MSB, reg ← reg x 2 If reg MSB ≠ CY: V ← 1 If reg MSB = CY: V ← 0	U	x	x	x	x	x
		mem, 1	1101000W	mod100 mem	2-4	7/11	CY ← (mem) MSB, (mem) ← (mem) x 2 If (mem) MSB ≠ CY: V ← 1 If (mem) MSB = CY: V ← 0	U	x	x	x	x	x
		reg, CL	1101001W	11100 reg	2	2 + n	temp ← CL, while temp ≠0 the following operation are repeated: CY ← reg MSB, reg ← reg x 2 temp ← temp – 1	U	x	U	x	x	x
		mem, CL	1101001W	mod100 mem	2-4	6/10 + n	temp ← CL, while temp ≠0 the following operation are repeated: CY ← (mem) MSB, (mem) ← (mem) x 2 temp ← temp – 1	U	x	U	x	x	x
		reg, imm8	1100000W	11100 reg	3	2 + n	temp ← imm8, while temp ≠ 0 the following operations are repeated: CY ← reg MSB, reg← reg x 2 temp ← temp – 1	U	x	U	x	x	x
		mem, imm8	1100000W	mod100 mem	3-5	6/10 + n	temp ← imm8, while temp ≠ 0 the following operations are repeated: CY ← (mem) MSB, (mem) ← (mem) x 2 temp ← temp – 1	U	x	U	x	x	x

Remark n indicates the shift number.

Instruction Group	Mnemonic	Operand(s)	Operation Code 76543210	Operation Code 76543210	Bytes	Clock Cycles	Operation	Flags AC	CY	V	P	S	Z
Shift instructions	SHR	reg, 1	1101000W	11101 reg	2	2	CY ← reg LSB, reg ← reg ÷ 2 If reg MSB ≠ bit after reg MSB : V ← 1 If reg MSB = bit after reg MSB : V ← 0	U	x	x	x	x	x
		mem, 1	1101000W	mod101 mem	2-4	7/11	CY ← (mem) LSB, (mem) ← (mem) ÷ 2 If (mem) MSB ≠ bit after (mem) MSB : V ← 1 If (mem) MSB = bit after (mem) MSB : V ← 0	U	x	x	x	x	x
		reg, CL	1101001W	11101 reg	2	2 + n	temp ← CL, while temp ≠ 0 the following operations are repeated: CY ← reg LSB, reg ← reg ÷ 2 temp ← temp − 1	U	x	U	x	x	x
		mem, CL	1101001W	mod101 mem	2-4	6/10 + n	temp ← CL, while temp ≠ 0 the following operations are repeated: CY ← (mem) LSB, (mem) ← (mem) ÷ 2 temp ← temp − 1	U	x	U	x	x	x
		reg, imm8	1100000W	11101 reg	3	2 + n	temp ← imm8, while temp ≠ 0 the following operations are repeated: CY ← reg LSB, reg ← reg ÷ 2 temp ← temp − 1	U	x	U	x	x	x
		mem, imm8	1100000W	mod101 mem	3-5	6/10 + n	temp ← imm8, while temp ≠ 0 the following operations are repeated: CY ← (mem) LSB,(mem) ← (mem) ÷ 2 temp ← temp − 1	U	x	U	x	x	x
	SHRA	reg, 1	1101000W	11111 reg	2	2	CY ← reg LSB, reg ← reg ÷ 2, V ← 0 MSB of operand is unchanged.	U	x	0	x	x	x
		mem, 1	1101000W	mod111 mem	2-4	7/11	CY ← (mem) LSB,(mem) ← (mem) ÷ 2, V ← 0 MSB of operand is unchanged.	U	x	0	x	x	x
		reg, CL	1101001W	11111 reg	2	2 + n	temp ← CL, while temp ≠ 0 the following operations are repeated: CY ← reg LSB, reg ← reg ÷ 2 temp ← temp − 1, MSB of operand is unchanged.	U	x	U	x	x	x
		mem, CL	1101001W	mod111 mem	2-4	6/10 + n	temp ← CL, while temp ≠ 0 the following operations are repeated: CY ← (mem) LSB, (mem) ← (mem) ÷ 2 temp ← temp − 1, MSB of operand is unchanged.	U	x	U	x	x	x
		reg, imm8	1100000W	11111 reg	3	2 + n	temp ← imm8, while temp ≠ 0 the following operations are repeated: CY ← reg LSB, reg ← reg ÷ 2 temp ← temp − 1, MSB of operand is unchanged.	U	x	U	x	x	x
		mem, imm8	1100000W	mod111 mem	3-5	6/10 + n	temp ← imm8, while temp ≠ 0 the following operations are repeated: CY ← (mem) LSB,(mem) ← (mem) ÷ 2 temp ← temp − 1, MSB of operand is unchanged.	U	x	U	x	x	x

Remark n indicates the shift number.

Instruction Group	Mnemonic	Operand(s)	Operation Code 76543210	Operation Code 76543210	Bytes	Clock Cycles	Operation	Flags AC	CY	V	P	S	Z
Rotate instructions	ROL	reg, 1	1101000W	11000 reg	2	2	CY ← reg MSB, reg ← reg x 2 + CY reg MSB ≠ CY : V ← 1 reg MSB = CY : V ← 0		x	x			
		mem, 1	1101000W	mod000 mem	2-4	7/11	CY ← (mem) MSB, (mem) ← (mem) × 2 + CY (mem) MSB ≠ CY : V ← 1 (mem) MSB = CY : V ← 0		x	x			
		reg, CL	1101001W	11000 reg	2	2 + n	temp ← CL, while temp ≠ 0 the following operations are repeated: CY ← reg MSB, reg ← reg x 2 + CY temp ← temp – 1		x	U			
		mem, CL	1101001W	mod000 mem	2-4	6/10 + n	temp ← CL, while temp ≠ 0 the following operations are repeated: CY ← (mem) MSB, (mem) ← (mem) x 2 + CY temp ← temp – 1		x	U			
		reg, imm8	1100000W	11000 reg	3	2 + n	temp ← imm8, while temp ≠ 0 the following operations are repeated: CY ← reg MSB, reg ← reg x 2 + CY temp ← temp – 1		x	U			
		mem, imm8	1100000W	mod000 mem	3-5	6/10 + n	temp ← imm8, while temp ≠ 0 the following operations are repeated: CY ← (mem) MSB, (mem) ← (mem) x 2 + CY temp ← temp – 1		x	U			
	ROR	reg, 1	1101000W	11001 reg	2	2	CY ← reg LSB, reg← reg + 2 reg MSB ← CY reg MSB ≠ bit after reg MSB : V ← 1 reg MSB = bit after reg MSB : V ← 0		x	x			
		mem, 1	1101000W	mod001 mem	2-4	7/11	CY ← (mem) LSB, (mem) ← (mem) + 2 (mem) MSB ← CY (mem) MSB ≠ bit after (mem) MSB : V ← 1 (mem) MSB = bit after (mem) MSB : V ← 0		x	x			
		reg, CL	1101001W	11001 reg	2	2 + n	temp ← CL, while temp ≠ 0 the following operations are repeated: CY ← reg LSB, reg ← reg + 2 reg MSB ← CY temp ← temp – 1		x	U			
		mem, CL	1101001W	mod001 mem	2-4	6/10 + n	temp ← CL, while temp ≠ 0 the following operations are repeated: CY ← (mem) LSB,(mem) ← (mem) + 2 (mem) MSB ← CY temp ← temp – 1		x	U			
		reg, imm8	1100000W	11001 reg	3	2 + n	temp ← imm8, while temp ≠ 0 the following operations are repeated: CY ← reg LSB,reg ← reg + 2 reg MSB ← CY temp ← temp – 1		x	U			
		mem, imm8	1100000W	mod001 mem	3-5	6/10 + n	temp ← imm8, while temp ≠ 0 the following operations are repeated: CY ← (mem) LSB,(mem) ← (mem) + 2 (mem) MSB ← CY temp ← temp – 1		x	U			

Remark n indicates the shift number.

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles	Operation	Flags					
			76543210	76543210				AC	CY	V	P	S	Z
Rotate instructions	ROLC	reg, 1	1101000W	11010 reg	2	2	tmpcy ← CY, CY ← reg MSB reg ← reg × 2 + tmpcy reg MSB ≠ CY : V ← 1 reg MSB = CY : V ← 0		x	x			
		mem, 1	1101000W	mod 010 mem	2-4	7/11	tmpcy ← CY, CY ← (mem) MSB (mem)← (mem) x 2 + tmpcy (mem) MSB ≠ CY : V ← 1 (mem) MSB = CY : V ← 0		x	x			
		reg, CL	1101001W	11010 reg	2	2 + n	temp ← CL, while temp ≠ 0 the following operations are repeated: tmpcy← CY, CY ← reg MSB reg ← reg x 2 + tmpcy temp ← temp – 1		x	U			
		mem, CL	1101001W	mod 010 mem	2-4	6/10 + n	temp ← CL, while temp ≠ 0 the following operations are repeated: tmpcy ← CY, CY ← (mem) MSB (mem) ← (mem) x 2 + tmpcy temp ← temp – 1		x	U			
		reg, imm8	1100000W	11010 reg	3	2 + n	temp ← imm8, while temp ≠ 0 the following operations are repeated: tmpcy ← CY, CY ← reg MSB reg ← reg x 2 + tmpcy temp ← temp – 1		x	U			
		mem, imm8	1100000W	mod 010 mem	3-5	6/10 + n	temp ← imm8, while temp ≠ 0 the following operations are repeated: tmpcy ← CY, CY ← (mem) MSB (mem) ← (mem) x 2 + tmpcy temp ← temp – 1		x	U			

Remark n indicates the shift number.

Instruction Group	Mnemonic	Operand(s)	Operation Code 76543210	Operation Code 76543210	Bytes	Clock Cycles	Operation	Flags AC	CY	V	P	S	Z
Rotate instructions	RORC	reg, 1	1 1 0 1 0 0 0 W	1 1 0 1 1 reg	2	2	tmpcy ← CY, CY ← reg LSB reg ← reg + 2 reg MSB ← tmpcy reg MSB ≠ bit after reg MSB : V ← 1 reg MSB = bit after reg MSB : V ← 0		x	x			
		mem, 1	1 1 0 1 0 0 0 W	mod 0 1 1 mem	2-4	7/11	tmpcy ← CY, CY ← (mem) LSB (mem) ← (mem) + 2 (mem) MSB ← tmpcy (mem) MSB ≠ bit after (mem) MSB : V ← 1 (mem) MSB = bit after (mem) MSB : V ← 0		x	x			
		reg, CL	1 1 0 1 0 0 1 W	1 1 0 1 1 reg	2	2 + n	temp ← CL, while temp ≠ 0 the following operations are repeated: tmpcy ← CY, CY ← reg LSB reg ← reg + 2 reg MSB ← tmpcy temp ← temp – 1		x	U			
		mem, CL	1 1 0 1 0 0 1 W	mod 0 1 1 mem	2-4	6/10 + n	temp ← CL, while temp ≠ 0 the following operations are repeated: tmpcy ← CY, CY ← (mem) LSB (mem) ← (mem) + 2 (mem) MSB ← tmpcy temp ← temp – 1		x	U			
		reg, imm8	1 1 0 0 0 0 0 W	1 1 0 1 1 reg	3	2 + n	temp ←imm8, while temp ≠ 0 the following operations are repeated: tmpcy ← CY, CY ← reg LSB reg ← reg + 2 reg MSB ← tmpcy temp ← temp – 1		x	U			
		mem, imm8	1 1 0 0 0 0 0 W	mod 0 1 1 mem	3-5	6/10 + n	temp ← imm8, while temp ≠ 0 the following operations are repeated: tmpcy ← CY, CY ← (mem) LSB (mem) ← (mem) + 2 (mem) MSB ← tmpcy temp ← temp – 1		x	U			

Remark n indicates the shift number.

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles	Operation	Flags					
			76543210	76543210				AC	CY	V	P	S	Z
Subroutine control instructions	CALL	near-proc	11101000		3	7/9	SP ← SP – 2, (SP + 1, SP) ← PC PC ← PC + disp						
		regptr16	11111111	11010 reg	2	7/9	SP ← SP – 2, (SP + 1, SP) ← PC PC ← regptr16						
		memptr16	11111111	mod 0 1 0 mem	2-4	11/15	TA ← (memptr16) SP ← SP – 2, (SP + 1, SP) ← PC, PC ← TA						
		far-proc	10011010		5	9/13	SP ← SP – 2, (SP + 1, SP) ← PS, PS ← seg SP ← SP – 2, (SP + 1, SP) ← PC, PC ← offset						
		memptr32	11111111	mod 0 1 1 mem	2-4	15/23	TA ← (memptr32),TB ← (memptr32 + 2) SP ← SP – 2, (SP + 1, SP) ← PS, PS ← TB SP ← SP – 2, (SP + 1, SP) ← PC, PC ← TA						
	RET		11000011		1	10/12	PC ← (SP + 1, SP) SP ← SP + 2						
		pop-value	11000010		3	10/12	PC ← (SP + 1, SP) SP ← SP + 2, SP ← SP + pop-value						
			11001011		1	12/16	PC ← (SP + 1, SP) PS ← (SP + 3, SP + 2) PS ← SP + 4						
		pop-value	11001010		3	12/16	PC ← (SP + 1, SP) PS ← (SP + 3, SP + 2) SP ← SP + 4, SP ← SP + pop-value						

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles	Operation	Flags					
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0				AC	CY	V	P	S	Z
Stack manipulation instructions	PUSH	mem16	1 1 1 1 1 1 1 1	mod 1 1 0 mem	2-4	5/9	SP ← SP – 2 (SP + 1, SP) ← (mem16)						
		reg16	0 1 0 1 0 reg		1	3/5	SP ← SP – 2 (SP + 1, SP) ← reg16						
		sreg	0 0 0 sreg 1 1 0		1	3/5	SP ← SP – 2 (SP + 1, SP) ← sreg						
		PSW	1 0 0 1 1 1 0 0		1	3/5	SP ← SP – 2 (SP + 1, SP) ← PSW						
		R	0 1 1 0 0 0 0 0		1	20/36	Push registers on the stack						
		imm8	0 1 1 0 1 0 1 0		2	3/5	(SP – 1, SP – 2) ← imm 8 sign extension SP ← SP – 2						
		imm16	0 1 1 0 1 0 0 0		3	3/5	(SP – 1, SP – 2) ← imm16 SP ← SP – 2						
	POP	mem16	1 0 0 0 1 1 1 1	mod 0 0 0 mem	2-4	5/9	SP ← SP + 2 (mem16) ← (SP – 1, SP – 2)						
		reg16	0 1 0 1 1 reg		1	5/7	SP ← SP + 2 reg16 ← (SP – 1, SP – 2)						
		sreg	0 0 0 sreg 1 1 1		1	5/7	SP ← SP + 2 sreg ← (SP – 1, SP – 2) sreg : SS, DS0, DS1						
		PSW	1 0 0 1 1 1 0 1		1	5/7	SP ← SP + 2 PSW ← (SP – 1, SP – 2)	R	R	R	R	R	R
		R	0 1 1 0 0 0 0 1		1	22/38	Pop registers from the stack						
	PREPARE	imm16, imm8	1 1 0 0 1 0 0 0		4	Note	Prepare New Stack Frame						
	DISPOSE		1 1 0 0 1 0 0 1		1	6/8	Dispose of Stack Frame						
Branch instructions	BR	near-label	1 1 1 0 1 0 0 1		3	7	PC ← PC+ dsip						
		short-label	1 1 1 0 1 0 1 1		2	7	PC ← PC+ ext-disp8						
		regptr16	1 1 1 1 1 1 1 1	1 1 1 0 0 reg	2	7	PC ← regptr16						
		memptr16	1 1 1 1 1 1 1 1	mod 1 0 0 mem	2-4	11/13	PC ← (memptr16)						
		far-label	1 1 1 0 1 0 1 0		5	7	PS ← seg PC ← offset						
		memptr32	1 1 1 1 1 1 1 1	mod 1 0 1 mem	2-4	13/17	PS ← (memptr32 + 2) PC ← (memptr32)						

Note When imm8 = 0 : 15
When imm8 ≥ 1 : 15 + 8 (imm 8 – 1)/17 + 12 (imm8 – 1)

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles[Note]	Operation		Flags					
			76543210	76543210					AC	CY	V	P	S	Z
Conditional branch instructions	BV	short-label	01110000		2	6/3	if V = 1	PC ← PC + ext-disp8						
	BNV	short-label	0001		2	6/3	if V = 0	PC ← PC + ext-disp8						
	BC BL	short-label	0010		2	6/3	if CY = 1	PC ← PC + ext-disp8						
	BNC BNL	short-label	0011		2	6/3	if CY = 0	PC ← PC + ext-disp8						
	BE BZ	short-label	0100		2	6/3	if Z = 1	PC ← PC + ext-disp8						
	BNE BNZ	short-label	0101		2	6/3	if Z = 0	PC ← PC + ext-disp8						
	BNH	short-label	0110		2	6/3	if CY ∨ Z = 1	PC ← PC + ext-disp8						
	BH	short-label	0111		2	6/3	if CY ∨ Z = 0	PC ← PC + ext-disp8						
	BN	short-label	1000		2	6/3	if S = 1	PC ← PC + ext-disp8						
	BP	short-label	1001		2	6/3	if S = 0	PC ← PC + ext-disp8						
	BPE	short-label	1010		2	6/3	if P = 1	PC ← PC + ext-disp8						
	BPO	short-label	1011		2	6/3	if P = 0	PC ← PC + ext-disp8						
	BLT	short-label	1100		2	6/3	if S ⊻ V = 1	PC ← PC + ext-disp8						
	BGE	short-label	1101		2	6/3	if S ⊻ V = 0	PC ← PC + ext-disp8						
	BLE	short-label	1110		2	6/3	if (S ⊻ V) ∨ Z = 1	PC ← PC + ext-disp8						
	BGT	short-label	1111		2	6/3	if (S ⊻ V) ∨ Z = 0	PC ← PC + ext-disp8						
	DBNZNE	short-label	11100000		2	6/3	CW = CW − 1 if Z = 0 and CW ≠ 0	PC ← PC + ext-disp8						
	DBNZE	short-label	0001		2	6/3	CW = CW − 1 if Z = 1 and CW ≠ 0	PC ← PC + ext-disp8						
	DBNZ	short-label	0010		2	6/3	CW = CW − 1 if CW ≠ 0	PC ← PC + ext-disp8						
	BCWZ	short-label	0011		2	6/3	if CW = 0	PC ← PC + ext-disp8						

Note Condition decision : true/false

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles	Operation	Flags					
			76543210	76543210				AC	CY	V	P	S	Z
Interrupt instructions	BRK	3	11001100		1	18/24	TA ← (00DH, 00CH), TC ← (00FH, 00EH) SP ← SP − 2, (SP + 1, SP) ← PSW, IE ← 0, BRK ← 0 SP ← SP − 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP − 2, (SP + 1, SP) ← PC[Note 2], PC ← TA						
		imm8 (≠ 3)	11001101		2	18/24	TA ← (4 n + 1, 4n), TC ← (4n + 3, 4n + 2) n = imm8 SP ← SP − 2, (SP + 1, SP) ← PSW, IE ← 0, BRK ← 0 SP ← SP − 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP − 2, (SP + 1, SP) ← PC[Note 2], PC ← TA						
	BRKV		11001110		1	**Note 1**	If V = 1 TA ← (011H, 010H), TC ← (013H, 012H) SP ← SP − 2, (SP + 1, SP) ← PSW, IE ← 0, BRK ← 0 SP ← SP − 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP − 2, (SP + 1, SP) ← PC[Note 2], PC ← TA						
	RETI		11001111		1	13/19	PC ← (SP + 1, SP), PS ← (SP + 3, SP + 2), PSW ← (SP + 5, SP + 4), SP ← SP + 6	R	R	R	R	R	R
	CHKIND	reg16, mem32	01100010	mod reg mem	2-4	**Note 3**	If (mem32) > reg16 or (mem32 + 2) < reg16 TA ← (015H, 014H), TC ← (017H, 016H) SP ← SP − 2, (SP + 1, SP) ← PSW, IE ← 0, BRK ← 0 SP ← SP − 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP − 2, (SP + 1, SP) ← PC[Note 2], PC ← TA						

Notes 1. When V = 1 : 20/26
When V = 0 : 3

2. Start address of instruction after BRK/BRKV/CHKIND instruction

3. When interrupt condition is established : 24 to 26/30 to 32
When interrupt condition is not established : 12/14

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles	Operation	Flags					
			76543210	76543210				AC	CY	V	P	S	Z
CPU control instructions	HALT		11110100		1	2	CPU Halt						
	POLL[Note 1]		10011011		1	2 + 2n	Poll and wait n: Number of times $\overline{\text{CPBUSY}}$ pin is sampled						
	DI		11111010		1	2	IE ← 0						
	EI		11111011		1	2	IE ← 1						
	BUSLOCK		11110000		1	2	Bus Lock Prefix						
	FPO1[Note 1]	fp-op	11011XXX	11YYYZZZ	2	**Note 2**	No Operation						
		fp-op, mem	11011XXX	mod YYY mem	2-4	**Note 2**	data bus ← (mem)						
	FPO2[Note 1]	fp-op	01100011X	11YYYZZZ	2	**Note 2**	No Operation						
		fp-op, mem	01100011X	mod YYY mem	2-4	**Note 2**	data bus ← (mem)						
	NOP		10010000		1	3	No Operation						
Segment operation instruction	DS0 : DS1 : PS : SS :		00111110 00100110 00101110 00110110		1	2	Segment override prefix						
Extended address mode special instruction	BRKXA	imm8	00001111	11100000	3	12	temp1 ← (imm8 × 4 + 1, imm8 × 4) temp2 ← (imm8 × 4 + 3, imm8 × 4 + 2) XA ← 1 PC ← temp1 PS ← temp2 Extended address mode setting						
	RETXA	imm8	00001111	11110000	3	12	temp1 ← (imm8 × 4 + 1, imm8 × 4) temp2 ← (imm8 × 4 + 3, imm8 × 4 + 2) XA ← 0 PC ← temp1 PS ← temp2 Extended address mode release						

Caution Do not attach 8 or more prefix instructions to a non-prefix instruction.

Notes 1. If the POLL instruction, the FPO1 instruction and FPO2 instruction are executed with no coprocessor connected, a coprocessor absent interrupt is generated (interrupted vector 130).

2. The clock cycle of this instruction depends on the presence or absence of coprocessor.

15. ELECTRICAL SPECIFICATIONS

Available Electrical Specifications

		μPD70236A-10	μPD70236A-12	μPD70236A-16	μPD70236A-20
V_{DD} = 5 V ±10%	T_A = −40 to +85 °C	√ (10 MHz)	√ (12.5 MHz)	√ (16 MHz)	√ (20 MHz)
	T_A = −10 to +70 °C	—	—	√ (16 MHz)	√ (20 MHz)
V_{DD} = 3.6 to 4.5 V	T_A = −40 to +85 °C	—	—	√ (12.5 MHz)	√ (16 MHz)
V_{DD} = 2.7 to 3.6 V	T_A = −40 to +85 °C	—	—	√ (8 MHz)	√ (10 MHz)

Remarks 1. √: Electrical specification available —: No electrical specification

2. Figures in parentheses show the maximum operating frequency fx.

15.1 SPECIFICATIONS WHEN V_{DD} = 5 V ± 10%

Absolute Maximum Ratings (T_A = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATING	UNIT
Supply voltage	V_{DD}		−0.5 to +7.0	V
Input voltage	V_I	Except X1, V_{DD} = 5 V ±10%	−0.5 to V_{DD}+0.3	V
Clock input voltage	V_K	X1, V_{DD} = 5 V ±10%	−0.5 to V_{DD}+1.0	V
Output short current	I_{OS}		50	mA
Output voltage	V_O	V_{DD} = 5 V ±10%	−0.5 to V_{DD}+0.3	V
Operating ambient temperature	T_A		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

Cautions 1. **Do not connect output pin (or I/O pin) of IC product directly to other output pins, V_{DD}, V_{CC} or GND. Open drain output pins or open collector output pins, however, can be connected each other. Output pins having high impedance capability can be also connected each other in an external circuit designed the timing to prevent output conflict.**

2. **Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics.**

DC Characteristics (μPD70236A-10/-12/-16/-20 : T_A = −40 to +85 °C, V_{DD} = 5 V ± 10 %)
(μPD70236A-16/-20 : T_A = −10 to +70 °C, V_{DD} = 5 V ± 10 %)

	PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Input voltage, high	V_{IH}	Except $\overline{RESET}$	2.2		V_{DD}+0.3	V
			$\overline{RESET}$	0.8 V_{DD}		V_{DD}+0.3	V
	Input voltage, low	V_{IL}	Except $\overline{RESET}$	−0.5		+0.8	V
			$\overline{RESET}$	−0.5		0.2 V_{DD}	V
	Clock input voltage, high	V_{KH}	X2, X1	0.8 V_{DD}		V_{DD}+0.5	V
	Clock input voltage, low	V_{KL}	X2, X1	−0.5		+0.6	V
	Output voltage, high	V_{OH}	I_{OH} = −2.5 mA	0.7 V_{DD}			V
			I_{OH} = −100 μA	V_{DD}−0.4			V
	Output voltage, low	V_{OL}	Except $\overline{TC}$, I_{OL} = 2.5 mA			0.45	V
			$\overline{TC}$, I_{OL} = 5.0 mA			0.45	V
	Input leak current, high	I_{LIH}	V_I = V_{DD}			10	μA
	Input leak current, low	I_{LIL}	V_I = 0 V			−10	μA
	Output leak current, high	I_{LOH}	V_O = V_{DD}			10	μA
	Output leak current, low	I_{LOL}	V_O = 0 V			−10	μA
	High-level latch leakage current	I_{LLH}	V_I = 3.0 V	−20		−200	μA
	Low-level latch leakage current	I_{LLL}	V_I = 0.8 V	20		200	μA
	Latch inversion current (L → H)	I_{ILH}				200	μA
	Latch inversion current (H → L)	I_{ILL}				−200	μA
*	Supply current[Note]	I_{DD}	In operation (fx = 2 to 20 [MHz])		3.9fx + 3	6fx + 5	mA
*			HALT (fx=2 to 20 MHz)		0.025fx+0.5	0.35fx+3	mA
			STOP		5.0	200	μA

Note Setting condition : The CPU clock is used for the TCLK0 to TCLK2 with refreshing enabled.
The units of the constants 3.9, 6, 0.025 and 0.35 are mA/MHz.

Remark The TYP. values are the reference values when T_A = 25 °C and V_{DD} = 5.0 V.

Capacitance (T_A = 25 °C, V_{DD} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_I	fc = 1 MHz Unmeasured pins returned to 0 V.			15	pF
Input output capacitance	C_{IO}				15	pF
Output capacitance	C_O				15	pF

Recommended Oscillator Circuit

(a) Ceramic resonator connection (T_A = –40 to +85 °C, V_{DD} = 5 V ± 10 %)

Fig. 1

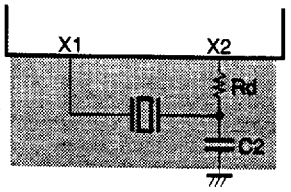
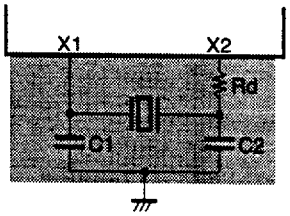


Fig. 2

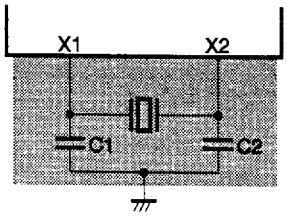


MANUFACTURER	OSCILLATOR FREQUENCY fxx [MHz]	PRODUCT NAME	RECOMMENDED CONSTANT			CIRCUIT DIAGRAM
			C1 [pF]	C2 [pF]	Rd [Ω]	
Murata Mfg. Co., Ltd.	40	CSA40.00MXZ040	—	5	33	Fig.1
	32	CSA32.00MXZ040	—	5	33	
	25	CSA25.00MXZ040	—	5	33	
	20	CSA20.00MXZ040	7	15	33	Fig. 2

Cautions
1. The oscillation circuit should be located as close as possible to the X1 and X2 pins.
2. No other signal lines should cross the shaded area.
3. Sufficient evaluation is required for matching between the μPD70236A and the resonator.

(b) Crystal resonator connection (T_A = –40 to +85 °C, V_{DD} = 5 V ± 10 %)

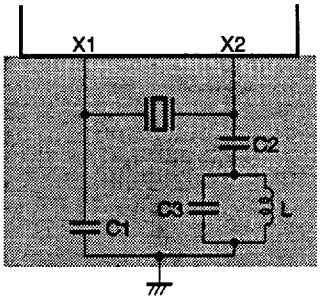
(i) Recommended conditions of oscillation with basic wave



MANUFACTURER	OSCILLATOR FREQUENCY fxx [MHz]	PRODUCT NAME	RECOMMENDED CONSTANT	
			C1 [pF]	C2 [pF]
Kinseki, Ltd.	20	HC-49/U	10	10

Cautions
1. The oscillation circuit should be located as close as possible to the X1 and X2 pins.
2. No other signal lines should cross the shaded area.
3. Sufficient evaluation is required for matching between the μPD70236A and the resonator.

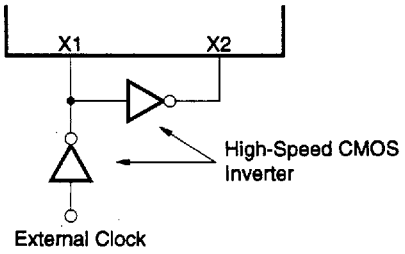
(ii) Recommended conditions with third overtone

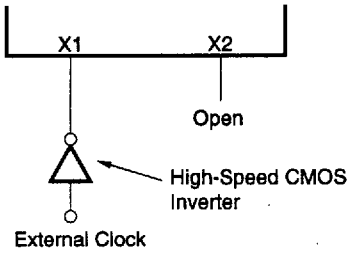


MANUFACTURER	OSCILLATOR FREQUENCY fxx [MHz]	PRODUCT NAME	RECOMMENDED CONSTANT			
			C1 [pF]	C2 [pF]	C3 [pF]	L [μH]
Kinseki, Ltd.	40	HC-49/U	5	1000	5	3.3
	32		5	1000	5	5.6
	25		5	1000	10	4.7

Cautions 1. The oscillation circuit should be located as close as possible to the X1 and X2 pins.
2. No other signal lines should cross the shaded area.
3. Sufficient evaluation is required for matching between the μPD70236A and the resonator.

(c) External clock input





Cautions 1. The high-speed CMOS inverter should be located as close as possible to the X1 and X2 pins.
2. Ensure that matching between the μPD70236A and the high-speed CMOS inverter is fully evaluated.

AC Characteristics (V_{DD} = 5 V ± 10 %, Output pin load capacitance : C_L = 100 pF)

(1) μPD70236A-10 (V_{DD} = 5 V ± 10 %)

(1/4)

PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
External clock input cycle	①	t_{CYX}	15–1		50	250	ns
External clock input high-level width	②	t_{XKH}	15–1		15		ns
External clock input low-level width	③	t_{XKL}	15–1		15		ns
External clock input rise time	④	t_{XKR}	15–1			10	ns
External clock input fall time	⑤	t_{XKF}	15–1			10	ns
CPU operating frequency	–	fx	–		2	10	MHz
CLKOUT output frequency	⑥	t_{CYK}	15–1		100	500	ns
CLKOUT high-level width	⑦	t_{KKH}	15–1		0.5t_{CYK}–12		ns
CLKOUT low-level width	⑧	t_{KKL}	15–1		0.5t_{CYK}–12		ns
CLKOUT rise time	⑨	t_{KR}	15–1	1.0 V → 3.5 V		12	ns
CLKOUT fall time	⑩	t_{KF}	15–1	3.5 V → 1.0 V		12	ns
CLKOUT delay time (from external clock)	⑪	t_{DXK}	15–1		4	30	ns
PCLKOUT output frequency	⑫	t_{CYPK}	15–1		4t_{CYX}	1000	ns
PCLKOUT high-level width	⑬	t_{PKH}	15–1		2t_{CYX}–12		ns
PCLKOUT low-level width	⑭	t_{PKL}	15–1		2t_{CYX}–12		ns
PCLKOUT output rise time	⑮	t_{PKR}	15–1	1.0 V → 3.5 V		12	ns
PCKLOUT output fall time	⑯	t_{PKF}	15–1	3.5 V → 1.0 V		12	ns
Input rise time[Note 1]	⑰	t_{IR}		0.8 V → 2.2 V		15	ns
Input fall time[Note 1]	⑱	t_{IF}		2.2 V → 0.8 V		10	ns
Output rise time[Note 2]	⑲	t_{OR}		0.8 V → 2.2 V		15	ns
Output fall time[Note 2]	⑳	t_{OF}		2.2 V → 0.8 V		10	ns
$\overline{\text{RESET}}$ setup time (to CLKOUT↓)	㉑	t_{SRSTK}	15–2		30		ns
$\overline{\text{RESET}}$ hold time (from CLKOUT↓)	㉒	t_{HKRST}	15–2		15		ns
RESOUT output delay time (from CLKOUT↓)	㉓	t_{DKRO}	15–2		0	40	ns
$\overline{\text{RESET}}$ low-level width	㉔	t_{WRSTL}	15–2		6t_{CYK}		ns
$\overline{\text{READY}}$ setup time (to CLKOUT↑)	㉕	t_{SRYK}	15–3, etc.		10		ns
$\overline{\text{READY}}$ hold time (from CLKOUT↑)	㉖	t_{HKRY}	15–3, etc.		20		ns
$\overline{\text{BCYST}}$ high-level width	㉗	t_{SCBCH}	15–5, etc.		t_{CYK}(n+1)–10[Note 3]		ns
$\overline{\text{BCYST}}$ low-level width	㉘	t_{SCBCL}	15–5, etc.		t_{CYK}–10		ns
$\overline{\text{BCYST}}$ delay time from CLKOUT↓	㉙	t_{DKBC}	15–5, etc.		3	35	ns
$\overline{\text{MRD}}$ delay time from CLKOUT	㉚	t_{DKMR}	15–5, etc.		0	40	ns

Notes 1. Except external clock and $\overline{\text{RESET}}$
2. Except CLKOUT and PCLKOUT
3. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-10 (V_{DD} = 5 V ± 10 %)

(2/4)

PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C MIN.	T_A = −40 to +85 °C MAX.	UNIT
$\overline{MRD}$↓, $\overline{IORD}$↓ delay time from address/status output	(31)	t_{DARL}	15–5, etc.		0.5t_{CYK}–15		ns
Data hold time (from $\overline{MRD}$↑, from $\overline{IORD}$↑)	(32)	t_{HRD}	15–5, etc.		0		ns
Address delay time from CLKOUT↓ Note 1	(33)	t_{DKA}	15–5, etc.		2	35	ns
Data hold time (from R/$\overline{W}$↓)	(34)	t_{HRWD}	15–5		0		ns
Status delay time from CLKOUT↓	(35)	t_{DKST}	15–5, etc.		3	35	ns
$\overline{DSTB}$↓ output delay time from CLKOUT↑	(36)	t_{DKDS}	15–5, etc.		5	40	ns
$\overline{DSTB}$↑ output delay time from CLKOUT	(37)	t_{DKDSH}	15–5, etc.		3	40	ns
$\overline{DSTB}$↓ delay time from address/status output	(38)	t_{DADSL}	15–5, etc.		0.5t_{CYK}–15		ns
$\overline{DSTB}$ high-level width	(39)	t_{DSDSH}	15–5, etc.		0.5t_{CYK}–10		ns
$\overline{DSTB}$ low-level width	(40)	t_{DSDSL}	15–6, etc.		t_{CYK}(n+1)–10 Note 4		ns
Data hold time (from $\overline{DSTB}$↑)	(41)	t_{HDSD}	15–5, etc.		0		ns
Data hold time (from address/status change point)	(42)	t_{HASD}	15–5		0		ns
Control 1 Note 2 delay time from CLKOUT	(43)	t_{DKCT1}	15–21		0	40	ns
Control 2 Note 3 delay time from CLKOUT	(44)	t_{DKCT2}	15–5, etc.		0	40	ns
Data setup time (to CLKOUT↓)	(45)	t_{SDK}	15–5, etc.		10		ns
Data hold time (from CLKOUT↓)	(46)	t_{HKD}	15–5, etc.		10		ns
Output floating time from $\overline{DSTB}$↓	(47)	t_{DHZ}	15–5, etc.			0	ns
Address/status hold time from $\overline{MWR}$↑	(48)	t_{HMWHA}	15–6		0.5t_{CYK}–15		ns
$\overline{MWR}$ delay time from CLKOUT	(49)	t_{DKMW}	15–6, etc.		0	40	ns
$\overline{MWR}$↓, $\overline{IOWR}$↓ delay time from address/status output	(50)	t_{DAWL}	15–6, etc.		0.5t_{CYK}–15		ns
$\overline{MWR}$, $\overline{IOWR}$ low-level width	(51)	t_{WWL}	15–6, etc.		t_{CYK}(n+1)–10 Note 4		ns
Address/status hold time from $\overline{DSTB}$↑	(52)	t_{HDSHA}	15–6, etc.		0.5t_{CYK}–15		ns
Data output delay time from $\overline{DSTB}$↑	(53)	t_{DDSHD}	15–6, etc.		0.5t_{CYK}–15		ns
Data delay time from address/status output	(54)	t_{DAD}	15–6, etc.		0.5t_{CYK}–15		ns
Output setting time from $\overline{DSTB}$↑	(55)	t_{DLZ}	15–6, etc.		0.5t_{CYK}–15		ns

* **Notes** 1. These specifications apply to the following delay times from the falling edge of the CLKOUT signal.
(1) Address delay time
(2) $\overline{BUSLOCK}$ delay time
(3) Delay time of signals below immediately after release of bus hold:
A23-A0, D15-D0, M/$\overline{IO}$, BUSST1, BUSST0, $\overline{UBE}$, $\overline{BCYST}$, $\overline{DSTB}$.

2. Control 1 applies to the $\overline{MWR}$ and $\overline{IOWR}$ signals in a DMA cycle.
3. Control 2 applies to the $\overline{BUFEN}$, $\overline{INTAK}$ and $\overline{REFRQ}$ setups.
4. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remarks 1. The number in the symbol column correspond to the numbers in the timing charts.
2. Regarding the five specifications (32) t_{HRD}, (34) t_{HRWD}, (41) t_{HDSD}, (42) t_{HASD}, and (46) t_{HKD}, at least one should be observed.

μPD70236A-10 (V_{DD} = 5 V ± 10 %)

(3/4)

PARAMETER	SYMBOL	FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
				MIN.	MAX.	
Data output delay time from CLKOUT↑	⑯ t_{DKD}	15–6, etc.		3	40	ns
Float delay time from CLKOUT	⑰ t_{FK}	15–6, etc.		0	35	ns
$\overline{IORD}$ delay time from CLKOUT	⑱ t_{DKIR}	15–7		0	40	ns
$\overline{IOWR}$ delay time from CLKOUT	⑲ t_{DKIW}	15–8		0	40	ns
$\overline{NMI}$, INTPn (n = 0 to 7), $\overline{CPBUSY}$ setup time (to CLKOUT↓)	⑳ t_{SIK}	15–11		10		ns
$\overline{NMI}$, INTPn(n = 0 to 7), $\overline{CPBUSY}$ hold time (from CLKOUT↓)	㉑ t_{HKI}	15–11		10		ns
$\overline{BS8}$/BS16 setup time (to CLKOUT↑)	㉒ t_{SBSK}	15–13		10		ns
$\overline{BS8}$/BS16 hold time (from CLKOUT↑)	㉓ t_{HKBS}	15–13		10		ns
HLDRQ setup time (to CLKOUT↑)	㉔ t_{SHQK}	15–14		10		ns
HLDRQ hold time (from CLKOUT↑)	㉕ t_{HKHQ}	15–14		15		ns
HLDAK delay time from CLKOUT↑	㉖ t_{DKHA}	15–14		3	40	ns
HLDAK delay time from output float	㉗ t_{DFHA}	15–14		0.5t_{CYK}–15		ns
INTPn(n = 0 to 7) low-level width	㉘ t_{IPIPL}	15–17		80		ns
TCTLn (n = 0 to 2) setup time (to CLKOUT↓)	㉙ t_{SGK}	15–18		40		ns
TCTLn (n = 0 to 2) hold time (from CLKOUT↓)	㉚ t_{HKG}	15–18		80		ns
TCTLn (n = 0 to 2) high-level width	㉛ t_{GGH}	15–18, etc.		40		ns
TCTLn (n = 0 to 2) low-level width	㉜ t_{GGL}	15–18, etc.		40		ns
TOUTn (n = 0 to 2) output delay time (from TCTLn(n = 0 to 2)↓)	㉝ t_{DGTO}	15–18, etc.			90	ns
TOUTn (n = 0 to 2) output delay time (from CLKOUT↓)	㉞ t_{DKTO}	15–18			50	ns
TCLK cycle	㉟ t_{CYTK}	15–19		100	DC	ns
TCLK high-level width	㊱ t_{TKTKH}	15–19		30		ns
TCLK low-level width	㊲ t_{TKTKL}	15–19		45		ns
TCLK rise time	㊳ t_{TKR}	15–19			15	ns
TCLK fall time	㊴ t_{TKF}	15–19			15	ns
TCTLn (n = 0 to 2) hold time (from TCLK↑)	㊵ t_{HTKG}	15–19		40		ns
TCTLn (n = 0 to 2) setup time (to TCLK↑)	㊶ t_{SGTK}	15–19		40		ns
TOUTn (n = 0 to 2) output delay time (from TCLK↓)	㊷ t_{DTKTO}	15–19			100	ns
RxD setup time (to SCU internal clock↓)	㊸ t_{SRX}	15–20		500		ns
RxD hold time (from SCU internal clock↓)	㊹ t_{HRX}	15–20		500		ns
TxD delay time from TOUT1↑	㊺ t_{DTX}	15–20			200	ns
$\overline{DMAAK}$n (n = 0 to 3) delay time from CLKOUT↑	㊻ t_{DKHDA}	15–21		0	45	ns
$\overline{MRD}$, $\overline{IORD}$↓ delay time from CLKOUT↓	㊼ t_{DKRL}	15–21		0	45	ns
$\overline{MRD}$, $\overline{IORD}$↑ delay time from CLKOUT↓	㊽ t_{DKRH}	15–21		0	45	ns
$\overline{DMAAK}$n (n = 0 to 3)↑ delay time (from $\overline{IORD}$↑)	㊾ t_{DRHDAH}	15–21		0.5t_{CYK}–15		ns
$\overline{IORD}$↓,$\overline{IOWR}$↓ delay time (from $\overline{DMAAK}$n (n = 0 to 3)↓)	㊿ t_{DDARW}	15–21		0.5t_{CYK}–15		ns

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-10 (V_{DD} = 5 V ± 10 %) (4/4)

		SYMBOL	FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
PARAMETER					MIN.	MAX.	
$\overline{IORD}$↑ delay time (from $\overline{MWR}$↑) $\overline{MRD}$↑ delay time (from $\overline{IOWR}$↑)	⑨①	t_{DWHRH}	15–21		0		ns
$\overline{IORD}$, $\overline{MRD}$ low-level width	⑨②	t_{RR}	15–21		$t_{CYK}(n+2)-40$ Note 1		ns
$\overline{IOWR}$, $\overline{MWR}$ low-level width (extended write)	⑨③	t_{WW1}	15–21	Extended write	$t_{CYK}(n+2)-40$ Note 1		ns
$\overline{IOWR}$, $\overline{MWR}$ low-level width (normal write)	⑨④	t_{WW2}	15–21	Normal write	$t_{CYK}(n+1)-40$ Note 1		ns
$\overline{TC}$ output delay time (from CLKOUT↑)	⑨⑤	t_{DKTCL}	15–22		0	40	ns
$\overline{TC}$ OFF output delay time (from CLKOUT↑)	⑨⑥	t_{DKTCF}	15–22		0	40	ns
$\overline{TC}$ pull-up delay time (from CLKOUT↑) Note 2	⑨⑦	t_{DKTCH}	15–22	R_{TC} = 2.2 kΩ	0	$2t_{CYK}-20$	ns
$\overline{TC}$ low-level width	⑨⑧	t_{TCTCL}	15–22		$t_{CYK}(n+1)-15$ Note 1		ns
$\overline{END}$ setup time (to CLKOUT↑)	⑨⑨	t_{SEDK}	15–22		20		ns
$\overline{END}$ low-level width	⑩⑩	t_{EDEDL}	15–22		100		ns
DMARQn (n = 0 to 3) setup time (to CLKOUT↑)	⑩①	t_{SDQK}	15–22, etc.		20		ns
$\overline{DMAAK}$n (n = 0 to 3) delay time from CLKOUT↓	⑩②	t_{DKLDA}	15–23		0	40	ns
$\overline{MRD}$ high-level width	⑩③	t_{MRMRH}	15–5		$0.5t_{CYK}-10$		ns
Data set time from $\overline{MRD}$↑	⑩④	t_{DMRHLZ}	15–6, etc.		$0.5t_{CYK}-15$		ns
Data output delay time from $\overline{MRD}$↑	⑩⑤	t_{DMRHD}	15–6, etc.		$0.5t_{CYK}-15$		ns
Cascade address delay time from CLKOUT	⑩⑥	t_{DKCA}	15–15, etc.		2	35	ns
* $\overline{INTAK}$ high-level width	⑩⑦	t_{IAIAH}	15–16		$2.5t_{CYK}-10$		ns
PCLKOUT delay time from CLKOUT	⑩⑧	t_{DKPK}	15–1	CLKC = 00		±5	ns
$\overline{IOWR}$, $\overline{MWR}$↓ delay time from $\overline{MRD}$, $\overline{IORD}$↓	⑩⑨	t_{DRLWL}	15–21	Normal write	$t_{CYK}-15$		ns

Notes 1. n indicates the number of wait clock cycles inserted in the bus cycle.
2. It is assumed that the $\overline{TC}$ pin is connected with the pull-up resistor R_{TC}.

Remark The number in the symbol column correspond to the numbers in the timing charts.

(2) μPD70236A-12 (V_{DD} = 5 V ± 10 %)

(1/4)

PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
External clock input cycle	①	t_{CYX}	15–1		40	250	ns
External clock input high-level width	②	t_{XKH}	15–1		13		ns
External clock input low-level width	③	t_{XKL}	15–1		13		ns
External clock input rise time	④	t_{XKR}	15–1			7	ns
External clock input fall time	⑤	t_{XKF}	15–1			7	ns
CPU operating frequency	–	f_X	–		2	12.5	MHz
CLKOUT output frequency	⑥	t_{CYK}	15–1		80	500	ns
CLKOUT high-level width	⑦	t_{KKH}	15–1		0.5t_{CYK}–10		ns
CLKOUT low-level width	⑧	t_{KKL}	15–1		0.5t_{CYK}–10		ns
CLKOUT rise time	⑨	t_{KR}	15–1	1.0 V → 3.5 V		10	ns
CLKOUT fall time	⑩	t_{KF}	15–1	3.5 V → 1.0 V		10	ns
CLKOUT delay time (from external clock)	⑪	t_{DXK}	15–1		4	30	ns
PCLKOUT output frequency	⑫	t_{CYPK}	15–1		4t_{CYX}	1000	ns
PCLKOUT high-level width	⑬	t_{PKH}	15–1		2t_{CYX}–10		ns
PCLKOUT low-level width	⑭	t_{PKL}	15–1		2t_{CYX}–10		ns
PCLKOUT output rise time	⑮	t_{PKR}	15–1	1.0 V → 3.5 V		10	ns
PCKLOUT output fall time	⑯	t_{PKF}	15–1	3.5 V → 1.0 V		10	ns
Input rise time[Note 1]	⑰	t_{IR}		0.8 V → 2.2 V		15	ns
Input fall time[Note 1]	⑱	t_{IF}		2.2 V → 0.8 V		10	ns
Output rise time[Note 2]	⑲	t_{OR}		0.8 V → 2.2 V		15	ns
Output fall time[Note 2]	⑳	t_{OF}		2.2 V → 0.8 V		10	ns
$\overline{\text{RESET}}$ setup time (to CLKOUT↓)	㉑	t_{SRSTK}	15–2		30		ns
$\overline{\text{RESET}}$ hold time (from CLKOUT↓)	㉒	t_{HKRST}	15–2		15		ns
RESOUT output delay time (from CLKOUT↓)	㉓	t_{DKRO}	15–2		0	40	ns
$\overline{\text{RESET}}$ low-level width	㉔	t_{WRSTL}	15–2		6t_{CYK}		ns
$\overline{\text{READY}}$ setup time (to CLKOUT↑)	㉕	t_{SRYK}	15–3, etc.		7		ns
$\overline{\text{READY}}$ hold time (from CLKOUT↑)	㉖	t_{HKRY}	15–3, etc.		15		ns
$\overline{\text{BCYST}}$ high-level width	㉗	t_{BCBCH}	15–5, etc.		t_{CYK}(n+1)–10[Note 3]		ns
$\overline{\text{BCYST}}$ low-level width	㉘	t_{BCBCL}	15–5, etc.		t_{CYK}–10		ns
$\overline{\text{BCYST}}$ delay time from CLKOUT↓	㉙	t_{DKBC}	15–5, etc.		3	30	ns
$\overline{\text{MRD}}$ delay time from CLKOUT	㉚	t_{DKMR}	15–5, etc.		0	35	ns

Notes 1. Except external clock and $\overline{\text{RESET}}$

2. Except CLKOUT and PCLKOUT

3. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-12 (V_{DD} = 5 V ± 10 %)

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PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
$\overline{MRD}$↓, $\overline{IORD}$↓ delay time from address/status output	㉛	t_{DARL}	15–5, etc.		0.5t_{CYK}–15		ns
Data hold time (from $\overline{MRD}$↑, from $\overline{IORD}$↑)	㉜	t_{HRD}	15–5, etc.		0		ns
Address delay time from CLKOUT↓ Note 1	㉝	t_{DKA}	15–5, etc.		2	30	ns
Data hold time (from R/$\overline{W}$↓)	㉞	t_{HRWD}	15–5		0		ns
Status delay time from CLKOUT↓	㉟	t_{DKST}	15–5, etc.		3	30	ns
$\overline{DSTB}$↓ output delay time from CLKOUT↑	㊱	t_{DKDS}	15–5, etc.		5	35	ns
$\overline{DSTB}$↑ output delay time from CLKOUT	㊲	t_{DKDSH}	15–5, etc.		3	35	ns
$\overline{DSTB}$↓ delay time from address/status output	㊳	t_{DADSL}	15–5, etc.		0.5t_{CYK}–15		ns
$\overline{DSTB}$ high-level width	㊴	t_{DSDSH}	15–5, etc.		0.5t_{CYK}–10		ns
$\overline{DSTB}$ low-level width	㊵	t_{DSDSL}	15–6, etc.		$t_{CYK}(n+1)$–10 Note 4		ns
Data hold time (from $\overline{DSTB}$↑)	㊶	t_{HDSD}	15–5, etc.		0		ns
Data hold time (from address/status change point)	㊷	t_{HASD}	15–5		0		ns
Control 1 Note 2 delay time from CLKOUT	㊸	t_{DKCT1}	15–21		0	35	ns
Control 2 Note 3 delay time from CLKOUT	㊹	t_{DKCT2}	15–5, etc.		0	35	ns
Data setup time (to CLKOUT↓)	㊺	t_{SDK}	15–5, etc.		7		ns
Data hold time (from CLKOUT↓)	㊻	t_{HKD}	15–5, etc.		7		ns
Output floating time from $\overline{DSTB}$↓	㊼	t_{DHZ}	15–5, etc.			0	ns
Address/status hold time from $\overline{MWR}$↑	㊽	t_{HMWHA}	15–6		0.5t_{CYK}–15		ns
$\overline{MWR}$ delay time from CLKOUT	㊾	t_{DKMW}	15–6, etc.		0	35	ns
$\overline{MWR}$↓, $\overline{IOWR}$↓ delay time from address/status output	㊿	t_{DAWL}	15–6, etc.		0.5t_{CYK}–15		ns
$\overline{MWR}$, $\overline{IOWR}$ low-level width	(51)	t_{WWL}	15–6, etc.		$t_{CYK}(n+1)$–10 Note 4		ns
Address/status hold time from $\overline{DSTB}$↑	(52)	t_{HDSHA}	15–6, etc.		0.5t_{CYK}–15		ns
Data output delay time from $\overline{DSTB}$↑	(53)	t_{DDSHD}	15–6, etc.		0.5t_{CYK}–15		ns
Data delay time from address/status output	(54)	t_{DAD}	15–6, etc.		0.5t_{CYK}–15		ns
Output setting time from $\overline{DSTB}$↑	(55)	t_{DLZ}	15–6, etc.		0.5t_{CYK}–15		ns

* **Notes** 1. These specifications apply to the following delay times from the falling edge of the CLKOUT signal.
(1) Address delay time
(2) $\overline{BUSLOCK}$ delay time
(3) Delay time of signals below immediately after release of bus hold:
A23-A0, D15-D0, M/$\overline{IO}$, BUSST1, BUSST0, $\overline{UBE}$, $\overline{BCYST}$, $\overline{DSTB}$.

2. Control 1 applies to the $\overline{MWR}$ and $\overline{IOWR}$ signals in a DMA cycle.
3. Control 2 applies to the $\overline{BUFEN}$, $\overline{INTAK}$ and $\overline{REFRQ}$ setups.
4. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remarks 1. The number in the symbol column correspond to the numbers in the timing charts.
2. Regarding the five specifications (32) t_{HRD}, (34) t_{HRWD}, (41) t_{HDSD}, (42) t_{HASD}, and (46) t_{HKD}, at least one should be observed.

μPD70236A-12 (V_{DD} = 5 V ± 10 %)

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PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
Data output delay time from CLKOUT↑	⑤⑥	t_{DKD}	15–6, etc.		3	35	ns
Float delay time from CLKOUT	⑤⑦	t_{FK}	15–6, etc.		0	30	ns
$\overline{IORD}$ delay time from CLKOUT	⑤⑧	t_{DKIR}	15–7		0	35	ns
$\overline{IOWR}$ delay time from CLKOUT	⑤⑨	t_{DKIW}	15–8		0	35	ns
$\overline{NMI}$, INTPn (n = 0 to 7), $\overline{CPBUSY}$ setup time (to CLKOUT↓)	⑥⓪	t_{SIK}	15–11		10		ns
$\overline{NMI}$, INTPn(n = 0 to 7), $\overline{CPBUSY}$ hold time (from CLKOUT↓)	⑥①	t_{HKI}	15–11		10		ns
$\overline{BS8}$/BS16 setup time (to CLKOUT↑)	⑥②	t_{SBSK}	15–13		10		ns
$\overline{BS8}$/BS16 hold time (from CLKOUT↑)	⑥③	t_{HKBS}	15–13		10		ns
HLDRQ setup time (to CLKOUT↑)	⑥④	t_{SHQK}	15–14		10		ns
HLDRQ hold time (from CLKOUT↑)	⑥⑤	t_{HKHQ}	15–14		15		ns
HLDAK delay time from CLKOUT↑	⑥⑥	t_{DKHA}	15–14		3	35	ns
HLDAK delay time from output float	⑥⑦	t_{DFHA}	15–14		0.5t_{CYK}–15		ns
INTPn(n = 0 to 7) low-level width	⑥⑧	t_{IPIPL}	15–17		80		ns
TCTLn (n = 0 to 2) setup time (to CLKOUT↓)	⑥⑨	t_{SGK}	15–18		40		ns
TCTLn (n = 0 to 2) hold time (from CLKOUT↓)	⑦⓪	t_{HKG}	15–18		80		ns
TCTLn (n = 0 to 2) high-level width	⑦①	t_{GGH}	15–18, etc.		40		ns
TCTLn (n = 0 to 2) low-level width	⑦②	t_{GGL}	15–18, etc.		40		ns
TOUTn (n = 0 to 2) output delay time (from TCTLn(= 0 to 2)↓)	⑦③	t_{DGTO}	15–18, etc.			90	ns
TOUTn (n = 0 to 2) output delay time (from CLKOUT↓)	⑦④	t_{DKTO}	15–18			50	ns
TCLK cycle	⑦⑤	t_{CYTK}	15–19		80	DC	ns
TCLK high-level width	⑦⑥	t_{TKTKH}	15–19		30		ns
TCLK low-level width	⑦⑦	t_{TKTKL}	15–19		35		ns
TCLK rise time	⑦⑧	t_{TKR}	15–19			15	ns
TCLK fall time	⑦⑨	t_{TKF}	15–19			15	ns
TCTLn (n = 0 to 2) hold time (from TCLK↑)	⑧⓪	t_{HTKG}	15–19		40		ns
TCTLn (n = 0 to 2) setup time (to TCLK↑)	⑧①	t_{SGTK}	15–19		40		ns
TOUTn (n = 0 to 2) output delay time (from TCLK↓)	⑧②	t_{DTKTO}	15–19			100	ns
RxD setup time (to SCU internal clock↓)	⑧③	t_{SRX}	15–20		500		ns
RxD hold time (from SCU internal clock↓)	⑧④	t_{HRX}	15–20		500		ns
TxD delay time from TOUT1↑	⑧⑤	t_{DTX}	15–20			200	ns
$\overline{DMAAK}$n (n = 0 to 3) delay time from CLKOUT↑	⑧⑥	t_{DKHDA}	15–21		0	40	ns
$\overline{MRD}$, $\overline{IORD}$↓ delay time from CLKOUT↓	⑧⑦	t_{DKRL}	15–21		0	40	ns
$\overline{MRD}$, $\overline{IORD}$↑ delay time from CLKOUT↓	⑧⑧	t_{DKRH}	15–21		0	40	ns
$\overline{DMAAK}$n (n = 0 to 3)↑ delay time (from $\overline{IORD}$↑)	⑧⑨	t_{DRHDAH}	15–21		0.5t_{CYK}–15		ns
$\overline{IORD}$↓,$\overline{IOWR}$↓ delay time (from $\overline{DMAAK}$n (n = 0 to 3)↓)	⑨⓪	t_{DDARW}	15–21		0.5t_{CYK}–15		ns

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-12 (V_{DD} = 5 V ± 10 %) (4/4)

		SYMBOL	FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
PARAMETER					MIN.	MAX.	
$\overline{IORD}$↑ delay time (from $\overline{MWR}$↑) $\overline{MRD}$↑ delay time (from $\overline{IOWR}$↑)	⑨①	t_{DWHRH}	15–21		0		ns
$\overline{IORD}$, $\overline{MRD}$ low-level width	⑨②	t_{RR}	15–21		$t_{CYK}(n+2)-35$ Note 1		ns
$\overline{IOWR}$, $\overline{MWR}$ low-level width (extended write)	⑨③	t_{WW1}	15–21	Extended write	$t_{CYK}(n+2)-35$ Note 1		ns
$\overline{IOWR}$, $\overline{MWR}$ low-level width (normal write)	⑨④	t_{WW2}	15–21	Normal write	$t_{CYK}(n+1)-35$ Note 1		ns
$\overline{TC}$ output delay time (from CLKOUT↑)	⑨⑤	t_{DKTCL}	15–22		0	35	ns
$\overline{TC}$ OFF output delay time (from CLKOUT↑)	⑨⑥	t_{DKTCF}	15–22		0	35	ns
$\overline{TC}$ pull-up delay time (from CLKOUT↑) Note 2	⑨⑦	t_{DKTCH}	15–22	R_{TC} = 1.1 kΩ	0	$2t_{CYK}-10$	ns
$\overline{TC}$ low-level width	⑨⑧	t_{TCTCL}	15–22		$t_{CYK}(n+1)-15$ Note 1		ns
$\overline{END}$ setup time (to CLKOUT↑)	⑨⑨	t_{SEDK}	15–22		10		ns
$\overline{END}$ low-level width	⑩⓪	t_{EDEDL}	15–22		100		ns
DMARQn (n = 0 to 3) setup time (to CLKOUT↑)	⑩①	t_{SDQK}	15–22, etc.		15		ns
$\overline{DMAAK}$n (n = 0 to 3) delay time from CLKOUT↓	⑩②	t_{DKLDA}	15–23		0	35	ns
$\overline{MRD}$ high-level width	⑩③	t_{MRMRH}	15–5		$0.5t_{CYK}-10$		ns
Data set time from $\overline{MRD}$↑	⑩④	t_{DMRHLZ}	15–6, etc.		$0.5t_{CYK}-15$		ns
Data output delay time from $\overline{MRD}$↑	⑩⑤	t_{DMRHD}	15–6, etc.		$0.5t_{CYK}-15$		ns
Cascade address delay time from CLKOUT	⑩⑥	t_{DKCA}	15–15, etc.		2	30	ns
* $\overline{INTAK}$ high-level width	⑩⑦	t_{IAIAH}	15–16		$2.5t_{CYK}-10$		ns
PCLKOUT delay time from CLKOUT	⑩⑧	t_{DKPK}	15–1	CLKC = 00		±5	ns
$\overline{IOWR}$, $\overline{MWR}$↓ delay time from $\overline{MRD}$, $\overline{IORD}$↓	⑩⑨	t_{DRLWL}	15–21	Normal write	$t_{CYK}-15$		ns

Notes 1. n indicates the number of wait clock cycles inserted in the bus cycle.
2. It is assumed that the $\overline{TC}$ pin is connected with the pull-up resistor R_{TC}.

Remark The number in the symbol column correspond to the numbers in the timing charts.

(3) μPD70236A-16 (V_{DD} = 5 V ± 10 %)

(1/4)

PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		T_A = −10 to +70 °C		UNIT
					MIN.	MAX.	MIN.	MAX.	
External clock input cycle	①	t_{CYX}	15–1		31.25	250	31.25	250	ns
External clock input high-level width	②	t_{XKH}	15–1		8		8		ns
External clock input low-level width	③	t_{XKL}	15–1		8		8		ns
External clock input rise time	④	t_{XKR}	15–1			7		7	ns
External clock input fall time	⑤	t_{XKF}	15–1			7		7	ns
CPU operating frequency	–	fx	–		2	16	2	16	MHz
CLKOUT output frequency	⑥	t_{CYK}	15–1		62.5	500	62.5	500	ns
CLKOUT high-level width	⑦	t_{KKH}	15–1		0.5t_{CYK}–7		0.5t_{CYK}–7		ns
CLKOUT low-level width	⑧	t_{KKL}	15–1		0.5t_{CYK}–7		0.5t_{CYK}–7		ns
CLKOUT rise time	⑨	t_{KR}	15–1	1.0 V → 3.5 V		7		7	ns
CLKOUT fall time	⑩	t_{KF}	15–1	3.5 V → 1.0 V		7		7	ns
CLKOUT delay time (from external clock)	⑪	t_{DXK}	15–1		4	30	5	30	ns
PCLKOUT output frequency	⑫	t_{CYPK}	15–1		4t_{CYX}	1000	4t_{CYX}	1000	ns
PCLKOUT high-level width	⑬	t_{PKH}	15–1		2t_{CYX}–7		2t_{CYX}–7		ns
PCLKOUT low-level width	⑭	t_{PKL}	15–1		2t_{CYX}–7		2t_{CYX}–7		ns
PCLKOUT output rise time	⑮	t_{PKR}	15–1	1.0 V → 3.5 V		7		7	ns
PCKLOUT output fall time	⑯	t_{PKF}	15–1	3.5 V → 1.0 V		7		7	ns
Input rise time[Note 1]	⑰	t_{IR}		0.8 V → 2.2 V		12		12	ns
Input fall time[Note 1]	⑱	t_{IF}		2.2 V → 0.8 V		10		10	ns
Output rise time[Note 2]	⑲	t_{OR}		0.8 V → 2.2 V		12		12	ns
Output fall time[Note 2]	⑳	t_{OF}		2.2 V → 0.8 V		10		10	ns
$\overline{\text{RESET}}$ setup time (to CLKOUT↓)	㉑	t_{SRSTK}	15–2		30		25		ns
$\overline{\text{RESET}}$ hold time (from CLKOUT↓)	㉒	t_{HKRST}	15–2		15		12		ns
RESOUT output delay time (from CLKOUT↓)	㉓	t_{DKRO}	15–2		0	40	0	40	ns
$\overline{\text{RESET}}$ low-level width	㉔	t_{WRSTL}	15–2		6t_{CYK}		6t_{CYK}		ns
$\overline{\text{READY}}$ setup time (to CLKOUT↑)	㉕	t_{SRYK}	15–3, etc.		5		5		ns
$\overline{\text{READY}}$ hold time (from CLKOUT↑)	㉖	t_{HKRY}	15–3, etc.		12		12		ns
$\overline{\text{BCYST}}$ high-level width	㉗	t_{BCBCH}	15–5, etc.		$t_{CYK}(n+1)-10$[Note 3]		$t_{CYK}(n+1)-10$[Note 3]		ns
$\overline{\text{BCYST}}$ low-level width	㉘	t_{BCBCL}	15–5, etc.		t_{CYK}–10		t_{CYK}–10		ns
$\overline{\text{BCYST}}$ delay time from CLKOUT↓	㉙	t_{DKBC}	15–5, etc.		3	30	4	25	ns
$\overline{\text{MRD}}$ delay time from CLKOUT	㉚	t_{DKMR}	15–5, etc.		0	35	0	25	ns

Notes 1. Except external clock and $\overline{\text{RESET}}$
2. Except CLKOUT and PCLKOUT
3. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-16 (V_{DD} = 5 V ± 10 %)

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PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		T_A = −10 to +70 °C		UNIT
					MIN.	MAX.	MIN.	MAX.	
$\overline{MRD}\downarrow$, $\overline{IORD}\downarrow$ delay time from address/status output	㉛	t_{DARL}	15–5, etc.		0.5t_{CYK}−15		0.5t_{CYK}−15		ns
Data hold time (from $\overline{MRD}\uparrow$, from $\overline{IORD}\uparrow$)	㉜	t_{HRD}	15–5, etc.		0		0		ns
Address delay time from CLKOUT↓ Note 1	㉝	t_{DKA}	15–5, etc.		2	30	3	20	ns
Data hold time (from R/$\overline{W}\downarrow$)	㉞	t_{HRWD}	15–5		0		0		ns
Status delay time from CLKOUT↓	㉟	t_{DKST}	15–5, etc.		3	30	4	20	ns
$\overline{DSTB}\downarrow$ output delay time from CLKOUT↑	㊱	t_{DKDS}	15–5, etc.		5	35	5	30	ns
$\overline{DSTB}\uparrow$ output delay time from CLKOUT	㊲	t_{DKDSH}	15–5, etc.		3	35	4	25	ns
$\overline{DSTB}\downarrow$ delay time from address/status output	㊳	t_{DADSL}	15–5, etc.		0.5t_{CYK}−15		0.5t_{CYK}−15		ns
$\overline{DSTB}$ high-level width	㊴	t_{DSDSH}	15–5, etc.		0.5t_{CYK}−10		0.5t_{CYK}−10		ns
$\overline{DSTB}$ low-level width	㊵	t_{DSDSL}	15–6, etc.		$t_{CYK}(n+1)-10$ Note 4		$t_{CYK}(n+1)-10$ Note 4		ns
Data hold time (from $\overline{DSTB}\uparrow$)	㊶	t_{HDSD}	15–5, etc.		0		0		ns
Data hold time (from address/status change point)	㊷	t_{HASD}	15–5		0		0		ns
Control 1 Note 2 delay time from CLKOUT	㊸	t_{DKCT1}	15–21		0	35	0	25	ns
Control 2 Note 3 delay time from CLKOUT	㊹	t_{DKCT2}	15–5, etc.		0	35	0	30	ns
Data setup time (to CLKOUT↓)	㊺	t_{SDK}	15–5, etc.		7		7		ns
Data hold time (from CLKOUT↓)	㊻	t_{HKD}	15–5, etc.		7		7		ns
Output floating time from $\overline{DSTB}\downarrow$	㊼	t_{DHZ}	15–5, etc.			0		0	ns
Address/status hold time from $\overline{MWR}\uparrow$	㊽	t_{HMWHA}	15–6		0.5t_{CYK}−15		0.5t_{CYK}−15		ns
$\overline{MWR}$ delay time from CLKOUT	㊾	t_{DKMW}	15–6, etc.		0	35	0	30	ns
$\overline{MWR}\downarrow$, $\overline{IOWR}\downarrow$ delay time from address/status output	㊿	t_{DAWL}	15–6, etc.		0.5t_{CYK}−15		0.5t_{CYK}−15		ns
$\overline{MWR}$, $\overline{IOWR}$ low-level width	(51)	t_{WWL}	15–6, etc.		$t_{CYK}(n+1)-10$ Note 4		$t_{CYK}(n+1)-10$ Note 4		ns
Address/status hold time from $\overline{DSTB}\uparrow$	(52)	t_{HDSHA}	15–6, etc.		0.5t_{CYK}−15		0.5t_{CYK}−15		ns
Data output delay time from $\overline{DSTB}\uparrow$	(53)	t_{DDSHD}	15–6, etc.		0.5t_{CYK}−15		0.5t_{CYK}−15		ns
Data delay time from address/status output	(54)	t_{DAD}	15–6, etc.		0.5t_{CYK}−15		0.5t_{CYK}−15		ns
Output setting time from $\overline{DSTB}\uparrow$	(55)	t_{DLZ}	15–6, etc.		0.5t_{CYK}−15		0.5t_{CYK}−15		ns

★ **Notes** 1. These specifications apply to the following delay times from the falling edge of the CLKOUT signal.
(1) Address delay time
(2) $\overline{BUSLOCK}$ delay time
(3) Delay time of signals below immediately after release of bus hold:
A23-A0, D15-D0, M/$\overline{IO}$, BUSST1, BUSST0, $\overline{UBE}$, $\overline{BCYST}$, $\overline{DSTB}$.

2. Control 1 applies to the $\overline{MWR}$ and $\overline{IOWR}$ signals in a DMA cycle.
3. Control 2 applies to the $\overline{BUFEN}$, $\overline{INTAK}$ and $\overline{REFRQ}$ setups.
4. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remarks 1. The number in the symbol column correspond to the numbers in the timing charts.
2. Regarding the five specifications (32) t_{HRD}, (34) t_{HRWD}, (41) t_{HDSD}, (42) t_{HASD}, and (46) t_{HKD}, at least one should be observed.

μPD70236A-16 (V_{DD} = 5 V ± 10 %)

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PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		T_A = −10 to +70 °C		UNIT
					MIN.	MAX.	MIN.	MAX.	
Data output delay time from CLKOUT↑	㊺⑥	t_{DKD}	15–6, etc.		3	35	4	30	ns
Float delay time from CLKOUT	㊺⑦	t_{FK}	15–6, etc.		0	30	0	25	ns
$\overline{IORD}$ delay time from CLKOUT	㊺⑧	t_{DKIR}	15–7		0	35	0	25	ns
$\overline{IOWR}$ delay time from CLKOUT	㊺⑨	t_{DKIW}	15–8		0	35	0	30	ns
$\overline{NMI}$, INTPn (n = 0 to 7), $\overline{CPBUSY}$ setup time (to CLKOUT↓)	㊻⓪	t_{SIK}	15–11		7		7		ns
$\overline{NMI}$, INTPn(n = 0 to 7), $\overline{CPBUSY}$ hold time (from CLKOUT↓)	㊻①	t_{HKI}	15–11		7		7		ns
$\overline{BS8}$/BS16 setup time (to CLKOUT↑)	㊻②	t_{SBSK}	15–13		7		7		ns
$\overline{BS8}$/BS16 hold time (from CLKOUT↑)	㊻③	t_{HKBS}	15–13		7		7		ns
HLDRQ setup time (to CLKOUT↑)	㊻④	t_{SHQK}	15–14		7		7		ns
HLDRQ hold time (from CLKOUT↑)	㊻⑤	t_{HKHQ}	15–14		10		10		ns
HLDAK delay time from CLKOUT↑	㊻⑥	t_{DKHA}	15–14		3	35	4	25	ns
HLDAK delay time from output float	㊻⑦	t_{DFHA}	15–14		0.5t_{CYK}−15		0.5t_{CYK}−15		ns
INTPn(n = 0 to 7) low-level width	㊻⑧	t_{IPIPL}	15–17		80		80		ns
TCTLn (n = 0 to 2) setup time (to CLKOUT↓)	㊻⑨	t_{SGK}	15–18		40		40		ns
TCTLn (n = 0 to 2) hold time (from CLKOUT↓)	㊼⓪	t_{HKG}	15–18		80		80		ns
TCTLn (n = 0 to 2) high-level width	㊼①	t_{GGH}	15–18, etc.		40		40		ns
TCTLn (n = 0 to 2) low-level width	㊼②	t_{GGL}	15–18, etc.		40		40		ns
TOUTn (n = 0 to 2) output delay time (from TCTLn (n = 0 to 2)↓)	㊼③	t_{DGTO}	15–18, etc.			90		90	ns
TOUTn (n = 0 to 2) output delay time (from CLKOUT↓)	㊼④	t_{DKTO}	15–18			50		50	ns
TCLK cycle	㊼⑤	t_{CYTK}	15–19		62.5	DC	62.5	DC	ns
TCLK high-level width	㊼⑥	t_{TKTKH}	15–19		25		25		ns
TCLK low-level width	㊼⑦	t_{TKTKL}	15–19		30		30		ns
TCLK rise time	㊼⑧	t_{TKR}	15–19			15		15	ns
TCLK fall time	㊼⑨	t_{TKF}	15–19			15		15	ns
TCTLn (n = 0 to 2) hold time (from TCLK↑)	㊽⓪	t_{HTKG}	15–19		40		40		ns
TCTLn (n = 0 to 2) setup time (to TCLK↑)	㊽①	t_{SGTK}	15–19		40		40		ns
TOUTn (n = 0 to 2) output delay time (from TCLK↓)	㊽②	t_{DTKTO}	15–19			100		100	ns
RxD setup time (to SCU internal clock↓)	㊽③	t_{SRX}	15–20		500		500		ns
RxD hold time (from SCU internal clock↓)	㊽④	t_{HRX}	15–20		500		500		ns
TxD delay time from TOUT1↑	㊽⑤	t_{DTX}	15–20			200		200	ns
$\overline{DMAAK}$n (n = 0 to 3) delay time from CLKOUT↑	㊽⑥	t_{DKHDA}	15–21		0	40	0	35	ns
$\overline{MRD}$, $\overline{IORD}$↓ delay time from CLKOUT↓	㊽⑦	t_{DKRL}	15–21		0	40	0	35	ns
$\overline{MRD}$, $\overline{IORD}$↑ delay time from CLKOUT↓	㊽⑧	t_{DKRH}	15–21		0	40	0	35	ns
$\overline{DMAAK}$n (n = 0 to 3)↑ delay time (from $\overline{IORD}$↑)	㊽⑨	t_{DRHDAH}	15–21		0.5t_{CYK}−15		0.5t_{CYK}−15		ns
$\overline{IORD}$↓,$\overline{IOWR}$↓ delay time (from $\overline{DMAAK}$n (n = 0 to 3)↓)	㊾⓪	t_{DDARW}	15–21		0.5t_{CYK}−15		0.5t_{CYK}−15		ns

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-16 (V_{DD} = 5 V ± 10 %) (4/4)

		SYMBOL	FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		T_A = −10 to +70 °C		UNIT
PARAMETER					MIN.	MAX.	MIN.	MAX.	
$\overline{IORD}$↑ delay time (from $\overline{MWR}$↑) $\overline{MRD}$↑ delay time (from $\overline{IOWR}$↑)	⑨①	t_{DWHRH}	15–21		0		0		ns
$\overline{IORD}$, $\overline{MRD}$ low-level width	⑨②	t_{RR}	15–21		$t_{CYK}(n+2)-35$[Note 1]		$t_{CYK}(n+2)-25$[Note 1]		ns
$\overline{IOWR}$, $\overline{MWR}$ low-level width (extended write)	⑨③	t_{WW1}	15–21	Extended write	$t_{CYK}(n+2)-35$[Note 1]		$t_{CYK}(n+2)-25$[Note 1]		ns
$\overline{IOWR}$, $\overline{MWR}$ low-level width (normal write)	⑨④	t_{WW2}	15–21	Normal write	$t_{CYK}(n+1)-35$[Note 1]		$t_{CYK}(n+1)-25$[Note 1]		ns
$\overline{TC}$ output delay time (from CLKOUT↑)	⑨⑤	t_{DKTCL}	15–22		0	35	0	25	ns
$\overline{TC}$ OFF output delay time (from CLKOUT↑)	⑨⑥	t_{DKTCF}	15–22		0	35	0	25	ns
$\overline{TC}$ pull-up delay time (from CLKOUT↑)[Note 2]	⑨⑦	t_{DKTCH}	15–22	R_{TC} = 1.1 kΩ	0	$2t_{CYK}-10$	0	$2t_{CYK}-10$	ns
$\overline{TC}$ low-level width	⑨⑧	t_{TCTCL}	15–22		$t_{CYK}(n+1)-15$[Note 1]		$t_{CYK}(n+1)-15$[Note 1]		ns
$\overline{END}$ setup time (to CLKOUT↑)	⑨⑨	t_{SEDK}	15–22		10		10		ns
$\overline{END}$ low-level width	⑩⓪	t_{EDEDL}	15–22		100		100		ns
DMARQn (n = 0 to 3) setup time (to CLKOUT↑)	⑩①	t_{SDQK}	15–22, etc.		12		12		ns
$\overline{DMAAK}$n (n = 0 to 3) delay time from CLKOUT↓	⑩②	t_{DKLDA}	15–23		0	35	0	25	ns
$\overline{MRD}$ high-level width	⑩③	t_{MRMRH}	15–5		$0.5t_{CYK}-10$		$0.5t_{CYK}-10$		ns
Data set time from $\overline{MRD}$↑	⑩④	t_{DMRHLZ}	15–6, etc.		$0.5t_{CYK}-15$		$0.5t_{CYK}-15$		ns
Data output delay time from $\overline{MRD}$↑	⑩⑤	t_{DMRHD}	15–6, etc.		$0.5t_{CYK}-15$		$0.5t_{CYK}-15$		ns
Cascade address delay time from CLKOUT	⑩⑥	t_{DKCA}	15–15, etc.		2	30	3	20	ns
* $\overline{INTAK}$ high-level width	⑩⑦	t_{IAIAH}	15–16		$2.5t_{CYK}-10$		$2.5t_{CYK}-10$		ns
PCLKOUT delay time from CLKOUT	⑩⑧	t_{DKPK}	15–1	CLKC = 00		±5		±5	ns
$\overline{IOWR}$, $\overline{MWR}$↓ delay time from $\overline{MRD}$, $\overline{IORD}$↓	⑩⑨	t_{DRLWL}	15–21	Normal write	$t_{CYK}-15$		$t_{CYK}-15$		ns

Notes 1. n indicates the number of wait clock cycles inserted in the bus cycle.
2. It is assumed that the $\overline{TC}$ pin is connected with the pull-up resistor R_{TC}.

Remark The number in the symbol column correspond to the numbers in the timing charts.

(4) μPD70236A-20 (V_{DD} = 5 V ± 10 %)

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PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		T_A = −10 to +70 °C		UNIT
					MIN.	MAX.	MIN.	MAX.	
External clock input cycle	①	t_{CYX}	15–1		25	250	25	250	ns
External clock input high-level width	②	t_{XKH}	15–1		8		8		ns
External clock input low-level width	③	t_{XKL}	15–1		8		8		ns
External clock input rise time	④	t_{XKR}	15–1			7		7	ns
External clock input fall time	⑤	t_{XKF}	15–1			7		7	ns
CPU operating frequency	–	fx	–		2	20	2	20	MHz
CLKOUT output frequency	⑥	t_{CYK}	15–1		50	500	50	500	ns
CLKOUT high-level width	⑦	t_{KKH}	15–1		0.5t_{CYK}–5		0.5t_{CYK}–5		ns
CLKOUT low-level width	⑧	t_{KKL}	15–1		0.5t_{CYK}–5		0.5t_{CYK}–5		ns
CLKOUT rise time	⑨	t_{KR}	15–1	1.0 V → 3.5 V		5		5	ns
CLKOUT fall time	⑩	t_{KF}	15–1	3.5 V → 1.0 V		5		5	ns
CLKOUT delay time (from external clock)	⑪	t_{DXK}	15–1		4	30	5	30	ns
PCLKOUT output frequency	⑫	t_{CYPK}	15–1		4t_{CYX}	1000	4t_{CYX}	1000	ns
PCLKOUT high-level width	⑬	t_{PKH}	15–1		2t_{CYX}–5		2t_{CYX}–5		ns
PCLKOUT low-level width	⑭	t_{PKL}	15–1		2t_{CYX}–5		2t_{CYX}–5		ns
PCLKOUT output rise time	⑮	t_{PKR}	15–1	1.0 V → 3.5 V		5		5	ns
PCKLOUT output fall time	⑯	t_{PKF}	15–1	3.5 V → 1.0 V		5		5	ns
Input rise time[Note 1]	⑰	t_{IR}		0.8 V → 2.2 V		10		10	ns
Input fall time[Note 1]	⑱	t_{IF}		2.2 V → 0.8 V		10		10	ns
Output rise time[Note 2]	⑲	t_{OR}		0.8 V → 2.2 V		10		10	ns
Output fall time[Note 2]	⑳	t_{OF}		2.2 V → 0.8 V		10		10	ns
$\overline{\text{RESET}}$ setup time (to CLKOUT↓)	㉑	t_{SRSTK}	15–2		30		25		ns
$\overline{\text{RESET}}$ hold time (from CLKOUT↓)	㉒	t_{HKRST}	15–2		15		12		ns
$\overline{\text{RESOUT}}$ output delay time (from CLKOUT↓)	㉓	t_{DKRO}	15–2		0	40	0	40	ns
$\overline{\text{RESET}}$ low-level width	㉔	t_{WRSTL}	15–2		6t_{CYK}		6t_{CYK}		ns
$\overline{\text{READY}}$ setup time (to CLKOUT↑)	㉕	t_{SRYK}	15–3, etc.		5		5		ns
$\overline{\text{READY}}$ hold time (from CLKOUT↑)	㉖	t_{HKRY}	15–3, etc.		12		12		ns
$\overline{\text{BCYST}}$ high-level width	㉗	t_{BCBCH}	15–5, etc.		$t_{CYK}(n+1)-7$[Note 3]		$t_{CYK}(n+1)-7$[Note 3]		ns
$\overline{\text{BCYST}}$ low-level width	㉘	t_{BCBCL}	15–5, etc.		t_{CYK}–7		t_{CYK}–7		ns
$\overline{\text{BCYST}}$ delay time from CLKOUT↓	㉙	t_{DKBC}	15–5, etc.		3	30	4	25	ns
$\overline{\text{MRD}}$ delay time from CLKOUT	㉚	t_{DKMR}	15–5, etc.		0	35	0	25	ns

Notes
1. Except external clock and $\overline{\text{RESET}}$
2. Except CLKOUT and PCLKOUT
3. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-20 (V_{DD} = 5 V ± 10 %)

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PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		T_A = −10 to +70 °C		UNIT
					MIN.	MAX.	MIN.	MAX.	
$\overline{MRD}$↓, $\overline{IORD}$↓ delay time from address/status output	(31)	t_{DARL}	15–5, etc.		0.5t_{CYK}−12		0.5t_{CYK}−12		ns
Data hold time (from $\overline{MRD}$↑, from $\overline{IORD}$↑)	(32)	t_{HRD}	15–5, etc.		0		0		ns
Address delay time from CLKOUT↓ Note 1	(33)	t_{DKA}	15–5, etc.		2	30	3	20	ns
Data hold time (from R/$\overline{W}$↓)	(34)	t_{HRWD}	15–5		0		0		ns
Status delay time from CLKOUT↓	(35)	t_{DKST}	15–5, etc.		3	30	4	20	ns
$\overline{DSTB}$↓ output delay time from CLKOUT↑	(36)	t_{DKDS}	15–5, etc.		5	35	5	30	ns
$\overline{DSTB}$↑ output delay time from CLKOUT	(37)	t_{DKDSH}	15–5, etc.		3	35	4	25	ns
$\overline{DSTB}$↓ delay time from address/status output	(38)	t_{DADSL}	15–5, etc.		0.5t_{CYK}−12		0.5t_{CYK}−12		ns
$\overline{DSTB}$ high-level width	(39)	t_{DSDSH}	15–5, etc.		0.5t_{CYK}−7		0.5t_{CYK}−7		ns
$\overline{DSTB}$ low-level width	(40)	t_{DSDSL}	15–6, etc.		$t_{CYK}(n+1)-7$ Note 4		$t_{CYK}(n+1)-7$ Note 4		ns
Data hold time (from $\overline{DSTB}$↑)	(41)	t_{HDSD}	15–5, etc.		0		0		ns
Data hold time (from address/status change point)	(42)	t_{HASD}	15–5		0		0		ns
Control 1 Note 2 delay time from CLKOUT	(43)	t_{DKCT1}	15–21		0	35	0	25	ns
Control 2 Note 3 delay time from CLKOUT	(44)	t_{DKCT2}	15–5, etc.		0	35	0	30	ns
Data setup time (to CLKOUT↓)	(45)	t_{SDK}	15–5, etc.		7		7		ns
Data hold time (from CLKOUT↓)	(46)	t_{HKD}	15–5, etc.		7		7		ns
Output floating time from $\overline{DSTB}$↓	(47)	t_{DHZ}	15–5, etc.			0		0	ns
Address/status hold time from $\overline{MWR}$↑	(48)	t_{HMWHA}	15–6		0.5t_{CYK}−12		0.5t_{CYK}−12		ns
$\overline{MWR}$ delay time from CLKOUT	(49)	t_{DKMW}	15–6, etc.		0	35	0	30	ns
$\overline{MWR}$↓, $\overline{IOWR}$↓ delay time from address/status output	(50)	t_{DAWL}	15–6, etc.		0.5t_{CYK}−12		0.5t_{CYK}−12		ns
$\overline{MWR}$, $\overline{IOWR}$ low-level width	(51)	t_{WWL}	15–6, etc.		$t_{CYK}(n+1)-7$ Note 4		$t_{CYK}(n+1)-7$ Note 4		ns
Address/status hold time from $\overline{DSTB}$↑	(52)	t_{HDSHA}	15–6, etc.		0.5t_{CYK}−12		0.5t_{CYK}−12		ns
Data output delay time from $\overline{DSTB}$↑	(53)	t_{DDSHD}	15–6, etc.		0.5t_{CYK}−12		0.5t_{CYK}−12		ns
Data delay time from address/status output	(54)	t_{DAD}	15–6, etc.		0.5t_{CYK}−12		0.5t_{CYK}−12		ns
Output setting time from $\overline{DSTB}$↑	(55)	t_{DLZ}	15–6, etc.		0.5t_{CYK}−12		0.5t_{CYK}−12		ns

* **Notes** 1. These specifications apply to the following delay times from the falling edge of the CLKOUT signal.
(1) Address delay time
(2) $\overline{BUSLOCK}$ delay time
(3) Delay time of signals below immediately after release of bus hold:
A23-A0, D15-D0, M/$\overline{IO}$, BUSST1, BUSST0, $\overline{UBE}$, $\overline{BCYST}$, $\overline{DSTB}$.

2. Control 1 applies to the $\overline{MWR}$ and $\overline{IOWR}$ signals in a DMA cycle.
3. Control 2 applies to the $\overline{BUFEN}$, $\overline{INTAK}$ and $\overline{REFRQ}$ setups.
4. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remarks 1. The number in the symbol column correspond to the numbers in the timing charts.
2. Regarding the five specifications (32) t_{HRD}, (34) t_{HRWD}, (41) t_{HDSD}, (42) t_{HASD}, and (46) t_{HKD}, at least one should be observed.

μPD70236A-20 (V_{DD} = 5 V ± 10 %)

(3/4)

PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		T_A = −10 to +70 °C		UNIT
					MIN.	MAX.	MIN.	MAX.	
Data output delay time from CLKOUT↑	⑤⑥	t_{DKD}	15–6, etc.		3	35	4	30	ns
Float delay time from CLKOUT	⑤⑦	t_{FK}	15–6, etc.		0	30	0	25	ns
$\overline{IORD}$ delay time from CLKOUT	⑤⑧	t_{DKIR}	15–7		0	35	0	25	ns
$\overline{IOWR}$ delay time from CLKOUT	⑤⑨	t_{DKIW}	15–8		0	35	0	30	ns
$\overline{NMI}$, INTPn (n = 0 to 7), $\overline{CPBUSY}$ setup time (to CLKOUT↓)	⑥⑩	t_{SIK}	15–11		7		7		ns
$\overline{NMI}$, INTPn(n = 0 to 7), $\overline{CPBUSY}$ hold time (from CLKOUT↓)	⑥①	t_{HKI}	15–11		7		7		ns
$\overline{BS8}$/BS16 setup time (to CLKOUT↑)	⑥②	t_{SBSK}	15–13		7		7		ns
$\overline{BS8}$/BS16 hold time (from CLKOUT↑)	⑥③	t_{HKBS}	15–13		7		7		ns
HLDRQ setup time (to CLKOUT↑)	⑥④	t_{SHQK}	15–14		7		7		ns
HLDRQ hold time (from CLKOUT↑)	⑥⑤	t_{HKHQ}	15–14		10		10		ns
HLDAK delay time from CLKOUT↑	⑥⑥	t_{DKHA}	15–14		3	35	4	25	ns
HLDAK delay time from output float	⑥⑦	t_{DFHA}	15–14		0.5t_{CYK}−15		0.5t_{CYK}−15		ns
INTPn (n = 0 to 7) low-level width	⑥⑧	t_{IPIPL}	15–17		80		80		ns
TCTLn (n = 0 to 2) setup time (to CLKOUT↓)	⑥⑨	t_{SGK}	15–18		40		40		ns
TCTLn (n = 0 to 2) hold time (from CLKOUT↓)	⑦⓪	t_{HKG}	15–18		80		80		ns
TCTLn (n = 0 to 2) high-level width	⑦①	t_{GGH}	15–18, etc.		40		40		ns
TCTLn (n = 0 to 2) low-level width	⑦②	t_{GGL}	15–18, etc.		40		40		ns
TOUTn (n = 0 to 2) output delay time (from TCTLn (n = 0 to 2)↓)	⑦③	t_{DGTO}	15–18, etc.			90		90	ns
TOUTn (n = 0 to 2) output delay time (from CLKOUT↓)	⑦④	t_{DKTO}	15–18			50		50	ns
TCLK cycle	⑦⑤	t_{CYTK}	15–19		50	DC	50	DC	ns
TCLK high-level width	⑦⑥	t_{TKTKH}	15–19		20		20		ns
TCLK low-level width	⑦⑦	t_{TKTKL}	15–19		25		25		ns
TCLK rise time	⑦⑧	t_{TKR}	15–19			15		15	ns
TCLK fall time	⑦⑨	t_{TKF}	15–19			15		15	ns
TCTLn (n = 0 to 2) hold time (from TCLK↑)	⑧⓪	t_{HTKG}	15–19		40		40		ns
TCTLn (n = 0 to 2) setup time (to TCLK↑)	⑧①	t_{SGTK}	15–19		40		40		ns
TOUTn (n = 0 to 2) output delay time (from TCLK↓)	⑧②	t_{DTKTO}	15–19			100		100	ns
RxD setup time (to SCU internal clock↓)	⑧③	t_{SRX}	15–20		500		500		ns
RxD hold time (from SCU internal clock↓)	⑧④	t_{HRX}	15–20		500		500		ns
TxD delay time from TOUT1↑	⑧⑤	t_{DTX}	15–20			200		200	ns
$\overline{DMAAK}$n (n = 0 to 3) delay time from CLKOUT↑	⑧⑥	t_{DKHDA}	15–21		0	40	0	35	ns
$\overline{MRD}$, $\overline{IORD}$↓ delay time from CLKOUT↓	⑧⑦	t_{DKRL}	15–21		0	40	0	35	ns
$\overline{MRD}$, $\overline{IORD}$↑ delay time from CLKOUT↓	⑧⑧	t_{DKRH}	15–21		0	40	0	35	ns
$\overline{DMAAK}$n (n = 0 to 3)↑ delay time (from $\overline{IORD}$↑)	⑧⑨	t_{DRHDAH}	15–21		0.5t_{CYK}−12		0.5t_{CYK}−12		ns
$\overline{IORD}$↓,$\overline{IOWR}$↓ delay time (from $\overline{DMAAK}$n (n = 0 to 3)↓)	⑨⓪	t_{DDARW}	15–21		0.5t_{CYK}−12		0.5t_{CYK}−12		ns

Remark The number in the symbol column correspond to the numbers in the timing charts.

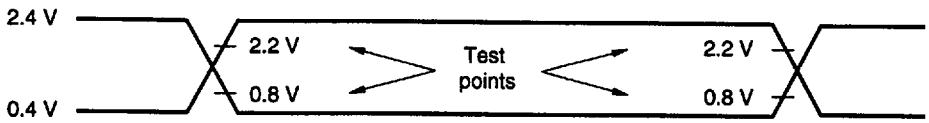
μPD70236A-20 (V_{DD} = 5 V ± 10 %) (4/4)

		PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		T_A = −10 to +70 °C		UNIT
							MIN.	MAX.	MIN.	MAX.	
		$\overline{IORD}$↑ delay time (from $\overline{MWR}$↑) $\overline{MRD}$↑ delay time (from $\overline{IOWR}$↑)	⑨①	t_{DWHRH}	15–21		0		0		ns
		$\overline{IORD}$, $\overline{MRD}$ low-level width	⑨②	t_{RR}	15–21		$t_{CYK}(n+2)-35$ [Note 1]		$t_{CYK}(n+2)-25$ [Note 1]		ns
		$\overline{IOWR}$, $\overline{MWR}$ low-level width (extended write)	⑨③	t_{WW1}	15–21	Extended write	$t_{CYK}(n+2)-35$ [Note 1]		$t_{CYK}(n+2)-25$ [Note 1]		ns
		$\overline{IOWR}$, $\overline{MWR}$ low-level width (normal write)	⑨④	t_{WW2}	15–21	Normal write	$t_{CYK}(n+1)-35$ [Note 1]		$t_{CYK}(n+1)-25$ [Note 1]		ns
		$\overline{TC}$ output delay time (from CLKOUT↑)	⑨⑤	t_{DKTCL}	15–22		0	35	0	25	ns
		$\overline{TC}$ OFF output delay time (from CLKOUT↑)	⑨⑥	t_{DKTCF}	15–22		0	35	0	25	ns
		$\overline{TC}$ pull-up delay time (from CLKOUT↑) [Note 2]	⑨⑦	t_{DKTCH}	15–22	R_{TC} = 1.1 kΩ	0	$2t_{CYK}-10$	0	$2t_{CYK}-10$	ns
		$\overline{TC}$ low-level width	⑨⑧	t_{TCTCL}	15–22		$t_{CYK}(n+1)-12$ [Note 1]		$t_{CYK}(n+1)-12$ [Note 1]		ns
		$\overline{END}$ setup time (to CLKOUT↑)	⑨⑨	t_{SEDK}	15–22		10		10		ns
		$\overline{END}$ low-level width	⑩⓪	t_{EDEDL}	15–22		100		100		ns
		DMARQn (n = 0 to 3) setup time (to CLKOUT↑)	⑩①	t_{SDQK}	15–22, etc.		12		12		ns
		$\overline{DMAAKn}$ (n = 0 to 3) delay time from CLKOUT↓	⑩②	t_{DKLDA}	15–23		0	35	0	25	ns
		$\overline{MRD}$ high-level width	⑩③	t_{MRMRH}	15–5		$0.5t_{CYK}-7$		$0.5t_{CYK}-7$		ns
		Data set time from $\overline{MRD}$↑	⑩④	t_{DMRHLZ}	15–6, etc.		$0.5t_{CYK}-12$		$0.5t_{CYK}-12$		ns
		Data output delay time from $\overline{MRD}$↑	⑩⑤	t_{DMRHD}	15–6, etc.		$0.5t_{CYK}-12$		$0.5t_{CYK}-12$		ns
		Cascade address delay time from CLKOUT	⑩⑥	t_{DKCA}	15–15, etc.		2	30	3	20	ns
*		$\overline{INTAK}$ high-level width	⑩⑦	t_{IAIAH}	15–16		$2.5t_{CYK}-7$		$2.5t_{CYK}-7$		ns
		PCLKOUT delay time from CLKOUT	⑩⑧	t_{DKPK}	15–1	CLKC = 00		±5		±5	ns
		$\overline{IOWR}$, $\overline{MWR}$↓ delay time from $\overline{MRD}$, $\overline{IORD}$↓	⑩⑨	t_{DRLWL}	15–21	Normal write	$t_{CYK}-12$		$t_{CYK}-12$		ns

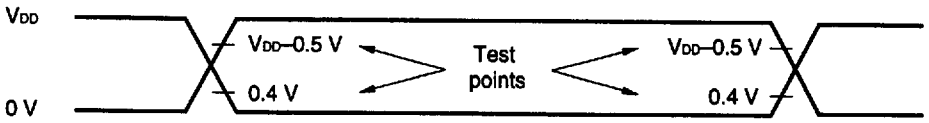
Notes 1. n indicates the number of wait clock cycles inserted in the bus cycle.
2. It is assumed that the $\overline{TC}$ pin is connected with the pull-up resistor R_{TC}.

Remark The number in the symbol column correspond to the numbers in the timing charts.

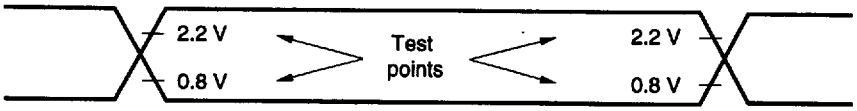
AC Test Input Waveform (Except X1)



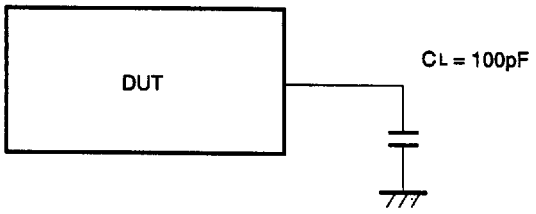
AC Test Input Waveform (X1)



AC Test Output Test Points



Load Conditions



Caution **If the load capacitance exceeds 100 pF due to the construction of the circuit, the load capacitance of this device should be reduced to 100 pF or less by insertion of a buffer, etc.**

15.2 SPECIFICATIONS WHEN V_{DD} = 3.6 TO 4.5 V

Absolute Maximum Ratings (T_A = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATING	UNIT
Supply voltage	V_{DD}		−0.5 to +7.0	V
Input voltage	V_I	Except X1, V_{DD} = 3.6 to 4.5 V	−0.5 to V_{DD}+0.3	V
Clock input voltage	V_K	X1, V_{DD} = 3.6 to 4.5 V	−0.5 to V_{DD}+1.0	V
Output short current	I_{OS}		50	mA
Output voltage	V_O	V_{DD} = 3.6 to 4.5 V	−0.5 to V_{DD}+0.3	V
Operating ambient temperature	T_A		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

Cautions 1. Do not connect output pin (or I/O pin) of IC product directly to other output pins, V_{DD}, V_{CC} or GND. Open drain output pins or open collector output pins, however, can be connected each other. Output pins having high impedance capability can be also connected each other in an external circuit designed the timing to prevent output conflict.

2. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics.

DC Characteristics (T_A = – 40 to +85 °C, V_{DD} = 3.6 to 4.5 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Input voltage, high	V_{IH}	Except $\overline{RESET}$	2.2		V_{DD}+0.3	V	
		$\overline{RESET}$	0.8 V_{DD}		V_{DD}+0.3	V	
Input voltage, low	V_{IL}	Except $\overline{RESET}$	–0.5		0.2 V_{DD}	V	
		$\overline{RESET}$	–0.5		0.2 V_{DD}	V	
Clock input voltage, high	V_{KH}	X2, X1	0.8 V_{DD}		V_{DD}+0.5	V	
Clock input voltage, low	V_{KL}	X2, X1	–0.5		+0.6	V	
Output voltage, high	V_{OH}	I_{OH} = –2.5 mA	0.7 V_{DD}			V	
		I_{OH} = –100 μA	V_{DD}–0.4			V	
Output voltage, low	V_{OL}	Except $\overline{TC}$, I_{OL} = 2.5 mA			0.4	V	
		$\overline{TC}$, I_{OL} = 5.0 mA			0.4	V	
Input leak current, high	I_{LIH}	V_I = V_{DD}			10	μA	
Input leak current, low	I_{LIL}	V_I = 0 V			–10	μA	
Output leak current, high	I_{LOH}	V_O = V_{DD}			10	μA	
Output leak current, low	I_{LOL}	V_O = 0 V			–10	μA	
High-level latch leakage current	I_{LLH}	V_I = 3.0 V	0		–200	μA	
Low-level latch leakage current	I_{LLL}	V_I = 0.8 V	0		200	μA	
Latch inversion current (L → H)	I_{ILH}				200	μA	
Latch inversion current (H → L)	I_{ILL}				–200	μA	
Supply current[Note]	I_{DD}	In operation (fx = 2 to 16 MHz)		2.9fx + 2	5fx + 5	mA	*
		HALT (fx = 2 to 16 MHz)		0.03125fx + 0.3	0.35fx + 2.0	mA	*
		STOP		4.0	150	μA	

Note Setting condition : The CPU clock is used for the TCLK0 to TCLK2 with refreshing enabled. The units of the constants 2.9, 5, 0.03125, 0.35 are mA/MHz.

Remark The TYP. values are the reference values when T_A = 25 °C and V_{DD} = 4.0 V.

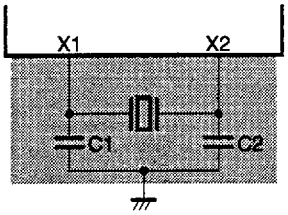
Capacitance (T_A = 25 °C, V_{DD} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_I	fc = 1 MHz Unmeasured pins returned to 0 V.			15	pF
Input output capacitance	C_{IO}				15	pF
Output capacitance	C_O				15	pF

Recommended Oscillator Circuit

(a) Crystal resonator connection (T_A = –40 to +85 °C, V_{DD} = 3.6 to 4.5 V)

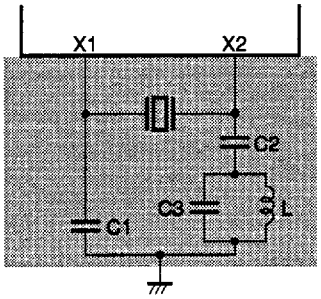
(i) Recommended conditions of oscillation with basic wave



MANUFACTURER	OSCILLATOR FREQUENCY fxx [MHz]	PRODUCT NAME	RECOMMENDED CONSTANT	
			C1 [pF]	C2 [pF]
Kinseki, Ltd.	20	HC-49/U	10	10

Cautions 1. The oscillation circuit should be located as close as possible to the X1 and X2 pins.
2. No other signal lines should cross the shaded area.
3. Sufficient evaluation is required for matching between the μPD70236A and the resonator.

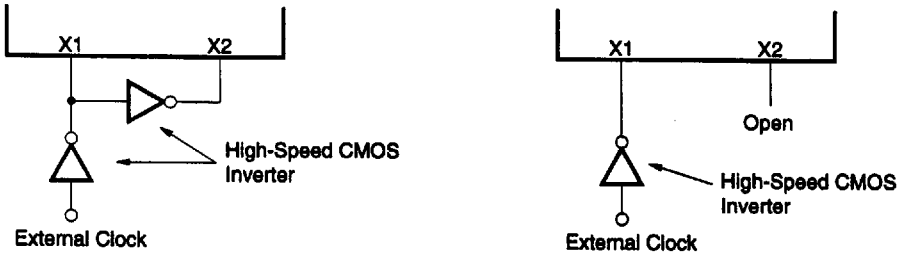
(ii) Recommended conditions with third overtone



MANUFACTURER	OSCILLATOR FREQUENCY fxx [MHz]	PRODUCT NAME	RECOMMENDED CONSTANT			
			C1 [pF]	C2 [pF]	C3 [pF]	L [μH]
Kinseki, Ltd.	32	HC-49/U	5	1000	5	5.6
	25		5	1000	10	4.7

Cautions 1. The oscillation circuit should be located as close as possible to the X1 and X2 pins.
2. No other signal lines should cross the shaded area.
3. Sufficient evaluation is required for matching between the μPD70236A and the resonator.

(b) External clock input



Cautions 1. The high-speed CMOS inverter should be located as close as possible to the X1 and X2 pins.

2. Ensure that matching between the μPD70236A and the high-speed CMOS inverter is fully evaluated.

AC Characteristics (V_{DD} = 3.6 to 4.5 V, Output pin load capacitance : C_L = 100 pF)

(1) μPD70236A-16 (V_{DD} = 3.6 to 4.5 V)

(1/4)

PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
External clock input cycle	①	t_{CYX}	15–1		40	250	ns
External clock input high-level width	②	t_{XKH}	15–1		10		ns
External clock input low-level width	③	t_{XKL}	15–1		10		ns
External clock input rise time	④	t_{XKR}	15–1			7	ns
External clock input fall time	⑤	t_{XKF}	15–1			7	ns
CPU operating frequency	–	fx	–		2	12.5	MHz
CLKOUT output frequency	⑥	t_{CYK}	15–1		80	500	ns
CLKOUT high-level width	⑦	t_{KKH}	15–1		0.5t_{CYK}–10		ns
CLKOUT low-level width	⑧	t_{KKL}	15–1		0.5t_{CYK}–10		ns
CLKOUT rise time	⑨	t_{KR}	15–1	0.2V_{DD} → 0.7V_{DD}		10	ns
CLKOUT fall time	⑩	t_{KF}	15–1	0.7V_{DD} → 0.2V_{DD}		10	ns
CLKOUT delay time (from external clock)	⑪	t_{DXK}	15–1		4	30	ns
PCLKOUT output frequency	⑫	t_{CYPK}	15–1		4t_{CYX}	1000	ns
PCLKOUT high-level width	⑬	t_{PKH}	15–1		2t_{CYX}–10		ns
PCLKOUT low-level width	⑭	t_{PKL}	15–1		2t_{CYX}–10		ns
PCLKOUT output rise time	⑮	t_{PKR}	15–1	0.2V_{DD} → 0.7V_{DD}		10	ns
PCKLOUT output fall time	⑯	t_{PKF}	15–1	0.7V_{DD} → 0.2V_{DD}		10	ns
Input rise time[Note 1]	⑰	t_{IR}		0.7V_{DD} → 0.2V_{DD}		12	ns
Input fall time[Note 1]	⑱	t_{IF}		0.2V_{DD} → 0.7V_{DD}		10	ns
Output rise time[Note 2]	⑲	t_{OR}		0.7V_{DD} → 0.2V_{DD}		12	ns
Output fall time[Note 2]	⑳	t_{OF}		0.2V_{DD} → 0.7V_{DD}		10	ns
$\overline{\text{RESET}}$ setup time (to CLKOUT↓)	㉑	t_{SRSTK}	15–2		30		ns
$\overline{\text{RESET}}$ hold time (from CLKOUT↓)	㉒	t_{HKRST}	15–2		15		ns
RESOUT output delay time (from CLKOUT↓)	㉓	t_{DKRO}	15–2		0	40	ns
$\overline{\text{RESET}}$ low-level width	㉔	t_{WRSTL}	15–2		6t_{CYK}		ns
$\overline{\text{READY}}$ setup time (to CLKOUT↑)	㉕	t_{SRYK}	15–3, etc.		7		ns
$\overline{\text{READY}}$ hold time (from CLKOUT↑)	㉖	t_{HKRY}	15–3, etc.		15		ns
$\overline{\text{BCYST}}$ high-level width	㉗	t_{BCBCH}	15–5, etc.		t_{CYK}(n+1)–10[Note 3]		ns
$\overline{\text{BCYST}}$ low-level width	㉘	t_{BCBCL}	15–5, etc.		t_{CYK}–10		ns
$\overline{\text{BCYST}}$ delay time from CLKOUT↓	㉙	t_{DKBC}	15–5, etc.		4	35	ns
$\overline{\text{MRD}}$ delay time from CLKOUT	㉚	t_{DKMR}	15–5, etc.		0	40	ns

Notes 1. Except external clock and $\overline{\text{RESET}}$
2. Except CLKOUT and PCLKOUT
3. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-16 (V_{DD} = 3.6 to 4.5 V)

(2/4)

PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
$\overline{MRD}$↓, $\overline{IORD}$↓ delay time from address/status output	㉛	t_{DARL}	15–5, etc.		0.5t_{CYK}–15		ns
Data hold time (from $\overline{MRD}$↑, from $\overline{IORD}$↑)	㉜	t_{HRD}	15–5, etc.		0		ns
Address delay time from CLKOUT↓ Note 1	㉝	t_{DKA}	15–5, etc.		3	35	ns
Data hold time (from R/$\overline{W}$↓)	㉞	t_{HRWD}	15–5		0		ns
Status delay time from CLKOUT↓	㉟	t_{DKST}	15–5, etc.		4	35	ns
$\overline{DSTB}$↓ output delay time from CLKOUT↑	㊱	t_{DKDS}	15–5, etc.		5	45	ns
$\overline{DSTB}$↑ output delay time from CLKOUT	㊲	t_{DKDSH}	15–5, etc.		4	40	ns
$\overline{DSTB}$↓ delay time from address/status output	㊳	t_{DADSL}	15–5, etc.		0.5t_{CYK}–15		ns
$\overline{DSTB}$ high-level width	㊴	t_{DSDSH}	15–5, etc.		0.5t_{CYK}–10		ns
$\overline{DSTB}$ low-level width	㊵	t_{DSDSL}	15–6, etc.		$t_{CYK}(n+1)-10$ Note 4		ns
Data hold time (from $\overline{DSTB}$↑)	㊶	t_{HDSD}	15–5, etc.		0		ns
Data hold time (from address/status change point)	㊷	t_{HASD}	15–5		0		ns
Control 1 Note 2 delay time from CLKOUT	㊸	t_{DKCT1}	15–21		0	40	ns
Control 2 Note 3 delay time from CLKOUT	㊹	t_{DKCT2}	15–5, etc.		0	40	ns
Data setup time (to CLKOUT↓)	㊺	t_{SDK}	15–5, etc.		10		ns
Data hold time (from CLKOUT↓)	㊻	t_{HKD}	15–5, etc.		10		ns
Output floating time from $\overline{DSTB}$↓	㊼	t_{DHZ}	15–5, etc.			0	ns
Address/status hold time from $\overline{MWR}$↑	㊽	t_{HMWHA}	15–6		0.5t_{CYK}–15		ns
$\overline{MWR}$ delay time from CLKOUT	㊾	t_{DKMW}	15–6, etc.		0	40	ns
$\overline{MWR}$↓, $\overline{IOWR}$↓ delay time from address/status output	㊿	t_{DAWL}	15–6, etc.		0.5t_{CYK}–15		ns
$\overline{MWR}$, $\overline{IOWR}$ low-level width	(51)	t_{WWL}	15–6, etc.		$t_{CYK}(n+1)-10$ Note 4		ns
Address/status hold time from $\overline{DSTB}$↑	(52)	t_{HDSHA}	15–6, etc.		0.5t_{CYK}–15		ns
Data output delay time from $\overline{DSTB}$↑	(53)	t_{DDSHD}	15–6, etc.		0.5t_{CYK}–15		ns
Data delay time from address/status output	(54)	t_{DAD}	15–6, etc.		0.5t_{CYK}–15		ns
Output setting time from $\overline{DSTB}$↑	(55)	t_{DLZ}	15–6, etc.		0.5t_{CYK}–15		ns

Notes 1. These specifications apply to the following delay times from the falling edge of the CLKOUT signal. *

(1) Address delay time

(2) $\overline{BUSLOCK}$ delay time

(3) Delay time of signals below immediately after release of bus hold:
A23-A0, D15-D0, M/$\overline{IO}$, BUSST1, BUSST0, $\overline{UBE}$, $\overline{BCYST}$, $\overline{DSTB}$.

2. Control 1 applies to the $\overline{MWR}$ and $\overline{IOWR}$ signals in a DMA cycle.
3. Control 2 applies to the $\overline{BUFEN}$, $\overline{INTAK}$ and $\overline{REFRQ}$ setups.
4. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remarks 1. The number in the symbol column correspond to the numbers in the timing charts.

2. Regarding the five specifications ㉜ t_{HRD}, ㉞ t_{HRWD}, ㊶ t_{HDSD}, ㊷ t_{HASD}, and ㊻ t_{HKD}, at least one should be observed.

μPD70236A-16 (V_{DD} = 3.6 to 4.5 V) (3/4)

PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
Data output delay time from CLKOUT↑	⑯	t_{DKD}	15–6, etc.		4	40	ns
Float delay time from CLKOUT	⑰	t_{FK}	15–6, etc.		0	40	ns
$\overline{IORD}$ delay time from CLKOUT	⑱	t_{DKIR}	15–7		0	40	ns
$\overline{IOWR}$ delay time from CLKOUT	⑲	t_{DKIW}	15–8		0	40	ns
$\overline{NMI}$, INTPn (n = 0 to 7), $\overline{CPBUSY}$ setup time (to CLKOUT↓)	⑳	t_{SIK}	15–11		10		ns
$\overline{NMI}$, INTPn(n = 0 to 7), $\overline{CPBUSY}$ hold time (from CLKOUT↓)	㉑	t_{HKI}	15–11		10		ns
$\overline{BS8}$/BS16 setup time (to CLKOUT↑)	㉒	t_{SBSK}	15–13		10		ns
$\overline{BS8}$/BS16 hold time (from CLKOUT↑)	㉓	t_{HKBS}	15–13		10		ns
HLDRQ setup time (to CLKOUT↑)	㉔	t_{SHQK}	15–14		10		ns
HLDRQ hold time (from CLKOUT↑)	㉕	t_{HKHQ}	15–14		15		ns
HLDAK delay time from CLKOUT↑	㉖	t_{DKHA}	15–14		4	40	ns
HLDAK delay time from output float	㉗	t_{DFHA}	15–14		0.5t_{CYK}–15		ns
INTPn(n = 0 to 7) low-level width	㉘	t_{PIPL}	15–17		90		ns
TCTLn (n = 0 to 2) setup time (to CLKOUT↓)	㉙	t_{SGK}	15–18		55		ns
TCTLn (n = 0 to 2) hold time (from CLKOUT↓)	㉚	t_{HKG}	15–18		90		ns
TCTLn (n = 0 to 2) high-level width	㉛	t_{GGH}	15–18, etc.		45		ns
TCTLn (n = 0 to 2) low-level width	㉜	t_{GGL}	15–18, etc.		45		ns
TOUTn (n = 0 to 2) output delay time (from TCTLn (n = 0 to 2)↓)	㉝	t_{DGTO}	15–18, etc.			100	ns
TOUTn (n = 0 to 2) output delay time (from CLKOUT↓)	㉞	t_{DKTO}	15–18			70	ns
TCLK cycle	㉟	t_{CYTK}	15–19		80	DC	ns
TCLK high-level width	㊱	t_{TKTKH}	15–19		30		ns
TCLK low-level width	㊲	t_{TKTKL}	15–19		35		ns
TCLK rise time	㊳	t_{TKR}	15–19			15	ns
TCLK fall time	㊴	t_{TKF}	15–19			15	ns
TCTLn (n = 0 to 2) hold time (from TCLK↑)	㊵	t_{HTKG}	15–19		60		ns
TCTLn (n = 0 to 2) setup time (to TCLK↑)	㊶	t_{SGTK}	15–19		45		ns
TOUTn (n = 0 to 2) output delay time (from TCLK↓)	㊷	t_{DTKTO}	15–19			120	ns
RxD setup time (to SCU internal clock↓)	㊸	t_{SRX}	15–20		700		ns
RxD hold time (from SCU internal clock↓)	㊹	t_{HRX}	15–20		700		ns
TxD delay time from TOUT1↑	㊺	t_{DTX}	15–20			300	ns
$\overline{DMAAK}$n (n = 0 to 3) delay time from CLKOUT↑	㊻	t_{DKHDA}	15–21		0	40	ns
$\overline{MRD}$, $\overline{IORD}$↓ delay time from CLKOUT↓	㊼	t_{DKRL}	15–21		0	40	ns
$\overline{MRD}$, $\overline{IORD}$↑ delay time from CLKOUT↓	㊽	t_{DKRH}	15–21		0	40	ns
$\overline{DMAAK}$n (n = 0 to 3)↑ delay time (from $\overline{IORD}$↑)	㊾	t_{DRHDAH}	15–21		0.5t_{CYK}–15		ns
$\overline{IORD}$↓,$\overline{IOWR}$↓ delay time (from $\overline{DMAAK}$n (n = 0 to 3)↓)	㊿	t_{DDARW}	15–21		0.5t_{CYK}–15		ns

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-16 (V_{DD} = 3.6 to 4.5 V)

(4/4)

PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
$\overline{IORD}$↑ delay time (from $\overline{MWR}$↑) $\overline{MRD}$↑ delay time (from $\overline{IOWR}$↑)	⑨①	t_{DWHRH}	15–21		0		ns
$\overline{IORD}$, $\overline{MRD}$ low-level width	⑨②	t_{RR}	15–21		$t_{CYK}(n+2)-40$ Note 1		ns
$\overline{IOWR}$, $\overline{MWR}$ low-level width (extended write)	⑨③	t_{WW1}	15–21	Extended write	$t_{CYK}(n+2)-40$ Note 1		ns
$\overline{IOWR}$, $\overline{MWR}$ low-level width (normal write)	⑨④	t_{WW2}	15–21	Normal write	$t_{CYK}(n+1)-40$ Note 1		ns
$\overline{TC}$ output delay time (from CLKOUT↑)	⑨⑤	t_{DKTCL}	15–22		0	40	ns
$\overline{TC}$ OFF output delay time (from CLKOUT↑)	⑨⑥	t_{DKTCF}	15–22		0	40	ns
$\overline{TC}$ pull-up delay time (from CLKOUT↑) Note 2	⑨⑦	t_{DKTCH}	15–22	R_{TC} = 1.1 kΩ	0	$2t_{CYK}-15$	ns
$\overline{TC}$ low-level width	⑨⑧	t_{TCTCL}	15–22		$t_{CYK}(n+1)-15$ Note 1		ns
$\overline{END}$ setup time (to CLKOUT↑)	⑨⑨	t_{SEDK}	15–22		15		ns
$\overline{END}$ low-level width	⑩⓪	t_{EDEDL}	15–22		100		ns
DMARQn (n = 0 to 3) setup time (to CLKOUT↑)	⑩①	t_{SDQK}	15–22, etc.		15		ns
$\overline{DMAAK}$n (n = 0 to 3) delay time from CLKOUT↓	⑩②	t_{DKLDA}	15–23		0	40	ns
$\overline{MRD}$ high-level width	⑩③	t_{MRMRH}	15–5		$0.5t_{CYK}-10$		ns
Data set time from $\overline{MRD}$↑	⑩④	t_{DMRHLZ}	15–6, etc.		$0.5t_{CYK}-15$		ns
Data output delay time from $\overline{MRD}$↑	⑩⑤	t_{DMRHD}	15–6, etc.		$0.5t_{CYK}-15$		ns
Cascade address delay time from CLKOUT	⑩⑥	t_{DKCA}	15–15, etc.		3	35	ns
$\overline{INTAK}$ high-level width	⑩⑦	t_{IAIAH}	15–16		$2.5t_{CYK}-10$		ns *
PCLKOUT delay time from CLKOUT	⑩⑧	t_{DKPK}	15–1	CLKC = 00		±5	ns
$\overline{IOWR}$, $\overline{MWR}$↓ delay time from $\overline{MRD}$, $\overline{IORD}$↓	⑩⑨	t_{DRLWL}	15–21	Normal write	$t_{CYK}-15$		ns

Notes 1. n indicates the number of wait clock cycles inserted in the bus cycle.
2. It is assumed that the $\overline{TC}$ pin is connected with the pull-up resistor R_{TC}.

Remark The number in the symbol column correspond to the numbers in the timing charts.

(2) μPD70236A-20 (V_{DD} = 3.6 to 4.5 V)

(1/4)

PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
External clock input cycle	①	t_{CYX}	15–1		31.25	250	ns
External clock input high-level width	②	t_{XKH}	15–1		8		ns
External clock input low-level width	③	t_{XKL}	15–1		8		ns
External clock input rise time	④	t_{XKR}	15–1			7	ns
External clock input fall time	⑤	t_{XKF}	15–1			7	ns
CPU operating frequency	–	fx	–		2	16	MHz
CLKOUT output frequency	⑥	t_{CYK}	15–1		62.5	500	ns
CLKOUT high-level width	⑦	t_{KKH}	15–1		0.5t_{CYK}–10		ns
CLKOUT low-level width	⑧	t_{KKL}	15–1		0.5t_{CYK}–10		ns
CLKOUT rise time	⑨	t_{KR}	15–1	0.2V_{DD} → 0.7V_{DD}		10	ns
CLKOUT fall time	⑩	t_{KF}	15–1	0.7V_{DD} → 0.2V_{DD}		10	ns
CLKOUT delay time (from external clock)	⑪	t_{DXK}	15–1		4	30	ns
PCLKOUT output frequency	⑫	t_{CYPK}	15–1		4t_{CYX}	1000	ns
PCLKOUT high-level width	⑬	t_{PKH}	15–1		2t_{CYX}–10		ns
PCLKOUT low-level width	⑭	t_{PKL}	15–1		2t_{CYX}–10		ns
PCLKOUT output rise time	⑮	t_{PKR}	15–1	0.2V_{DD} → 0.7V_{DD}		10	ns
PCKLOUT output fall time	⑯	t_{PKF}	15–1	0.7V_{DD} → 0.2V_{DD}		10	ns
Input rise time[Note 1]	⑰	t_{IR}		0.7V_{DD} → 0.2V_{DD}		12	ns
Input fall time[Note 1]	⑱	t_{IF}		0.2V_{DD} → 0.7V_{DD}		10	ns
Output rise time[Note 2]	⑲	t_{OR}		0.7V_{DD} → 0.2V_{DD}		12	ns
Output fall time[Note 2]	⑳	t_{OF}		0.2V_{DD} → 0.7V_{DD}		10	ns
$\overline{\text{RESET}}$ setup time (to CLKOUT↓)	㉑	t_{SRSTK}	15–2		30		ns
$\overline{\text{RESET}}$ hold time (from CLKOUT↓)	㉒	t_{HKRST}	15–2		15		ns
RESOUT output delay time (from CLKOUT↓)	㉓	t_{DKRO}	15–2		0	40	ns
$\overline{\text{RESET}}$ low-level width	㉔	t_{WRSTL}	15–2		6t_{CYK}		ns
$\overline{\text{READY}}$ setup time (to CLKOUT↑)	㉕	t_{SRYK}	15–3, etc.		7		ns
$\overline{\text{READY}}$ hold time (from CLKOUT↑)	㉖	t_{HKRY}	15–3, etc.		15		ns
$\overline{\text{BCYST}}$ high-level width	㉗	t_{BCBCH}	15–5, etc.		t_{CYK}(n+1)–10[Note 3]		ns
$\overline{\text{BCYST}}$ low-level width	㉘	t_{BCBCL}	15–5, etc.		t_{CYK}–10		ns
$\overline{\text{BCYST}}$ delay time from CLKOUT↓	㉙	t_{DKBC}	15–5, etc.		4	35	ns
$\overline{\text{MRD}}$ delay time from CLKOUT	㉚	t_{DKMR}	15–5, etc.		0	40	ns

Notes 1. Except external clock and $\overline{\text{RESET}}$

2. Except CLKOUT and PCLKOUT

3. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-20 (V_{DD} = 3.6 to 4.5 V)

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PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
$\overline{MRD}$↓, $\overline{IORD}$↓ delay time from address/status output	㉛	t_{DARL}	15–5, etc.		0.5t_{CYK}–15		ns
Data hold time (from $\overline{MRD}$↑, from $\overline{IORD}$↑)	㉜	t_{HRD}	15–5, etc.		0		ns
Address delay time from CLKOUT↓ Note 1	㉝	t_{DKA}	15–5, etc.		3	35	ns
Data hold time (from R/$\overline{W}$↓)	㉞	t_{HRWD}	15–5		0		ns
Status delay time from CLKOUT↓	㉟	t_{DKST}	15–5, etc.		4	35	ns
$\overline{DSTB}$↓ output delay time from CLKOUT↑	㊱	t_{DKDS}	15–5, etc.		5	45	ns
$\overline{DSTB}$↑ output delay time from CLKOUT	㊲	t_{DKDSH}	15–5, etc.		4	40	ns
$\overline{DSTB}$↓ delay time from address/status output	㊳	t_{DADSL}	15–5, etc.		0.5t_{CYK}–15		ns
$\overline{DSTB}$ high-level width	㊴	t_{DSDSH}	15–5, etc.		0.5t_{CYK}–10		ns
$\overline{DSTB}$ low-level width	㊵	t_{DSDSL}	15–6, etc.		$t_{CYK}(n+1)$–10 Note 4		ns
Data hold time (from $\overline{DSTB}$↑)	㊶	t_{HDSD}	15–5, etc.		0		ns
Data hold time (from address/status change point)	㊷	t_{HASD}	15–5		0		ns
Control 1 Note 2 delay time from CLKOUT	㊸	t_{DKCT1}	15–21		0	40	ns
Control 2 Note 3 delay time from CLKOUT	㊹	t_{DKCT2}	15–5, etc.		0	40	ns
Data setup time (to CLKOUT↓)	㊺	t_{SDK}	15–5, etc.		10		ns
Data hold time (from CLKOUT↓)	㊻	t_{HKD}	15–5, etc.		10		ns
Output floating time from $\overline{DSTB}$↓	㊼	t_{DHZ}	15–5, etc.			0	ns
Address/status hold time from $\overline{MWR}$↑	㊽	t_{HMWHA}	15–6		0.5t_{CYK}–15		ns
$\overline{MWR}$ delay time from CLKOUT	㊾	t_{DKMW}	15–6, etc.		0	40	ns
$\overline{MWR}$↓, $\overline{IOWR}$↓ delay time from address/status output	㊿	t_{DAWL}	15–6, etc.		0.5t_{CYK}–15		ns
$\overline{MWR}$, $\overline{IOWR}$ low-level width	(51)	t_{WWL}	15–6, etc.		$t_{CYK}(n+1)$–10 Note 4		ns
Address/status hold time from $\overline{DSTB}$↑	(52)	t_{HDSHA}	15–6, etc.		0.5t_{CYK}–15		ns
Data output delay time from $\overline{DSTB}$↑	(53)	t_{DDSHD}	15–6, etc.		0.5t_{CYK}–15		ns
Data delay time from address/status output	(54)	t_{DAD}	15–6, etc.		0.5t_{CYK}–15		ns
Output setting time from $\overline{DSTB}$↑	(55)	t_{DLZ}	15–6, etc.		0.5t_{CYK}–15		ns

Notes 1. These specifications apply to the following delay times from the falling edge of the CLKOUT signal. *

(1) Address delay time

(2) $\overline{BUSLOCK}$ delay time

(3) Delay time of signals below immediately after release of bus hold:
A23-A0, D15-D0, M/$\overline{IO}$, BUSST1, BUSST0, $\overline{UBE}$, $\overline{BCYST}$, $\overline{DSTB}$.

2. Control 1 applies to the $\overline{MWR}$ and $\overline{IOWR}$ signals in a DMA cycle.
3. Control 2 applies to the $\overline{BUFEN}$, $\overline{INTAK}$ and $\overline{REFRQ}$ setups.
4. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remarks 1. The number in the symbol column correspond to the numbers in the timing charts.

2. Regarding the five specifications ㉜ t_{HRD}, ㉞ t_{HRWD}, ㊶ t_{HDSD}, ㊷ t_{HASD}, and ㊻ t_{HKD}, at least one should be observed.

μPD70236A-20 (V_{DD} = 3.6 to 4.5 V)

(3/4)

PARAMETER	SYMBOL	FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
				MIN.	MAX.	
Data output delay time from CLKOUT↑	⑯ t_{DKD}	15–6, etc.		4	40	ns
Float delay time from CLKOUT	⑰ t_{FK}	15–6, etc.		0	40	ns
$\overline{IORD}$ delay time from CLKOUT	⑱ t_{DKIR}	15–7		0	40	ns
$\overline{IOWR}$ delay time from CLKOUT	⑲ t_{DKIW}	15–8		0	40	ns
$\overline{NMI}$, INTPn (n = 0 to 7), $\overline{CPBUSY}$ setup time (to CLKOUT↓)	⑳ t_{SIK}	15–11		10		ns
$\overline{NMI}$, INTPn(n = 0 to 7), $\overline{CPBUSY}$ hold time (from CLKOUT↓)	㉑ t_{HKI}	15–11		10		ns
$\overline{BS8}$/BS16 setup time (to CLKOUT↑)	㉒ t_{SBSK}	15–13		10		ns
$\overline{BS8}$/BS16 hold time (from CLKOUT↑)	㉓ t_{HKBS}	15–13		10		ns
HLDRQ setup time (to CLKOUT↑)	㉔ t_{SHQK}	15–14		10		ns
HLDRQ hold time (from CLKOUT↑)	㉕ t_{HKHQ}	15–14		15		ns
HLDAK delay time from CLKOUT↑	㉖ t_{DKHA}	15–14		4	40	ns
HLDAK delay time from output float	㉗ t_{DFHA}	15–14		0.5t_{CYK}–15		ns
INTPn(n = 0 to 7) low-level width	㉘ t_{IPIPL}	15–17		90		ns
TCTLn (n = 0 to 2) setup time (to CLKOUT↓)	㉙ t_{SGK}	15–18		55		ns
TCTLn (n = 0 to 2) hold time (from CLKOUT↓)	㉚ t_{HKG}	15–18		90		ns
TCTLn (n = 0 to 2) high-level width	㉛ t_{GGH}	15–18, etc.		45		ns
TCTLn (n = 0 to 2) low-level width	㉜ t_{GGL}	15–18, etc.		45		ns
TOUTn (n = 0 to 2) output delay time (from TCTLn (n = 0 to 2)↓)	㉝ t_{DGTO}	15–18, etc.			100	ns
TOUTn (n = 0 to 2) output delay time (from CLKOUT↓)	㉞ t_{DKTO}	15–18			70	ns
TCLK cycle	㉟ t_{CYTK}	15–19		62.5	DC	ns
TCLK high-level width	㊱ t_{TKTKH}	15–19		25		ns
TCLK low-level width	㊲ t_{TKTKL}	15–19		30		ns
TCLK rise time	㊳ t_{TKR}	15–19			15	ns
TCLK fall time	㊴ t_{TKF}	15–19			15	ns
TCTLn (n = 0 to 2) hold time (from TCLK↑)	㊵ t_{HTKG}	15–19		60		ns
TCTLn (n = 0 to 2) setup time (to TCLK↑)	㊶ t_{SGTK}	15–19		45		ns
TOUTn (n = 0 to 2) output delay time (from TCLK↓)	㊷ t_{DTKTO}	15–19			120	ns
RxD setup time (to SCU internal clock↓)	㊸ t_{SRX}	15–20		700		ns
RxD hold time (from SCU internal clock↓)	㊹ t_{HRX}	15–20		700		ns
TxD delay time from TOUT1↑	㊺ t_{DTX}	15–20			300	ns
$\overline{DMAAK}$n (n = 0 to 3) delay time from CLKOUT↑	㊻ t_{DKHDA}	15–21		0	40	ns
$\overline{MRD}$, $\overline{IORD}$↓ delay time from CLKOUT↓	㊼ t_{DKRL}	15–21		0	40	ns
$\overline{MRD}$, $\overline{IORD}$↑ delay time from CLKOUT↓	㊽ t_{DKRH}	15–21		0	40	ns
$\overline{DMAAK}$n (n = 0 to 3)↑ delay time (from $\overline{IORD}$↑)	㊾ t_{DRHDAH}	15–21		0.5t_{CYK}–15		ns
$\overline{IORD}$↓,$\overline{IOWR}$↓ delay time (from $\overline{DMAAK}$n (n = 0 to 3)↓)	㊿ t_{DDARW}	15–21		0.5t_{CYK}–15		ns

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-20 (V_{DD} = 3.6 to 4.5 V)

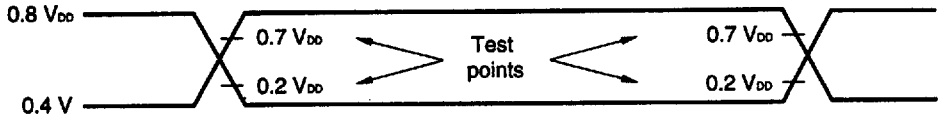
(4/4)

PARAMETER		SYMBOL	FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
$\overline{IORD}$↑ delay time (from $\overline{MWR}$↑) $\overline{MRD}$↑ delay time (from $\overline{IOWR}$↑)	⑨①	t_{DWHRH}	15–21		0		ns
$\overline{IORD}$, $\overline{MRD}$ low-level width	⑨②	t_{RR}	15–21		$t_{CYK}(n+2)-40$ Note 1		ns
$\overline{IOWR}$, $\overline{MWR}$ low-level width (extended write)	⑨③	t_{WW1}	15–21	Extended write	$t_{CYK}(n+2)-40$ Note 1		ns
$\overline{IOWR}$, $\overline{MWR}$ low-level width (normal write)	⑨④	t_{WW2}	15–21	Normal write	$t_{CYK}(n+1)-40$ Note 1		ns
$\overline{TC}$ output delay time (from CLKOUT↑)	⑨⑤	t_{DKTCL}	15–22		0	40	ns
$\overline{TC}$ OFF output delay time (from CLKOUT↑)	⑨⑥	t_{DKTCF}	15–22		0	40	ns
$\overline{TC}$ pull-up delay time (from CLKOUT↑) Note 2	⑨⑦	t_{DKTCH}	15–22	R_{TC} = 1.1 kΩ	0	$2t_{CYK}-15$	ns
$\overline{TC}$ low-level width	⑨⑧	t_{TCTCL}	15–22		$t_{CYK}(n+1)-15$ Note 1		ns
$\overline{END}$ setup time (to CLKOUT↑)	⑨⑨	t_{SEDK}	15–22		15		ns
$\overline{END}$ low-level width	⑩⓪	t_{EDEDL}	15–22		100		ns
DMARQn (n = 0 to 3) setup time (to CLKOUT↑)	⑩①	t_{SDQK}	15–22, etc.		15		ns
$\overline{DMAAK}$n (n = 0 to 3) delay time from CLKOUT↓	⑩②	t_{DKLDA}	15–23		0	40	ns
$\overline{MRD}$ high-level width	⑩③	t_{MRMRH}	15–5		$0.5t_{CYK}-10$		ns
Data set time from $\overline{MRD}$↑	⑩④	t_{DMRHLZ}	15–6, etc.		$0.5t_{CYK}-15$		ns
Data output delay time from $\overline{MRD}$↑	⑩⑤	t_{DMRHD}	15–6, etc.		$0.5t_{CYK}-15$		ns
Cascade address delay time from CLKOUT	⑩⑥	t_{DKCA}	15–15, etc.		3	35	ns
$\overline{INTAK}$ high-level width	⑩⑦	t_{IAIAH}	15–16		$2.5t_{CYK}-10$		ns *
PCLKOUT delay time from CLKOUT	⑩⑧	t_{DKPK}	15–1	CLKC = 00		±5	ns
$\overline{IOWR}$, $\overline{MWR}$↓ delay time from $\overline{MRD}$, $\overline{IORD}$↓	⑩⑨	t_{DRLWL}	15–21	Normal write	$t_{CYK}-15$		ns

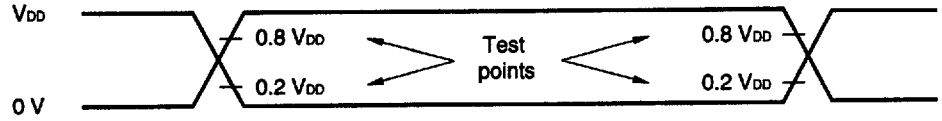
Notes 1. n indicates the number of wait clock cycles inserted in the bus cycle.
2. It is assumed that the $\overline{TC}$ pin is connected with the pull-up resistor R_{TC}.

Remark The number in the symbol column correspond to the numbers in the timing charts.

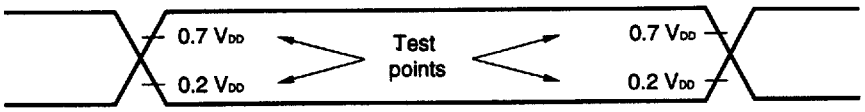
AC Test Input Waveform (Except X1)



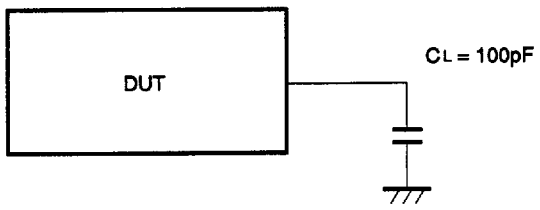
AC Test Input Waveform (X1)



AC Test Output Test Points



Load Conditions



Caution **If the load capacitance exceeds 100 pF due to the construction of the circuit, the load capacitance of this device should be reduced to 100 pF or less by insertion of a buffer, etc.**

15.3 SPECIFICATIONS WHEN V_{DD} = 2.7 TO 3.6 V

Absolute Maximum Ratings (T_A = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATING	UNIT
Supply voltage	V_{DD}		−0.5 to +7.0	V
Input voltage	V_I	Except X1, V_{DD} = 2.7 to 3.6 V	−0.5 to V_{DD} +0.3	V
Clock input voltage	V_K	X1, V_{DD} = 2.7 to 3.6 V	−0.5 to V_{DD} +1.0	V
Output short current	I_{OS}		50	mA
Output voltage	V_O	V_{DD} = 2.7 to 3.6 V	−0.5 to V_{DD} +0.3	V
Operating ambient temperature	T_A		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

Cautions

1. **Do not connect output pin (or I/O pin) of IC product directly to other output pins, V_{DD}, V_{CC} or GND. Open drain output pins or open collector output pins, however, can be connected each other. Output pins having high impedance capability can be also connected each other in an external circuit designed the timing to prevent output conflict.**
2. **Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics.**

DC Characteristics (T_A = – 40 to +85 °C, V_{DD} = 2.7 to 3.6 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input voltage, high	V_{IH}	Except $\overline{RESET}$	0.7 V_{DD}		V_{DD}+0.3	V
		$\overline{RESET}$	0.8 V_{DD}		V_{DD}+0.3	V
Input voltage, low	V_{IL}	Except $\overline{RESET}$	–0.5		0.2 V_{DD}	V
		$\overline{RESET}$	–0.5		0.2 V_{DD}	V
Clock input voltage, high	V_{KH}	X2, X1	0.8 V_{DD}		V_{DD}+0.5	V
Clock input voltage, low	V_{KL}	X2, X1	–0.5		0.14 V_{DD}	V
Output voltage, high	V_{OH}	I_{OH} = –2.5 mA	0.7 V_{DD}			V
		I_{OH} = –100 μA	V_{DD}–0.4			V
Output voltage, low	V_{OL}	I_{OL} = 2.5 mA			0.4	V
Input leak current, high	I_{LIH}	V_I = V_{DD}			10	μA
Input leak current, low	I_{LIL}	V_I = 0 V			–10	μA
Output leak current, high	I_{LOH}	V_O = V_{DD}			10	μA
Output leak current, low	I_{LOL}	V_O = 0 V			–10	μA
High-level latch leakage current	I_{LLH}	V_I = 2.5 V	0		–200	μA
Low-level latch leakage current	I_{LLL}	V_I = 0.8 V	0		200	μA
Latch inversion current (L → H)	I_{ILH}				200	μA
Latch inversion current (H → L)	I_{ILL}				–200	μA
* Supply current[Note]	I_{DD}	In operation (fx = 2 to 10 MHz)		2.2fx + 2	4fx + 5	mA
		HALT (fx = 2 to 10 MHz)		0.035fx+ 0.2	0.35fx+1.5	mA
		STOP		3.0	100	μA

Note Setting condition : The CPU clock is used for the TCLK0 to TCLK2 with refreshing enabled. The units of the constants 2.2, 4, 0.035 and 0.35 are mA/MHz.

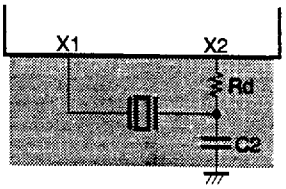
Remark The TYP. values are the reference values when T_A = 25 °C and V_{DD} = 3.0 V.

Capacitance (T_A = 25 °C, V_{DD} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_I	fc = 1 MHz Unmeasured pins returned to 0 V.			15	pF
Input output capacitance	C_{IO}				15	pF
Output capacitance	C_O				15	pF

Recommended Oscillator Circuit

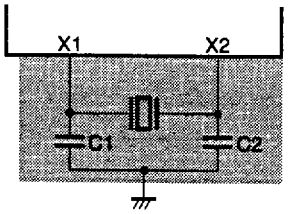
(a) Ceramic resonator connection (T_A = –40 to +85 °C, V_{DD} = 2.8 to 3.6 V)



MANUFACTURER	OSCILLATOR FREQUENCY fxx [MHz]	PRODUCT NAME	RECOMMENDED CONSTANT		
			C1 [pF]	C2 [pF]	Rd [Ω]
Murata Mfg. Co., Ltd.	20	CSA20.00MXZ040	—	5	33

Cautions
1. **The oscillation circuit should be located as close as possible to the X1 and X2 pins.**
2. **No other signal lines should cross the shaded area.**
3. **Sufficient evaluation is required for matching between the μPD70236A and the resonator.**

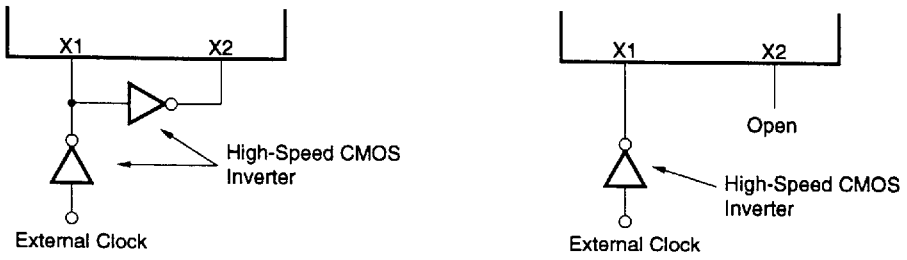
(b) Crystal resonator connection (T_A = –40 to +85 °C, V_{DD} = 2.7 to 3.6 V) : Recommended conditions of oscillation with basic wave



MANUFACTURER	OSCILLATOR FREQUENCY fxx [MHz]	PRODUCT NAME	RECOMMENDED CONSTANT	
			C1 [pF]	C2 [pF]
Kinseki, Ltd.	20	HC-49/U	10	10
	16		20	20

Cautions
1. **The oscillation circuit should be located as close as possible to the X1 and X2 pins.**
2. **No other signal lines should cross the shaded area.**
3. **Sufficient evaluation is required for matching between the μPD70236A and the resonator.**

(c) External clock input



Cautions
1. **The high-speed CMOS inverter should be located as close as possible to the X1 and X2 pins.**
2. **Ensure that matching between the μPD70236A and the high-speed CMOS inverter is fully evaluated.**

AC Characteristics (V_{DD} = 2.7 to 3.6 V, Output pin load capacitance : C_L = 100 pF)

(1) μPD70236A-16 (V_{DD} = 2.7 to 3.6 V)

(1/4)

PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
External clock input cycle	①	t_{CYX}	15–1		62.5	250	ns
External clock input high-level width	②	t_{XKH}	15–1		20		ns
External clock input low-level width	③	t_{XKL}	15–1		20		ns
External clock input rise time	④	t_{XKR}	15–1			10	ns
External clock input fall time	⑤	t_{XKF}	15–1			10	ns
CPU operating frequency	–	f_X	–		2	8	MHz
CLKOUT output frequency	⑥	t_{CYK}	15–1		125	500	ns
CLKOUT high-level width	⑦	t_{KKH}	15–1		0.5t_{CYK}–20		ns
CLKOUT low-level width	⑧	t_{KKL}	15–1		0.5t_{CYK}–20		ns
CLKOUT rise time	⑨	t_{KR}	15–1	0.2V_{DD} → 0.7V_{DD}		20	ns
CLKOUT fall time	⑩	t_{KF}	15–1	0.7V_{DD} → 0.2V_{DD}		20	ns
CLKOUT delay time (from external clock)	⑪	t_{DXK}	15–1		5	50	ns
PCLKOUT output frequency	⑫	t_{CYPK}	15–1		4t_{CYX}	1000	ns
PCLKOUT high-level width	⑬	t_{PKH}	15–1		2t_{CYX}–20		ns
PCLKOUT low-level width	⑭	t_{PKL}	15–1		2t_{CYX}–20		ns
PCLKOUT output rise time	⑮	t_{PKR}	15–1	0.2V_{DD} →0.7V_{DD}		20	ns
PCKLOUT output fall time	⑯	t_{PKF}	15–1	0.7V_{DD} → 0.2V_{DD}		20	ns
Input rise time[Note 1]	⑰	t_{IR}		0.7V_{DD} → 0.2V_{DD}		15	ns
Input fall time[Note 1]	⑱	t_{IF}		0.2V_{DD} → 0.7V_{DD}		10	ns
Output rise time[Note 2]	⑲	t_{OR}		0.7V_{DD} → 0.2V_{DD}		15	ns
Output fall time[Note 2]	⑳	t_{OF}		0.2V_{DD} → 0.7V_{DD}		10	ns
$\overline{\text{RESET}}$ setup time (to CLKOUT↓)	㉑	t_{SRSTK}	15–2		30		ns
$\overline{\text{RESET}}$ hold time (from CLKOUT↓)	㉒	t_{HKRST}	15–2		15		ns
RESOUT output delay time (from CLKOUT↓)	㉓	t_{DKRO}	15–2		0	60	ns
$\overline{\text{RESET}}$ low-level width	㉔	t_{WRSTL}	15–2		6t_{CYK}		ns
$\overline{\text{READY}}$ setup time (to CLKOUT↑)	㉕	t_{SRYK}	15–3, etc.		10		ns
$\overline{\text{READY}}$ hold time (from CLKOUT↑)	㉖	t_{HKRY}	15–3, etc.		20		ns
$\overline{\text{BCYST}}$ high-level width	㉗	t_{BCBCH}	15–5, etc.		t_{CYK}(n+1)–15[Note 3]		ns
$\overline{\text{BCYST}}$ low-level width	㉘	t_{BCBCL}	15–5, etc.		t_{CYK}–15		ns
$\overline{\text{BCYST}}$ delay time from CLKOUT↓	㉙	t_{DKBC}	15–5, etc.		5	40	ns
$\overline{\text{MRD}}$ delay time from CLKOUT	㉚	t_{DKMR}	15–5, etc.		0	60	ns

Notes 1. Except external clock and $\overline{\text{RESET}}$
2. Except CLKOUT and PCLKOUT
3. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-16 (V_{DD} = 2.7 to 3.6 V)

(2/4)

PARAMETER	SYMBOL	FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C MIN.	T_A = −40 to +85 °C MAX.	UNIT
$\overline{MRD}\downarrow$, $\overline{IORD}\downarrow$ delay time from address/status output	(31) t_{DARL}	15–5, etc.		0.5t_{CYK}–20		ns
Data hold time (from $\overline{MRD}\uparrow$, from $\overline{IORD}\uparrow$)	(32) t_{HRD}	15–5, etc.		0		ns
Address delay time from CLKOUT↓ Note 1	(33) t_{DKA}	15–5, etc.		4	45	ns
Data hold time (from R/$\overline{W}\downarrow$)	(34) t_{HRWD}	15–5		0		ns
Status delay time from CLKOUT↓	(35) t_{DKST}	15–5, etc.		5	45	ns
$\overline{DSTB}\downarrow$ output delay time from CLKOUT↑	(36) t_{DKDS}	15–5, etc.		5	60	ns
$\overline{DSTB}\uparrow$ output delay time from CLKOUT	(37) t_{DKDSH}	15–5, etc.		5	50	ns
$\overline{DSTB}\downarrow$ delay time from address/status output	(38) t_{DADSL}	15–5, etc.		0.5t_{CYK}–20		ns
$\overline{DSTB}$ high-level width	(39) t_{DSDSH}	15–5, etc.		0.5t_{CYK}–15		ns
$\overline{DSTB}$ low-level width	(40) t_{DSDSL}	15–6, etc.		$t_{CYK}(n+1)$–15 Note 4		ns
Data hold time (from $\overline{DSTB}\uparrow$)	(41) t_{HDSD}	15–5, etc.		0		ns
Data hold time (from address/status change point)	(42) t_{HASD}	15–5		0		ns
Control 1 Note 2 delay time from CLKOUT	(43) t_{DKCT1}	15–21		0	60	ns
Control 2 Note 3 delay time from CLKOUT	(44) t_{DKCT2}	15–5, etc.		0	60	ns
Data setup time (to CLKOUT↓)	(45) t_{SDK}	15–5, etc.		10		ns
Data hold time (from CLKOUT↓)	(46) t_{HKD}	15–5, etc.		10		ns
Output floating time from $\overline{DSTB}\downarrow$	(47) t_{DHZ}	15–5, etc.			0	ns
Address/status hold time from $\overline{MWR}\uparrow$	(48) t_{HMWHA}	15–6		0.5t_{CYK}–20		ns
$\overline{MWR}$ delay time from CLKOUT	(49) t_{DKMW}	15–6, etc.		0	60	ns
$\overline{MWR}\downarrow$, $\overline{IOWR}\downarrow$ delay time from address/status output	(50) t_{DAWL}	15–6, etc.		0.5t_{CYK}–20		ns
$\overline{MWR}$, $\overline{IOWR}$ low-level width	(51) t_{WWL}	15–6, etc.		$t_{CYK}(n+1)$–15 Note 4		ns
Address/status hold time from $\overline{DSTB}\uparrow$	(52) t_{HDSHA}	15–6, etc.		0.5t_{CYK}–20		ns
Data output delay time from $\overline{DSTB}\uparrow$	(53) t_{DDSHD}	15–6, etc.		0.5t_{CYK}–20		ns
Data delay time from address/status output	(54) t_{DAD}	15–6, etc.		0.5t_{CYK}–20		ns
Output setting time from $\overline{DSTB}\uparrow$	(55) t_{DLZ}	15–6, etc.		0.5t_{CYK}–20		ns

Notes 1. These specifications apply to the following delay times from the falling edge of the CLKOUT signal. *

(1) Address delay time

(2) $\overline{BUSLOCK}$ delay time

(3) Delay time of signals below immediately after release of bus hold:
A23-A0, D15-D0, M/$\overline{IO}$, BUSST1, BUSST0, $\overline{UBE}$, $\overline{BCYST}$, $\overline{DSTB}$.

2. Control 1 applies to the $\overline{MWR}$ and $\overline{IOWR}$ signals in a DMA cycle.
3. Control 2 applies to the $\overline{BUFEN}$, $\overline{INTAK}$ and $\overline{REFRQ}$ setups.
4. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remarks 1. The number in the symbol column correspond to the numbers in the timing charts.

2. Regarding the five specifications (32) t_{HRD}, (34) t_{HRWD}, (41) t_{HDSD}, (42) t_{HASD}, and (46) t_{HKD}, at least one should be observed.

μPD70236A-16 (V_{DD} = 2.7 to 3.6 V) (3/4)

PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
Data output delay time from CLKOUT↑	㊺	t_{DKD}	15–6, etc.		5	60	ns
Float delay time from CLKOUT	㊼	t_{FK}	15–6, etc.		0	60	ns
$\overline{IORD}$ delay time from CLKOUT	㊽	t_{DKIR}	15–7		0	60	ns
$\overline{IOWR}$ delay time from CLKOUT	㊾	t_{DKIW}	15–8		0	60	ns
$\overline{NMI}$, INTPn (n = 0 to 7), $\overline{CPBUSY}$ setup time (to CLKOUT↓)	㊿	t_{SIK}	15–11		10		ns
$\overline{NMI}$, INTPn(n = 0 to 7), $\overline{CPBUSY}$ hold time (from CLKOUT↓)	(61)	t_{HKI}	15–11		5		ns
$\overline{BS8}$/BS16 setup time (to CLKOUT↑)	(62)	t_{SBSK}	15–13		5		ns
$\overline{BS8}$/BS16 hold time (from CLKOUT↑)	(63)	t_{HKBS}	15–13		5		ns
HLDRQ setup time (to CLKOUT↑)	(64)	t_{SHQK}	15–14		5		ns
HLDRQ hold time (from CLKOUT↑)	(65)	t_{HKHQ}	15–14		20		ns
HLDAK delay time from CLKOUT↑	(66)	t_{DKHA}	15–14		5	45	ns
HLDAK delay time from output float	(67)	t_{DFHA}	15–14		0.5t_{CYK}–20		ns
INTPn(n = 0 to 7) low-level width	(68)	t_{IPIPL}	15–17		100		ns
TCTLn (n = 0 to 2) setup time (to CLKOUT↓)	(69)	t_{SGK}	15–18		100		ns
TCTLn (n = 0 to 2) hold time (from CLKOUT↓)	(70)	t_{HKG}	15–18		100		ns
TCTLn (n = 0 to 2) high-level width	(71)	t_{GGH}	15–18, etc.		50		ns
TCTLn (n = 0 to 2) low-level width	(72)	t_{GGL}	15–18, etc.		50		ns
TOUTn (n = 0 to 2) output delay time (from TCTLn (n = 0 to 2)↓)	(73)	t_{DGTO}	15–18, etc.			120	ns
TOUTn (n = 0 to 2) output delay time (from CLKOUT↓)	(74)	t_{DKTO}	15–18			100	ns
TCLK cycle	(75)	t_{CYTK}	15–19		125	DC	ns
TCLK high-level width	(76)	t_{TKTKH}	15–19		30		ns
TCLK low-level width	(77)	t_{TKTKL}	15–19		45		ns
TCLK rise time	(78)	t_{TKR}	15–19			15	ns
TCLK fall time	(79)	t_{TKF}	15–19			15	ns
TCTLn (n = 0 to 2) hold time (from TCLK↑)	(80)	t_{HTKG}	15–19		100		ns
TCTLn (n = 0 to 2) setup time (to TCLK↑)	(81)	t_{SGTK}	15–19		50		ns
TOUTn (n = 0 to 2) output delay time (from TCLK↓)	(82)	t_{DTKTO}	15–19			150	ns
RxD setup time (to SCU internal clock↓)	(83)	t_{SRX}	15–20		100		ns
RxD hold time (from SCU internal clock↓)	(84)	t_{HRX}	15–20		100		ns
TxD delay time from TOUT1↑	(85)	t_{DTX}	15–20			500	ns
$\overline{DMAAK}$n (n = 0 to 3) delay time from CLKOUT↑	(86)	t_{DKHDA}	15–21		0	60	ns
$\overline{MRD}$, $\overline{IORD}$↓ delay time from CLKOUT↓	(87)	t_{DKRL}	15–21		0	60	ns
$\overline{MRD}$, $\overline{IORD}$↑ delay time from CLKOUT↓	(88)	t_{DKRH}	15–21		0	60	ns
$\overline{DMAAK}$n (n = 0 to 3)↑ delay time (from $\overline{IORD}$↑)	(89)	t_{DRHDAH}	15–21		0.5t_{CYK}–20		ns
$\overline{IORD}$↓,$\overline{IOWR}$↓ delay time (from $\overline{DMAAK}$n (n = 0 to 3)↓)	(90)	t_{DDARW}	15–21		0.5t_{CYK}–20		ns

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-16 (V_{DD} = 2.7 to 3.6 V)

(4/4)

PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C MIN.	MAX.	UNIT
$\overline{IORD}$↑ delay time (from $\overline{MWR}$↑) $\overline{MRD}$↑ delay time (from $\overline{IOWR}$↑)	⑨①	t_{DWHRH}	15–21		0		ns
$\overline{IORD}$, $\overline{MRD}$ low-level width	⑨②	t_{RR}	15–21		$t_{CYK}(n+2)-60$ Note 1		ns
$\overline{IOWR}$, $\overline{MWR}$ low-level width (extended write)	⑨③	t_{WW1}	15–21	Extended write	$t_{CYK}(n+2)-60$ Note 1		ns
$\overline{IOWR}$, $\overline{MWR}$ low-level width (normal write)	⑨④	t_{WW2}	15–21	Normal write	$t_{CYK}(n+1)-60$ Note 1		ns
$\overline{TC}$ output delay time (from CLKOUT↑)	⑨⑤	t_{DKTCL}	15–22		0	60	ns
$\overline{TC}$ OFF output delay time (from CLKOUT↑)	⑨⑥	t_{DKTCF}	15–22		0	60	ns
$\overline{TC}$ pull-up delay time (from CLKOUT↑) Note 2	⑨⑦	t_{DKTCH}	15–22	R_{TC} = 2.2 kΩ	0	$2t_{CYK}-20$	ns
$\overline{TC}$ low-level width	⑨⑧	t_{TCTCL}	15–22		$t_{CYK}(n+1)-25$ Note 1		ns
$\overline{END}$ setup time (to CLKOUT↑)	⑨⑨	t_{SEDK}	15–22		20		ns
$\overline{END}$ low-level width	⑩⓪	t_{EDEDL}	15–22		100		ns
DMARQn (n = 0 to 3) setup time (to CLKOUT↑)	⑩①	t_{SDQK}	15–22, etc.		20		ns
$\overline{DMAAK}$n (n = 0 to 3) delay time from CLKOUT↓	⑩②	t_{DKLDA}	15–23		0	60	ns
$\overline{MRD}$ high-level width	⑩③	t_{MRMRH}	15–5		$0.5t_{CYK}-15$		ns
Data set time from $\overline{MRD}$↑	⑩④	t_{DMRHLZ}	15–6, etc.		$0.5t_{CYK}-20$		ns
Data output delay time from $\overline{MRD}$↑	⑩⑤	t_{DMRHD}	15–6, etc.		$0.5t_{CYK}-20$		ns
Cascade address delay time from CLKOUT	⑩⑥	t_{DKCA}	15–15, etc.		4	45	ns
$\overline{INTAK}$ high-level width	⑩⑦	t_{IAIAH}	15–16		$2.5t_{CYK}-15$		ns *
PCLKOUT delay time from CLKOUT	⑩⑧	t_{DKPK}	15–1	CLKC = 00		±5	ns
$\overline{IOWR}$, $\overline{MWR}$↓ delay time from $\overline{MRD}$, $\overline{IORD}$↓	⑩⑨	t_{DRLWL}	15–21	Normal write	$t_{CYK}-20$		ns

Notes 1. n indicates the number of wait clock cycles inserted in the bus cycle.
2. It is assumed that the $\overline{TC}$ pin is connected with the pull-up resistor R_{TC}.

Remark The number in the symbol column correspond to the numbers in the timing charts.

(2) μPD70236A-20 (V_{DD} = 2.7 to 3.6 V)

(1/4)

PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
External clock input cycle	①	t_{CYX}	15–1		50	250	ns
External clock input high-level width	②	t_{XKH}	15–1		15		ns
External clock input low-level width	③	t_{XKL}	15–1		15		ns
External clock input rise time	④	t_{XKR}	15–1			10	ns
External clock input fall time	⑤	t_{XKF}	15–1			10	ns
CPU operating frequency	–	fx	–		2	10	MHz
CLKOUT output frequency	⑥	t_{CYK}	15–1		100	500	ns
CLKOUT high-level width	⑦	t_{KKH}	15–1		0.5t_{CYK}–20		ns
CLKOUT low-level width	⑧	t_{KKL}	15–1		0.5t_{CYK}–20		ns
CLKOUT rise time	⑨	t_{KR}	15–1	0.2V_{DD} → 0.7V_{DD}		20	ns
CLKOUT fall time	⑩	t_{KF}	15–1	0.7V_{DD} → 0.2V_{DD}		20	ns
CLKOUT delay time (from external clock)	⑪	t_{DXK}	15–1		5	50	ns
PCLKOUT output frequency	⑫	t_{CYPK}	15–1		4t_{CYX}	1000	ns
PCLKOUT high-level width	⑬	t_{PKH}	15–1		2t_{CYX}–20		ns
PCLKOUT low-level width	⑭	t_{PKL}	15–1		2t_{CYX}–20		ns
PCLKOUT output rise time	⑮	t_{PKR}	15–1	0.2V_{DD} → 0.7V_{DD}		20	ns
PCKLOUT output fall time	⑯	t_{PKF}	15–1	0.7V_{DD} → 0.2V_{DD}		20	ns
Input rise time[Note 1]	⑰	t_{IR}		0.7V_{DD} → 0.2V_{DD}		15	ns
Input fall time[Note 1]	⑱	t_{IF}		0.2V_{DD} → 0.7V_{DD}		10	ns
Output rise time[Note 2]	⑲	t_{OR}		0.7V_{DD} → 0.2V_{DD}		15	ns
Output fall time[Note 2]	⑳	t_{OF}		0.2V_{DD} → 0.7V_{DD}		10	ns
$\overline{RESET}$ setup time (to CLKOUT↓)	㉑	t_{SRSTK}	15–2		30		ns
$\overline{RESET}$ hold time (from CLKOUT↓)	㉒	t_{HKRST}	15–2		15		ns
RESOUT output delay time (from CLKOUT↓)	㉓	t_{DKRO}	15–2		0	60	ns
$\overline{RESET}$ low-level width	㉔	t_{WRSTL}	15–2		6t_{CYK}		ns
$\overline{READY}$ setup time (to CLKOUT↑)	㉕	t_{SRYK}	15–3, etc.		10		ns
$\overline{READY}$ hold time (from CLKOUT↑)	㉖	t_{HKRY}	15–3, etc.		20		ns
$\overline{BCYST}$ high-level width	㉗	t_{BCBCH}	15–5, etc.		t_{CYK}(n+1)–15[Note 3]		ns
$\overline{BCYST}$ low-level width	㉘	t_{BCBCL}	15–5, etc.		t_{CYK}–15		ns
$\overline{BCYST}$ delay time from CLKOUT↓	㉙	t_{DKBC}	15–5, etc.		5	40	ns
$\overline{MRD}$ delay time from CLKOUT	㉚	t_{DKMR}	15–5, etc.		0	60	ns

Notes 1. Except external clock and $\overline{RESET}$
2. Except CLKOUT and PCLKOUT
3. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-20 (V_{DD} = 2.7 to 3.6 V)

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PARAMETER	SYMBOL	FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
				MIN.	MAX.	
$\overline{MRD}$↓, $\overline{IORD}$↓ delay time from address/status output	㉛ t_{DARL}	15–5, etc.		0.5t_{CYK}–20		ns
Data hold time (from $\overline{MRD}$↑, from $\overline{IORD}$↑)	㉜ t_{HRD}	15–5, etc.		0		ns
Address delay time from CLKOUT↓ Note 1	㉝ t_{DKA}	15–5, etc.		4	45	ns
Data hold time (from R/$\overline{W}$↓)	㉞ t_{HRWD}	15–5		0		ns
Status delay time from CLKOUT↓	㉟ t_{DKST}	15–5, etc.		5	45	ns
$\overline{DSTB}$↓ output delay time from CLKOUT↑	㊱ t_{DKDS}	15–5, etc.		5	60	ns
$\overline{DSTB}$↑ output delay time from CLKOUT	㊲ t_{DKDSH}	15–5, etc.		5	50	ns
$\overline{DSTB}$↓ delay time from address/status output	㊳ t_{DADSL}	15–5, etc.		0.5t_{CYK}–20		ns
$\overline{DSTB}$ high-level width	㊴ t_{DSDSH}	15–5, etc.		0.5t_{CYK}–15		ns
$\overline{DSTB}$ low-level width	㊵ t_{DSDSL}	15–6, etc.		t_{CYK}(n+1)–15 Note 4		ns
Data hold time (from $\overline{DSTB}$↑)	㊶ t_{HDSD}	15–5, etc.		0		ns
Data hold time (from address/status change point)	㊷ t_{HASD}	15–5		0		ns
Control 1 Note 2 delay time from CLKOUT	㊸ t_{DKCT1}	15–21		0	60	ns
Control 2 Note 3 delay time from CLKOUT	㊹ t_{DKCT2}	15–5, etc.		0	60	ns
Data setup time (to CLKOUT↓)	㊺ t_{SDK}	15–5, etc.		10		ns
Data hold time (from CLKOUT↓)	㊻ t_{HKD}	15–5, etc.		10		ns
Output floating time from $\overline{DSTB}$↓	㊼ t_{DHZ}	15–5, etc.			0	ns
Address/status hold time from $\overline{MWR}$↑	㊽ t_{HMWHA}	15–6		0.5t_{CYK}–20		ns
$\overline{MWR}$ delay time from CLKOUT	㊾ t_{DKMW}	15–6, etc.		0	60	ns
$\overline{MWR}$↓, $\overline{IOWR}$↓ delay time from address/status output	㊿ t_{DAWL}	15–6, etc.		0.5t_{CYK}–20		ns
$\overline{MWR}$, $\overline{IOWR}$ low-level width	(51) t_{WWL}	15–6, etc.		t_{CYK}(n+1)–15 Note 4		ns
Address/status hold time from $\overline{DSTB}$↑	(52) t_{HDSHA}	15–6, etc.		0.5t_{CYK}–20		ns
Data output delay time from $\overline{DSTB}$↑	(53) t_{DDSHD}	15–6, etc.		0.5t_{CYK}–20		ns
Data delay time from address/status output	(54) t_{DAD}	15–6, etc.		0.5t_{CYK}–20		ns
Output setting time from $\overline{DSTB}$↑	(55) t_{DLZ}	15–6, etc.		0.5t_{CYK}–20		ns

* **Notes** 1. These specifications apply to the following delay times from the falling edge of the CLKOUT signal.
(1) Address delay time
(2) $\overline{BUSLOCK}$ delay time
(3) Delay time of signals below immediately after release of bus hold:
A23-A0, D15-D0, M/$\overline{IO}$, BUSST1, BUSST0, $\overline{UBE}$, $\overline{BCYST}$, $\overline{DSTB}$.

2. Control 1 applies to the $\overline{MWR}$ and $\overline{IOWR}$ signals in a DMA cycle.
3. Control 2 applies to the $\overline{BUFEN}$, $\overline{INTAK}$ and $\overline{REFRQ}$ setups.
4. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remarks 1. The number in the symbol column correspond to the numbers in the timing charts.
2. Regarding the five specifications (32) t_{HRD}, (34) t_{HRWD}, (41) t_{HDSD}, (42) t_{HASD} and (46) t_{HKD}, at least one should be observed.

μPD70236A-20 (V_{DD} = 2.7 to 3.6 V) (3/4)

PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
Data output delay time from CLKOUT↑	㊺⑥	t_{DKD}	15–6, etc.		5	60	ns
Float delay time from CLKOUT	㊺⑦	t_{FK}	15–6, etc.		0	60	ns
$\overline{IORD}$ delay time from CLKOUT	㊺⑧	t_{DKIR}	15–7		0	60	ns
$\overline{IOWR}$ delay time from CLKOUT	㊺⑨	t_{DKIW}	15–8		0	60	ns
$\overline{NMI}$, INTPn (n = 0 to 7), $\overline{CPBUSY}$ setup time (to CLKOUT↓)	㊻⓪	t_{SIK}	15–11		10		ns
$\overline{NMI}$, INTPn(n = 0 to 7), $\overline{CPBUSY}$ hold time (from CLKOUT↓)	㊻①	t_{HKI}	15–11		15		ns
$\overline{BS8}$/BS16 setup time (to CLKOUT↑)	㊻②	t_{SBSK}	15–13		15		ns
$\overline{BS8}$/BS16 hold time (from CLKOUT↑)	㊻③	t_{HKBS}	15–13		15		ns
HLDRQ setup time (to CLKOUT↑)	㊻④	t_{SHQK}	15–14		15		ns
HLDRQ hold time (from CLKOUT↑)	㊻⑤	t_{HKHQ}	15–14		20		ns
HLDAK delay time from CLKOUT↑	㊻⑥	t_{DKHA}	15–14		5	45	ns
HLDAK delay time from output float	㊻⑦	t_{DFHA}	15–14		0.5t_{CYK}–20		ns
INTPn(n = 0 to 7) low-level width	㊻⑧	t_{IPIPL}	15–17		100		ns
TCTLn (n = 0 to 2) setup time (to CLKOUT↓)	㊻⑨	t_{SGK}	15–18		100		ns
TCTLn (n = 0 to 2) hold time (from CLKOUT↓)	㊼⓪	t_{HKG}	15–18		100		ns
TCTLn (n = 0 to 2) high-level width	㊼①	t_{GGH}	15–18, etc.		50		ns
TCTLn (n = 0 to 2) low-level width	㊼②	t_{GGL}	15–18, etc.		50		ns
TOUTn (n = 0 to 2) output delay time (from TCTLn (n = 0 to 2)↓)	㊼③	t_{DGTO}	15–18, etc.			120	ns
TOUTn (n = 0 to 2) output delay time (from CLKOUT↓)	㊼④	t_{DKTO}	15–18			100	ns
TCLK cycle	㊼⑤	t_{CYTK}	15–19		100	DC	ns
TCLK high-level width	㊼⑥	t_{TKTKH}	15–19		30		ns
TCLK low-level width	㊼⑦	t_{TKTKL}	15–19		45		ns
TCLK rise time	㊼⑧	t_{TKR}	15–19			15	ns
TCLK fall time	㊼⑨	t_{TKF}	15–19			15	ns
TCTLn (n = 0 to 2) hold time (from TCLK↑)	㊽⓪	t_{HTKG}	15–19		100		ns
TCTLn (n = 0 to 2) setup time (to TCLK↑)	㊽①	t_{SGTK}	15–19		50		ns
TOUTn (n = 0 to 2) output delay time (from TCLK↓)	㊽②	t_{DTKTO}	15–19			150	ns
RxD setup time (to SCU internal clock↓)	㊽③	t_{SRX}	15–20		1000		ns
RxD hold time (from SCU internal clock↓)	㊽④	t_{HRX}	15–20		1000		ns
TxD delay time from TOUT1↑	㊽⑤	t_{DTX}	15–20			500	ns
$\overline{DMAAK}$n (n = 0 to 3) delay time from CLKOUT↑	㊽⑥	t_{DKHDA}	15–21		0	60	ns
$\overline{MRD}$, $\overline{IORD}$↓ delay time from CLKOUT↓	㊽⑦	t_{DKRL}	15–21		0	60	ns
$\overline{MRD}$, $\overline{IORD}$↑ delay time from CLKOUT↓	㊽⑧	t_{DKRH}	15–21		0	60	ns
$\overline{DMAAK}$n (n = 0 to 3)↑ delay time (from $\overline{IORD}$↑)	㊽⑨	t_{DRHDAH}	15–21		0.5t_{CYK}–20		ns
$\overline{IORD}$↓,$\overline{IOWR}$↓ delay time (from $\overline{DMAAK}$n (n = 0 to 3)↓)	㊾⓪	t_{DDARW}	15–21		0.5t_{CYK}–20		ns

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-20 (V_{DD} = 2.7 to 3.6 V)

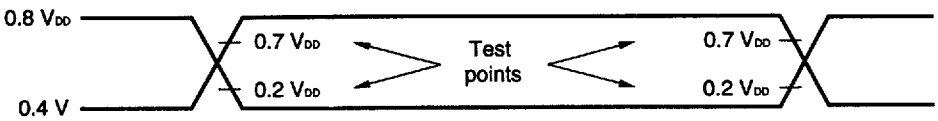
(4/4)

PARAMETER		SYMBOL	FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C MIN.	MAX.	UNIT	
$\overline{IORD}$↑ delay time (from $\overline{MWR}$↑) $\overline{MRD}$↑ delay time (from $\overline{IOWR}$↑)	⑨①	t_{DWHRH}	15–21		0		ns	
$\overline{IORD}$, $\overline{MRD}$ low-level width	⑨②	t_{RR}	15–21		$t_{CYK}(n+2)-60$ Note 1		ns	
$\overline{IOWR}$, $\overline{MWR}$ low-level width (extended write)	⑨③	t_{WW1}	15–21	Extended write	$t_{CYK}(n+2)-60$ Note 1		ns	
$\overline{IOWR}$, $\overline{MWR}$ low-level width (normal write)	⑨④	t_{WW2}	15–21	Normal write	$t_{CYK}(n+1)-60$ Note 1		ns	
$\overline{TC}$ output delay time (from CLKOUT↑)	⑨⑤	t_{DKTCL}	15–22		0	60	ns	
$\overline{TC}$ OFF output delay time (from CLKOUT↑)	⑨⑥	t_{DKTCF}	15–22		0	60	ns	
$\overline{TC}$ pull-up delay time (from CLKOUT↑) Note 2	⑨⑦	t_{DKTCH}	15–22	R_{TC} = 2.2 kΩ	0	$2t_{CYK}-20$	ns	
$\overline{TC}$ low-level width	⑨⑧	t_{TCTCL}	15–22		$t_{CYK}(n+1)-25$ Note 1		ns	
$\overline{END}$ setup time (to CLKOUT↑)	⑨⑨	t_{SEDK}	15–22		20		ns	
$\overline{END}$ low-level width	⑩⓪	t_{EDEDL}	15–22		100		ns	
DMARQn (n = 0 to 3) setup time (to CLKOUT↑)	⑩①	t_{SDQK}	15–22, etc.		20		ns	
$\overline{DMAAK}$n (n = 0 to 3) delay time from CLKOUT↓	⑩②	t_{DKLDA}	15–23		0	60	ns	
$\overline{MRD}$ high-level width	⑩③	t_{MRMRH}	15–5		$0.5t_{CYK}-15$		ns	
Data set time from $\overline{MRD}$↑	⑩④	t_{DMRHLZ}	15–6, etc.		$0.5t_{CYK}-20$		ns	
Data output delay time from $\overline{MRD}$↑	⑩⑤	t_{DMRHD}	15–6, etc.		$0.5t_{CYK}-20$		ns	
Cascade address delay time from CLKOUT	⑩⑥	t_{DKCA}	15–15, etc.		4	45	ns	
$\overline{INTAK}$ high-level width	⑩⑦	t_{IAIAH}	15–16		$2.5t_{CYK}-15$		ns	*
PCLKOUT delay time from CLKOUT	⑩⑧	t_{DKPK}	15–1	CLKC = 00		±5	ns	
$\overline{IOWR}$, $\overline{MWR}$↓ delay time from $\overline{MRD}$, $\overline{IORD}$↓	⑩⑨	t_{DRLWL}	15–21	Normal write	$t_{CYK}-20$		ns	

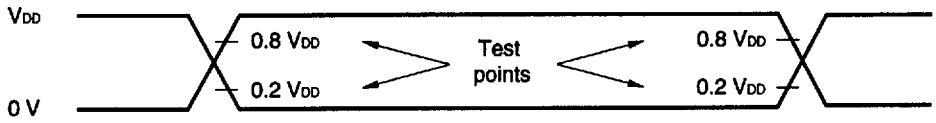
Notes 1. n indicates the number of wait clock cycles inserted in the bus cycle.
2. It is assumed that the $\overline{TC}$ pin is connected with the pull-up resistor R_{TC}.

Remark The number in the symbol column correspond to the numbers in the timing charts.

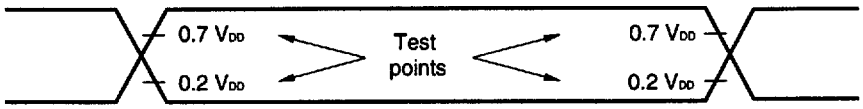
AC Test Input Waveform (Except X1)



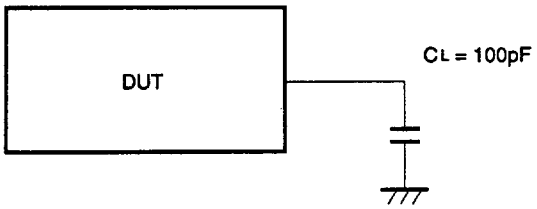
AC Test Input Waveform (X1)



AC Test Output Test Points



Load Conditions

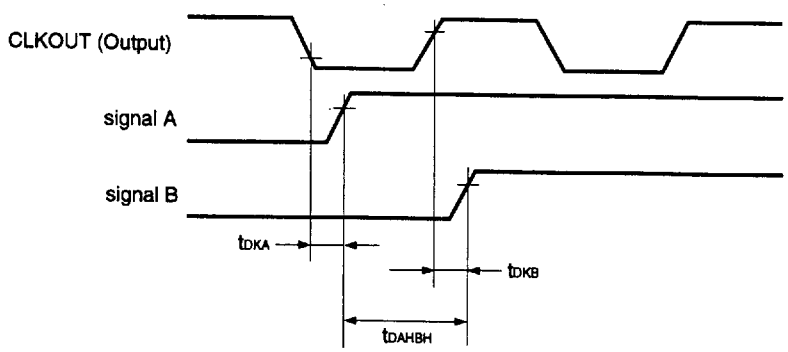


Caution **If the load capacitance exceeds 100 pF due to the construction of the circuit, the load capacitance of this device should be reduced to 100 pF or less by insertion of a buffer, etc.**

15.4 RELATIVE SPECIFICATIONS

*

When two signals change with a phase difference of 0.5n (n = 1, 2, 3, . . .) in relation to CLKOUT as signal A and signal B in the figure below, the minimum value of the relative specifications (delay time from signal A ↑ to signal B ↑) of the two signals is as shown below.



Remark t_{DKA} : Delay time from CLKOUT ↓ to signal A ↑
t_{DKB} : Delay time from CLKOUT ↑ to signal B ↑
t_{DAHBH} : Delay time from signal A ↑ to signal B ↑

Table 15-1 V53A Relative Specifications

Symbol	Power supply voltage (V_{DD})	μPD70236A-10	μPD70236A-12	μPD70236A-16	μPD70236A-20	Unit
t_{DAHBH} (MIN.)	5 V ± 10 %	0.5n x t_{CYK} – 15	0.5n x t_{CYK} – 15	0.5n x t_{CYK} – 15	0.5n x t_{CYK} – 12	ns
	3.6 to 4.5 V	—	—	0.5n x t_{CYK} – 15	0.5n x t_{CYK} – 15	ns
	2.7 to 3.6 V	—	—	0.5n x t_{CYK} – 20	0.5n x t_{CYK} – 20	ns

15.5 TIMING CHART

The timing chart of the μPD70236A is described below.

On this timing chart, it is assumed that the WCU programmable wait is 0.

Fig. 15-1 Clock Timing

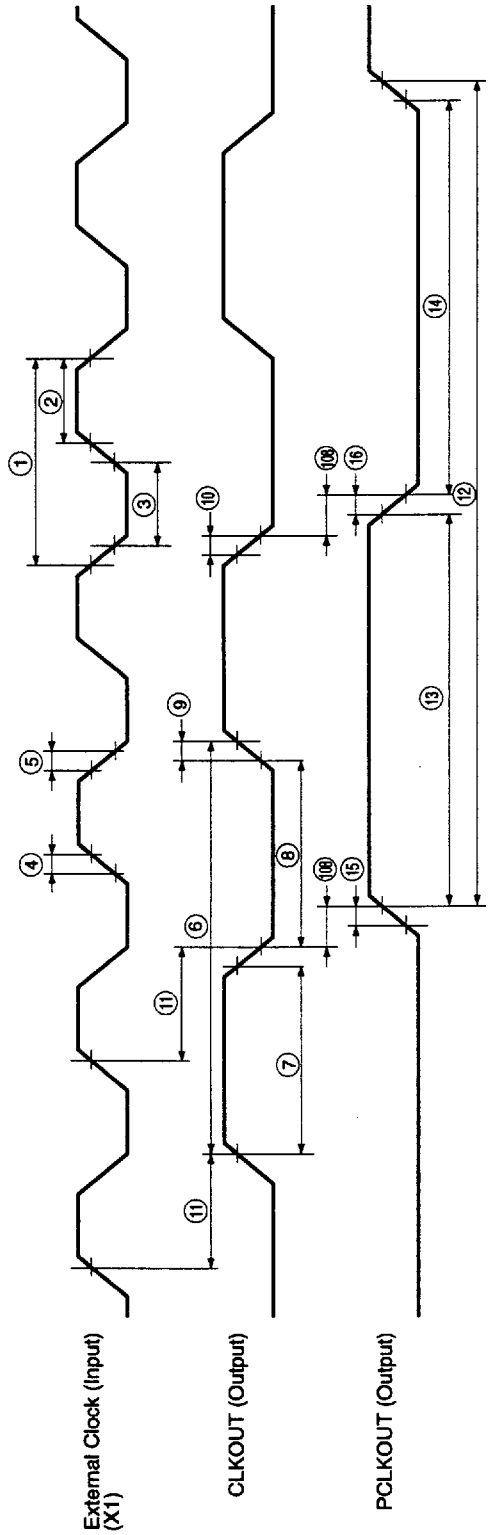
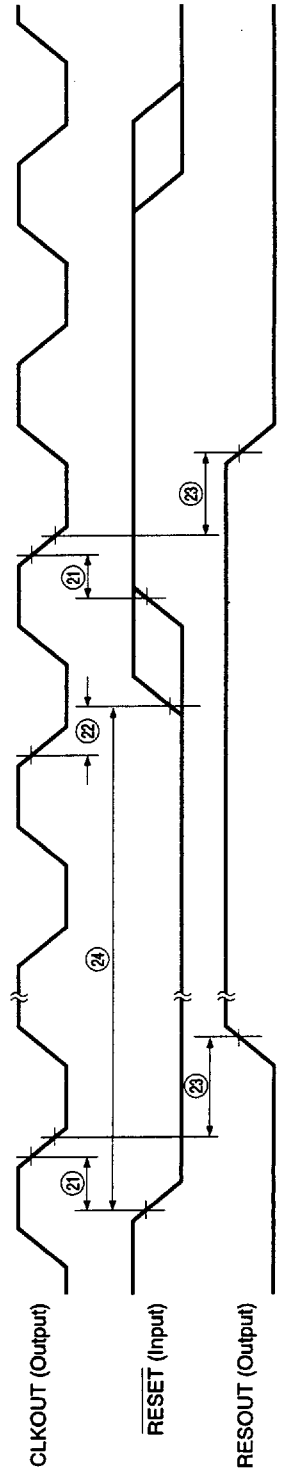


Fig. 15-2 Reset Timing



Remark $\overline{\text{RESET}}$ can be input asynchronously with respect to CLKOUT.

Fig. 15-3 CPU Ready Timing (No Wait)

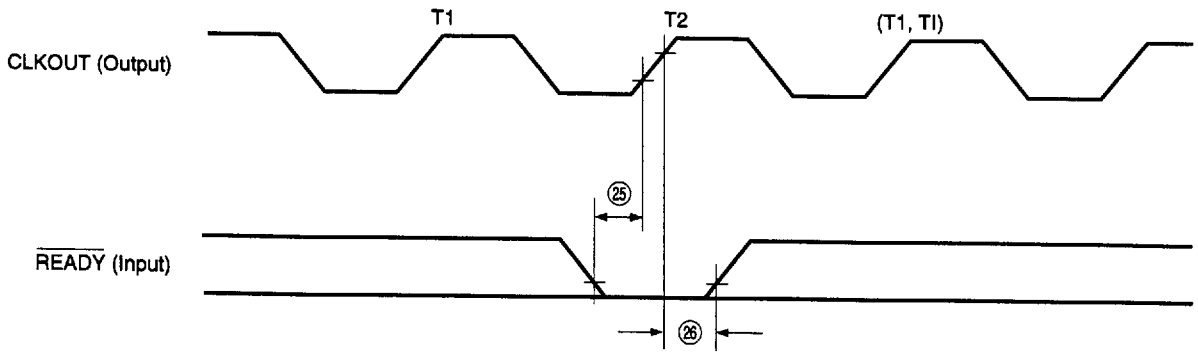


Fig. 15-4 CPU Ready Timing (1 Wait)

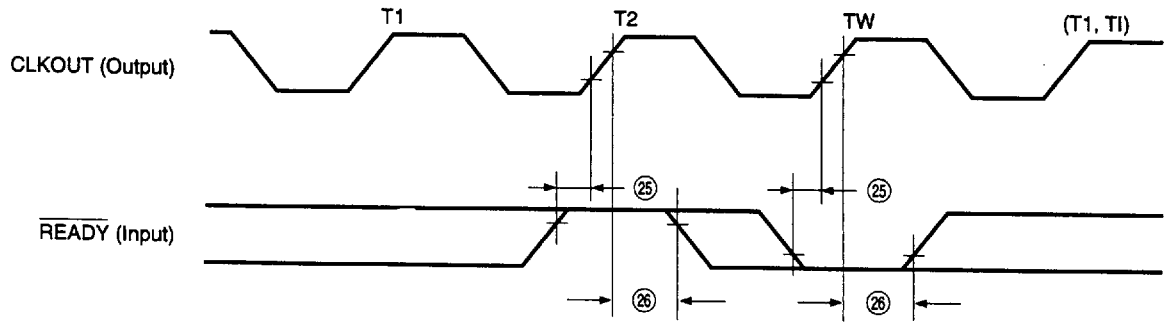
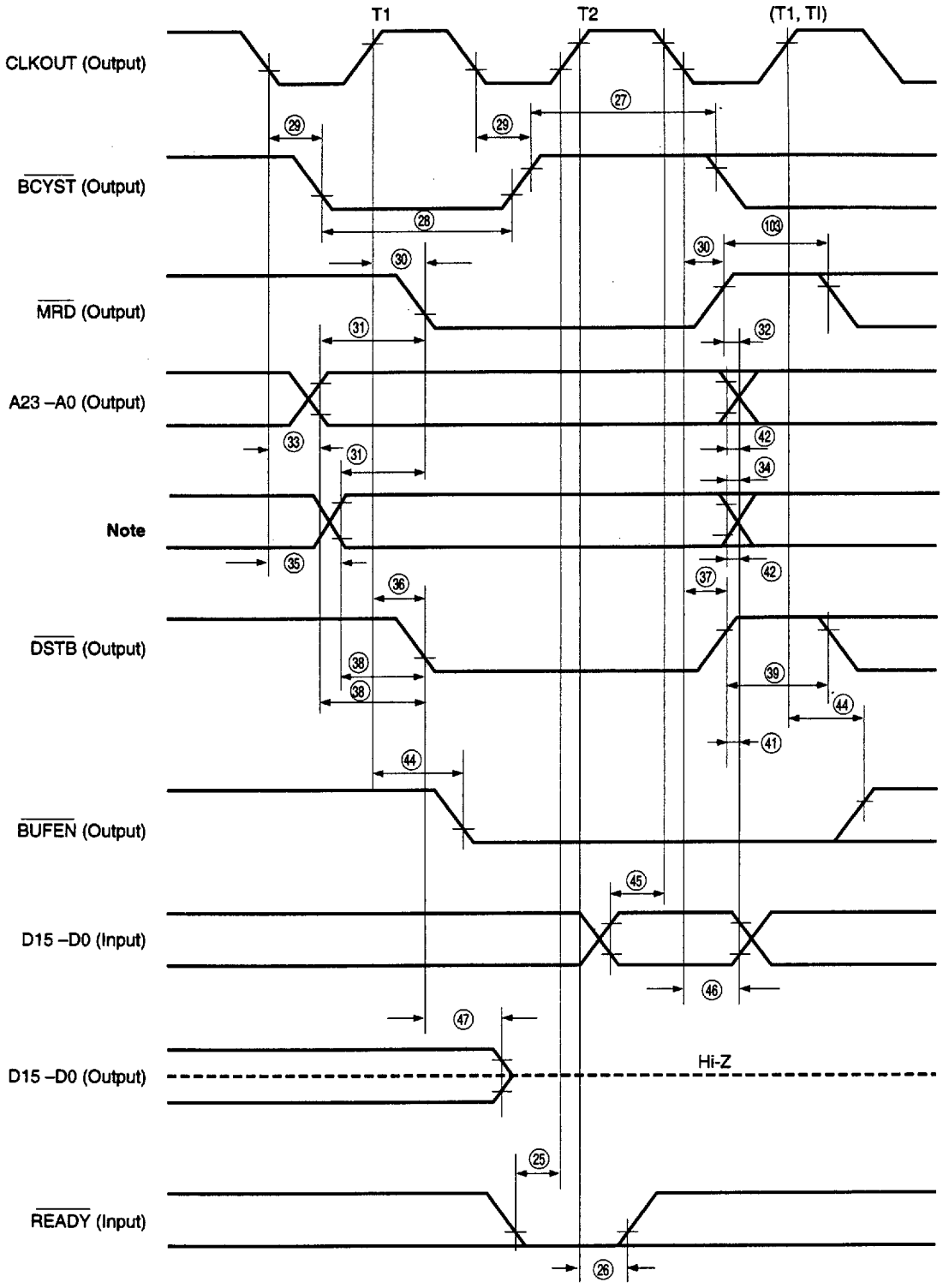
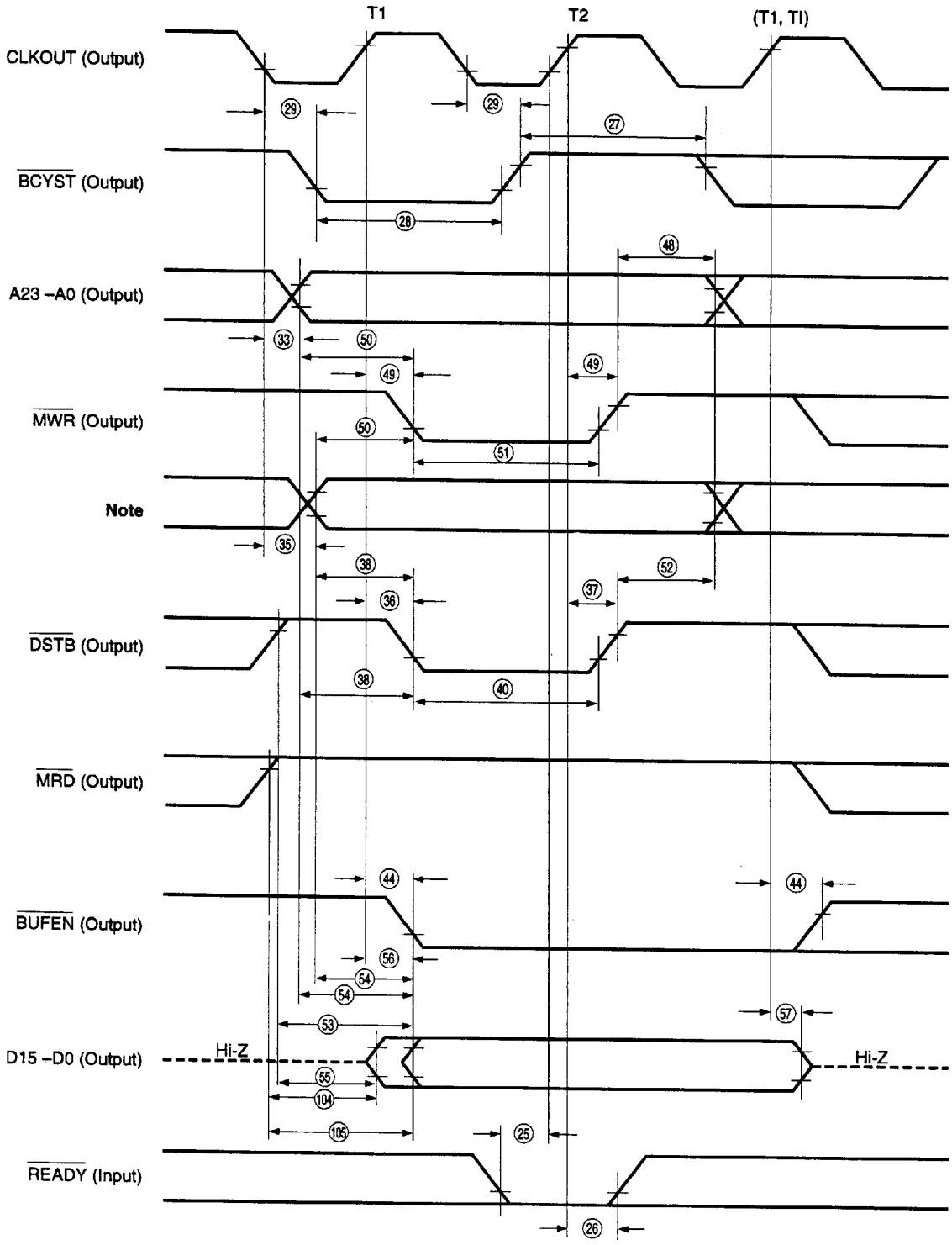


Fig. 15-5 Basic Read Cycle (No Wait)



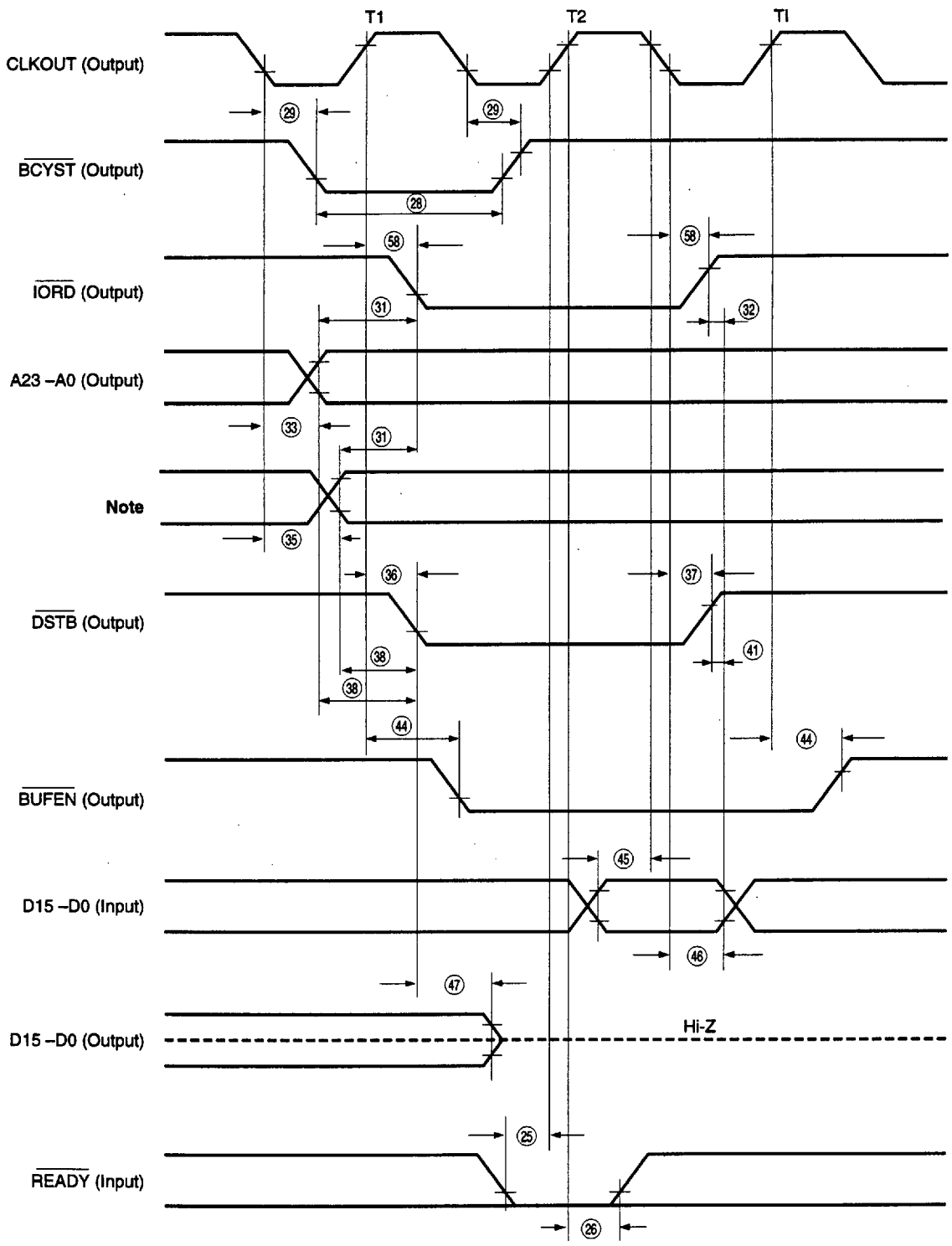
Note R/$\overline{W}$, M/$\overline{IO}$, BUSST2, BUSST1, BUSST0, $\overline{UBE}$, AEX (all output)

Fig. 15-6 Basic Write Cycle (No Wait)



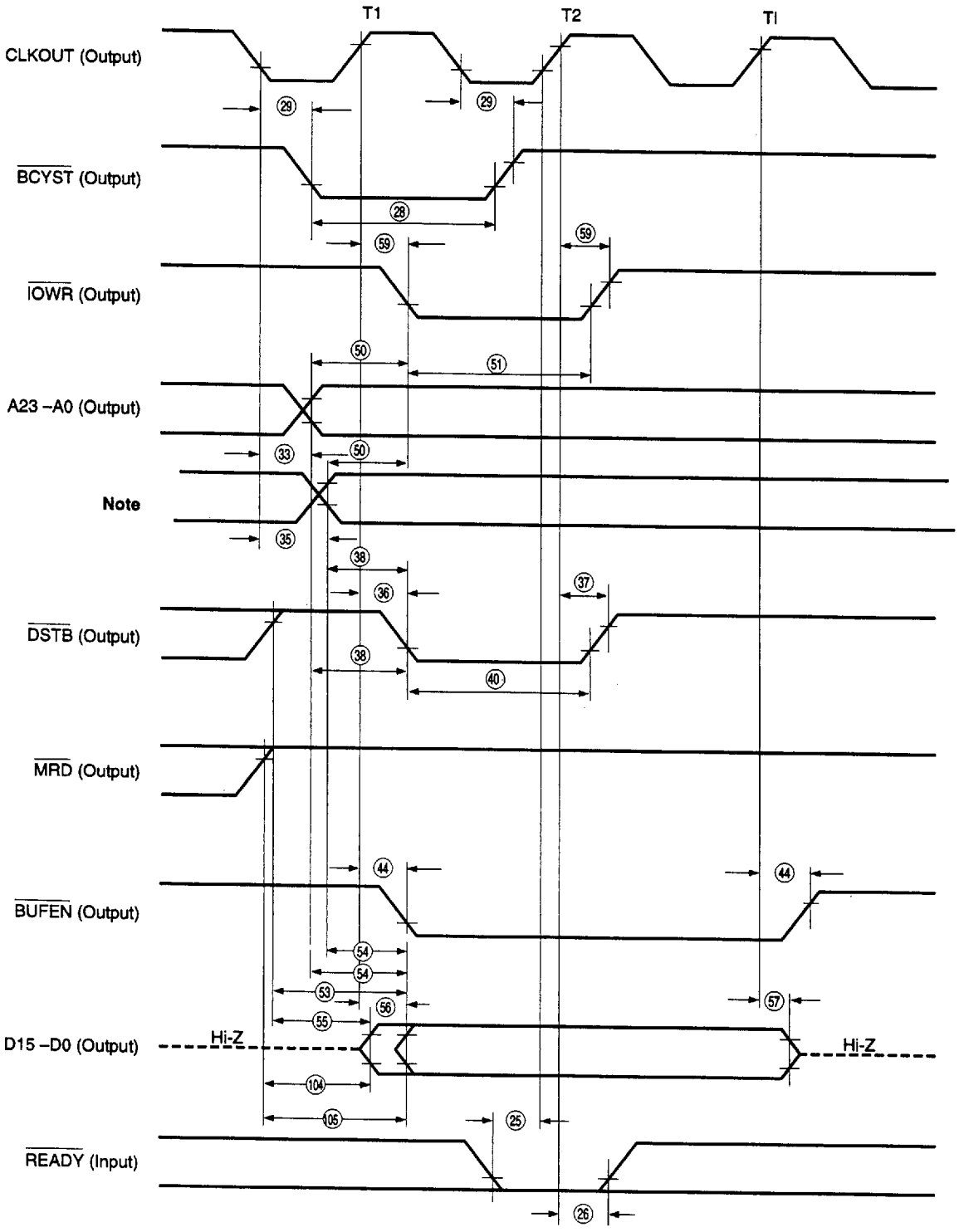
Note R/$\overline{W}$, M/$\overline{IO}$, BUSST2, BUSST1, BUSST0, $\overline{UBE}$, AEX (all output)

Fig. 15-7 External I/O Read Cycle (No Wait)



Note R/$\overline{W}$, M/$\overline{IO}$, BUSST2, BUSST1, BUSST0, $\overline{UBE}$, AEX (all output)

Fig. 15-8 External I/O Write Cycle (No Wait)



Note R/$\overline{W}$, M/$\overline{IO}$, BUSST2, BUSST1, BUSST0, $\overline{UBE}$, AEX (all output)

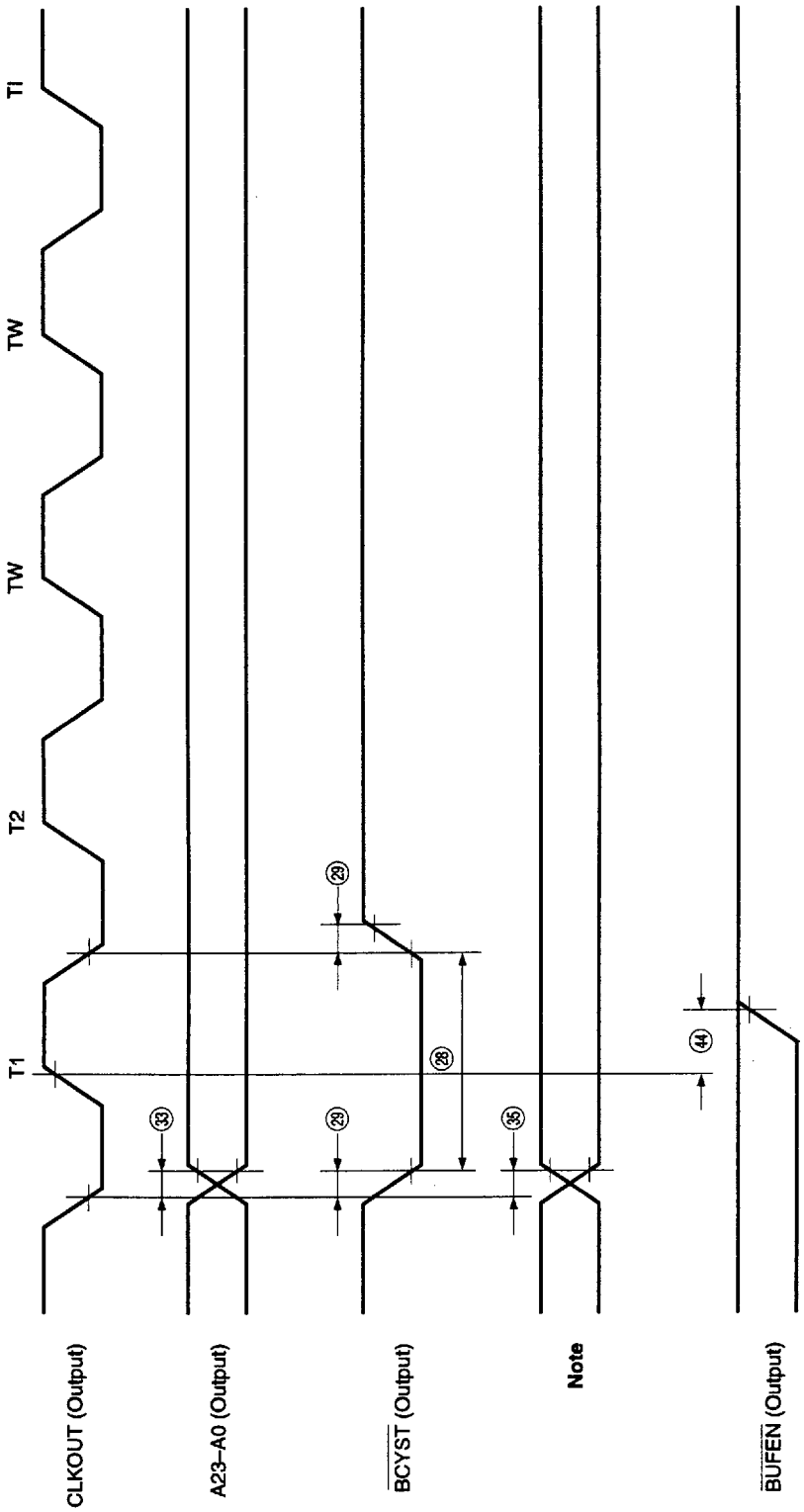


Fig. 15-9 Internal I/O Read Cycle

Note R/W, M/IO, BUSST2, BUSST1, BUSST0, UBE, AEX (all output)

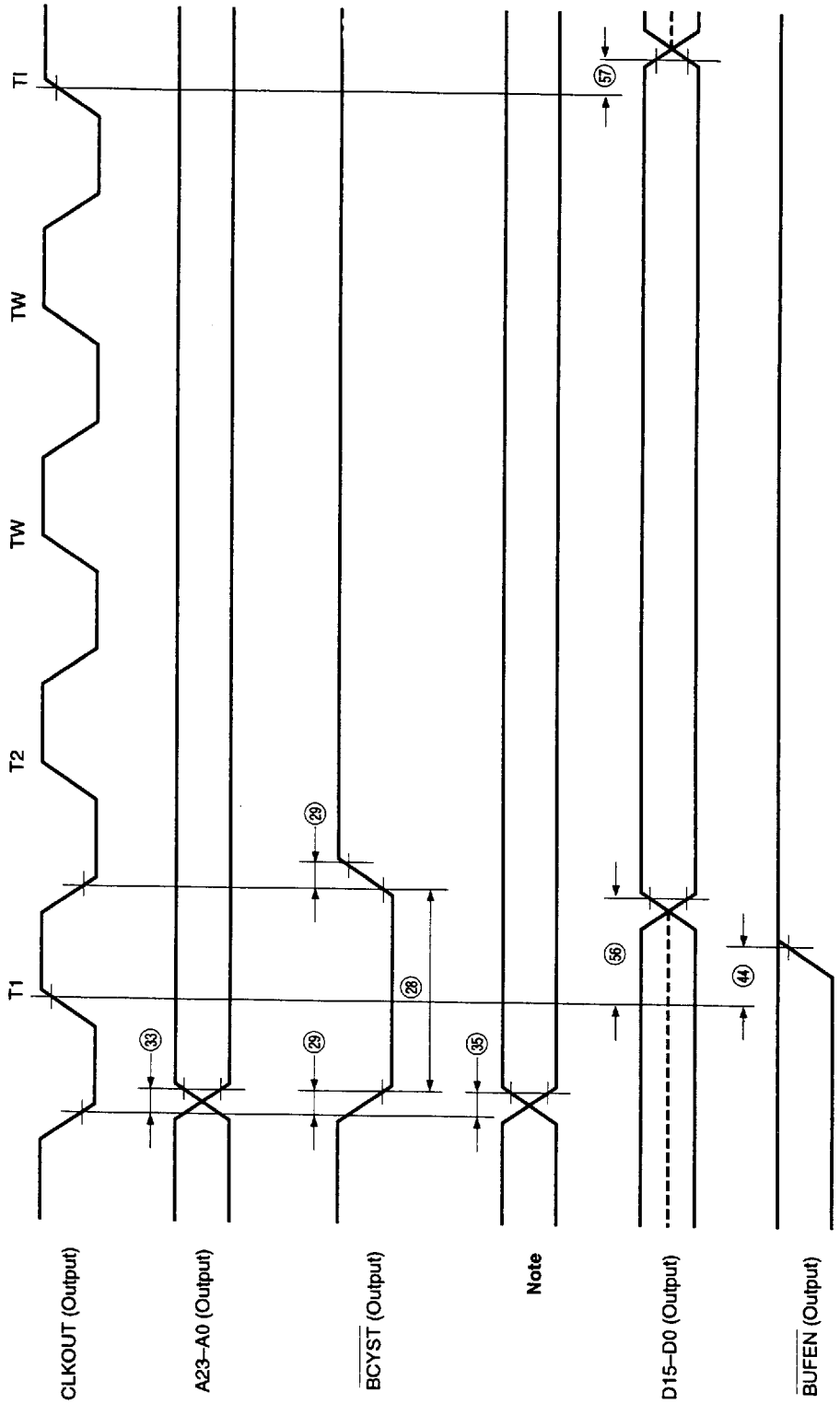
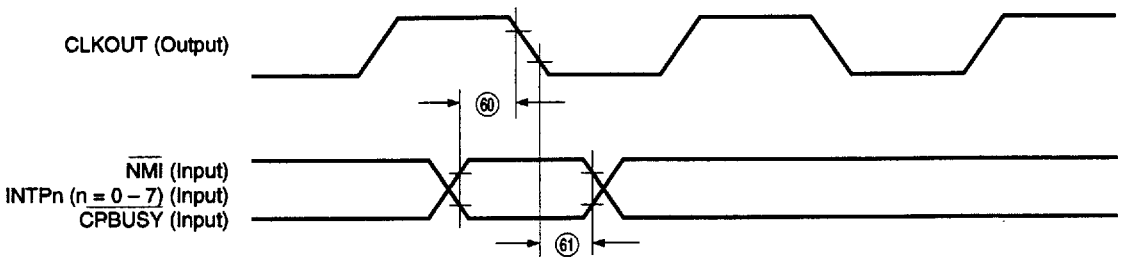


Fig. 15-10 Internal I/O Write Cycle

Note R/$\overline{W}$, M/$\overline{IO}$, BUSST2, BUSST1, BUSST0, $\overline{UBE}$, AEX (all output)

Remark A dashed line indicates high impedance.

Fig. 15-11 Input Setup & Input Hold Times



Remark $\overline{NMI}$, INTP0 to INTP7, and $\overline{CPBUSY}$ can be input asynchronously with respect to CLKOUT.

Fig. 15-12 Bus Lock

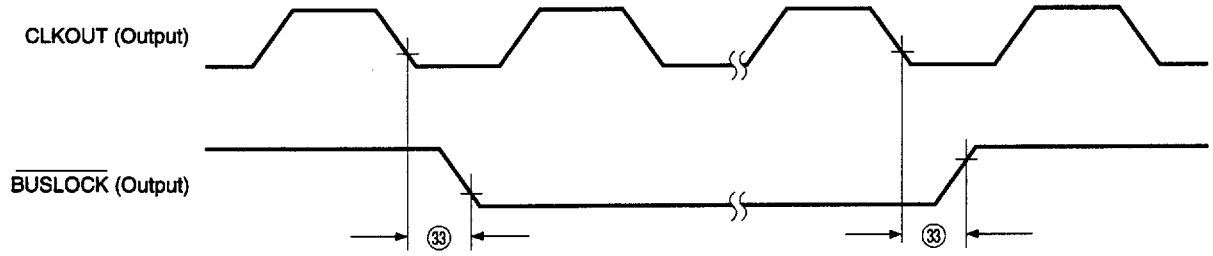
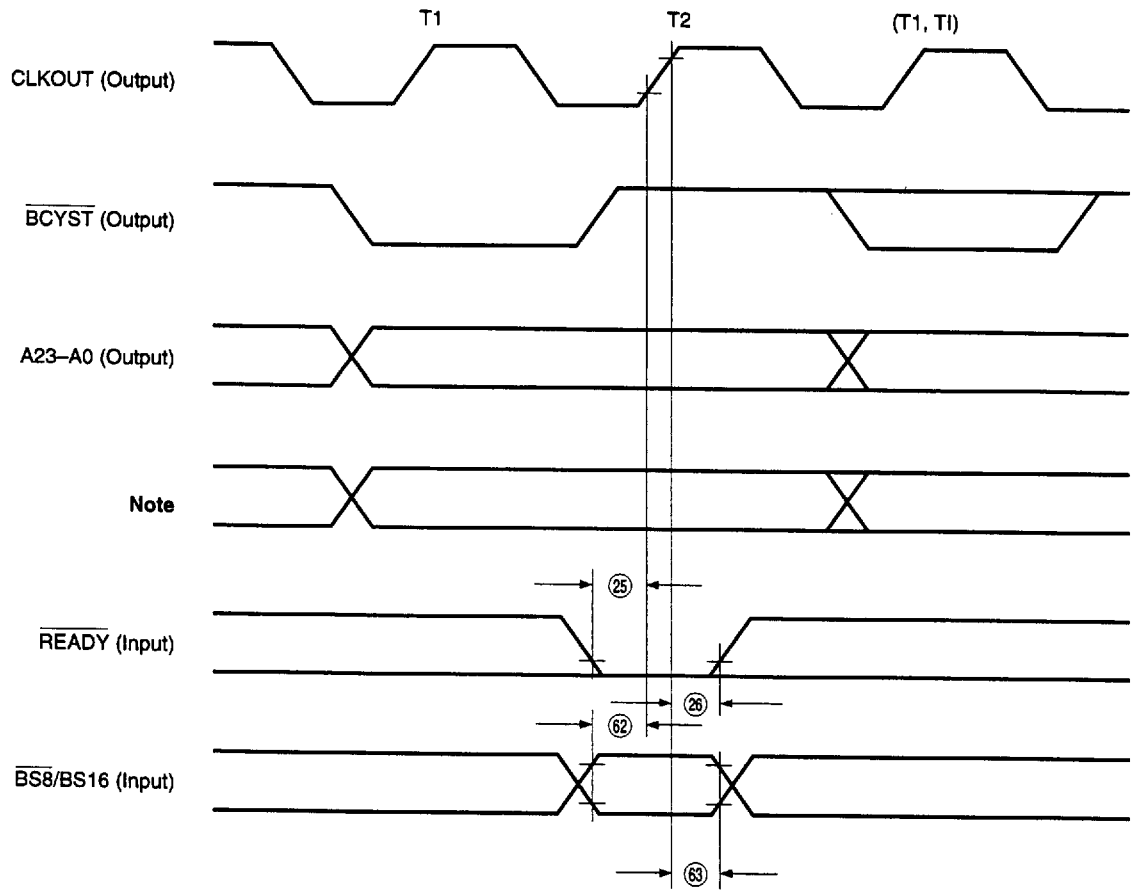


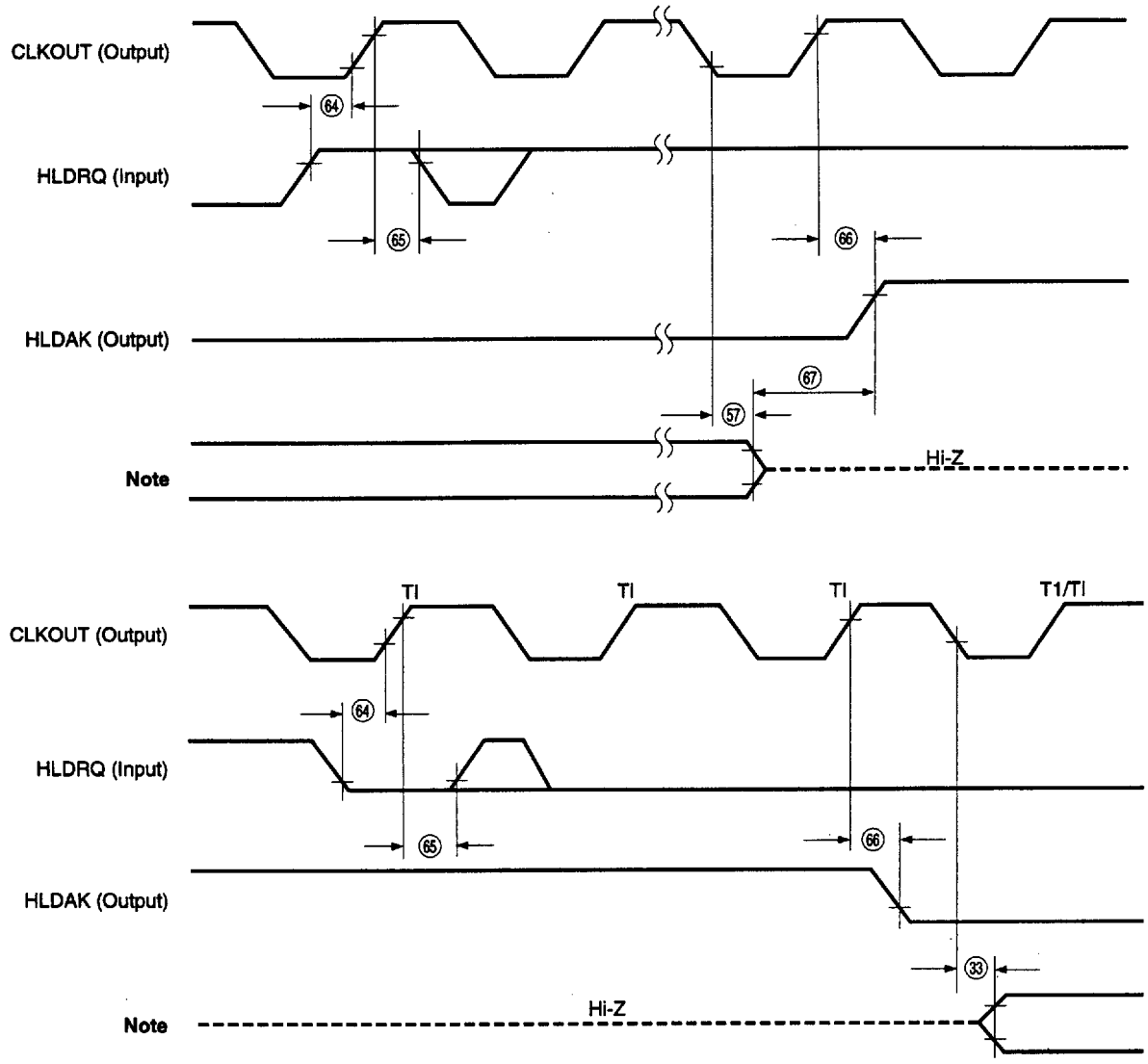
Fig. 15-13 Bus Sizing Cycle (No Wait)



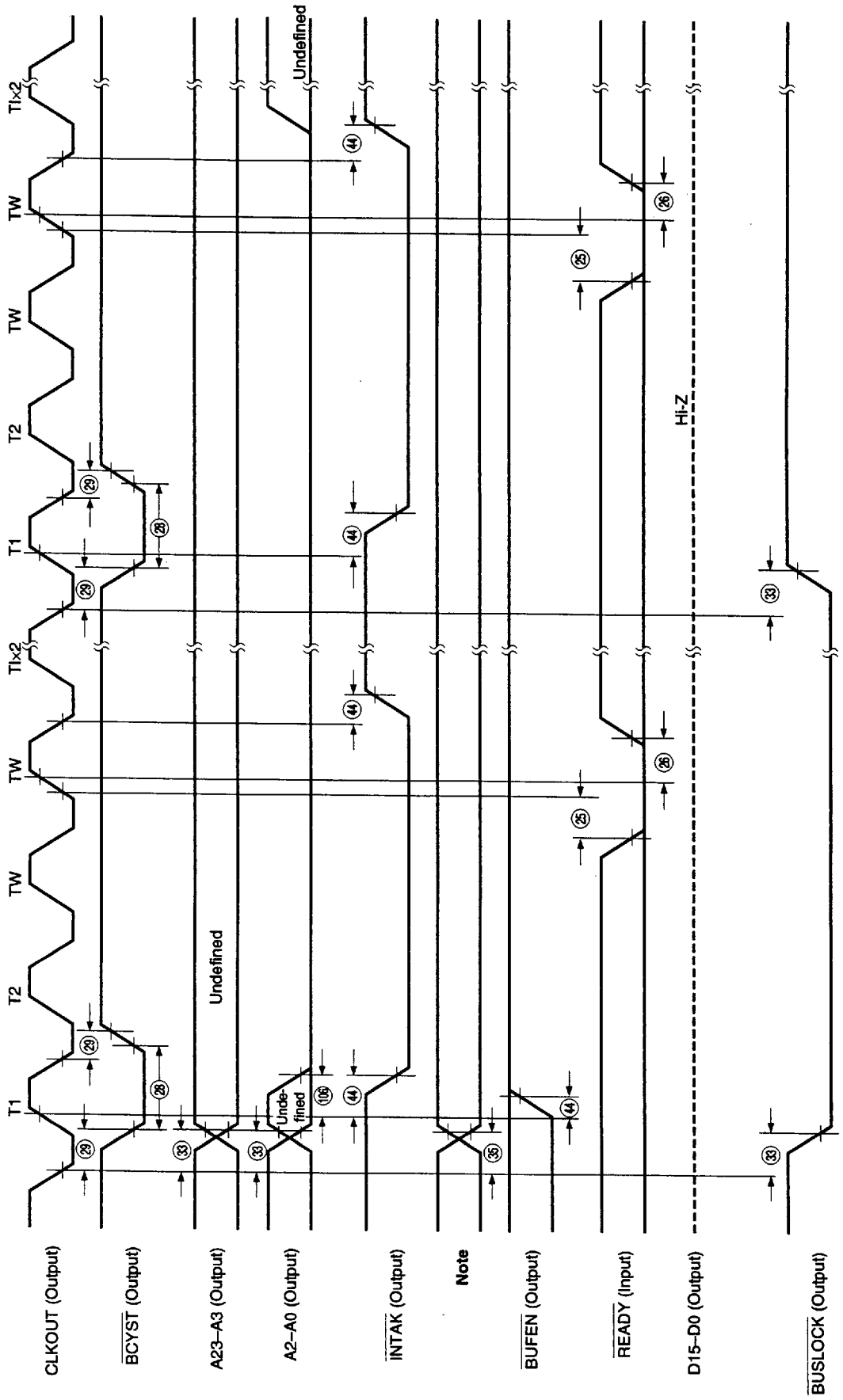
Note R/$\overline{W}$, M/$\overline{IO}$, BUSST2, BUSST1, BUSST0, $\overline{UBE}$, AEX (all output)

*

Fig. 15-14 Bus Hold



Note R/$\overline{W}$, M/$\overline{IO}$, BUSST2, BUSST1, BUSST0, $\overline{UBE}$ (all output)



Note R/$\overline{W}$, M/$\overline{IO}$, BUSST2, BUSST1, BUSST0, $\overline{UBE}$, AEX (all output)

Remark $\overline{DSTB}$ is inactive.

Fig. 15-15 Interrupt Acknowledge (Single Mode)

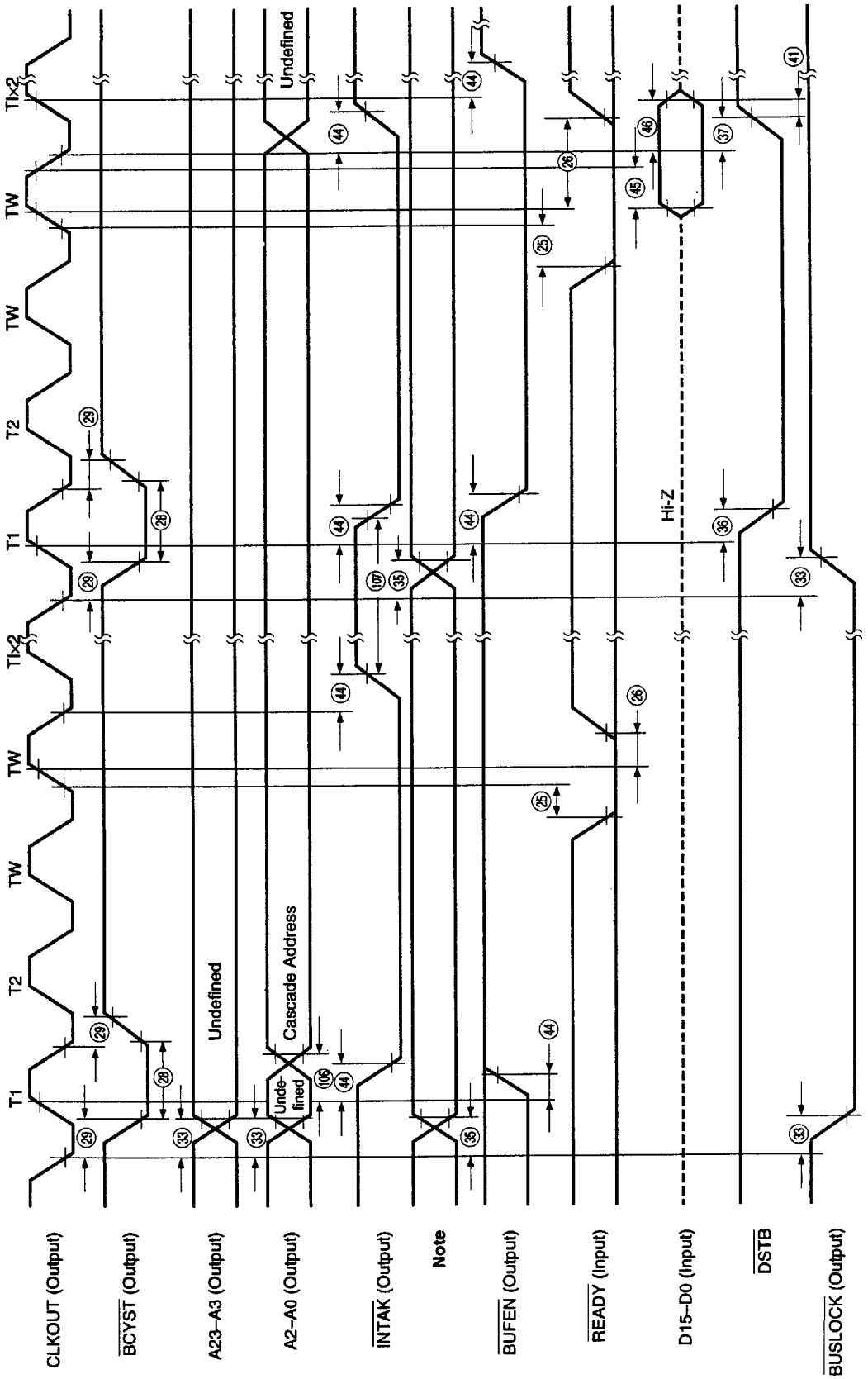


Fig. 15-16 Interrupt Acknowledge (Cascade Mode)

Note R/$\overline{W}$, M/$\overline{IO}$, BUSST2, BUSST1, BUSST0, $\overline{UBE}$, AEX (all output)

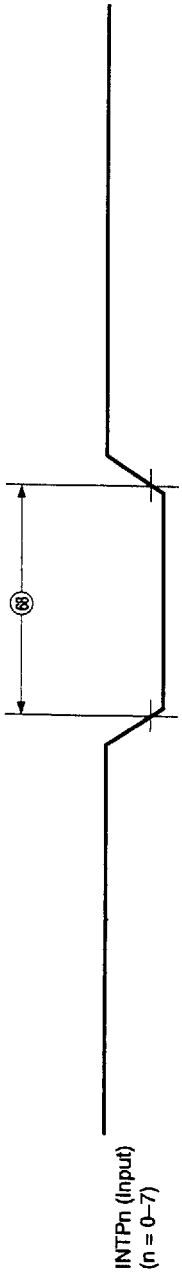


Fig. 15-17 ICU Timing

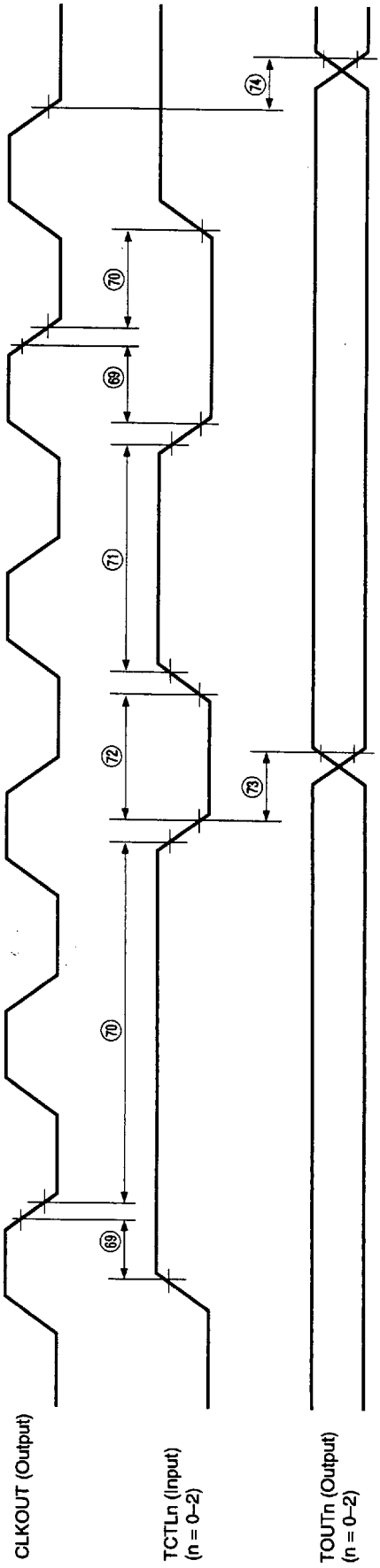


Fig. 15-18 TCU Timing (1)

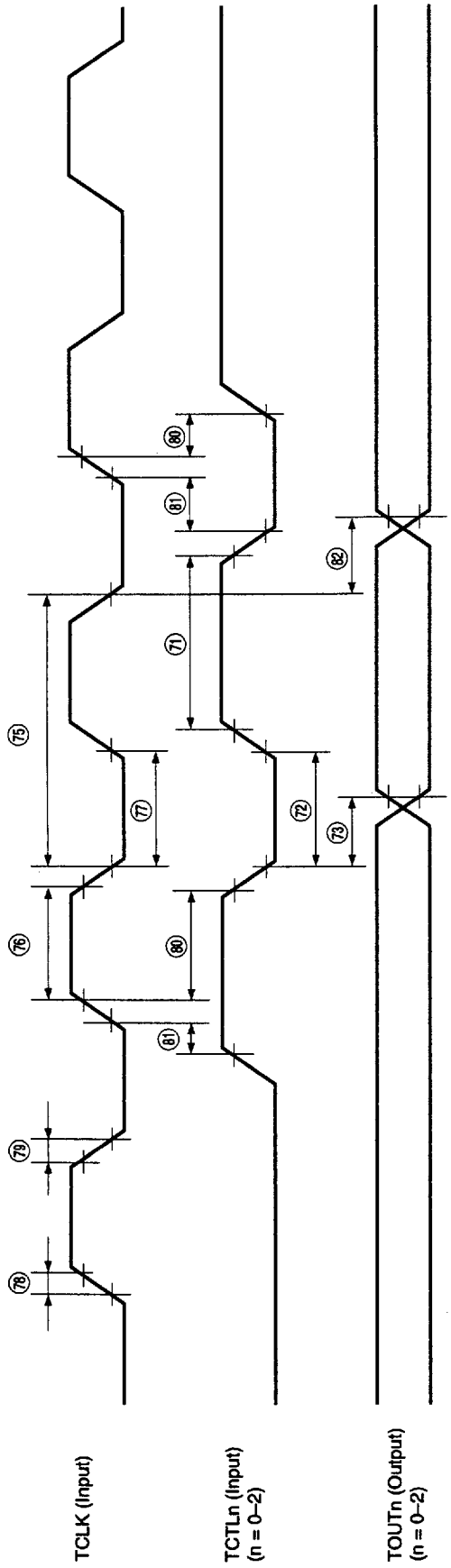


Fig. 15-19 TCU Timing (2)

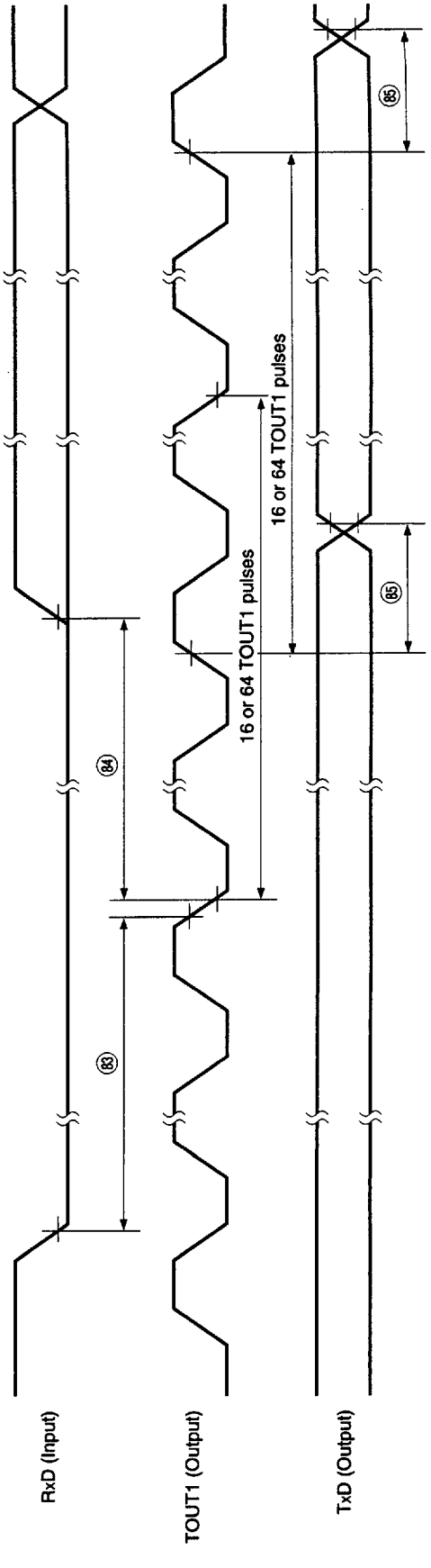
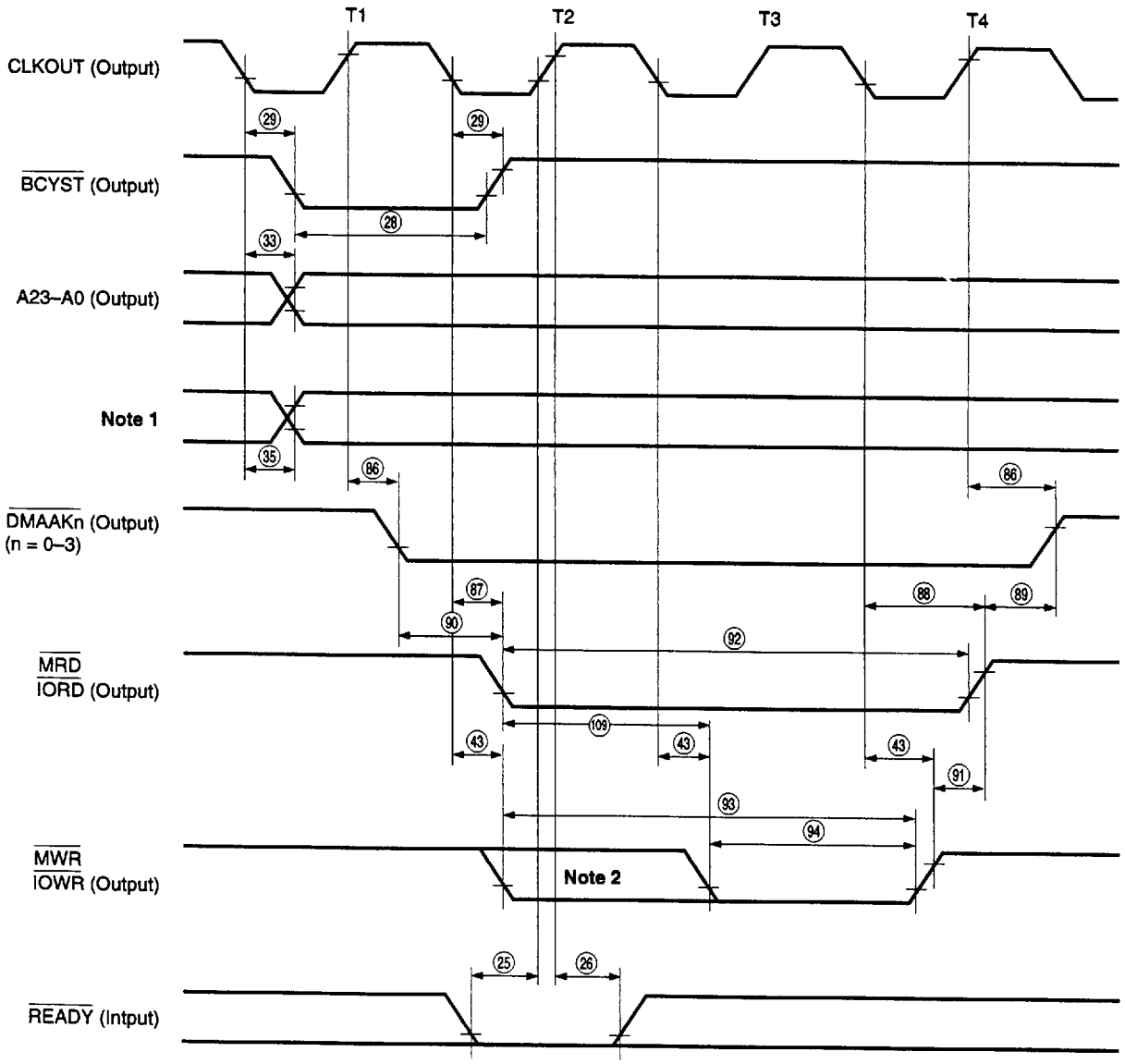


Fig. 15-20 SCU Timing

Fig. 15-21 DMAU Timing (1)



Notes 1. R/$\overline{W}$, M/$\overline{IO}$, BUSST2 to BUSST0, $\overline{UBE}$ (all output)

2. In extended write mode, a low-level signal is output.

Remark $\overline{DSTB}$ and $\overline{BUFEN}$ are inactive.

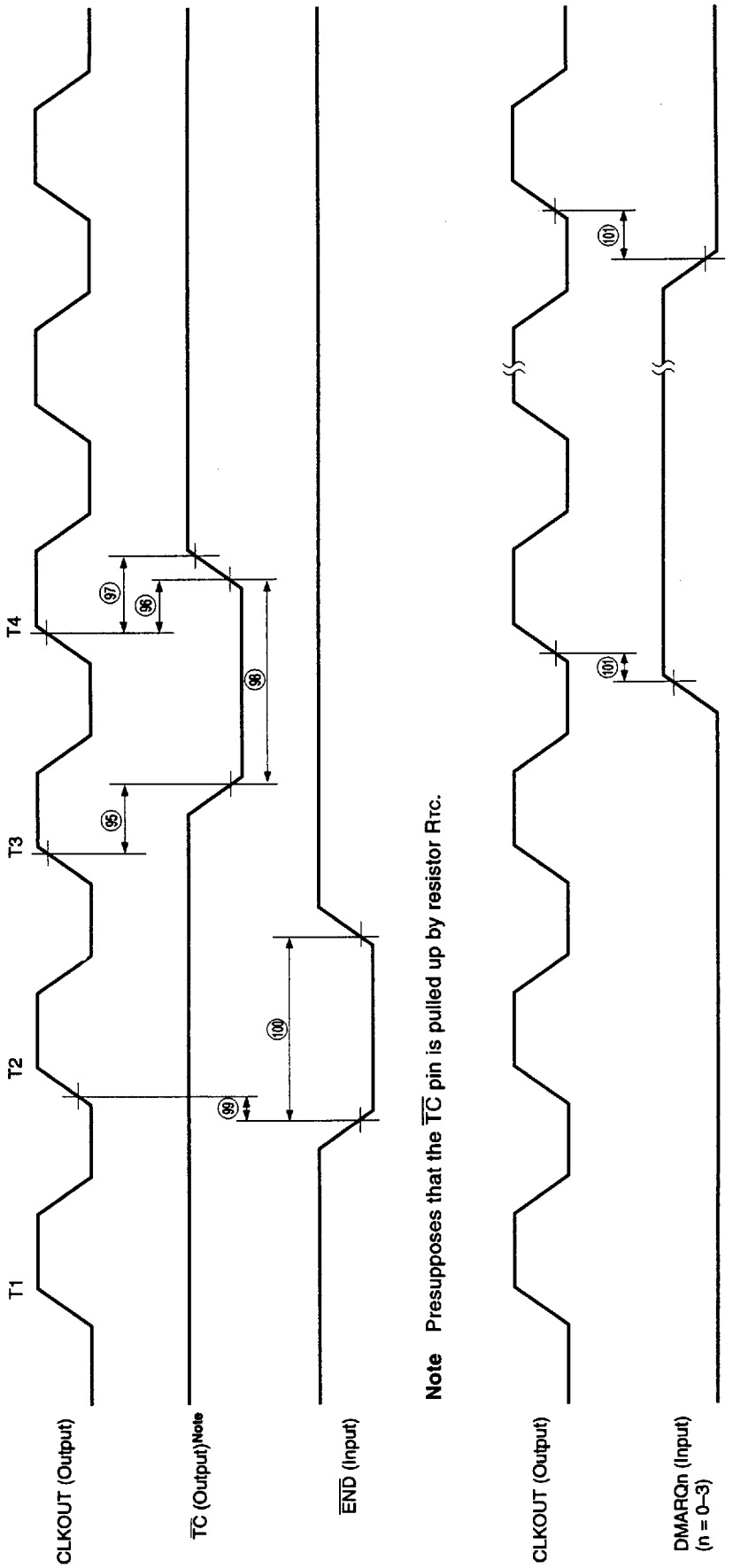


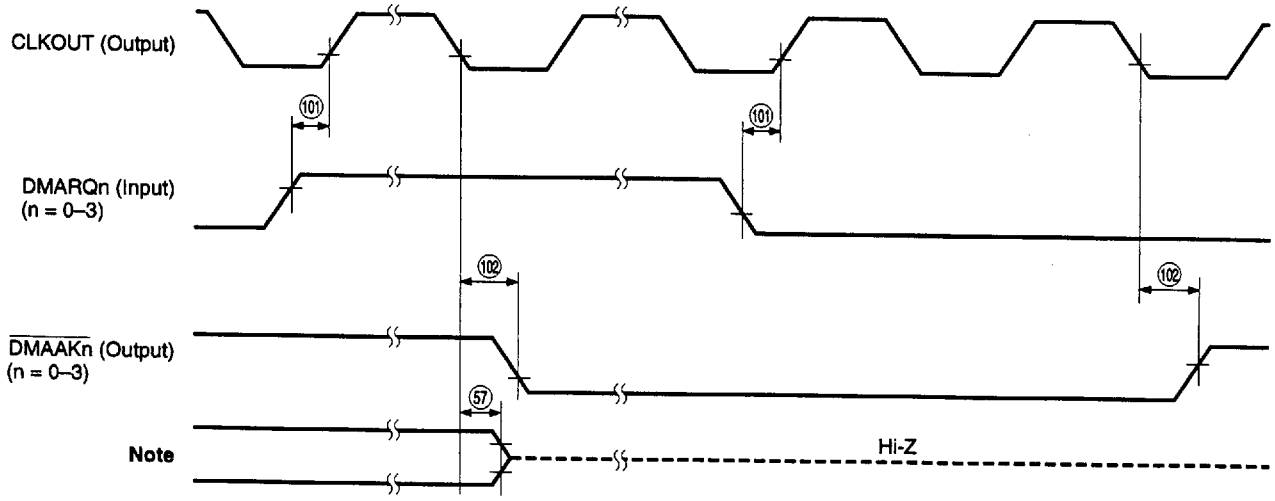
Fig. 15-22 DMAU Timing (2)

Note Presupposes that the $\overline{TC}$ pin is pulled up by resistor RTC.

Remark DMARQn (n = 0 to 3) can be input asynchronously with respect to CLKOUT.

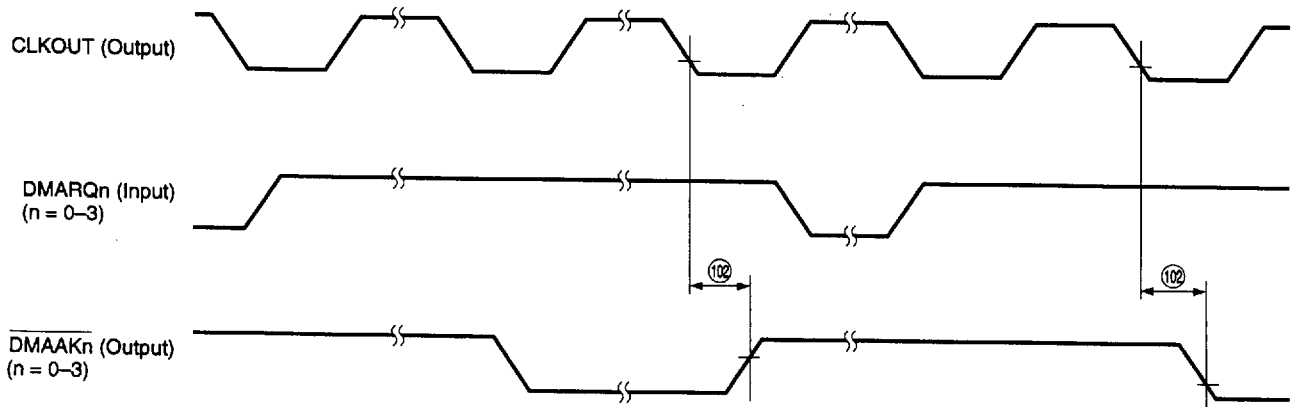
Fig. 15-23 DMAU Timing (3) (Cascade Mode)

(a) Normal Operation



Note A23 to A0, $\overline{UBE}$, $\overline{MRD}$, $\overline{MWR}$, $\overline{IORD}$, $\overline{IOWR}$, $\overline{BUFEN}$, $\overline{BCYST}$, $\overline{DSTB}$

(b) With Refresh Cycle Inserted



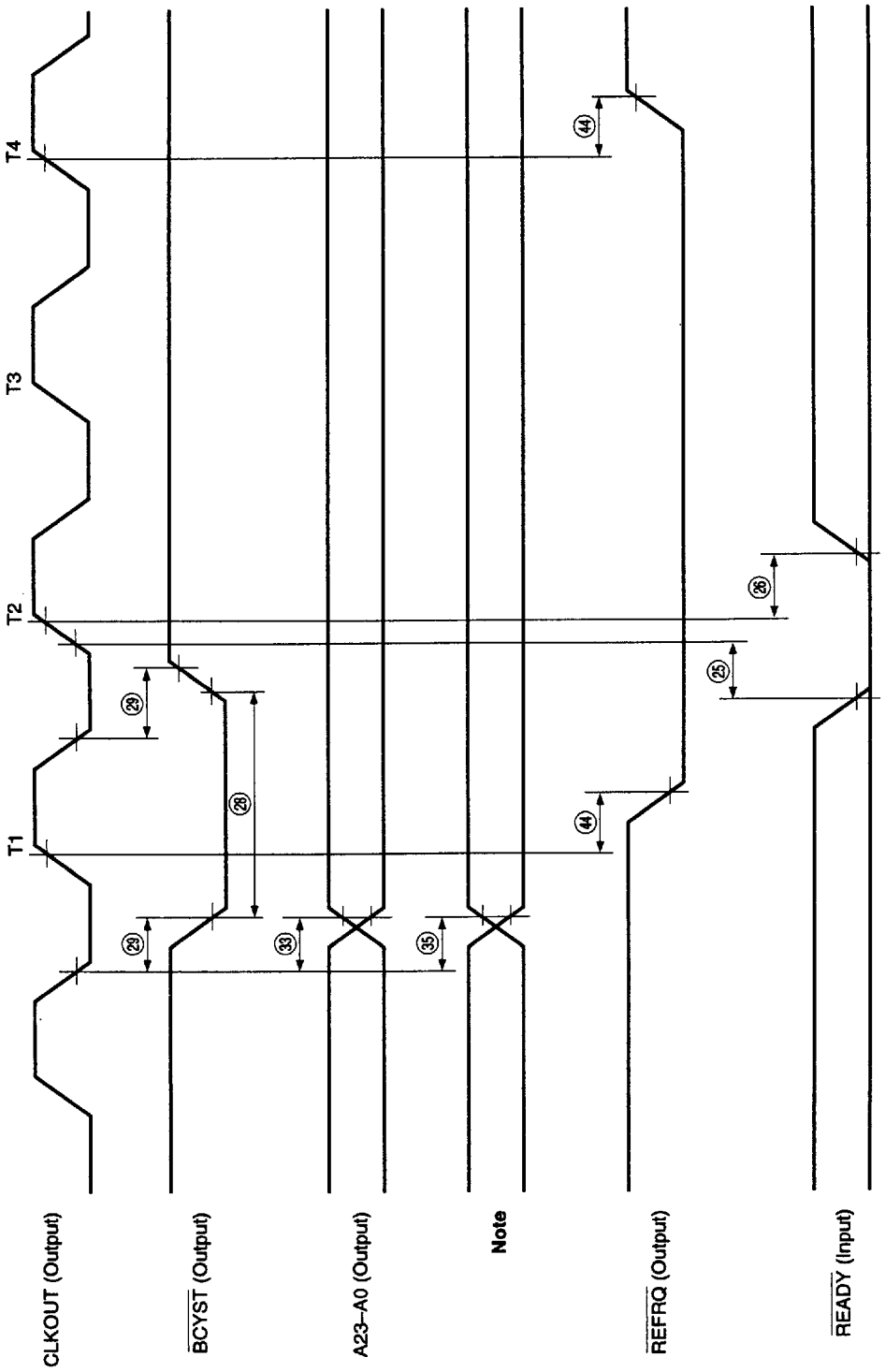
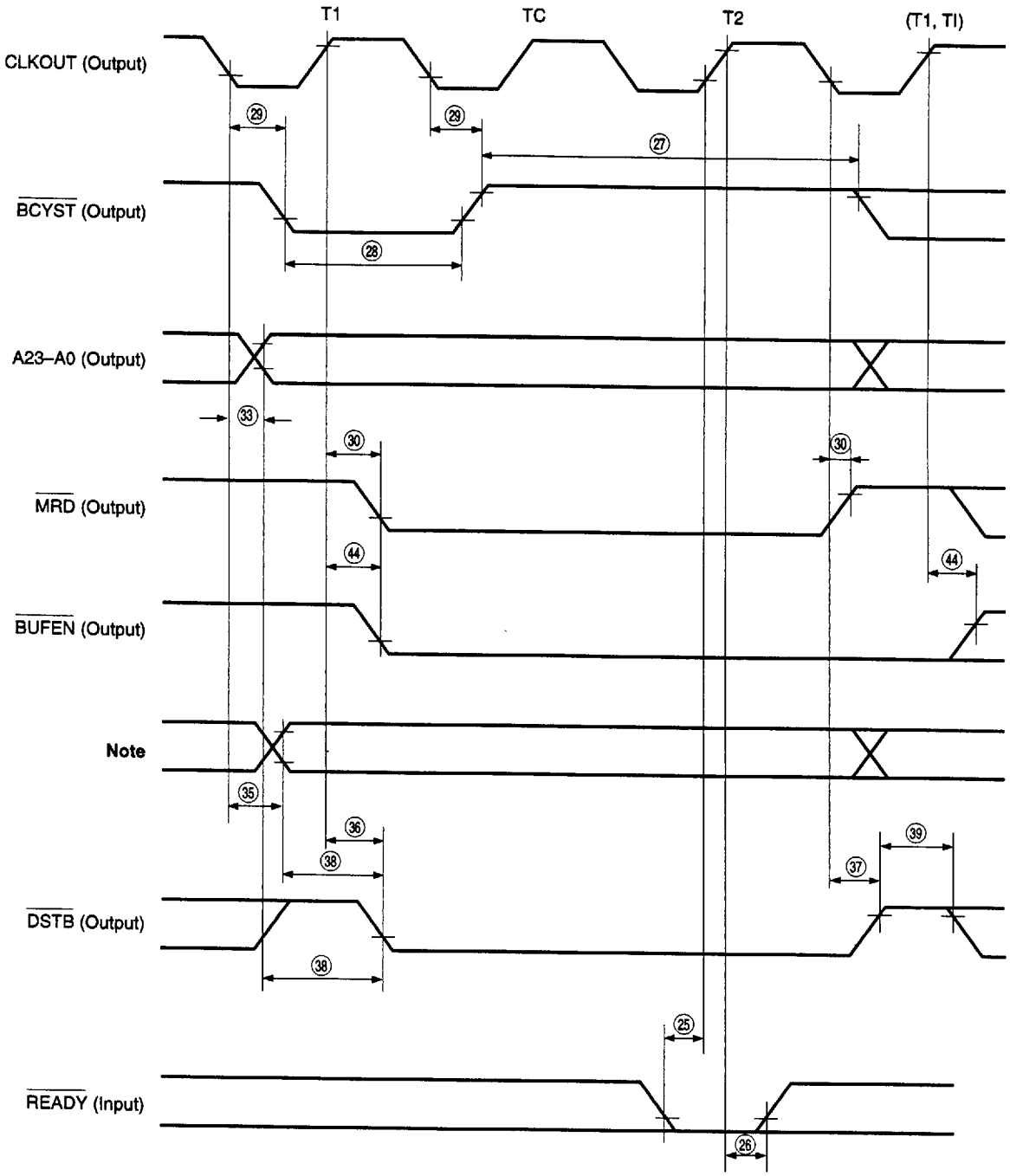


Fig. 15-24 Refresh Timing

Note R/$\overline{W}$, M/$\overline{IO}$, BUSST2, BUSST1, BUSST0, $\overline{UBE}$, AEX (all output)

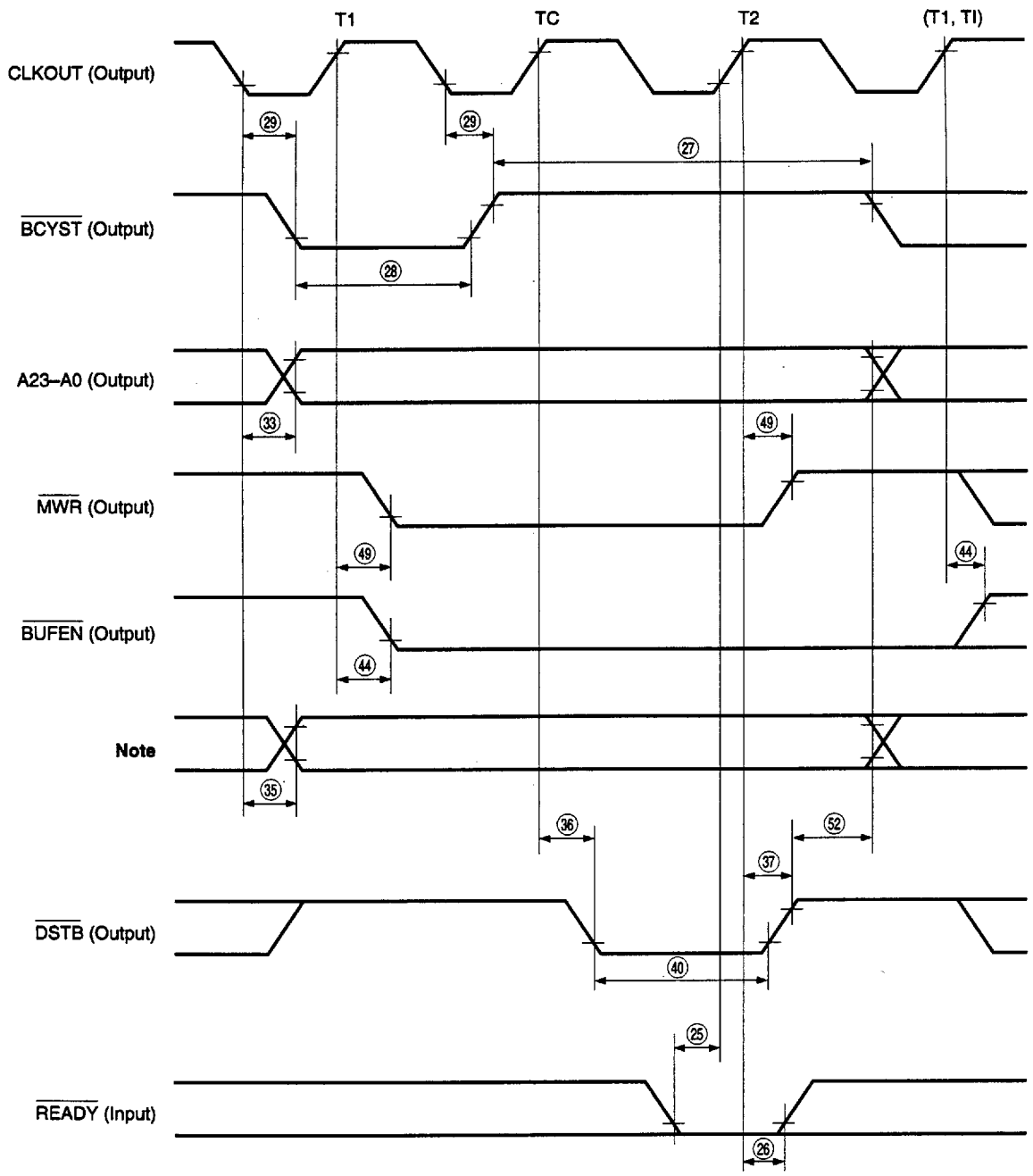
Remark $\overline{DSTB}$ and $\overline{BUFEN}$ are inactive.

Fig. 15-25 Coprocessor Memory Read Cycle (No Wait)



Note R/$\overline{W}$, M/$\overline{IO}$, BUSST2, BUSST1, BUSST0, $\overline{UBE}$, AEX (all output)

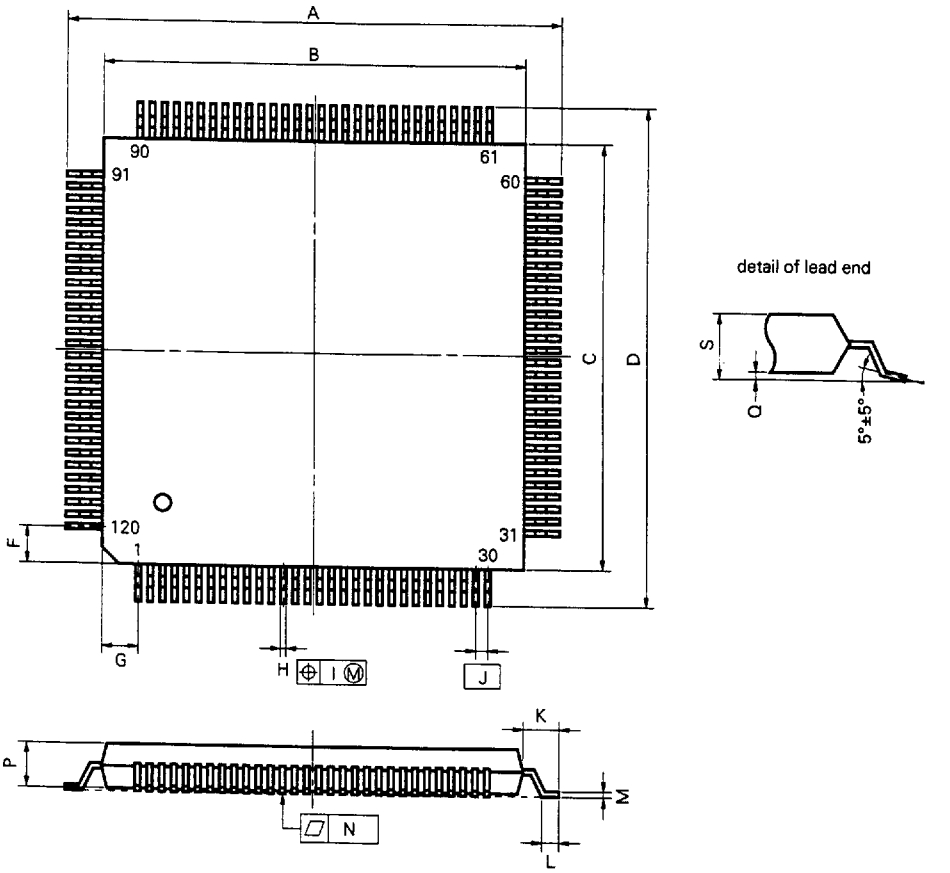
Fig. 15-26 Coprocessor Memory Write Cycle (No Wait)



Note R/$\overline{W}$, M/$\overline{IO}$, BUSST2, BUSST1, BUSST0, $\overline{UBE}$, AEX (all output)

16. PACKAGE DRAWINGS

120 PIN PLASTIC QFP (□28)



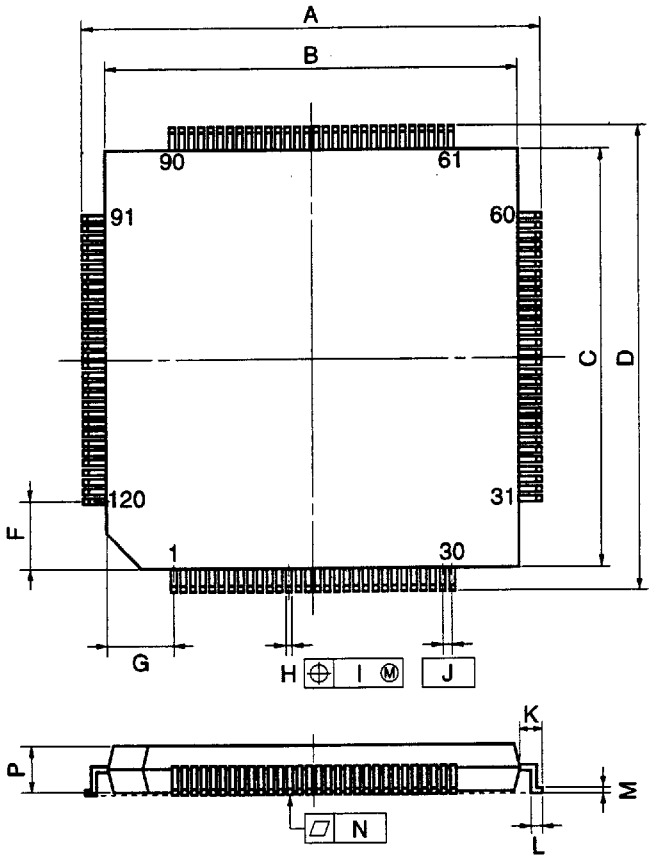
P120GD-80-5BB-3

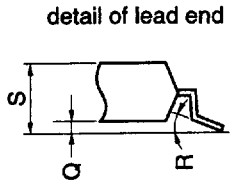
NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	32.0±0.4	1.260±0.016
B	28.0±0.2	$1.102^{+0.009}_{-0.008}$
C	28.0±0.2	$1.102^{+0.009}_{-0.008}$
D	32.0±0.4	1.260±0.016
F	2.4	0.094
G	2.4	0.094
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	2.0±0.2	$0.079^{+0.009}_{-0.008}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	3.7	0.146
Q	0.1±0.1	0.004±0.004
S	4.0 MAX.	0.157 MAX.

120 PIN PLASTIC QFP (FINE PITCH) (□20)





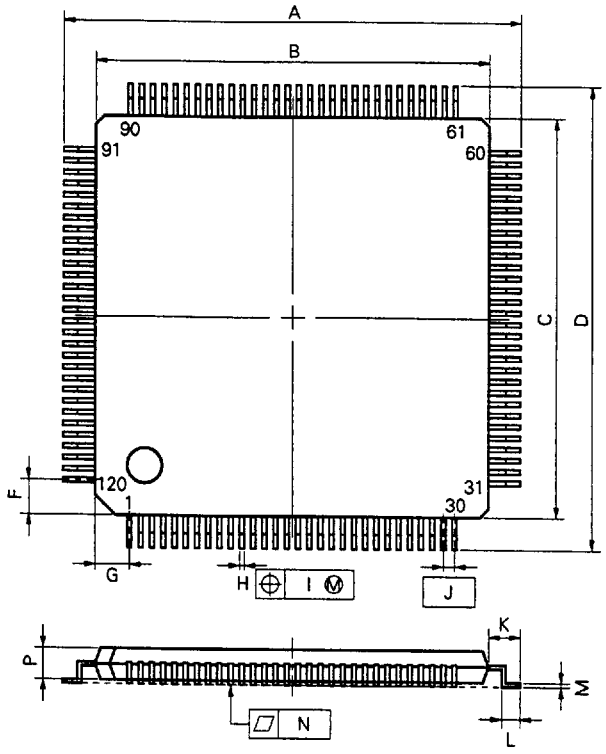
NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

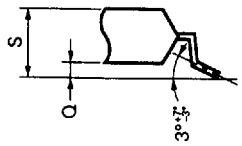
ITEM	MILLIMETERS	INCHES
A	22.0±0.2	0.866±0.008
B	20.0±0.2	$0.787^{+0.009}_{-0.008}$
C	20.0±0.2	$0.787^{+0.009}_{-0.008}$
D	22.0±0.2	0.866±0.008
F	2.75	0.108
G	2.75	0.108
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S120GJ-50-3EB-2

120 PIN PLASTIC TQFP (FINE PITCH) (□14) *



detail of lead end



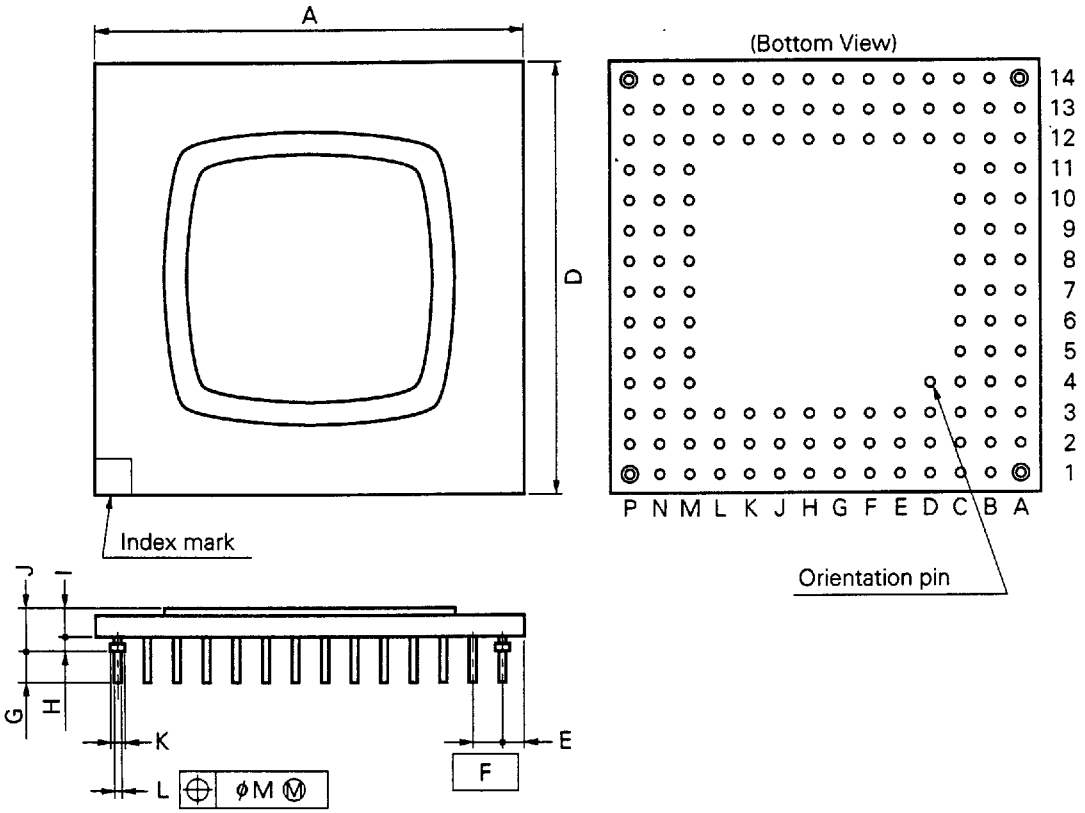
NOTE

Each lead centerline is located within 0.09 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

S120GC-40-9EV

ITEM	MILLIMETERS	INCHES
A	16.0±0.2	0.630±0.008
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	16.0±0.2	0.630±0.008
F	1.2	0.047
G	1.2	0.047
H	0.18±0.05	0.007±0.002
I	0.09	0.004
J	0.4 (T.P.)	0.016 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	0.145±0.05	$0.006^{+0.002}_{-0.003}$
N	0.08	0.003
P	1.0±0.1	$0.039^{+0.005}_{-0.004}$
Q	0.1±0.05	0.004±0.002
S	1.2 MAX.	0.048 MAX.

132 PIN CERAMIC PGA



X132R-100A-1

ITEM	MILLIMETERS	INCHES
A	35.56±0.3	1.400±0.012
D	35.56±0.3	1.400±0.012
E	1.27	0.050
F	2.54 (T.P.)	0.100 (T.P.)
G	2.8±0.3	0.110±0.012
H	0.9 MIN.	0.035 MIN.
I	2.95	0.116
J	4.57 MAX.	0.180 MAX.
K	φ1.2±0.2	$\phi 0.047^{+0.009}_{-0.008}$
L	φ0.46±0.05	φ0.018±0.002
M	0.254	0.010

NOTE

Each lead centerline is located within φ0.5 mm (φ0.020 inch) of its true position (T.P.) at maximum material condition.

17. RECOMMENDED SOLDERING CONDITIONS *

This product should be soldered and mounted under the conditions recommended in the table below.

For details of recommended soldering conditions, refer to the information document **"Semiconductor Device Mounting Technology Manual" (IEI-1207)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 17-1 Surface Mount Type Soldering Conditions

(1) μPD70236AGD-xx-5BB : 120-pin plastic QFP (28 x 28 mm)

Soldering Method	Soldering Conditions	Symbol
Infrared ray reflow	Package peak temperature: 235 °C, Reflow time: 30 seconds or less (at 210 °C or higher), Number of reflow processes: Twice or less, Exposure limit: 7 days[Note] (36 hours pre-baking is required at 125 °C afterwards) <Cautions> (1) The second reflow should be started after the device temperature raised by the first reflow has returned to room temperature. (2) Do not perform flux cleaning with water after the first reflow.	IR35-367-2
VPS	Package peak temperature: 215 °C, Reflow time: 40 seconds or less (at 200 °C or higher), Number of reflow proceses: Twice or less, Exposure limit: 7 days[Note] (36 hours pre-baking is required at 125 °C afterwards) <Cautions> (1) The second reflow should be started after the device temperature raised by the first reflow has returned to room temperature. (2) Do not perform flux cleaning with water after the first reflow.	VP15-367-2
Partial heating	Pin temperature: 300 °C or below, Flow time: 3 seconds or less (per device side)	—

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Use of more than one soldering method should be avoided (except for partial heating).

(2) μPD70236AGJ-xx-3EB : 120-pin plastic QFP (Fine pitch) (20 x 20 mm)

Soldering Method	Soldering Conditions	Symbol
Infrared ray reflow	Package peak temperature: 235 °C, Reflow time: 30 seconds or less (at 210 °C or higher), Number of reflow processes: Twice or less, Exposure limit: 7 days[Note] (36 hours pre-baking is required at 125 °C afterwards) <Cautions> (1) The second reflow should be started after the device temperature raised by the first reflow has returned to room temperature. (2) Do not perform flux cleaning with water after the first reflow.	IR35-367-2
VPS	Package peak temperature: 215 °C, Reflow time: 40 seconds or less (at 200 °C or higher), Number of reflow proceses: Twice or less, Exposure limit: 7 days[Note] (36 hours pre-baking is required at 125 °C afterwards) <Cautions> (1) The second reflow should be started after the device temperature raised by the first reflow has returned to room temperature. (2) Do not perform flux cleaning with water after the first reflow.	VP15-367-2
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or less, Number of flow processes: Once, Preheating temperature: 120°C Max. (package surface temperature), Exposure limit: 7 days[Note] (36 hours pre-baking is required at 125 °C afterwards)	WS60-367-1
Partial heating	Pin temperature: 300 °C or below, Flow time: 3 seconds or less (per device side)	—

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Use of more than one soldering method should be avoided (except for partial heating).

(3) μPD70236AGC-xx-9EV : 120-pin plastic TQFP (Fine pitch) (14 x 14 mm)

Soldering Method	Soldering Conditions	Symbol
Infrared ray reflow	Package peak temperature: 235 °C, Reflow time: 30 seconds or less (at 210 °C or higher), Number of reflow processes: Twice or less, Exposure limit: 3 days[Note] (10 hours pre-baking is required at 125 °C afterwards) <Cautions> (1) The second reflow should be started after the device temperature raised by the first reflow has returned to room temperature. (2) Do not perform flux cleaning with water after the first reflow.	IR35-103-2
VPS	Package peak temperature: 215 °C, Reflow time: 40 seconds or less (at 200 °C or higher), Number of reflow proceses: Twice or less, Exposure limit: 3 days[Note] (10 hours pre-baking is required at 125 °C afterwards) <Cautions> (1) The second reflow should be started after the device temperature raised by the first reflow has returned to room temperature. (2) Do not perform flux cleaning with water after the first reflow.	VP15-103-2
Partial heating	Pin temperature: 300 °C or below, Flow time: 3 seconds or less (per device side)	—

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Use of more than one soldering method should be avoided (except for partial heating).

Table 17-2 Through-Hole Type Soldering Conditions

μPD70236ARB-xx : 132-pin ceramic PGA

Soldering Method	Soldering Conditions
Wave soldering (only to pins)	Solder temperature: 260 °C or below, Flow time: 10 seconds or less
Partial heating	Pin temperature: 300 °C or below, Flow time: 3 seconds or less (per pin)

Caution The wave soldering process must be applied only to pins, and make sure that the package body does not get jet soldered.

APPENDIX SOFTWARE DIFFERENCES BETWEEN μPD70236A AND μPD70236

Item		μPD70236A	μPD70236, 70236(A)
Prefix		· Up to 7 can be stored. · If two or more prefixes of the same kind are attached, only the prefix nearest the instruction is valid, and the others are ignored.	· Any number of prefixes can be attached as long as they are of different kinds (up to three kinds in total). · Two or more prefixes of the same kind should not be attached.
ADJ4A, ADJ4S instructions[Note 1]		If 9AH ≤ AL ≤ 9FH: Adjustment of higher 4 bits is performed only when AC = 0. [Instruction function] · When AL ∧ 0FH > 9 or AC = 1 Adjusts lower 4 bits of AL register. · When AL > 9FH or CY = 1 Adjusts higher 4 bits of AL register. · When 99H < AL < A0H and AC = 0 Adjusts higher 4 bits of AL register.	If 9AH ≤ AL ≤ 9FH: Adjustment of higher 4 bits is always performed. [Instruction function] · When AL ∧ 0FH > 9 or AC = 1 Adjusts lower 4 bits of AL register. · When AL > 99H or CY = 1 Adjusts higher 4 bits of AL register.
CVTBD, CVTDB instructions		Calculation always performed even if 2nd byte of operation code is not 0AH.	Misoperation results if 2nd byte of operation code is not 0AH.
PUSH SP instruction POP SP instruction		(SP – 2) ← SP – 2[Note 2] SP ← (SP)	(SP – 2) ← SP SP ← (SP)
PREPARE instruction restrictions		None	Restrictions on instructions that can be executed directly after PREPARE instruction.
DIV error/CHKIND exception interrupt return address		Returns to instruction address after that at which exception was generated.	Returns to instruction address at which exception was generated.
DIV instruction (signed division)		A DIV information divide error occurs if the quotient is 80H (in a byte operation) or 8000H (in a word operation).	Calculation is performed normally if the quotient is 80H (in a byte operation) or 8000H (in a word operation).
Interrupt vector numbers	Unimplemented instruction	6	122
	Coprocessor non-existent	7	130
	μPD72291 error	16	128

Notes 1. This difference appears as such if adjustment is performed on the result of an operation on non-decimal data. (The situation in which 9AH ≤ AL ≤ 9FH and AC=1 will not arise in an operation on decimal data.)

2. When executing a combination of the PUSH and POP instructions for the SP register, the value before instruction execution, minus 2 is saved to the SP register.

Remark There are three kinds of prefix, as follows:
- Repeat ... REPC, REPNC, REPZ, REPNZ
- Segment override ... PS:, DS0:, DS1:, SS:
- Bus lock ... BUSLOCK

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.