
HM62832UH Series

256 k High Speed SRAM (32-kword × 8-bit)

HITACHI

Features

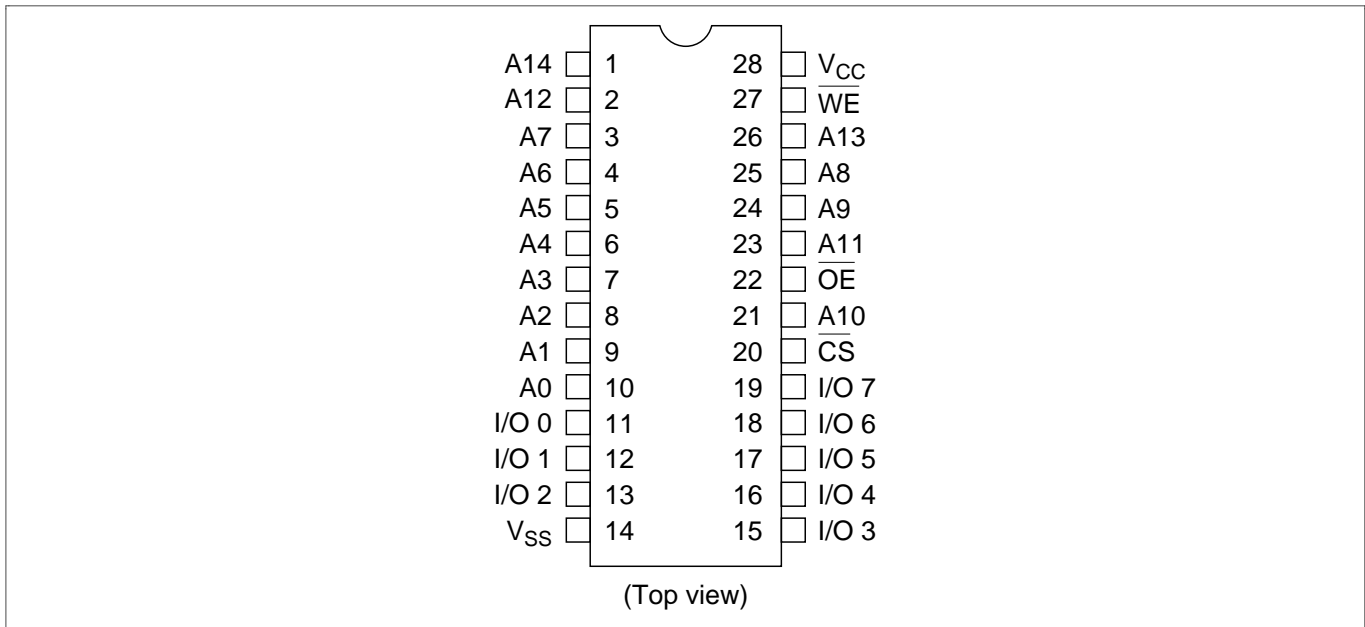
- High speed: Fast access time 15/20 ns (max)
- Low Power
Standby: 15 μ W (typ) (L-version)
Operation: 675/600 mW (typ)
- Single 5 V supply
- Completely static memory
No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs

Ordering Information

Type No.	Access Time	Package
HM62832UHP-15	15 ns	300-mil 28-pin plastic DIP (DP-28NA)
HM62832UHP-20	20 ns	
HM62832UHLP-15	15 ns	
HM62832UHLP-20	20 ns	
HM62832UHJP-15	15 ns	300-mil 28-pin plastic SOJ (CP-28DN)
HM62832UHJP-20	20 n	
HM62832UHLJP-15	15 ns	
HM62832UHLJP-20	20 ns	

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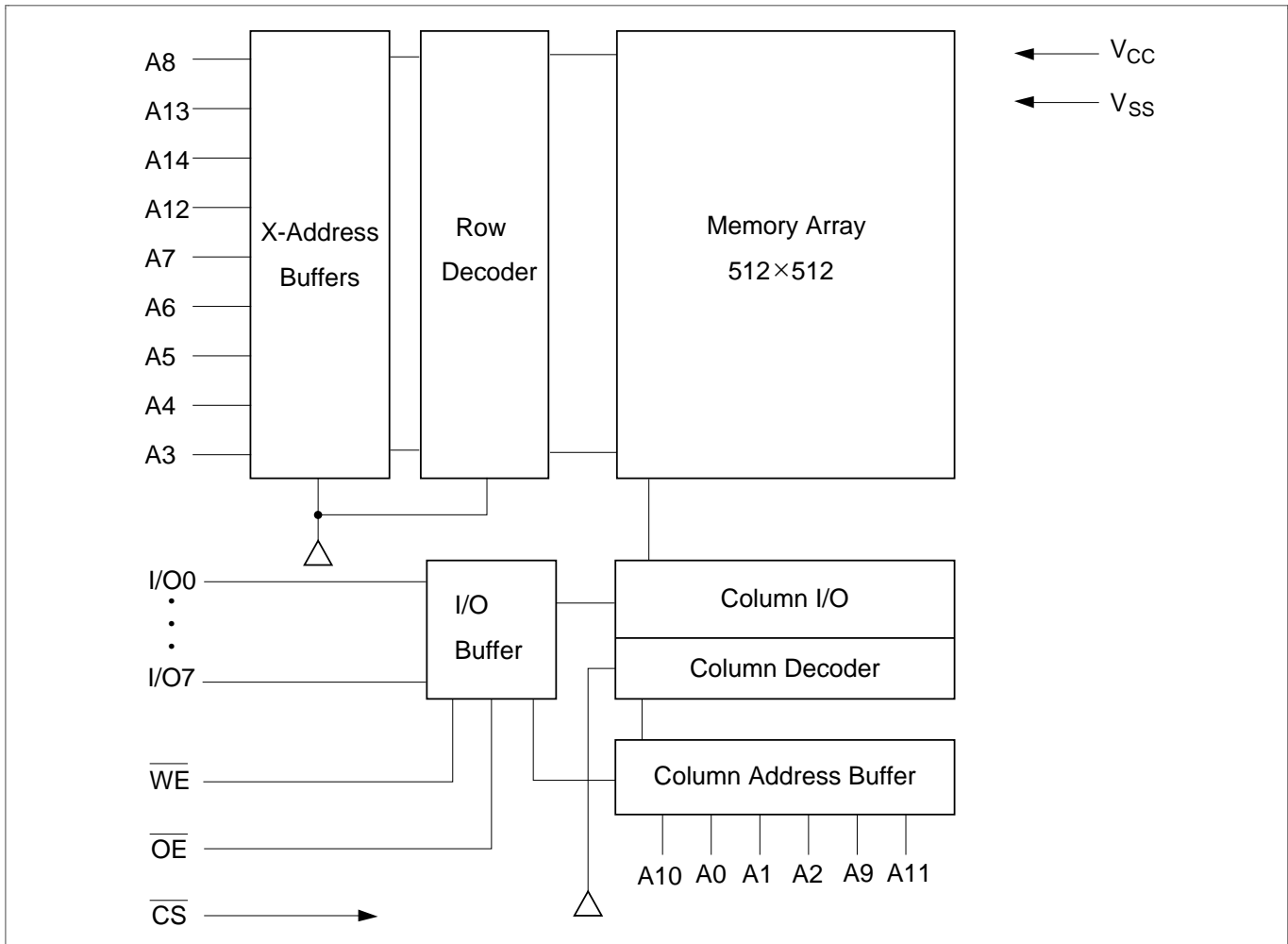
Pin Arrangement



Pin Description

Pin name	Function
A0 – A14	Address
I/O0 – I/O7	Input/output
\overline{CS}	Chip select
\overline{WE}	Write enable
\overline{OE}	Output enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Function Table

\overline{CS}	\overline{OE}	\overline{WE}	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	Standby	I_{SB}, I_{SB1}	High-Z	
L	L	H	Read	I_{CC}	Dout	Read cycle 1, 2, 3
L	H	L	Write	I_{CC}	Din	Write cycle 1
L	L	L	Write	I_{CC}	Din	Write cycle 2

Note: X : H or L

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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage ¹	V_{CC}	-0.5 ² to +7.0	V
Voltage on any pin relative to V_{SS} ¹	V_T	-0.5 ² to $V_{CC} + 0.5$	V
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C
Storage temperature under bias	T_{bias}	-10 to +85	°C

Notes: 1. With respect to V_{SS}
2. V_{CC} and V_T min = -2.5 V for pulse width ≤ 10 ns

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	$V_{CC} + 0.5$	V
Input low (logic 0) voltage	V_{IL}	-0.5 ¹	—	0.8	V

Note: 1. V_{IL} min = -2.0 V for pulse width ≤ 10 ns

DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Min	Typ ¹	Max	Unit	Test Conditions
Input leakage current	$ I_{UI} $	—	—	2.0	μA	$V_{CC} = 5.5\text{ V}$ $V_{in} = V_{SS}$ to V_{CC}
Output leakage current	$ I_{LO} $	—	—	2.0	μA	$\overline{CS} = V_{IH}$ $V_{IO} = V_{SS}$ to V_{CC}
Operating V_{CC} current	$I_{CC1}(-15)^3$	—	135	170	mA	min cycle ²
	$I_{CC2}(-15)$	—	100	120	mA	2x min cycle
	$I_{CC1}(-20)$	—	120	150	mA	min cycle
	$I_{CC2}(-20)$	—	90	110	mA	2x min cycle
Standby V_{CC} current	$I_{SB}(-15)$	—	40	60	mA	$\overline{CS} = V_{IH}$, min cycle
	$I_{SB}(-20)$	—	30	50		
Standby V_{CC} current (1)	$I_{SB1}(\text{L-version})$	—	0.02	2.0	mA	$\overline{CS} \geq V_{CC} - 0.2\text{ V}$ $0\text{ V} \leq V_{in} \leq 0.2\text{ V}$ or $V_{CC} - 0.2\text{ V} \leq V_{in}$
		—	0.003	0.1		
Output low voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 8\text{ mA}$
Output high voltage	V_{OH}	2.4	—	—	V	$I_{OH} = -4.0\text{ mA}$

Notes: 1. Typical values are at $V_{CC} = 5.0\text{ V}$, $T_a = 25^\circ\text{C}$ and not guaranteed.

2. $\overline{CS} = V_{IL}$, $I_{out} = 0\text{ mA}$

3. Access time version

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$)*¹

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{in}	—	—	6	pF	$V_{in} = 0\text{ V}$
Output capacitance	C_{out}	—	—	10	pF	$V_{IO} = 0\text{ V}$

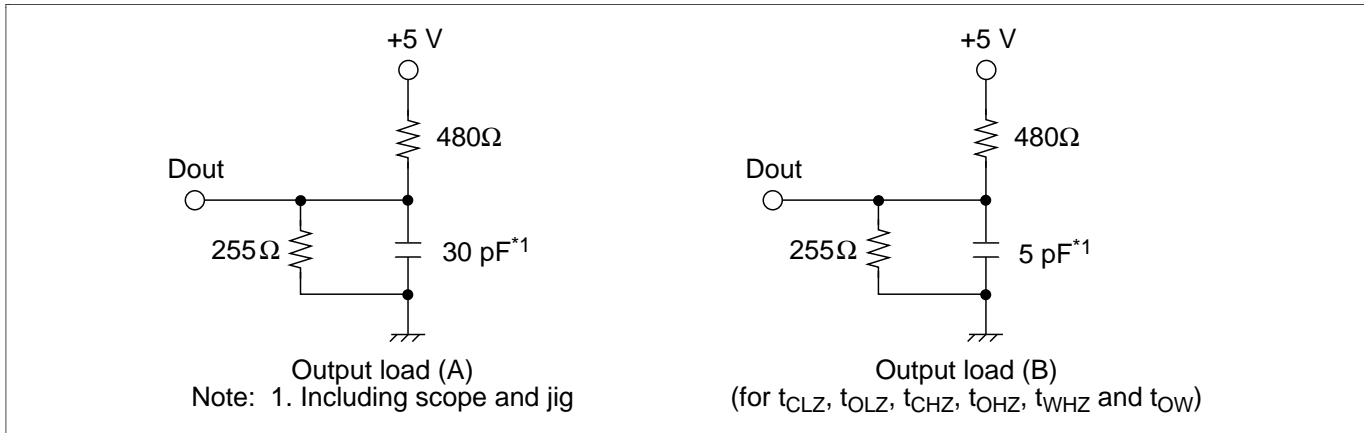
Note: 1. This parameter is sampled and not 100% tested.

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AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall time: 4 ns
- Input and Output timing reference levels: 1.5 V
- Output load: See figures

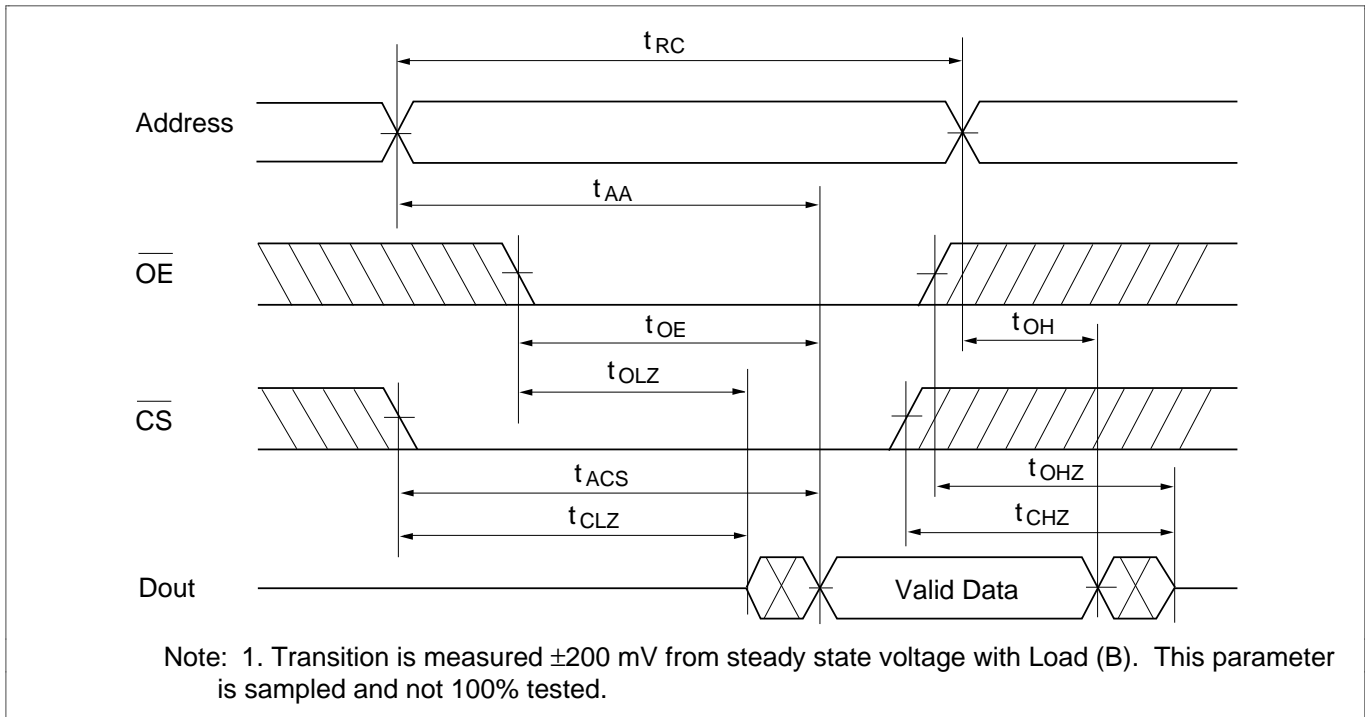


Read Cycle

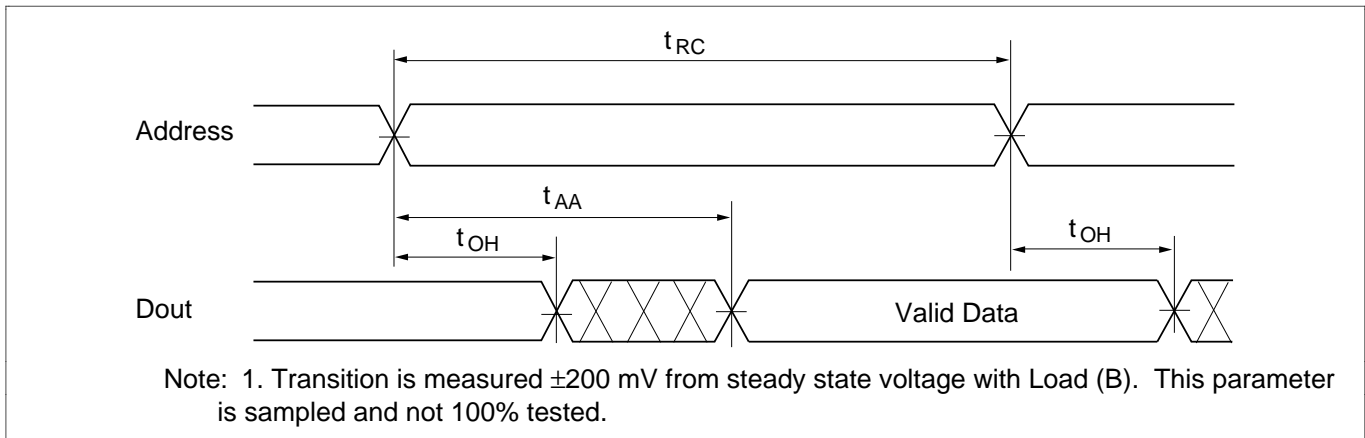
Parameter	Symbol	HM62832UH-15		HM62832UH-20		Unit
		Min	Max	Min	Max	
Read cycle time	t_{RC}	15	—	20	—	ns
Address access time	t_{AA}	—	15	—	20	ns
Chip select access time	t_{ACS}	—	15	—	20	ns
Chip selection to output in low-Z	t_{CLZ}^{*1}	3	—	3	—	ns
Output enable to output valid	t_{OE}	—	8	—	10	ns
Output enable to output in low-Z	t_{OLZ}^{*1}	0	—	0	—	ns
Chip deselection to output in high-Z	t_{CHZ}^{*1}	0	7	0	10	ns
Chip disable to output in high-Z	t_{OHZ}^{*1}	0	7	0	10	ns
Output hold from address change	t_{OH}	3	—	3	—	ns

Note: 1. Transition is measured ± 200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

Read Timing Waveform (1)*1 ($\overline{WE} = V_{IH}$)

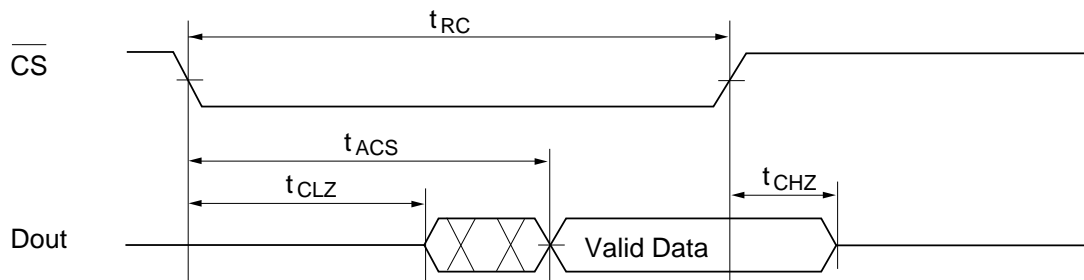


Read Timing Waveform (2)*1 ($\overline{WE} = V_{IH}, \overline{CS} = V_{IL}, \overline{OE} = V_{IL}$)



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Read Timing Waveform (3) ^{*1, *2} ($\overline{WE} = V_{IH}$, $\overline{OE} = V_{IL}$)



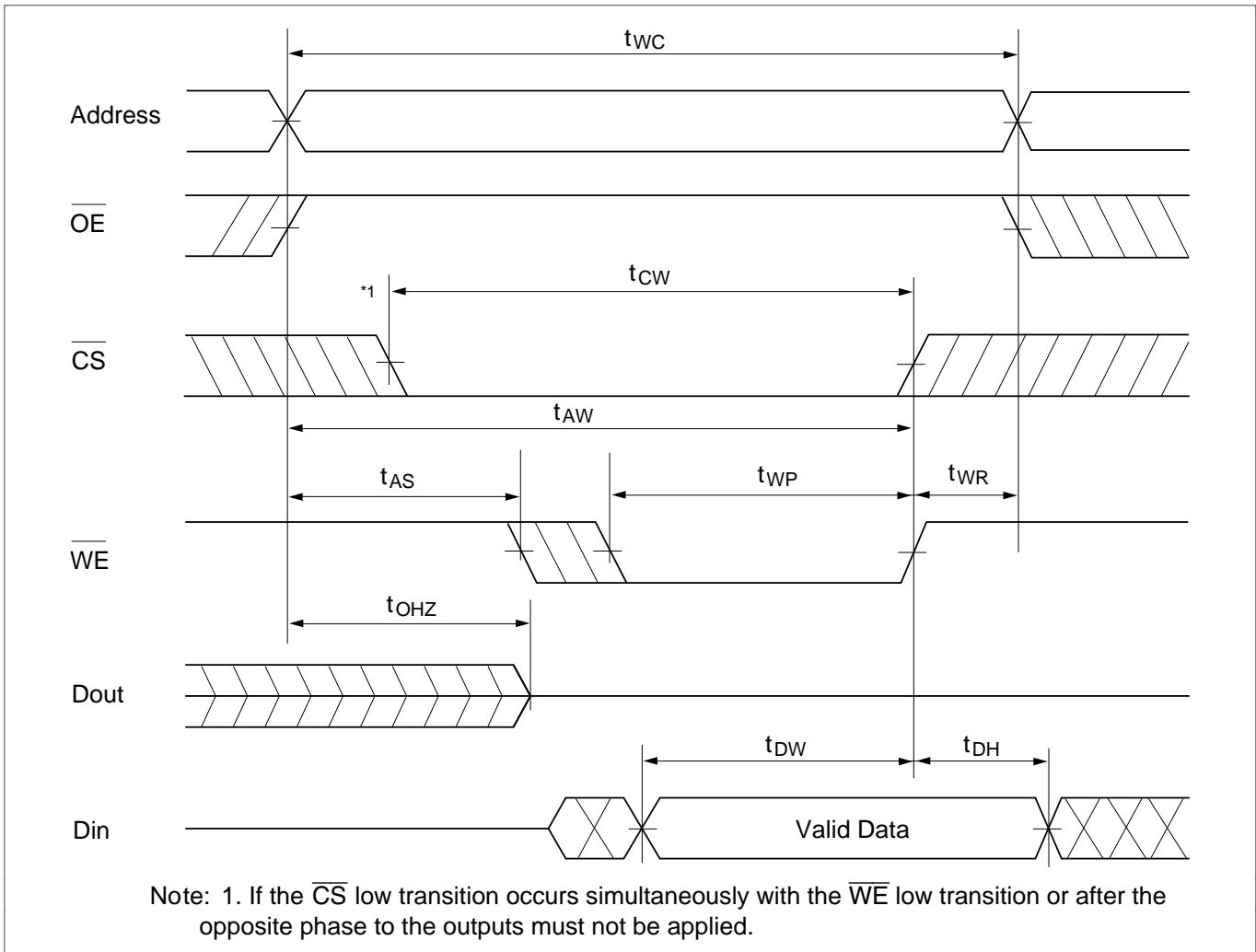
- Notes: 1. Transition is measured ± 200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
2. Address valid prior to or coincident with \overline{CS} transition low.

Write Cycle

Parameter	Symbol	HM62832UH-15		HM62832UH-20		Unit
		Min	Max	Min	Max	
Write cycle time	t_{WC}	15	—	20	—	ns
Chip selection to end of write	t_{CW}	10	—	12	—	ns
Address valid to end of write	t_{AW}	13	—	15	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width ²	t_{WP}	10	—	12	—	ns
Write recovery time ³	t_{WR}	0	—	0	—	ns
Output disable to output in high-Z ^{1, 4}	t_{OHZ}	0	7	0	10	ns
Write to output in high-Z ^{1, 4}	t_{WHZ}	0	7	0	10	ns
Data to write time overlap	t_{DW}	8	—	10	—	ns
Data hold from write time ⁶	t_{DH}	0	—	0	—	ns
Output active from end of write ^{1, 6}	t_{OW}	3	—	3	—	ns
Output hold from address change ⁵	t_{OH}	3	—	3	—	ns

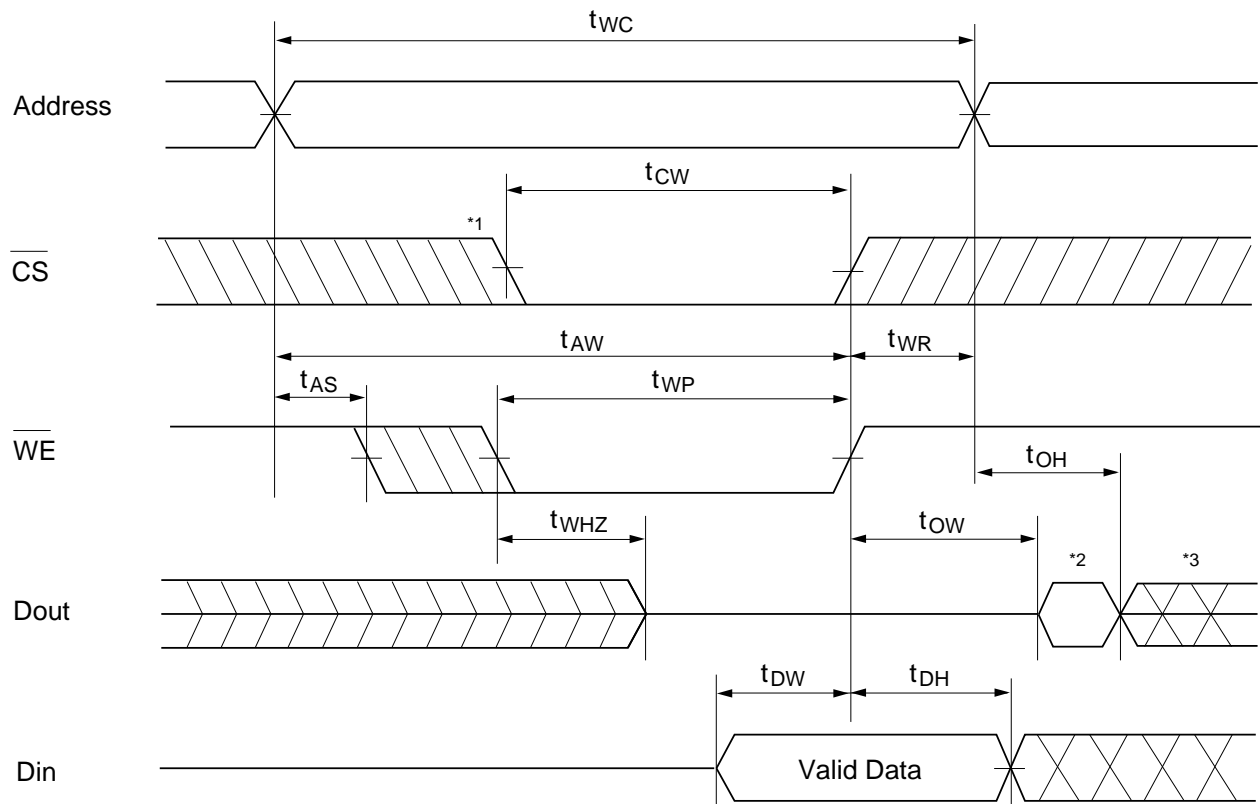
- Notes: 1. Transition is measured ± 200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.
2. A write occurs during the overlap (t_{WP}) to a low \overline{CS} and a low \overline{WE} .
3. t_{WR} is measured from the earliest of \overline{CS} or \overline{WE} going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
5. $Dout$ is the same phase of write data of this write cycle.
6. If \overline{CS} is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

Write Timing Waveform (1)



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Write Timing Waveform (2) (\overline{OE} low Fixed)^{*4}



Notes: 1. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transitions or after the \overline{WE} transition, output remain in a high impedance state.

2. Dout is the same phase of write data of this write cycle.

3. Dout is the read data of next address.

4. \overline{WE} must be high during all address transition except when device is disable with \overline{CS} .

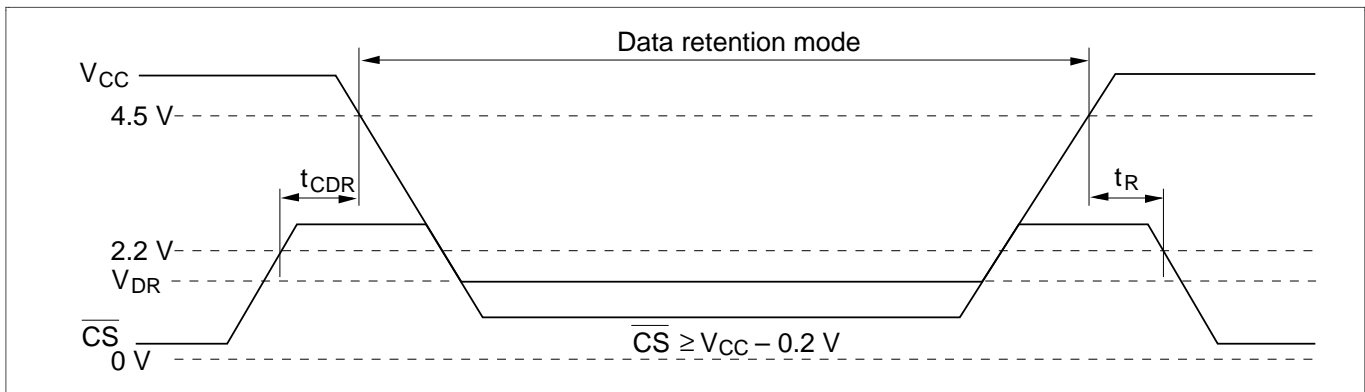
Low V_{CC} Data Retention Characteristics ($T_a = 0$ to $+70^{\circ}\text{C}$)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{CC} for data retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2\text{V}$, $V_{in} \geq V_{CC} - 0.2\text{V}$ or $0\text{V} < V_{in} \leq 0.2\text{V}$
Data retention current	I_{CCDR}	—	2	50^{+1}	μA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

Note: 1. $V_{CC} = 3.0\text{V}$

Low V_{CC} Data Retention Timing Waveform

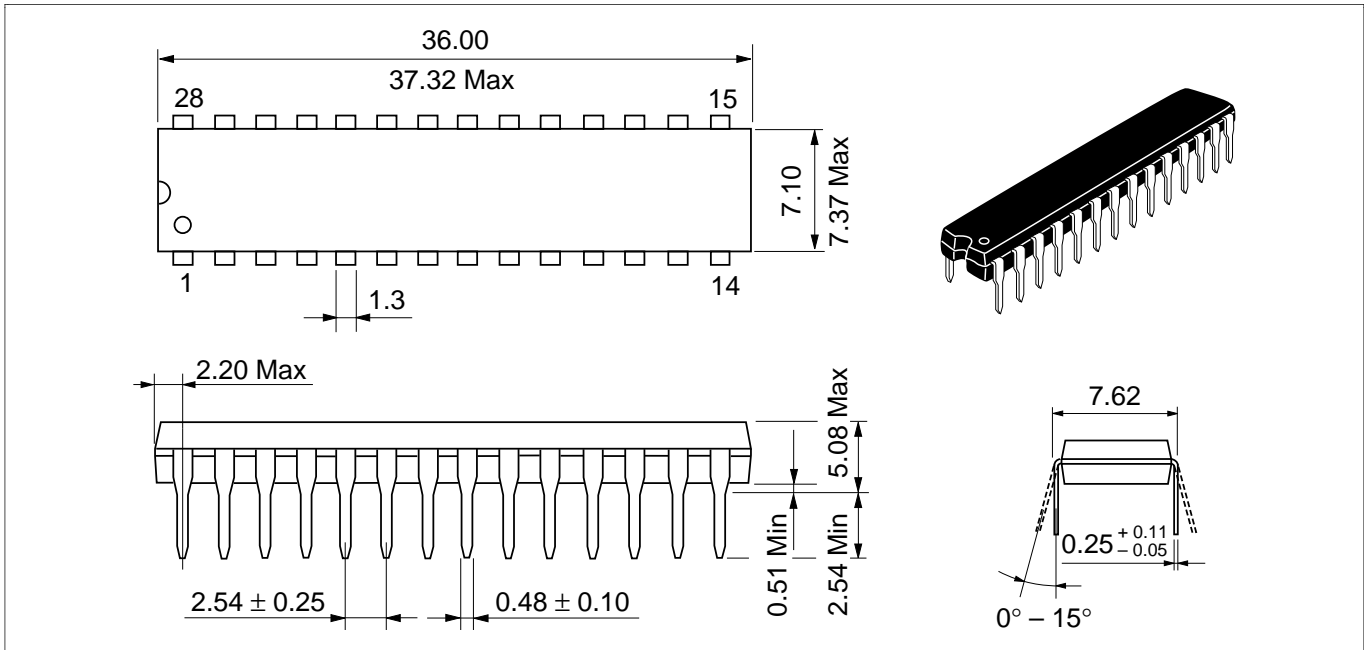


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Package Dimensions

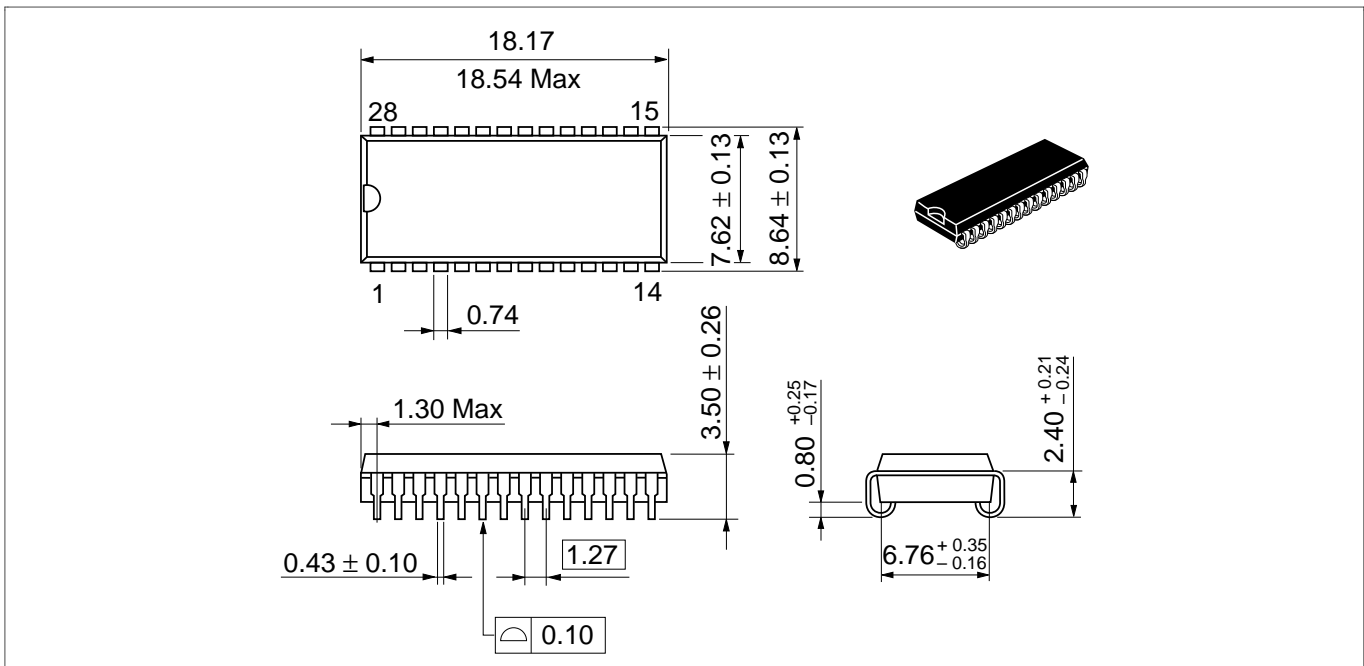
HM62832UHP/UHLP Series (DP-28NA)

Unit: mm



HM62832UHJP/UHLJP Series (CP-28DN)

Unit: mm



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