MB8876A
MB8877A

October 1986
Edition 2.0

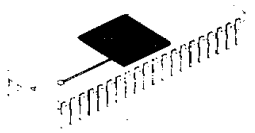
FLOPPY DISK FORMATTER/CONTROLLER (FDC)

DESCRIPTION

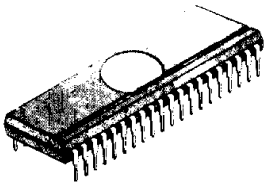
The Fujitsu MB8876A and MB8877A are one-chip Floppy Disk Formatter/Controllers (FDC) which are fabricated with N-channel E/D MOS technology. They can be applied to any single density floppy disk, double density floppy disk and mini floppy disk.

The IBM3740 format and the frequency modulation (FM) recording are used for the single density storage, and the IBM System-34 format and the modified frequency modulation (MFM) recording are used for the double density storage.

The MB8867A and MB8877A interface with an 8-bit parallel microprocessor to control data transfer and mechanical operation. They are packaged in a standard 40-pin dual in-line package.



CERAMIC DIP
DIP-40C-A01

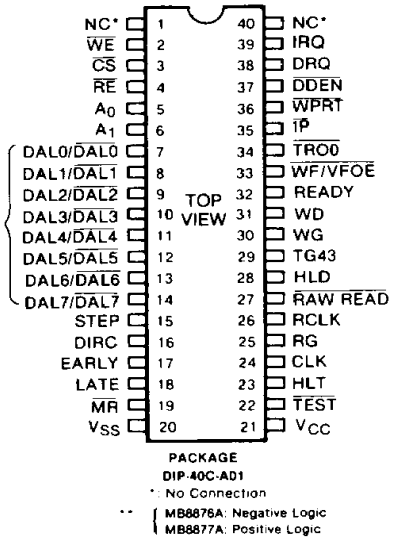


PLASTIC DIP
DIP-40P-M01

FEATURES

- **Interface to 8-bit Microprocessor**
  - **MB8876A: Negative-logic 8-bit Data Bus**
  - **MB8877A: Positive-logic 8-bit Data Bus**
- **IBM Compatible Sector Format**
- **Automatic Track Seeking and Verification**
- **Both Single and Double Density Formats**
  - **a) Single Density in IBM3740 Format and FM Recording**
  - **b) Double Density in IBM System-34 Format and MFM Recording**
- **Programmable Single Sector/ Multiple Sectors/Entire Track Read Operation**
- **Programmable Single Sector/ Multiple Sectors/Entire Track Write Operation**
- **Programmable Side Compare Function**
- **Programmable Sector Length**
- **Programmable Head Step Rate**
- **Applicable to Single Density, Double Density, and Mini Floppy Disks**
- **Programmable Head Engage/Head Settle Time**
- **Double Buffered Data I/O**
- **DMA Data Transfer Capability**
- **Write Precompensation Capability**
- **All TTL Compatible I/O**
- **Single +5V Power Supply**
- **N-Channel Silicon-gate E/D MOS Process**
- **MB8876A: Upward Compatible with Western Digital FD1791-02**
- **MB8877A: Upward Compatible with Western Digital FD1793-02**
- **Two Package Options**
  - **—40-pin Ceramic DIP (Suffix: -C)**
  - **—40-pin Plastic DIP (Suffix: -P)**

PIN ASSIGNMENT



PACKAGE
DIP-40C-A01

* : No Connection

** : MB8876A: Negative Logic
MB8877A: Positive Logic

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PIN DESCRIPTIONS

Pin No.	Symbol	Pin Name	I/O	Description
20	V_{SS}	Power Supply	I	Ground (GND)
21	V_{CC}			+5V DC supply
24	CLK	Clock	I	2-MHz fixed frequency clock signal (1-MHz for mini-floppy disk).
19	$\overline{MR}$	Master Reset	I	Signal for resetting the FDC.
22	$\overline{TEST}$	Test	I	Signal for setting the FDC into a test mode.
1, 40	NC	Non Connection	—	These pins are not used.

MPU INTERFACE PINS

37	$\overline{DDEN}$	Double Density	I	Signal for selecting a FDC operation mode: When $\overline{DDEN}$ = 0, the double density operation mode is selected. When $\overline{DDEN}$ = 1, the single density operation mode is selected. This input must be fixed while the FDC is in busy state.
3	$\overline{CS}$	Chip Select	I	Signal for controlling the DALs: When $\overline{CS}$ = 0, the DALs are activated and data transfer between the FDC and the MPU is enabled. When $\overline{CS}$ = 1, the DALs are in high impedance state and data transfer is inhibited. (i.e., $\overline{RE}$ and $\overline{WE}$ are ignored.)
4	$\overline{RE}$	Read Enable	I	Strobe signal provided when data is read from internal registers: When $\overline{CS}$ = $\overline{RE}$ = 0, data can be read from internal registers.
2	$\overline{WE}$	Write Enable	I	Strobe signal provided when data is written into internal registers: When $\overline{CS}$ = $\overline{WE}$ = 0, data can be written internal registers.
5, 6	A_0, A_1	Register Select Line	I	Signal for addressing an internal register among Command Register (CR), Status Register (STR), Track Register (TR), Sector Register (SCR) and Data Register (DR): Refer to table of REGISTER SELECTION (p. 6).
7 ~ 14	$\overline{DAL_0} \sim \overline{DAL_7}$ $DAL_0 \sim DAL_7$	Data Access Line	I/O	8-bit bidirectional bus for transferring 8-bit data between the FDC and the MPU. MB8876A: negative logic/MB8877A: positive logic.
38	DRQ	Data Request	O	Signal for informing the MPU of a DR status: Read operation: DRQ = 1 shows the DR is filled with a 8-bit data from a disk, and the FDC is requesting for the MPU to read the data. Write operation: DRQ = 1 shows the DR is empty, and the FDC is requesting for the MPU to write the next data into the DR.
39	IRQ	Interrupt Request	O	Interrupt signal to the MPU: IRQ is set when a Command is completed or the TYPE IV Command is executed. IRQ is reset when the next Command is written or the STR is read.

FLOPPY DISK INTERFACE PINS

Disk Head Control Signal

15	STEP	Step Move	O	Step pulse signal for moving a disk head.
16	DIRC	Direction	O	Signal for indicating a direction of disk head moving to the FDD: DIRC = 0 shows the head moves toward outside. DIRC = 1 shows the head moves toward inside.
28	HLD	Head Load	O	Signal for loading a disk head: When HLD = 1, the head is engaged on the disk. When HLD = 0, the head is released from the disk.

Disk Head Control Signal (Continued)

Pin No.	Symbol	Pin Name	I/O	Description
23	HLT	Head Load Timing	I	Signal for informing a disk head status: HLT = 1 shows a disk head is in an enagaged state. HLT is set when a disk head has been settled or a head settle time pre-determined by one shot circuit has elapsed after HLD = 1.
34	$\overline{TR00}$	Track 00	I	Signal for informing whether a disk head is positioned on Track No. 00 or not: $\overline{TR00}$ = 0 shows Track No. 00 is detected during track seaking operation.
32	READY	Ready	I	Signal for informing the FDC of a disk drive status: READY = 1 shows the disk drive is ready for operation, and only when READY = 1, read/write operation for disk can be executed. READY = 0 shows the disk drive is not ready, and neither read/write operation cannot be executed. However, seek operation is executed regardless of this signal.
35	$\overline{IP}$	Index Pulse	I	Signal for informing the FDC of an index hole of disk being detected in the FDD.

Disk Read Operation Signal

25	RG	Read Gate	O	Signal for informing synchronization between RCLK and $\overline{RAWREAD}$ to an external VFO circuit: RG = 1 show the FDC has found out a SYNC byte during disk reading operation.
26	RCLK	Read Clock	I	A data window signal which is generated in an external VFO circuit out of Read Data.
27	$\overline{RAWREAD}$	Raw Read	I	A raw read data signal transferred from the FDD.

Disk Write Operation Signal

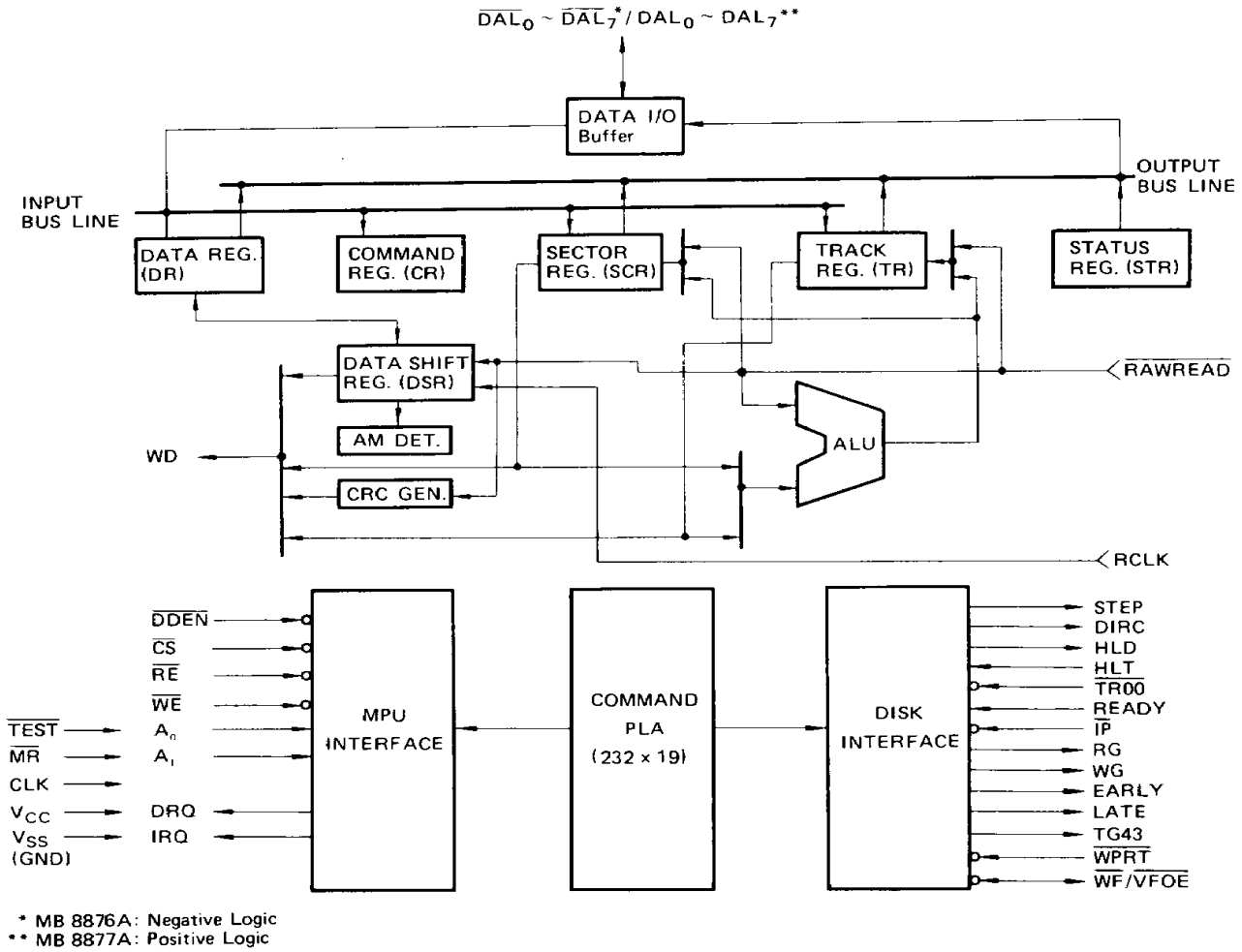
30	WG	Write Gate	O	Signal for indicating data is being written into a disk.
17	EARLY	Early Shift	O	Signal for indicating early pre-compensation of data write timing to a disk: EARLY = 1 shows a serial data to be transmitted via the WD pin to a disk must be shifted earlier.
18	LATE	Late Shift	O	Signal for indicating later pre-compensation of data write timing to a disk: LATE = 1 shows a serial data to be transmitted via the WD pin to a disk must be shifted later.
31	WD	Write Data	O	A write data signal transferred to the FDD.
29	TG43	Track Greater Than 43	O	Signal for indicating a head position of a disk: TG43 = 1 shows the head is located on any Track No. 44 thru 76. TG43 = 0 shows the head is located on any Track No. 0 thru 43.
33	$\overline{WF}/\overline{VFOE}$	Write Fault/Variable Frequency Oscillator Enable	I/O	Input signal for informing a fault is detected during write operation for a disk (during WG = 1). Output signal for informing the FDC is reading a disk (during WG = 0).
34	$\overline{WPRT}$	Write Protect	I	Signal for inhibiting write operation for disk.

REGISTER SELECTION

Chip Select	Address		Selected Register		Data Access Line Status
$\overline{CS}$	A_1	A_0	Read Mode ($\overline{RE}$ = 0)	Write Mode ($\overline{WE}$ = 0)	$\overline{DAL_7} \sim \overline{DAL_0}$ $\overline{DAL_7} \sim \overline{DAL_0}$
1	*	*	Deselected	Deselected	High Impedance
0	0	0	Status Register (STR)	Command Register (CR)	Enabled
0	0	1	Track Register (TR)	Track Register (TR)	Enabled
0	1	0	Sector Register (SCR)	Sector Register (SCR)	Enabled
0	1	1	Data Register (DR)	Data Register (DR)	Enabled

*: Don't care

MB8876A/MB8877A BLOCK DIAGRAM



* MB 8876A: Negative Logic
** MB 8877A: Positive Logic

FUNCTIONAL BLOCK DESCRIPTION

INTERNAL REGISTERS

- **Command Register (CR)**
  An 8-bit write-only register, holds the command which is being executed. This register should not be loaded when the BUSY flag is set (BUSY = 1) unless the execution of the current command is to be overridden, using the Force Interrupt command.
- **Status Register (STR)**
  An 8-bit read-only register, holds the device status information. The contents of STR are automatically updated according to the status of the executing Command. After the STR is read, the IRQ output is usually reset (IRQ = 0) except for the Type IV Command.
- **Data Register (DR)**
  An 8-bit read/write used as a holding register during Disk Read and Write operations. In Disk Read operations, the serial data assembled in the Data Shift Register is transferred to the DR, where it is made available to the data bus. In Disk Write operations, parallel data from the data bus is written into the DR where it is transferred to Data Shift Register. In a Seek Command, the data written into the DR holds the address of the desired Track address.
- **Data Shift Register (DSR)**
  An 8-bit shift register which cannot be accessed directly through the data bus. The DSR assembles serial data from the RAW READ input during Read operations and transfers the data to the DR. In Write operations, the DSR receives data from the DR and serially transfers it out through the WRITE DATA output.
- **Track Register (TR)**
  An 8-bit read/write register, holds the track number of the current disk head position for Restore, Seek, Step, Step-In and Step-Out Commands (i.e. TYPE 1 Commands), and is updated during the Command execution. The TR contents are compared with the track number (recorded in the disk's ID field) during Read, Write, and Verify operations. The TR should not be written to when the device is busy (BUSY = 1).
- **Sector Register (SCR)**
  An 8-bit read/write register, holds the address of the desired sector number. The sector number is written into the SCR prior to the Read and Write Data Command execution. It should not be written to during busy (BUSY = 1). Executing the Read Address Command causes the SCR to be loaded with the track number from the ID field.

OTHER FUNCTIONAL BLOCKS

- **Cycle Redundancy Check (CRC) Logic**
  This logic is used for checking or generating the 16-bit Cycle Redundancy Check that is in the ID and Data fields used for error detection. The polynominal is: $G(X) = X16 + X12 + X5 + 1$.
- **Arithmetic/Logic Unit (ALU)**
  The ALU is a serial comparator, incrementer, and decrementer used for register comparisons and modifications with the disk record ID fields.
- **Address Mark (AM) Detection Circuit**
  A circuit to detect specific bit pattern data in the serial data from a disk (i.e. Index Mark, ID Address Mark, Data Address Mark).
- **Data Modulator**
  A circuit to modulate data to be written onto a disk in the specific recording format: Single density recording format: Frequency Modulation (FM) Double density recording format: Modified Frequency Modulation (MFM)
- **Programmable Logic Array (PLA) for Commands**
  A micro-program to generate control signals (Commands) which control the FDC operation: The size of micro-program is approximately 232 x 19 bits.

BIT STRUCTURES OF COMMANDS

MB8876A/MB8877A

		BITS							
TYPE	**COMMAND**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Sector	1	0	0	m	S	E	C	0
II	Write Sector	1	0	1	m	S	E	C	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

NOTE: Bits shown in TRUE form.

TABLE 1. STEPPING RATES

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
$\overline{DDEN}$	0	1	0	1	X	X
R1 R0	$\overline{TEST}$ = 1	$\overline{TEST}$ = 1	$\overline{TEST}$ = 1	$\overline{TEST}$ = 1	$\overline{TEST}$ = 0	$\overline{TEST}$ = 0
0 0	3 ms	3 ms	6 ms	6 ms	184μs	368μs
0 1	6 ms	6 ms	12 ms	12 ms	190μs	380μs
1 0	10 ms	10 ms	20 ms	20 ms	198μs	396μs
1 1	15 ms	15 ms	30 ms	30 ms	208μs	416μs

TYPE I COMMANDS

h = Head Load Flag (Bit 3)
h = 1, Load head at beginning
h = 0, Unload head at beginning

V = Verify flag (Bit 2)
V = 1, Verify on destination track
V = 0, No verify

$r_1 r_0$ = Stepping motor rate (Bits 1-0)
Refer to Table 1 for rate summary

u = Update flag (Bit 4)
u = 1, Update Track register
u = 0, No update

TYPE II & III COMMANDS

m = Multiple Record flag (Bit 4)
m = 0, Single Record
m = 1, Multiple Records

a_0 f = Data Address Mark (Bit 0)
a_0 = 0, FB (Data Mark)
a_0 = 1, F8 (Deleted Data Mark)

E = 15 ms Delay (2MHz)
E = 1, 15 ms delay
E = 0, no 15 ms delay

S = Side Select Flag
S = 0, Compare for Side 0
S = 1, Compare for Side 1

C = Side Compare Flag
C = 0, diable side select compare
C = 1, enable side select compare

TYPE IV COMMAND

Ii = Interrupt Condition flags (Bits 3-0)
I0 = 1, Not-Ready to Ready Transition
I1 = 1, Ready to No-Ready Transition
I2 = 1, Index Pulse
I3 = 1, Immediate Interrupt
$I_3 - I_0$ = 0, Terminate with no Interrupt

STATUS REGISTER SUMMARY

Command	Status Bit							
	7	6	5	4	3	2	1	0
All Type I	Not Ready	Write Protect	Head Loaded	Seek Error	CRC Error	Track 0	Index	Busy
Read Sector	Not Ready	0	Record Type	Rec not Found	CRC Error	Lost Data	DRQ	Busy
Write Sector	Not Ready	Write Protect	Write Fault	Rec not Found	CRC Error	Lost Data	DRQ	Busy
Read Address	Not Ready	0	0	Rec not Found	CRC Error	Lost Data	DRQ	Busy
Read Track	Not Ready	0	0	0	0	Lost Data	DRQ	Busy
Write Track	Not Ready	Write Protect	Write Fault	0	0	Lost Data	DRQ	Busy

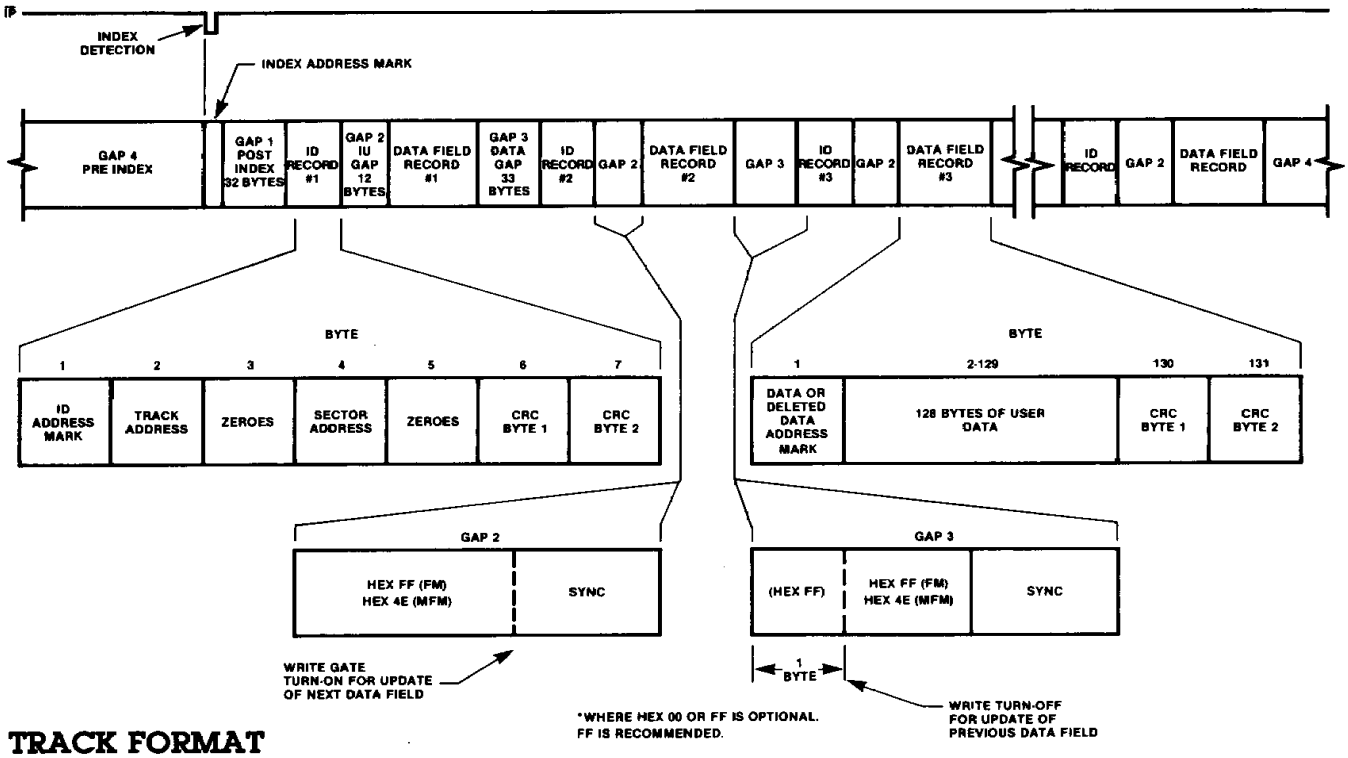
STATUS DESCRIPTION FOR TYPE I COMMANDS

Bit	Name	Meaning
S7	Not Ready	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6	Protected	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{WRPT}$ input.
S5	Head Loaded	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4	Seek Error	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3	CRC Error	CRC encountered in ID filed.
S2	Track 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{TR00}$ input.
S1	Index	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{IP}$ input.
S0	Busy	When set command is in progress. When reset no command is in progress.

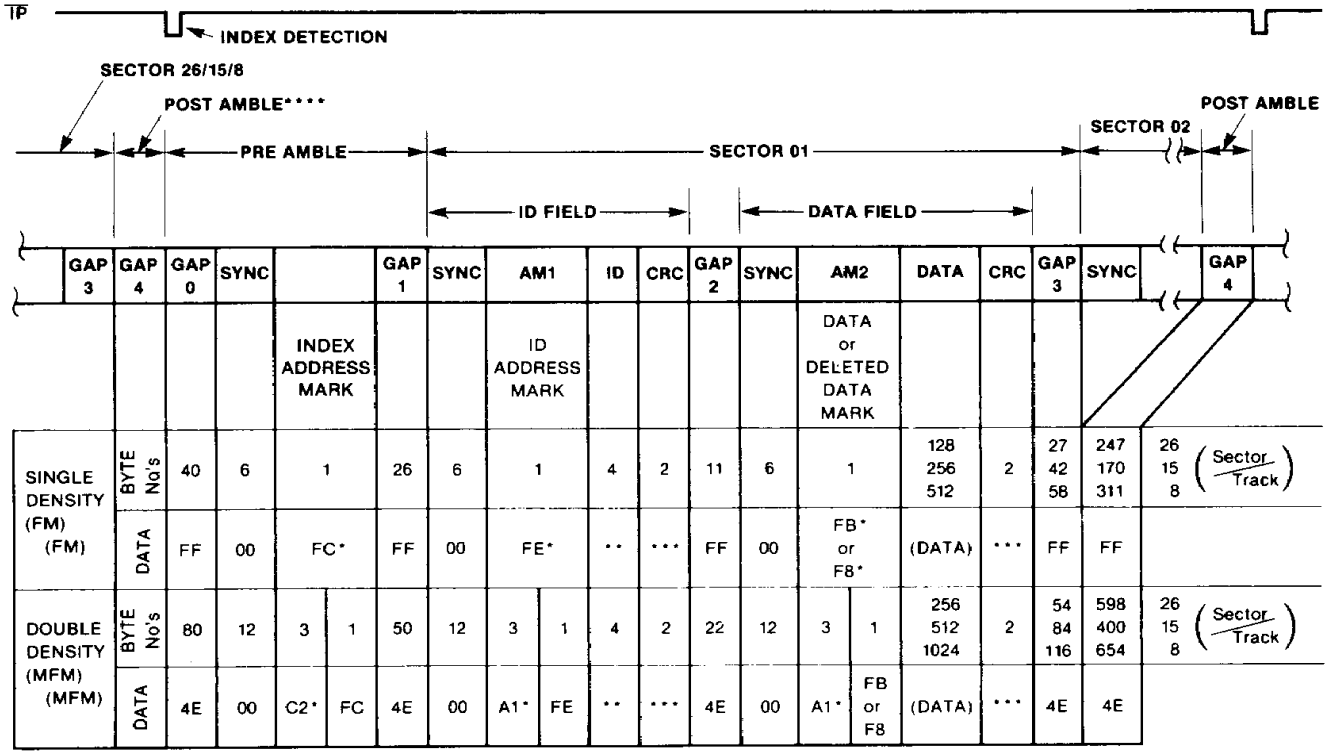
STATUS DESCRIPTION FOR TYPE II AND III COMMANDS

Bit	Name	Meaning
S7	Not Ready	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6	Write Protect	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5	Record Type/ Write Fault	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4	Record Not Found (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3	CRC Error	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2	Lost Data	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1	Data Request	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0	Busy	When set, command is under execution. When reset, no command is under execution.

TRACK FORMAT



TRACK FORMAT



		GAP 3	GAP 4	GAP 0	SYNC		GAP 1	SYNC	AM1		ID	CRC	GAP 2	SYNC	AM2		DATA	CRC	GAP 3	SYNC		GAP 4	
						INDEX ADDRESS MARK			ID ADDRESS MARK						DATA or DELETED DATA MARK								
SINGLE DENSITY (FM) (FM)	BYTE No's	40	6	1		26	6	1		4	2	11	6	1		128 256 512	2	27 42 58	247 170 311	26 15 8	(Sector / Track)	
	DATA	FF	00	FC*		FF	00	FE*		**	***	FF	00	FB* or F8*		(DATA)	***	FF	FF			
DOUBLE DENSITY (MFM) (MFM)	BYTE No's	80	12	3	1	50	12	3	1	4	2	22	12	3	1	256 512 1024	2	54 84 116	598 400 654	26 15 8	(Sector / Track)	
	DATA	4E	00	C2*	FC	4E	00	A1*	FE	**	***	4E	00	A1*	FB or F8	(DATA)	***	4E	4E			

NOTE: *: Shows to have missing clock.
**: Shows the ID field
***: Shows the cyclic Redundancy check polynomial $G(X) = X^0 + X^5 + X^{12} + X^{16}$
****: See the most right column for its byte numbers and data.

SECTOR FORMAT

SECTOR														
ID FIELD									DATA FIELD					
SYC	ID AM	TRACK NUMBER	SIDE NUMBER	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP 2	SYNC	DATA AM	DATA	CRC 1	CRC 2	GAP 3
6 bytes	1 byte	1 byte	1 byte	1 byte	1 byte	1 byte	1 byte	11 bytes	6 bytes	1 byte	*	1 byte	1 byte	27/42/58 bytes
12 bytes	4 bytes	1 byte	1 byte	1 byte	1 byte	1 byte	1 byte	22 bytes	12 bytes	4 byte	*	1 byte	1 byte	54/84/116 bytes

(FM) or (MFM)

(00)H** for 128 Bytes/Sector data
(01)H for 256 Bytes/Sector data
(02)H 412 Bytes/Sector data
(03)H for 1024 Bytes/Sector data

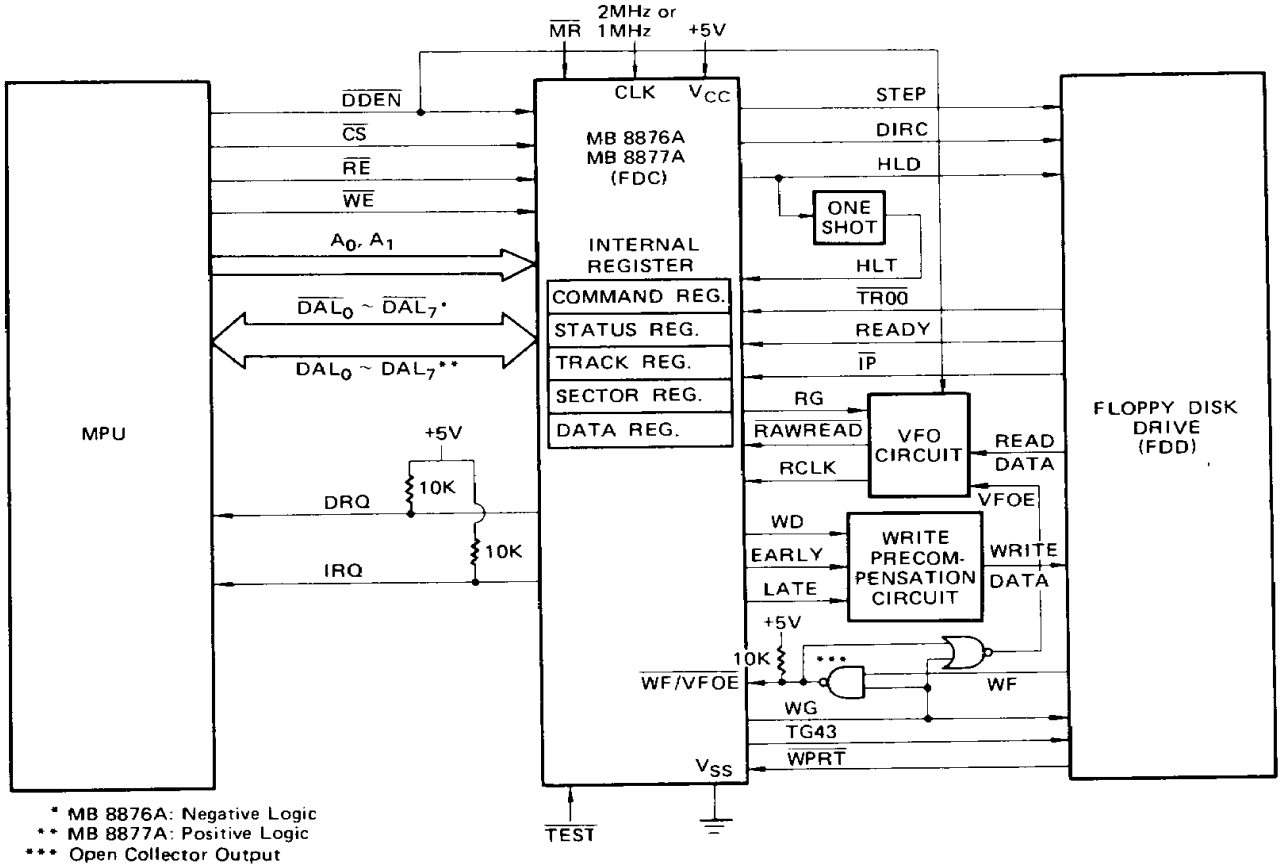
(01)H to (1A)H for 26 Sector/Track format
(01)H to (0F)H for 15 Sector/Track format
(01)H to (08)H for 8 Sector/Track format

(00)H for Side 0 of single-side of double-side disk
(01)H for Side 1 of double-side disk

(00)H to (4A)H for Track 0 thru Track 74***

NOTE *: Byte number of this column is defined in the SECTOR LENGTH column.
**: "H" after parentheses show that the parenthesized figures are hexa-decimal.
***: Track 75 and 76 are usually used for correction.

MB8876A/MB8877A TYPICAL SYSTEM CONSTRUCTION



* MB 8876A: Negative Logic
** MB 8877A: Positive Logic
*** Open Collector Output

4

IBM 3740 Format

This single-density (FM) format utilizes 128 bytes/sector. The bytes to be generated by the system MPU for use in the execution of the Write Track command are shown below.

	Data Byte (hex)	No. of Bytes	Comments
	FF	40	Gap 5 (Post Index)
	00	6	
	FC	1	Index AM
	FF	26	Gap 1
	00	6	
	FE	1	ID AM
	XX	1	Track Number (00-4A)
	0X	1	Side Number (00 or 01)
	XX	1	Sector Number (01-1A)
ONE SECTOR ①	00	1	Sector Length (128 bytes)
	F7	1	Causes 2-Byte CRC to be Written
	FF	11	Gap 2 (ID Gap)
	00	6	
	FB	1	Data AM
	E5	128	Data Field
	F7	1	Causes 2-Byte CRC to be Written
	FF	27	Part of Gap 3 (Data Gap)
	FF	247 ②	Gap 4 (Pre-Index)

Notes: 1. This pattern must be written 26 times per track.
2. Continue writing Hex FF until FDC completes sequence and generates INTRQ interrupt.

IBM System 34 Format

This double-density (MFM) format utilizes 256 bytes/sector. The bytes to be generated by the system MPU for use in the execution of the Write Track command are shown below.

	Data Byte (hex)	No. of Bytes	Comments
	4E	80	Gap 5 (Post Index)
	00	12	
	F6	3	Writes C2
	FC	1	Index AM
	4E	50	
	00	12	Gap 1
	F5	3	Writes ID AM Sync Bytes
	FE	1	ID AM
	XX	1	Track Number (00-4C)
	0X	1	Side Number (00 or 01)
	XX	1	Sector Number (01-1A)
	01	1	Sector Length (256 Bytes)
ONE SECTOR ①	F7	1	Causes 2-Byte CRC to be Written
	4E	22	Gap 2 (ID Gap)
	00	12	
	F5	3	Writes ID AM Sync Bytes
	FB	1	Data AM
	40	256	Data Field
	F7	1	Causes 2-Byte CRC to be Written
	4E	54	Part of Gap 3 (Data Gap)
	4E	598 ②	Gap 4 (Pre Index)

Notes: 1. This pattern must be written 26 times per track.
2. Continue writing Hex 4E until FDC completes sequence and generates INTRQ interrupt.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on any pin	V_{CC}, V_{IN}, V_{OUT}	V_{SS} −0.3 to V_{SS} +7.0	V
Operating Temperature	T_A	0 to 70	°C
Storage Temperature	T_{stg}	−55 to +150	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Operating Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.75	5.00	5.25	V	0°C to +70°C
	V_{SS}	—	0	—		
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	0.8	V	

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Output High Voltage (I_{OH} = −200μA)	V_{OH}	2.4	—	—	V
Output Low Voltage (I_{OL} = 1.8mA)	V_{OL}	—	—	0.4	V
Three-State (Off-State) Input Current (V_{IN} = 0.4V to 2.4)	I_{TSI}	—	—	10	μA
Input Leakage Current (See Note 1)	I_{IN1}	—	—	2.5	μA
Input Leakage Current (See Note 2)	I_{IN2}	—	—	100	μA
Output Leakage Current for Off-State (V_{OH} = 2.4V)	I_{LOH}	—	—	10	μA
Power Consumption	P_D	—	—	350	mW

Note1) Except for HLT, $\overline{TEST}$, $\overline{WF}$, $\overline{WPRT}$, and $\overline{DDEN}$. (V_{IN} = 0 to 5.25V)
2) For HLT, $\overline{TEST}$, $\overline{WF}$, $\overline{WPRT}$, and $\overline{DDEN}$. (V_{IN} = 0 to 5.25V)

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AC CHARACTERISTICS

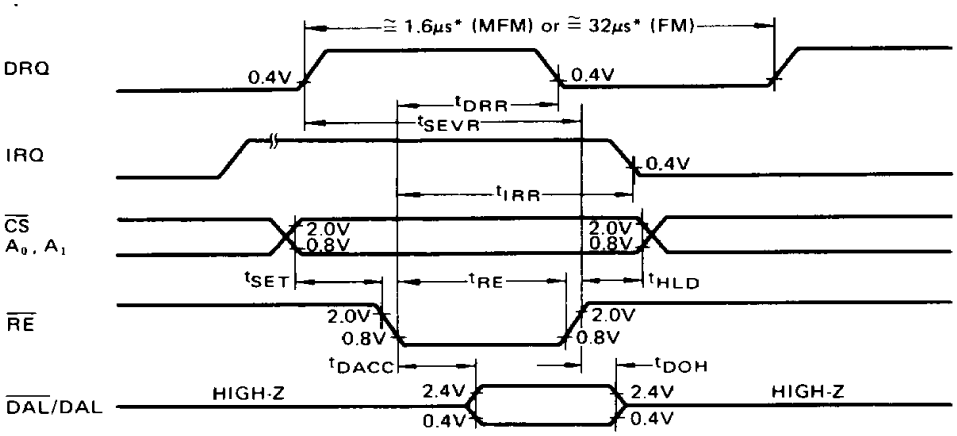
(Recommended Operating Conditions unless otherwise noted.)

MPU Read Timing (From FDC)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Address Setup Time	t_{SET}	50	—	—	ns
Address Hold Time	t_{HLD}	10	—	—	ns
$\overline{RE}$ Pulse Width	t_{RE}	280	—	—	ns
DRQ Reset Time	t_{DRR}	—	—	250	ns
IRQ Reset Time	t_{IRR}	—	—	500	ns
Data Delay Time (C_L = 25pF)	t_{DACC}	—	—	250	ns
Data Hold Time (C_L = 25pF)	t_{DOH}	50	—	150	ns
DRQ Service Time (RCLK Cycle = 2μs)	t_{SEVR}	—	—	13.5*	μs

*: These values are doubled when CLK = 1MHz.

READ TIMING

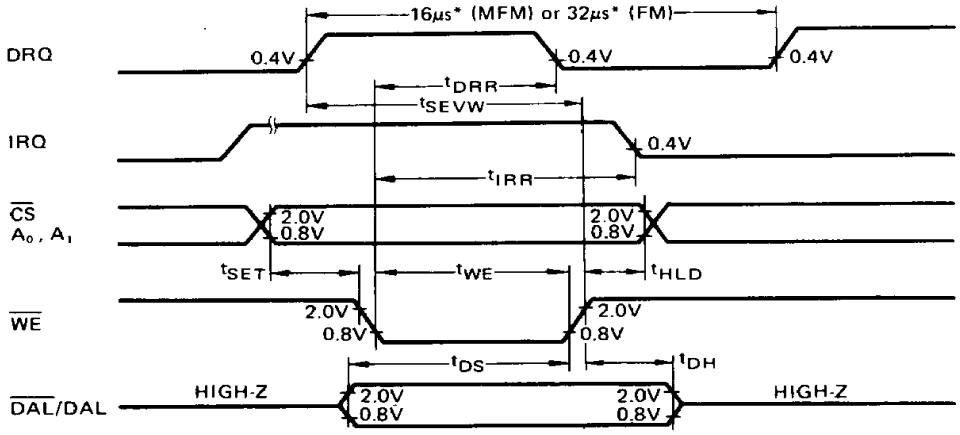


MPU Write Timing (To FDC)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Address Setup Time	t_{SET}	50	—	—	ns
Address Hold Time	t_{HLD}	10	—	—	ns
$\overline{WE}$ Pulse Width	t_{WE}	200	—	—	ns
DRQ Reset Time	t_{DRR}	—	—	250	ns
INTRQ Reset Time	t_{IRR}	—	—	500	ns
Data Setup Time	t_{DS}	250	—	—	ns
Data Hold Time	t_{DH}	0	—	—	ns
DRQ Service Time ($\overline{DDEN}$ = "L")	t_{SEVW}	—	—	11.5*	μs

*: These values are doubled when CLK = 1MHz.

WRITE TIMING



*: These values are doubled when CLK = 1MHz.

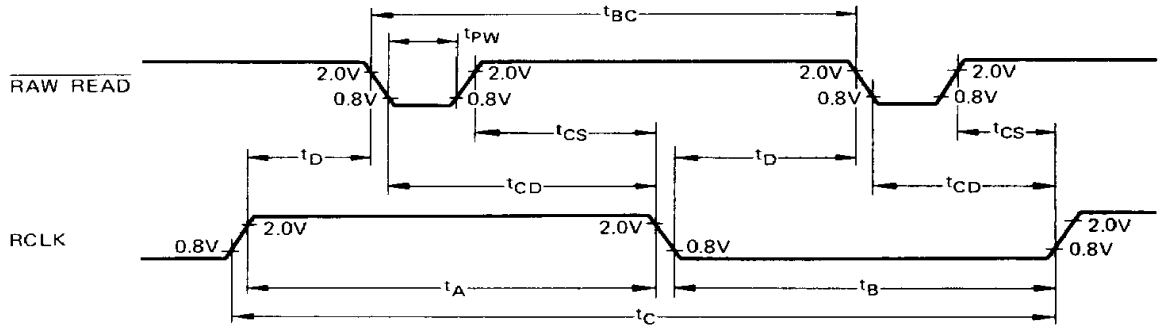
4

FDC Read Data Timing (From Disk)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
$\overline{\text{RAWREAD}}$ Pulse Width		t_{PW}	100	—	250*	ns
Clock Setup Time		t_D	40	—	—	ns
Clock Hold Time for MFM		t_{CD}	40	—	—	ns
Clock Hold Time for FM		t_{CS}	40	—	—	ns
$\overline{\text{RAWREAD}}$ Cycle Time	MFM	t_{BC}	—	2*, 3* or 4*	—	μs
	FM		—	2* or 4*	—	μs
RCLK High Pulse Width	MFM	t_A	0.8	1*	20	μs
	FM		0.8	2*	20	μs
RCLK Low Pulse Width	MFM	t_B	0.8	1*	20	μs
	FM		0.8	2*	20	μs
RCLK Cycle Time	MFM	t_C	—	2*	—	μs
	FM		—	4*	—	μs

*: These values are double when CLK = 1MHz.

READ DATA TIMING



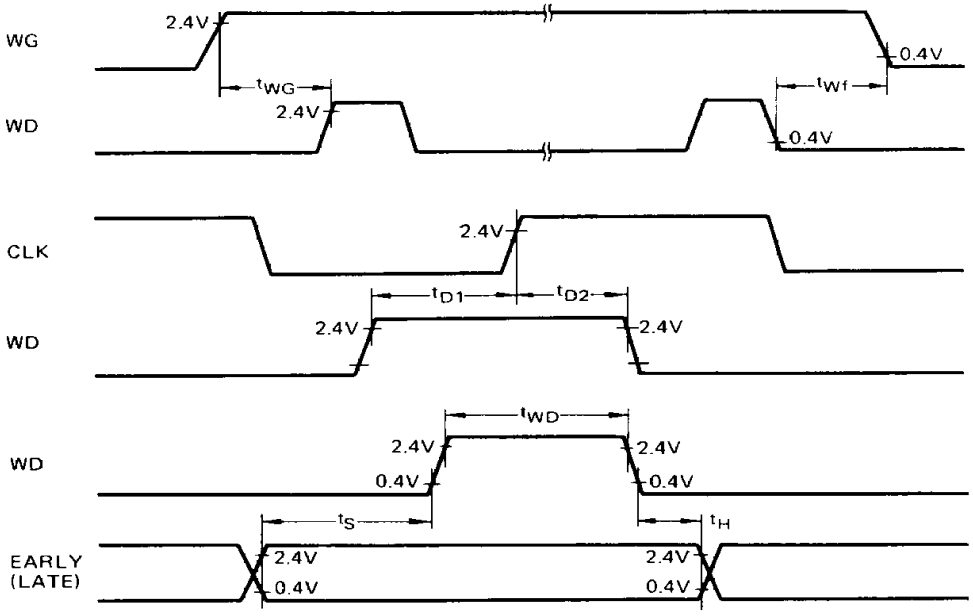
FDC Write Data Timing (To Disk)

Parameter	Symbol	Conditions		Value Min	Value Typ	Value Max	Unit
Write Data Pulse Width	t_{WD}**	CLK = 2 MHz	FM	450	500	550	ns
			MFM	150	200	250	
Write Gate To Write Data	t_{WG}**	CLK = 2 MHz	FM	—	2	—	μs
			MFM	—	1	—	
Write Gate off from WD	t_{WF}**	CLK = 2 MHz	FM	—	2	—	μs
			MFM	1	—	2	
Early (Late) to Write Data	t_S	CLK = 2 MHz	MFM	125	—	—	ns
Early (Late) from Write Data	t_H	CLK = 2 MHz	MFM	−50*	—	—	ns
WD Valid to CLK	t_{D1}	CLK = 1 MHz	MFM	200	—	—	ns
		CLK = 2 MHz	MFM	30	—	—	
WD Valid after CLK	t_{D2}	CLK = 1 MHz	MFM	50	—	—	ns
		CLK = 2 MHz	MFM	50	—	—	

*: This value, −50ns (min) indicated that Early (Late) signal changes 50ns (min) before WD falls down in worst case. See DISK DATA OUTPUT TIMING.

**: All times are doubled when CLK = 1 MHz.

WRITE DATA TIMING

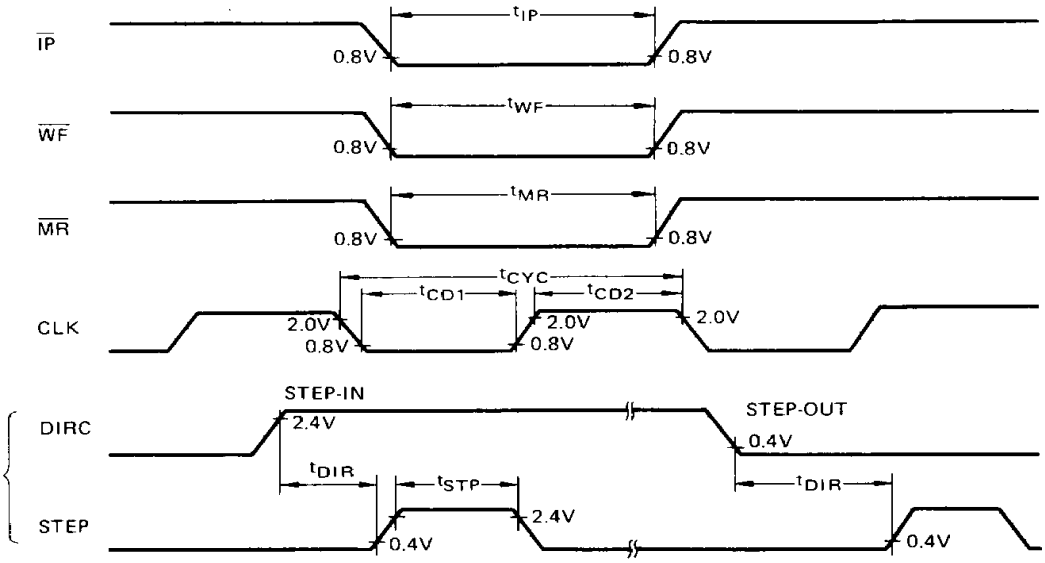


OTHER TIMINGS

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
CLK Low Pulse Width		t_{CD1}	230	—	20000	ns
CLK High Pulse Width		t_{CD2}	200	—	20000	ns
STEP Pulse Width	MFM	t_{STP}	2*	—	—	μs
	FM		4*	—	—	μs
DIRC Setup Time		t_{DIR}	12*	—	—	μs
$\overline{MR}$ Pulse Width**		t_{MR}	50*	—	—	μs
$\overline{IP}$ Pulse Width		t_{IP}	10*	—	—	μs
$\overline{WF}$ Pulse Width		t_{WF}	10*	—	—	μs
CLK Cycle Time		t_{CYC}	—	0.5*	—	μs

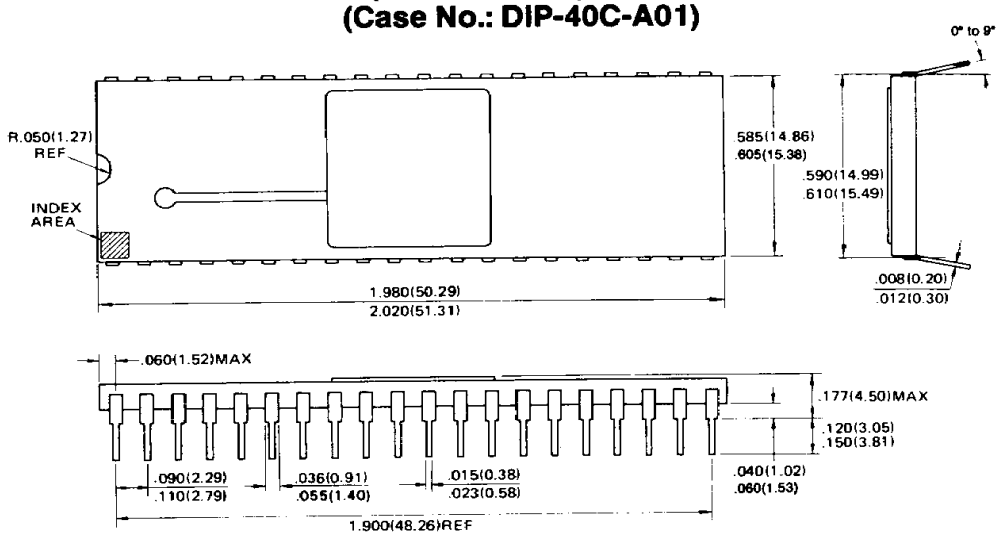
*: These Values are doubled when CLK = 1MHz.
**: During Master Reset, CLK of more than 10 cycles are required.

OTHER TIMINGS

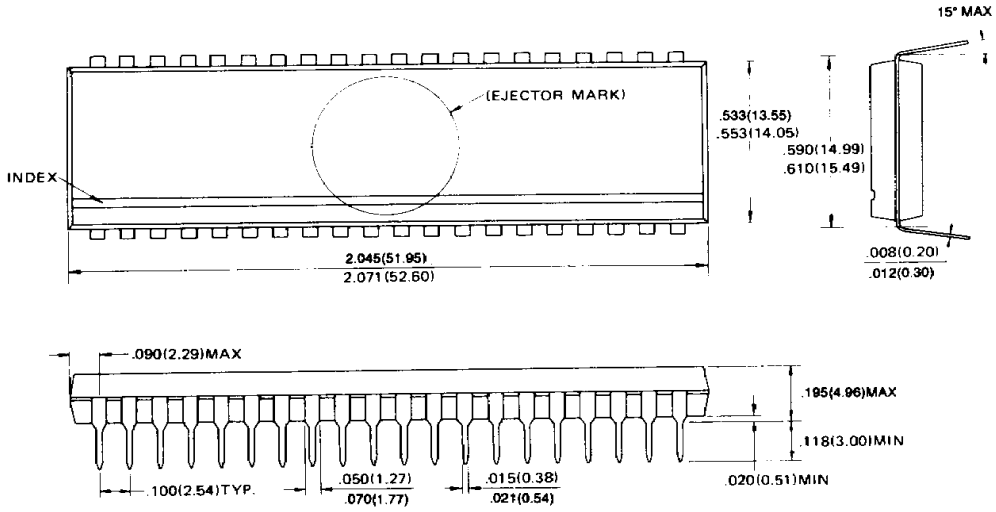


PACKAGE DIMENSIONS Dimensions in inches (millimeters)

40-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(Case No.: DIP-40C-A01)



40-LEAD PLASTIC DUAL IN-LINE PACKAGE
(Case No.: DIP-40P-M01)



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