

DESCRIPTION

The M5M5V108DFP,VP,KV are a 1048576-bit CMOS static RAM organized as 131072 word by 8-bit which are fabricated using high-performance triple-polysilicon and double metal CMOS technology. The use of thin film transistor (TFT) load cells and CMOS periphery result in a high density and low power static RAM.

They are low standby current and low operation current and ideal for the battery back-up application.

The M5M5V108DVP,KV are packaged in a 32-pin thin small outline package which is a high reliability and high density surface mount device(SMD).

FEATURES

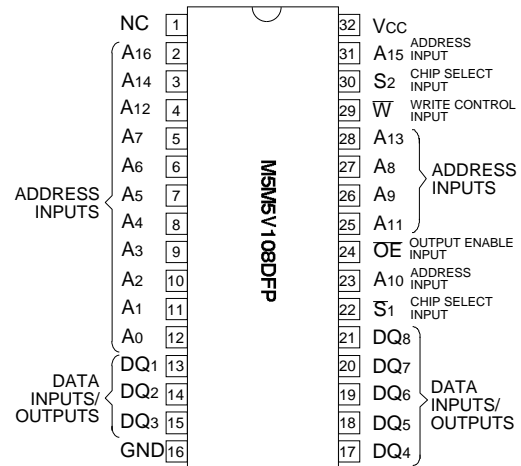
Type name	Access time (max)	Vcc	Power supply current	
			Active (1MHz) (max)	stand-by (max)
M5M5V108DFP,VP,KV-70H	70ns	2.7~3.6V	5mA	12μA

- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by \overline{S}_1, S_2
- Data hold on +2V power supply
- Three-state outputs : OR - tie capability
- \overline{OE} prevents data contention in the I/O bus
- Common data I/O
- Package

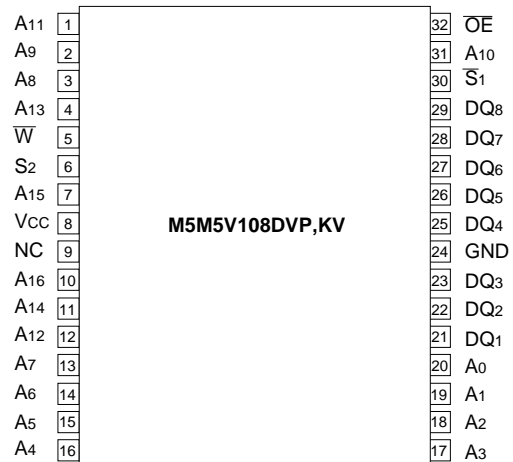
M5M5V108DFP 32pin 525mil SOP
M5M5V108DVP,RV 32pin 8 X 20 mm² TSOP
M5M5V108DKV,KR 32pin 8 X 13.4 mm² TSOP

APPLICATION

Small capacity memory units

PIN CONFIGURATION (TOP VIEW)

Outline 32P2M-A



Outline 32P3H-E(VP), 32P3K-B(KV)

NC : NO CONNECTION

FUNCTION

The operation mode of the M5M5V108D series are determined by a combination of the device control inputs $\overline{S}_1, S_2, \overline{W}$ and \overline{OE} .

Each mode is summarized in the function table.

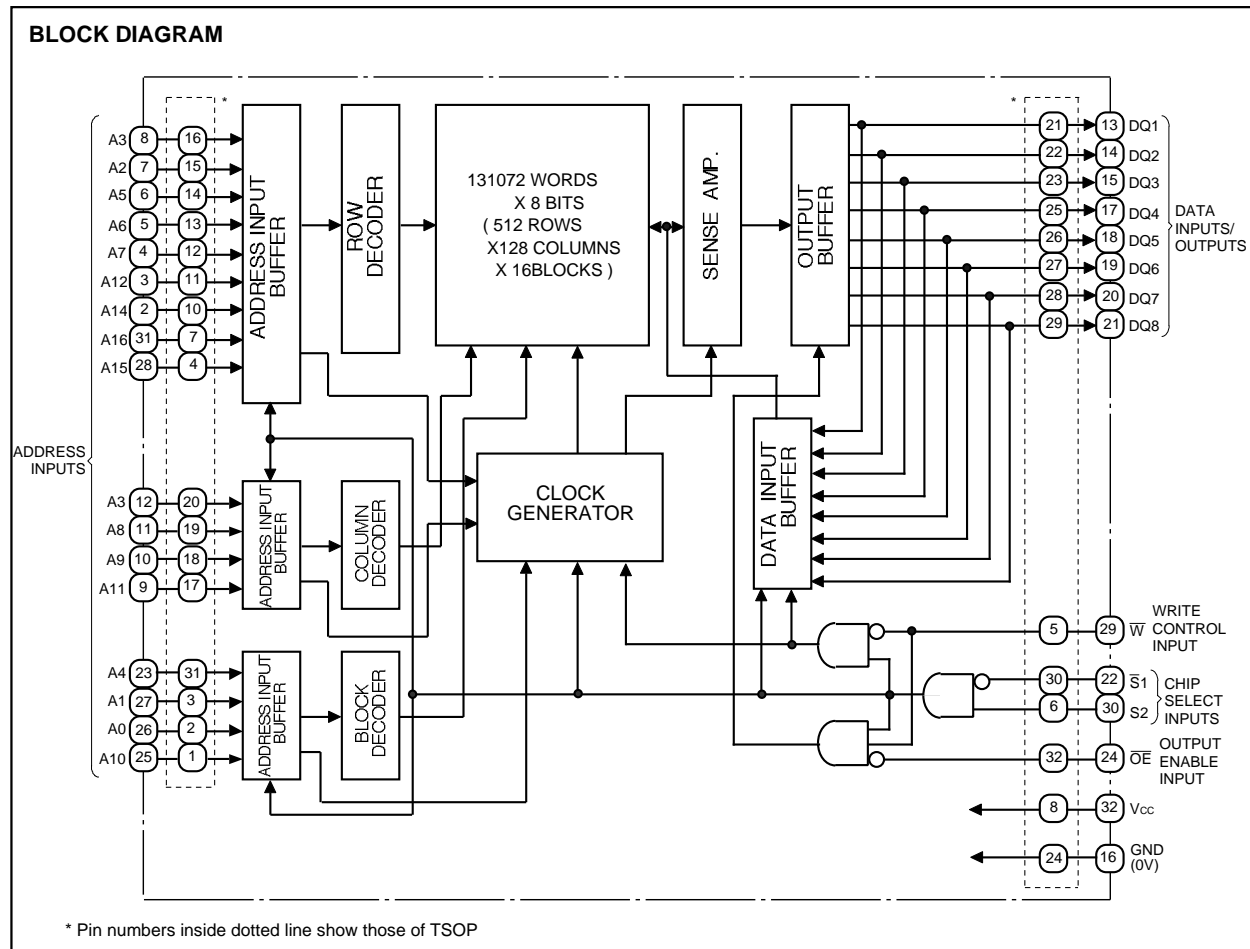
A write cycle is executed whenever the low level \overline{W} overlaps with the low level \overline{S}_1 and the high level S_2 . The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}, \overline{S}_1$ or S_2 , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input \overline{OE} directly controls the output stage. Setting the \overline{OE} at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting \overline{W} at a high level and \overline{OE} at a low level while \overline{S}_1 and S_2 are in an active state ($\overline{S}_1=L, S_2=H$).

FUNCTION TABLE

\overline{S}_1	S_2	\overline{W}	\overline{OE}	Mode	DQ	Icc
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

When setting \overline{S}_1 at a high level or S_2 at a low level, the chip are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by \overline{S}_1 and S_2 . The power supply current is reduced as low as the stand-by current which is specified as Icc3 or Icc4, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.



7th.July.2000 Ver. 1.0
MITSUBISHI LSIs
M5M5V108DFP,VP,KV -70H
1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to GND	- 0.3*~4.6	V
V _I	Input voltage		- 0.3*~V _{CC} + 0.3 (Max 4.6)	V
V _O	Output voltage		0~V _{CC}	V
P _d	Power dissipation	T _a =25°C	700	mW
T _{opr}	Operating temperature		0~70	°C
T _{stg}	Storage temperature		- 65~150	°C

* -3.0V in case of AC (Pulse width 30ns)

DC ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=2.7~3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{IH}	High-level input voltage		2.0		V _{CC} + 0.3	V
V _{IL}	Low-level input voltage		-0.3*		0.6	V
V _{OH1}	High-level output voltage 1	I _{OH} = - 0.5mA	2.4			V
V _{OH2}	High-level output voltage 2	I _{OH} = - 0.05mA	V _{CC} - 0.5			V
V _{OL}	Low-level output voltage	I _{OL} = 2mA			0.4	V
I _I	Input current	V _I =0~V _{CC}			±1	µA
I _O	Output current in off-state	\bar{S}_1 =V _{IH} or S ₂ =V _{IL} or $\bar{O}E$ =V _{IH} V _{I/O} =0~V _{CC}			±1	µA
I _{CC1}	Active supply current	\bar{S}_1 =V _{IL} , S ₂ =V _{IH} , other inputs=V _{IH} or V _{IL} Output-open(duty 100%)	70ns		35	
I _{CC2}	Active supply current		1MHz		5	
I _{CC3}	Stand-by current	1) S ₂ 0.2V other inputs=0~V _{CC} 2) \bar{S}_1 V _{CC} -0.2V, S ₂ V _{CC} -0.2V other inputs=0~V _{CC}	-H	~25°C	1.2	µA
				~40°C	3.6	
				~70°C	12	
I _{CC4}	Stand-by current	\bar{S}_1 =V _{IH} or S ₂ =V _{IL} , other inputs=0~V _{CC}			0.33	mA

* -3.0V in case of AC (Pulse width 30ns)

CAPACITANCE (T_a=0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _I	Input capacitance	V _I =GND, V _I =25mVrms, f=1MHz			8	pF
C _O	Output capacitance	V _O =GND, V _O =25mVrms, f=1MHz			10	pF

Note 1: Direction for current flowing into an IC is positive (no mark).

2: Typical value is V_{CC} = 3V, T_a = 25°C

AC ELECTRICAL CHARACTERISTICS ($T_a=0\sim 70^\circ\text{C}$, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

V_{CC} 2.7~3.6V
 Input pulse level V_{IH}=2.2V, V_{IL}=0.4V
 Input rise and fall time 5ns
 Reference level V_{OH}=V_{OL}=1.5V
 Output loads Fig.1, C_L=30pF

C_L=5pF (for t_{en}, t_{dis})

Transition is measured ± 500mV from steady state voltage. (for t_{en}, t_{dis})

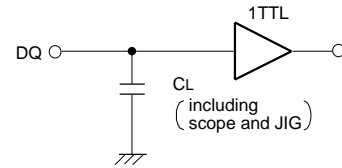


Fig.1 Output load

(2) READ CYCLE

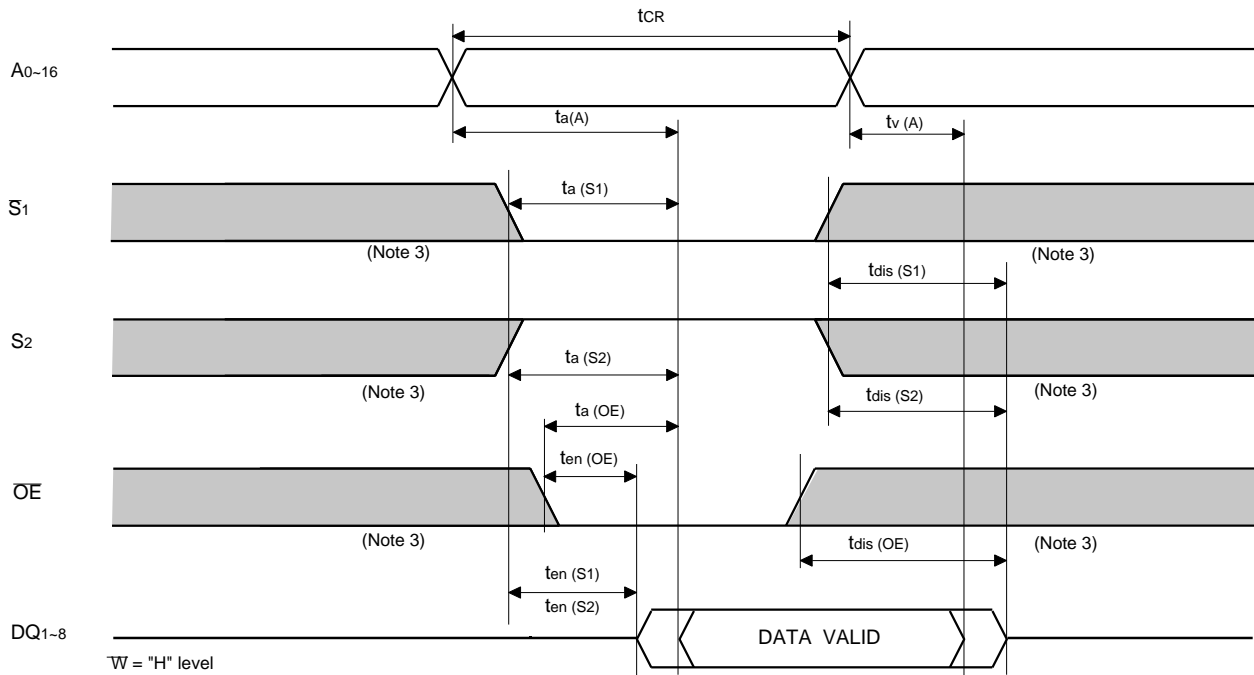
Symbol	Parameter	Limits		Unit
		-70H		
		Min	Max	
t _{CR}	Read cycle time	70		ns
t _{a(A)}	Address access time		70	ns
t _{a(S1)}	Chip select 1 access time		70	ns
t _{a(S2)}	Chip select 2 access time		70	ns
t _{a(OE)}	Output enable access time		35	ns
t _{dis(S1)}	Output disable time after \overline{S}_1 high		25	ns
t _{dis(S2)}	Output disable time after S ₂ low		25	ns
t _{dis(OE)}	Output disable time after OE high		25	ns
t _{en(S1)}	Output enable time after \overline{S}_1 low	10		ns
t _{en(S2)}	Output enable time after S ₂ high	10		ns
t _{en(OE)}	Output enable time after OE low	5		ns
t _{V(A)}	Data valid time after address	10		ns

(3) WRITE CYCLE

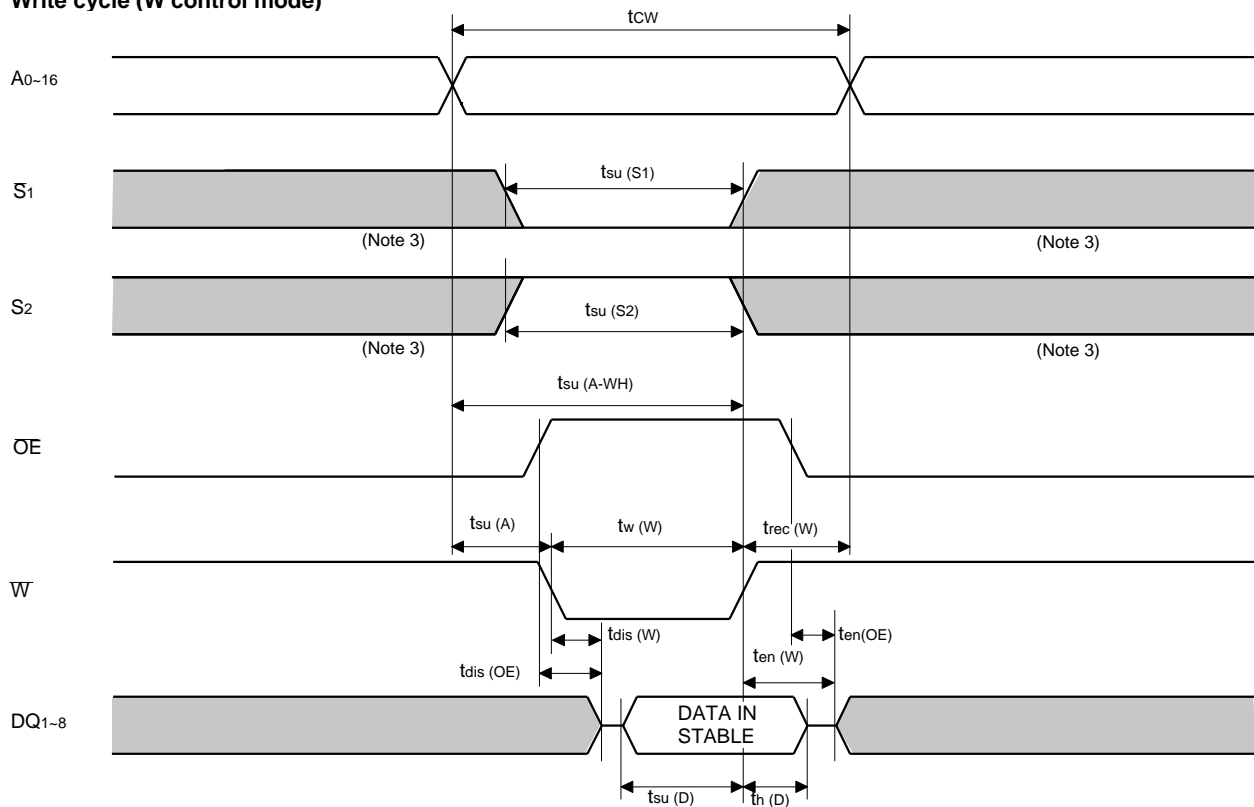
Symbol	Parameter	Limits		Unit
		-70H		
		Min	Max	
t _{CW}	Write cycle time	70		ns
t _{w(W)}	Write pulse width	55		ns
t _{su(A)}	Address setup time	0		ns
t _{su(A-WH)}	Address setup time with respect to \overline{W}	65		ns
t _{su(S1)}	Chip select 1 setup time	65		ns
t _{su(S2)}	Chip select 2 setup time	65		ns
t _{su(D)}	Data setup time	30		ns
t _{h(D)}	Data hold time	0		ns
t _{rec(W)}	Write recovery time	0		ns
t _{dis(W)}	Output disable time from \overline{W} low		25	ns
t _{dis(OE)}	Output disable time from OE high		25	ns
t _{en(W)}	Output enable time from \overline{W} high	5		ns
t _{en(OE)}	Output enable time from OE low	5		ns

(4) TIMING DIAGRAMS

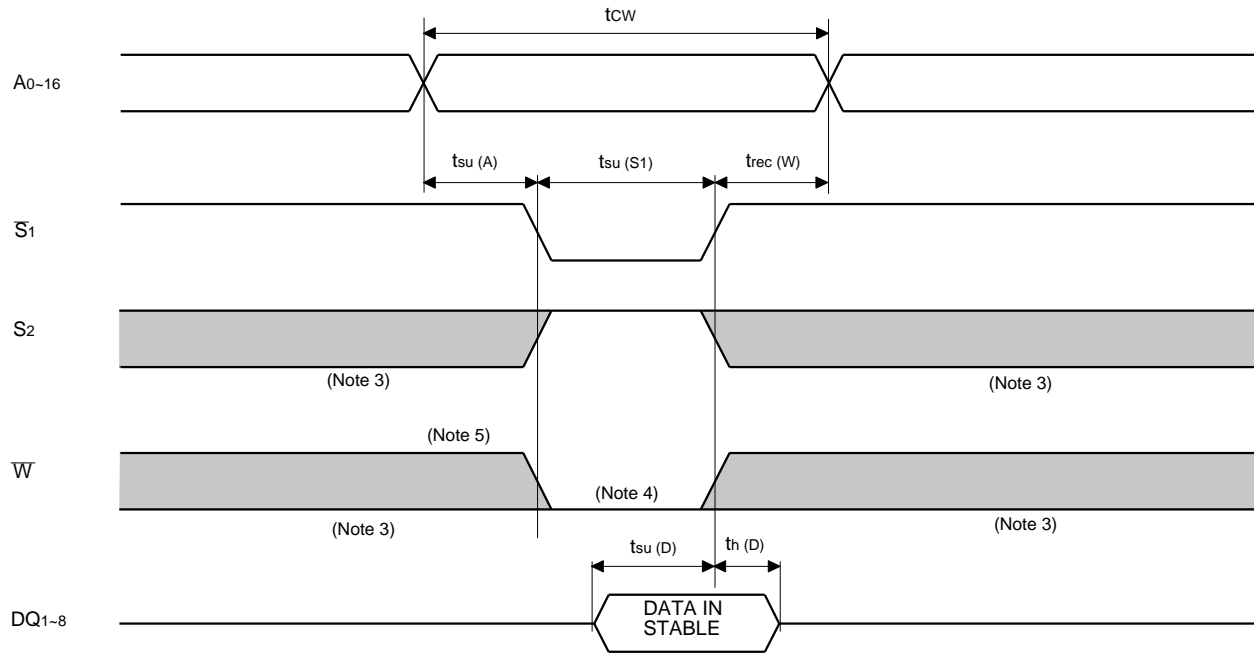
Read cycle



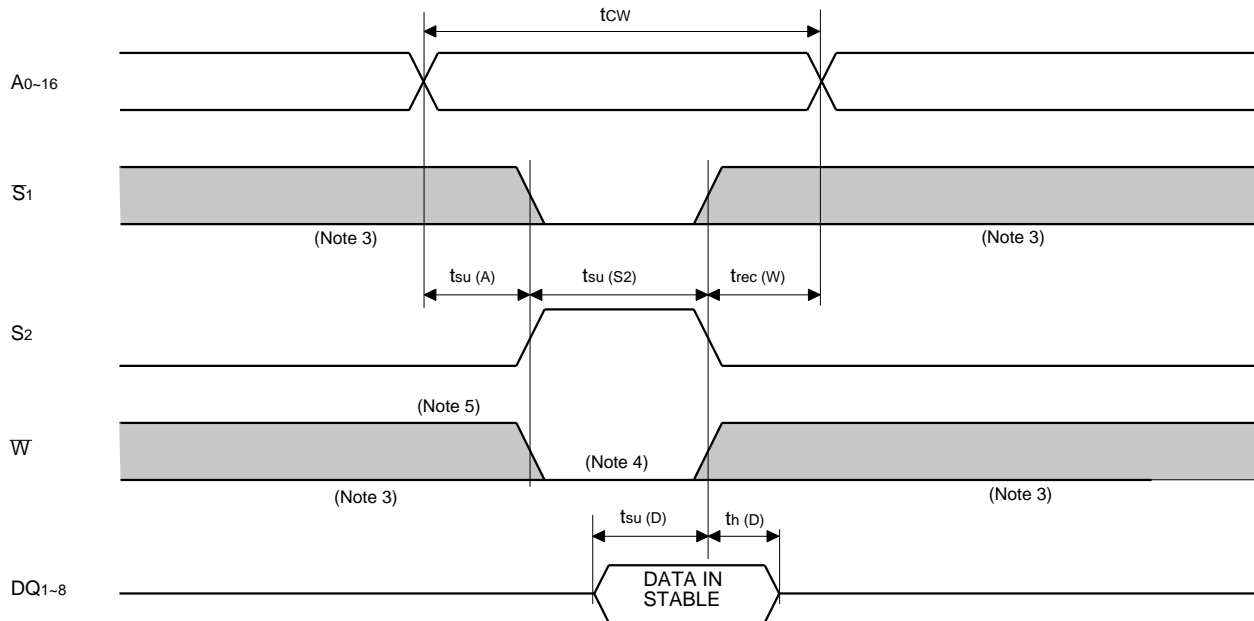
Write cycle (\bar{W} control mode)



Write cycle ($\overline{S1}$ control mode)



Write cycle (S2 control mode)



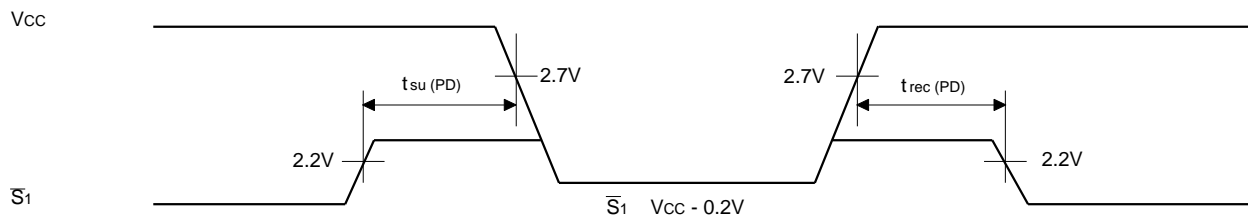
- Note 3: Hatching indicates the state is "don't care".
 4: Writing is executed while S2 high overlaps $\overline{S1}$ and W low.
 5: When the falling edge of W is simultaneously or prior to the falling edge of $\overline{S1}$ or rising edge of S2, the outputs are maintained in the high impedance state.
 6: Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS**(1) ELECTRICAL CHARACTERISTICS** (Ta=0~70°C, unless otherwise noted)

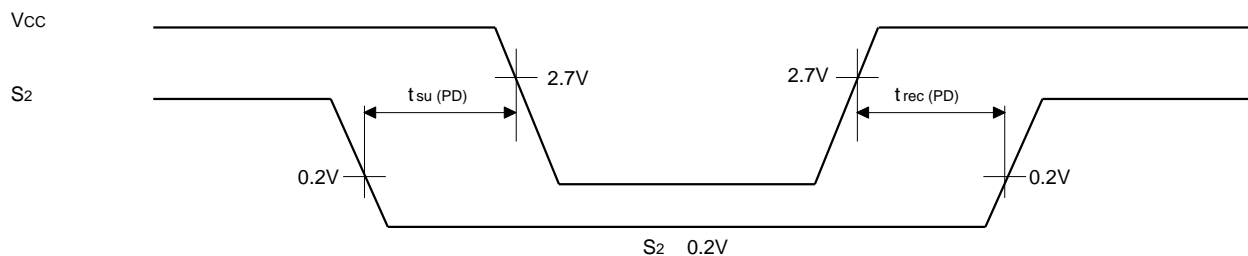
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{CC} (PD)	Power down supply voltage		2			V
V _I (S ₁)	Chip select input S ₁		2.0	V _{CC} (PD)		V
V _I (S ₂)	Chip select input S ₂	2.7V V _{CC} (PD)			0.6	V
		V _{CC} (PD)<2.7V			0.2	V
I _{CC} (PD)	Power down supply current	V _{CC} = 3V 1) S ₂ 0.2V, other inputs = 0~3V 2) S ₁ V _{CC} -0.2V, S ₂ V _{CC} -0.2V other inputs = 0~3V	-H	~25°C	1	μA
				~40°C	3	
				~70°C	10	

(2) TIMING REQUIREMENTS (Ta=0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t _{su} (PD)	Power down set up time		0			ns
t _{rec} (PD)	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS**S₁ control mode**

Note 7: On the power down mode by controlling $\overline{S_1}$, the input level of S₂ must be S₂ V_{CC} - 0.2V or S₂ 0.2V. The other pins(Address,I/O,WE,OE) can be in high impedance state.

S₂ control mode

Keep safety first in your circuit designs!

Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

These materials are intended as a reference to assist our customers in the selection of the Mitsubishi semiconductor product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Mitsubishi Electric Corporation or a third party.

Mitsubishi Electric Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.

All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Mitsubishi Electric Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor for the latest product information before purchasing a product listed herein.

The information described here may contain technical inaccuracies or typographical errors. Mitsubishi Electric Corporation assumes no responsibility for any damage, liability, or other loss arising from these inaccuracies or errors.

Please also pay attention to information published by Mitsubishi Electric Corporation by various means, including the Mitsubishi Semiconductor home page (<http://www.mitsubishichips.com>).

When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Mitsubishi Electric Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.

Mitsubishi Electric Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.

The prior written approval of Mitsubishi Electric Corporation is necessary to reprint or reproduce in whole or in part these materials.

If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination. Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.

Please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor for further details on these materials or the products contained therein.

