NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT
μPC4572

LOW SUPPLY VOLTAGE, ULTRA LOW-NOISE, HIGH SPEED, WIDE BAND, LOW I_B DUAL OPERATIONAL AMPLIFIER

DESCRIPTION

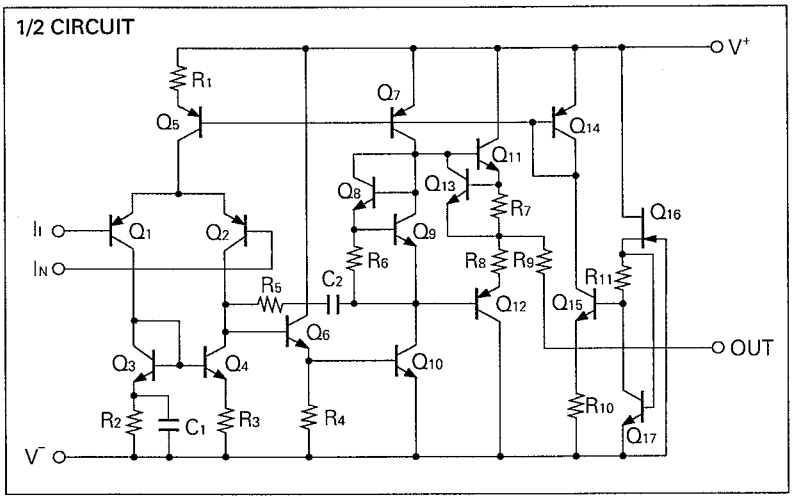
The μPC4572 is a dual wide band, ultra low noise operational amplifier designed for low supply voltage operation of +4 V to +14 V single supply and ±2 V to ±7 V split supplies. Using high h_{FE} PNP transistors for the input circuit, input bias current and input equivalent noise are better than conventional wide band operational amplifier.

The μPC4572 is an excellent choice for preamplifiers and active filters in audio, instrumentation, and communication circuit.

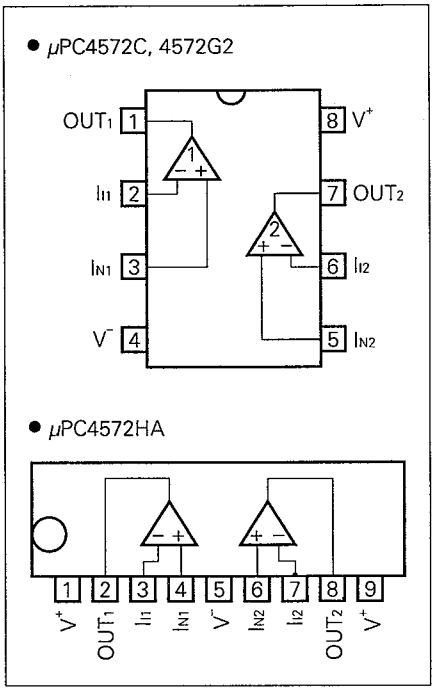
FEATURES

- Ultra low noise : e_n = 4 nV/√Hz
- Low input bias current : 100 nA
- High slew rate : 6 V/μs
- Low supply voltage : ±2 V to ±7 V (Split)
  +4 V to +14 V (Single)
- Internal frequency compensation

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM (Top View)



ORDERING INFORMATION

PART NUMBER	PACKAGE	QUALITY GRADE
μPC4572C	8 PIN PLASTIC DIP (300 mil)	Standard
μPC4572G2	8 PIN PLASTIC SOP (225 mil)	Standard
μPC4572HA	9 PIN SLIM SIP	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

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ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

PARAMETER		SYMBOL	μPC4572	UNIT
Voltage between V^+ and V^- (Note1)		$V^+ - V^-$	−0.3 to +15	V
Differential Input Voltage		V_{ID}	±10	V
Input Voltage (Note 2)		V_I	V^- −0.3 to V^+ +0.3	V
Output Voltage (Note 3)		V_O	V^- −0.3 to V^+ +0.3	V
Power Dissipation	C Package (Note 4)	P_T	350	mW
	G2 Package (Note 5)		440	mW
	HA Package (Note 4)		350	mW
Output Short Circuit Duration (Note 6)			10	sec
Operating Temperature Range		T_{opt}	−20 to +80	°C
Storage Temperature Range		T_{stg}	−55 to +125	°C

Note 1. Reverse connection of supply voltage can cause destruction.

Note 2. The input voltage should be allowed to input without damage or destruction. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The normal operation will establish when the both inputs are within the Common Mode Input Voltage Range of electrical characteristics.

Note 3. This specification is the voltage which should be allowed to supply to the output terminal from external without damage or destructive. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The output voltage of normal operation will be the Output Voltage Swing of electrical characteristics.

Note 4. Thermal derating factor is −5.0 mV / °C when ambient temperature is higher than 55 °C.

Note 5. Thermal derating factor is −4.4 mV / °C when ambient temperature is higher than 25 °C.

Note 6. Pay careful attention to the total power dissipation not to exceed the absolute maximum ratings, Note 4 and Note 5.

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage (Split)	$V^{\pm}$	±2	±5	±7	V
Supply Voltage (V^- = GND)	V^+	+4	+5/+12	±14	V
Output Current	I_O			±10	mA
Capacitive Load (A_V = +1)	C_L			100	pF

ELECTRICAL CHARACTERISTICS (T_a = 25 °C, $V^{\pm}$ = ±5 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Offset Voltage	V_{IO}		±0.3	±5	mV	$R_S \leqq 50\ \Omega$
Input Offset Current (Note7)	I_{IO}		±10	±100	nA	
Input Bias Current (Note7)	I_B		100	400	nA	
Large Signal Voltage Gain	A_V	10	100		V/mV	$R_L \geqq 2$ kΩ, V_O = ±2 V
Supply Current	I_{CC}		4.5	7	mA	I_O = 0 A, Both Amplifiers
Common Mode Rejection Ratio	CMR	70	90		dB	
Supply Voltage Rejection Ratio	SVR	70	85		dB	
Output Voltage Swing	V_{om}	±3.3	±3.7		V	$R_L \geqq 10$ kΩ
Output Voltage Swing	V_{om}	±3.0	±3.5		V	$R_L \geqq 2$ kΩ
Common Mode Input Voltage Range	V_{ICM}	±3.5	±4		V	
Output Short Circuit Current	$I_{o\ short}$	±15	±20		mA	R_L = 0
Slew Rate	SR	3.5	6		V/μs	A_V = 1, $R_L \geqq 2$ kΩ
Gain Band Width Product	GBW	10	16		MHz	f_O = 100 kHz
Unity Gain Frequency	f_{unity}		9		MHz	open loop
Phase Margin	ϕ_{unity}		60		°	open loop
Total Harmonic Distortion	THD		0.002		%	V_O = 1 $V_{r.m.s.}$, f = 20 Hz to 20 kHz (Fig. 1)
Input Equivalent Noise Voltage	V_n		0.8		μ$V_{r.m.s.}$	RIAA (Fig. 2)
			0.5	0.65	μ$V_{r.m.s.}$	FLAT + JIS A, R_S = 100 Ω (Fig. 3)
Input Equivalent Noise Voltage Density	e_n		4.5		nV/$\sqrt{Hz}$	f_O = 10 Hz
			4.0		nV/$\sqrt{Hz}$	f_O = 1 kHz
Input Equivalent Noise Current Density	i_n		0.7		pA/$\sqrt{Hz}$	f_O = 1 kHz
Channel Separation			120		dB	f = 20 Hz to 20 kHz
Average V_{IO} Temperature Drift	$\Delta V_{IO}/\Delta T$		±2		μV/°C	

Note 7. Input bias currents flow out from IC. Because each currents are base current of PNP-transistor on input stage.

ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V^+ = 5 V, V^- = GND)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Offset Voltage	V_{IO}		±0.3	±5	mV	$R_S \leqq 50\ \Omega$
Input Offset Current (Note7)	I_{IO}		±10	±100	nA	
Input Bias Current (Note7)	I_B		100	400	nA	
Large Signal Voltage Gain	A_V	8	80		V/mV	$R_L \geqq 2$ kΩ
Supply Current	I_{CC}		4	6	mA	I_O = 0 A, Both Amplifiers
Common Mode Rejection Ratio	CMR	60	75		dB	
Supply Voltage Rejection Ratio	SVR	60	70		dB	
Output Voltage (High)	V_{OH}	3.2	3.5		V	$R_L \geqq 2$ kΩ (R_L to 1/2 V^+)
Output Voltage (Low)	V_{OL}		1.3	1.6	V	$R_L \geqq 2$ kΩ (R_L to 1/2 V^+)
Common Mode Input Voltage Range	V_{ICM}	1.5		3.5	V	
Slew Rate	SR		4		V/μs	A_V = 1
Gain Band Width Product	GBW		12		MHz	

Note 7. Input bias currents flow out from IC. Because each currents are base current of PNP-transistor on input stage.

MEASUREMENT CIRCUIT

Fig. 1 Total Harmonic Distortion Measurement Circuit

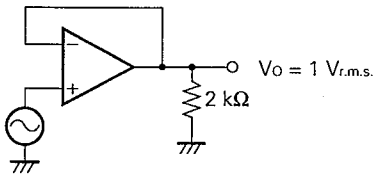


Fig. 2 Noise Measurement Circuit (RIAA)

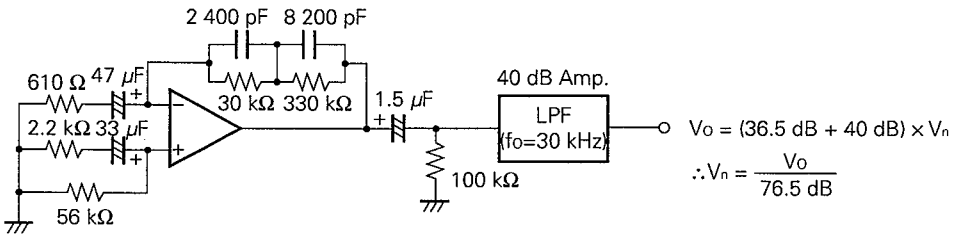
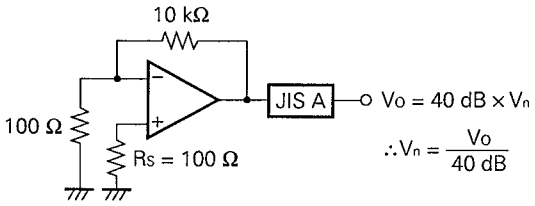
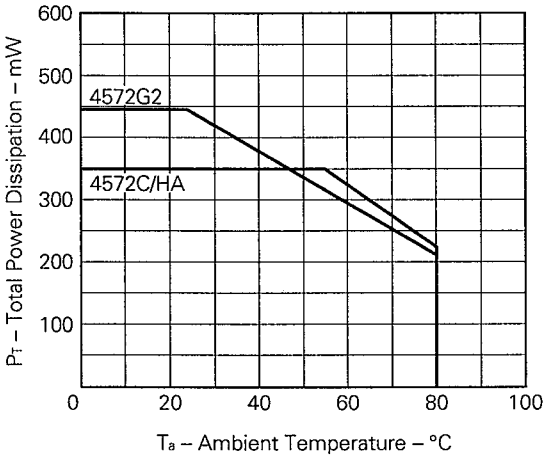


Fig. 3 Flat Noise Measurement Circuit (FLAT + JIS A)

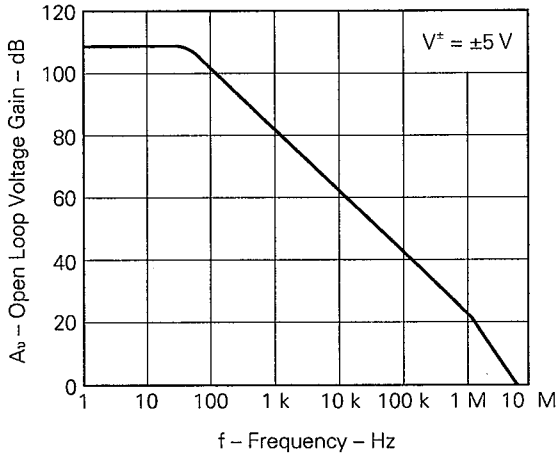


TYPICAL PERFORMANCE CHARACTERISTICS (T_a = 25 °C, TYP.)

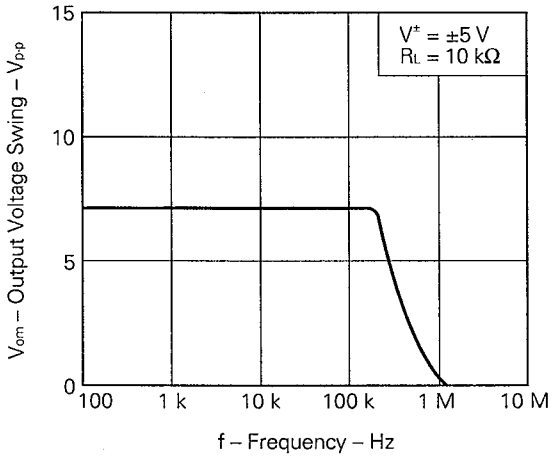
POWER DISSIPATION



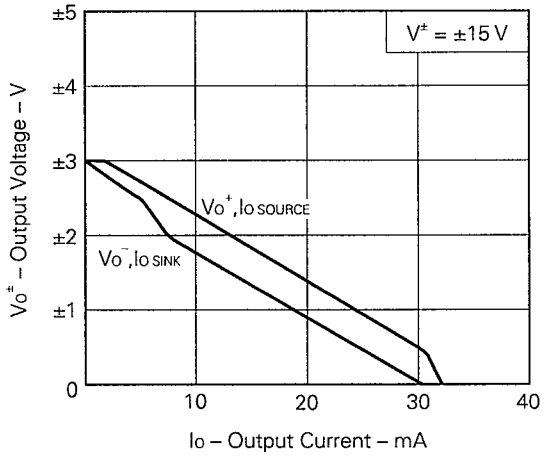
OPEN LOOP FREQUENCY RESPONSE



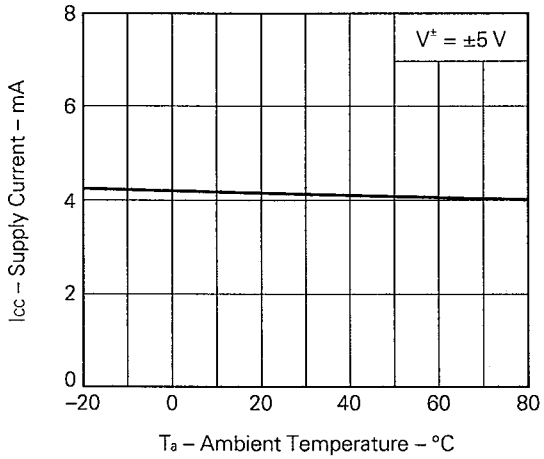
LARGE SIGNAL FREQUENCY RESPONSE



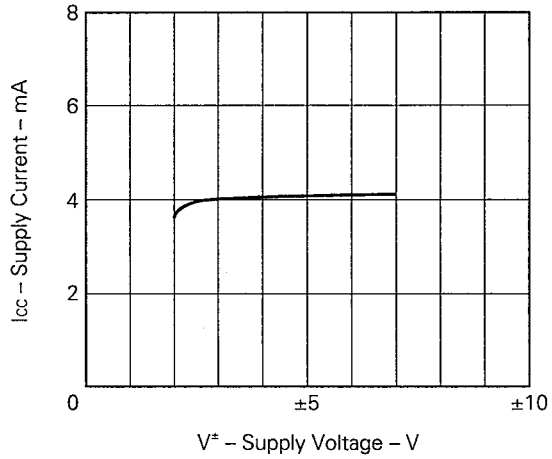
OUTPUT CURRENT LIMIT



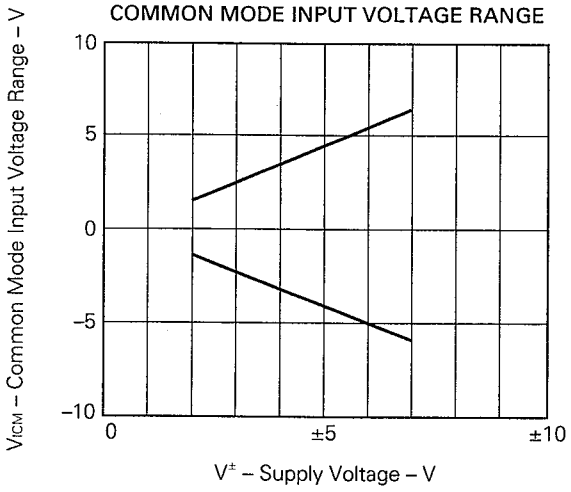
SUPPLY CURRENT



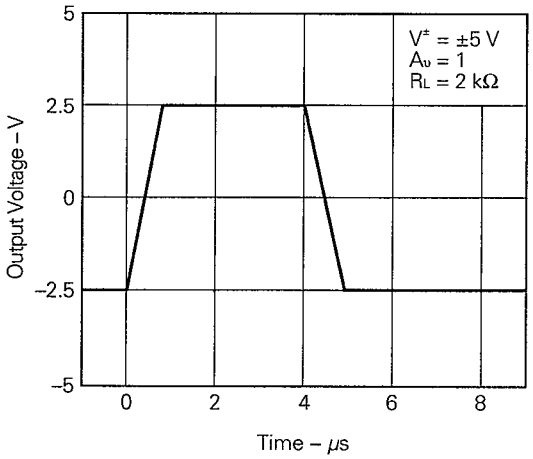
SUPPLY CURRENT



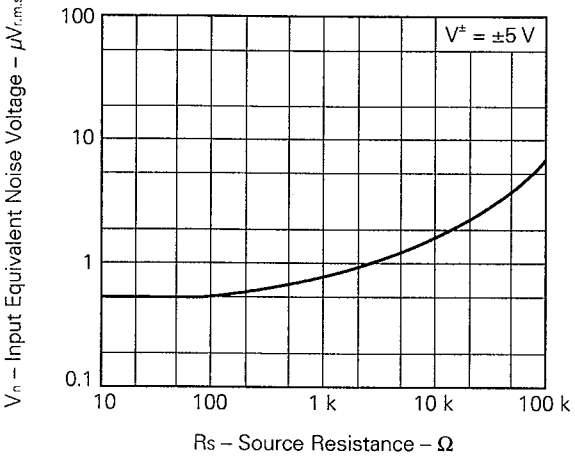
COMMON MODE INPUT VOLTAGE RANGE



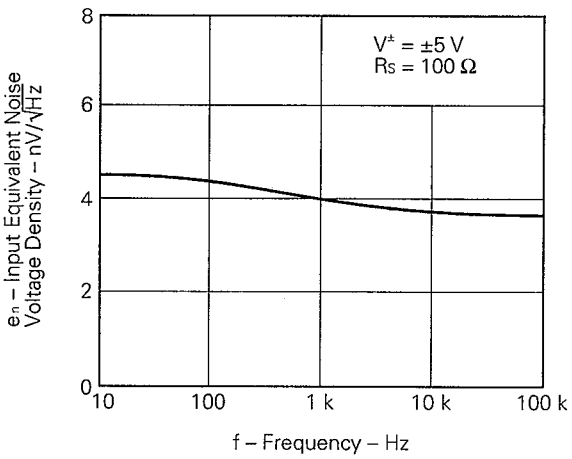
VOLTAGE FOLLOWER PULSE RESPONSE



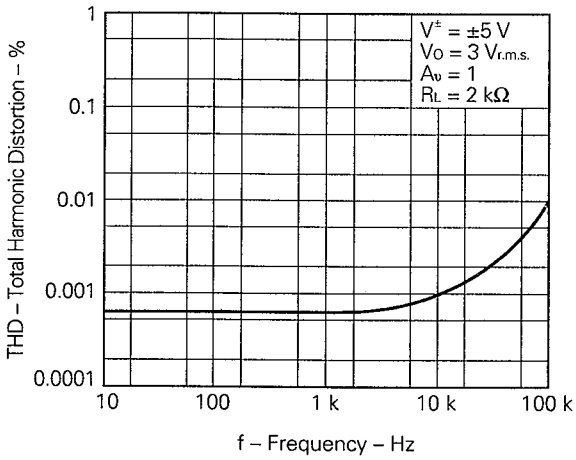
INPUT EQUIVALENT NOISE VOLTAGE (FLAT + JIS A)



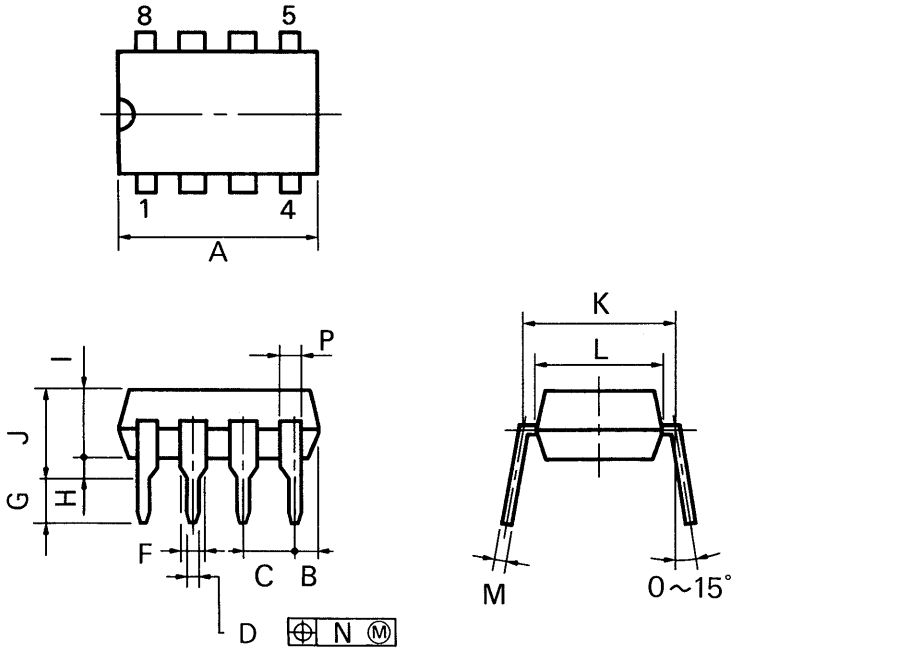
INPUT EQUIVALENT NOISE VOLTAGE DENSITY



TOTAL HARMONIC DISTORTION



8PIN PLASTIC DIP (300 mil)



P8C-100-300B,C

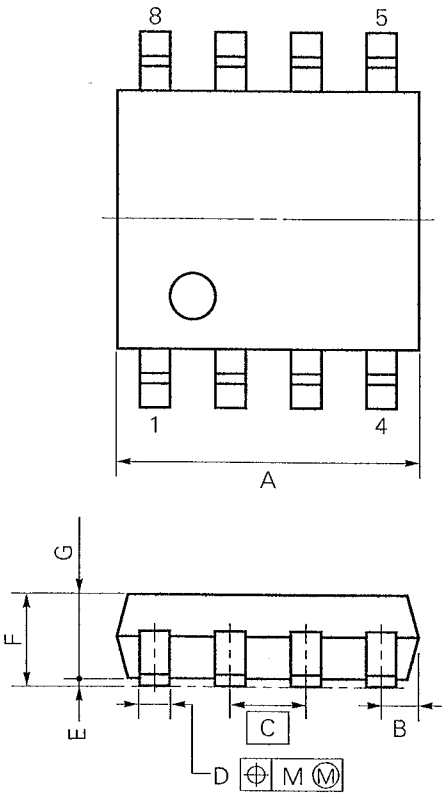
NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

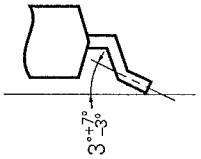
2) Item "K" to center of leads when formed parallel.

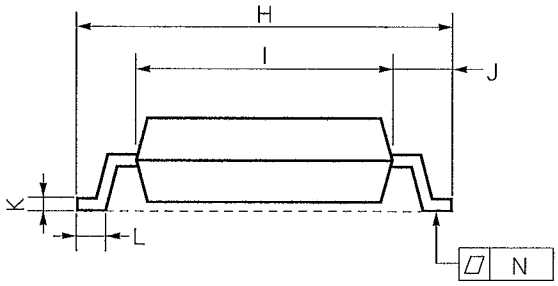
ITEM	MILLIMETERS	INCHES
A	10.16 MAX.	0.400 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.4 MIN.	0.055 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.

8 PIN PLASTIC SOP (225 mil)



detail of lead end





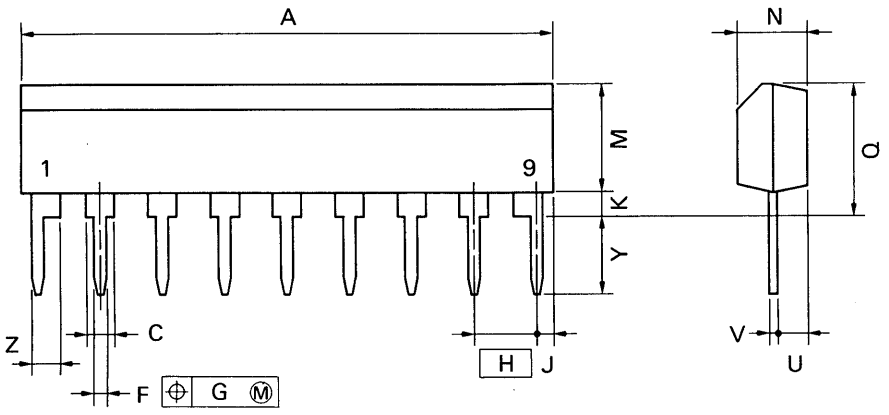
S8GM-50-225B-2

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	5.37 MAX.	0.212 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071MAX.
G	1.49	0.059
H	6.5±0.3	0.256±0.012
I	4.4	0.173
J	1.1	0.043
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005
N	0.15	0.006

9 PIN PLASTIC SLIM SIP



P9HA-254B

ITEM	MILLIMETERS	INCHES
A	22.86 MAX.	0.9 MAX.
C	1.1 MIN.	0.043 MIN.
F	$0.5^{\pm 0.1}$	$0.02^{+0.004}_{-0.005}$
G	0.25	0.01
H	2.54	0.1
J	1.27 MAX.	0.05 MAX.
K	0.51 MIN.	0.02 MIN.
M	5.08 MAX.	0.2 MAX.
N	$2.8^{\pm 0.2}$	$0.11^{+0.009}_{-0.008}$
Q	5.75 MAX.	0.227 MAX.
U	1.5 MAX.	0.059 MAX.
V	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.003}$
Y	$3.2^{\pm 0.5}$	$0.126^{\pm 0.02}$
Z	1.1 MIN.	0.043 MIN.

NOTE

Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.
Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI–1207).

[μPC4572G2]

Soldering method	Soldering conditions	Recommended condition symbol
Infrared ray reflow	Peak package's surface temperature: 230 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 1, Exposure limit*: None	IR30–00–1
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 1, Exposure limit*: None	VP15–00–1
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below, Number of flow process: 1, Exposure limit*: None	WS15–00–1
Partial heating method	Terminal temperature: 300 °C or below, Flow time: 10 seconds or below, Exposure limit*: None	

*: Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Note: Do not apply more than a single process at once, except for "Partial heating method."

TYPES OF THROUGH HOLE DEVICE

[μPC4572C, μPC4572HA]

Soldering method	Soldering conditions	Recommended condition symbol
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below	

[MEMO]

[MEMO]

M4 92.6