DATA SHEET

NEC

COMPOUND FIELD EFFECT TRANSISTOR ARRAY

μPA1550

N-CHANNEL POWER MOS FET ARRAY FOR SWITCHING

μPA1550 is a N-channel vertical power MOS FET and this switching device is available for direct drive by output of 5 V power supply IC.

This device features low on-resistance and excellent switching characteristic, and is ideal for control of devices such as mortars, solenoid, or ramp.

FEATURES

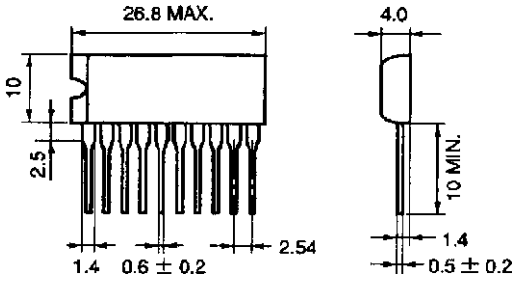
- Gate drive available at logic level (V_{GS} = 4 V)
- High current capacity and low on-resistnace
  $I_{D(pulse)}$ = ±20 A
  $R_{DS(on)}$ = 0.09 Ω TYP. @V_{GS} = 10 V
  $R_{DS(on)}$ = 0.11 Ω TYP. @V_{GS} = 4 V
- Easy to mount the printing board due to 2.54 mm (0.1 inch) interval of lead pins
- Small dimension and no electrode exposure except lead pins enable the high density mounting.

ORDERING INFORMATION

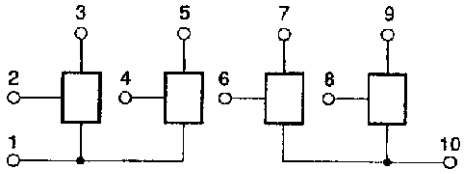
Part Number	Package	Quality
μPA1550H	10-pin SIP	Standard

Please refer to “Quality Grades on NEC Semiconductor Devices” (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

PACKAGE DRAWING (UNIT: mm)

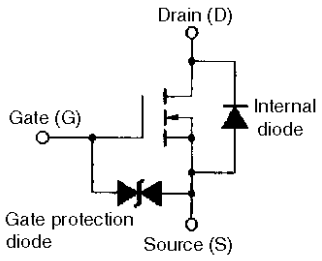


ELECTRODE CONNECTION



2, 4, 6, 8 : Gate (G)
3, 5, 7, 9 : Drain (D)
1, 10 : Source (S)

INTERNAL EQUIVALENT CIRCUIT



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ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

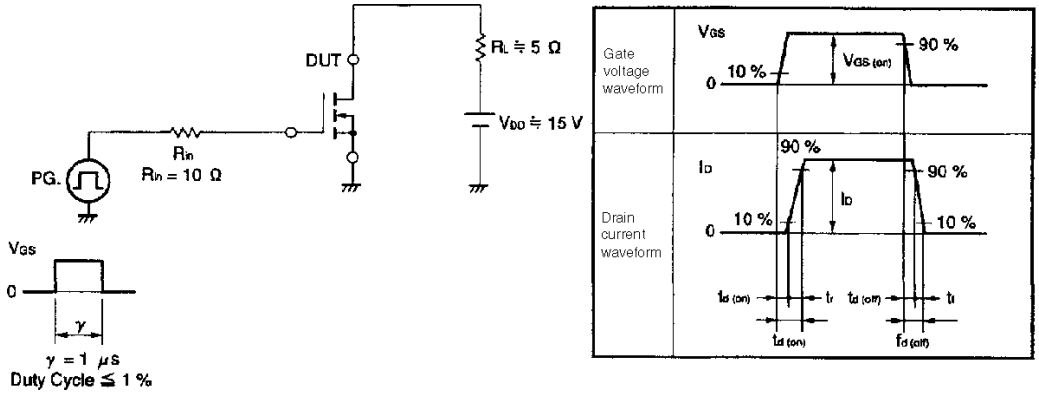
Parameter	Symbol	Conditions	Ratings	Unit
Drain to source voltage	V_{DSS}	V_{GS} = 0	30	V
Gate to source voltage	V_{GSS}	V_{DS} = 0	±20	V
Drain current (DC)	$I_{D(DC)}$	T_C = 25°C	±5	A/unit
Drain current (pulse)	$I_{D(pulse)}$	PW ≤ 10 μs duty cycle ≤ 1 %	±20	A/unit
Total power dissipation	P_{T1}*	T_C = 25°C	3.5	W
Total power dissipation	P_{T2}*	T_a = 25°C	28	W
Channel temperature	T_{ch}		150	°C
Storage temperature	T_{stg}		−55 to +150	°C

* When all 4 elements are ON.

ELECTRICAL CHARACTERISTICS (VCC = 5V, Ta = 25°C)

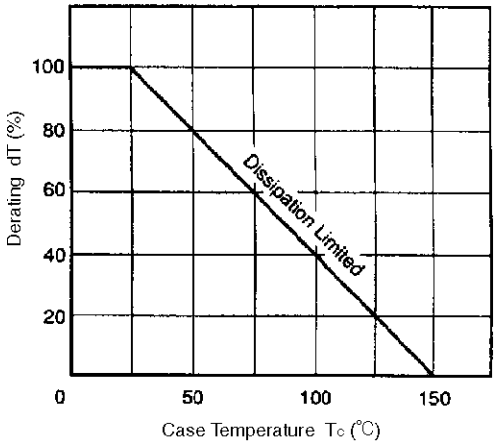
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Drain cutoff current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			10	μA
Gate leakage current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
Gate cutoff voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	0.8		2.5	V
Forward transfer admittance	$\|y_{ts}\|$	V_{DS} = 10 V, I_D = 3 A	4.0	5.0		S
Drain to source on-state resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 3 A		90	100	mΩ
Drain to source on-state resistance	$R_{DS(on)2}$	V_{GS} = 4 V, I_D = 3 A		110	150	mΩ
Input capacitance	C_{iss}	V_{DS} = 10 V		900		pF
Output capacitance	C_{oss}	V_{GS} = 0 V		400		pF
Return capacitance	C_{rss}	f = 1 MHz		100		pF
Turn-on delay time	$t_{d(on)}$	I_D = 3 A $V_{GS(on)}$ = 10 V V_{DD} = 5 Ω R_L = 5 Ω, R_{in} = 10 Ω Refer to the test circuit.		10		ns
Rise time	t_r			40		ns
Turn-off delay time	$t_{d(off)}$			110		ns
Fall time	t_f			30		ns

TEST CIRCUIT DIAGRAM: SWITCHING TIME

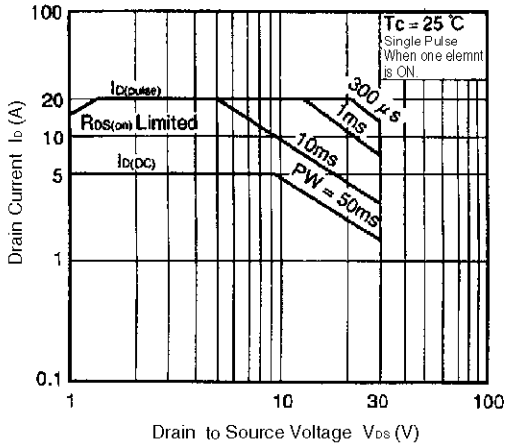


TYPICAL CHARACTERISTICS (Ta = 25°C)

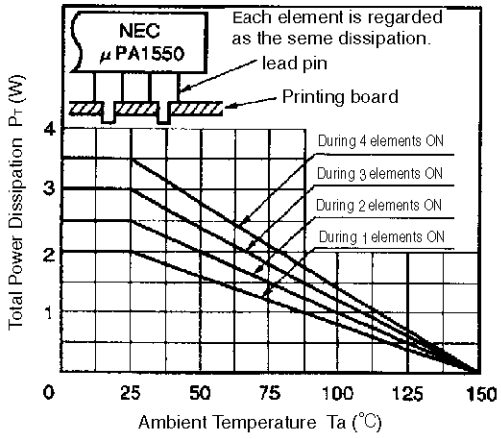
DERATING CURVE OF SAFE OPERATING AREA



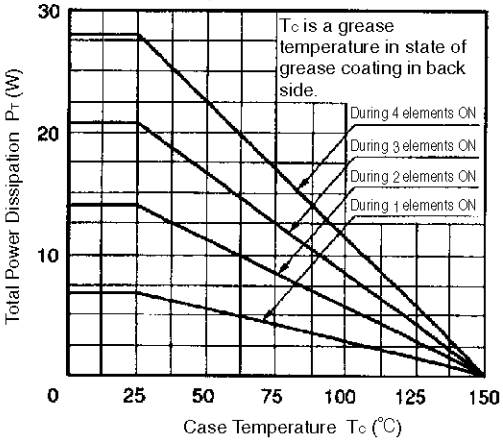
FORWARD BIAS SAFE OPERATING AREA



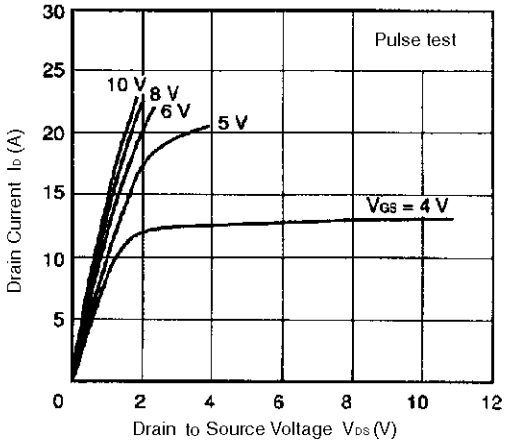
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



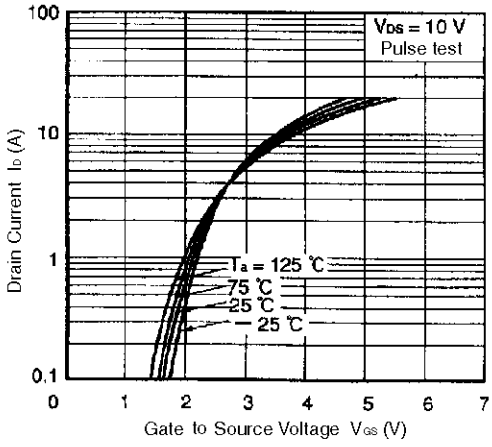
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



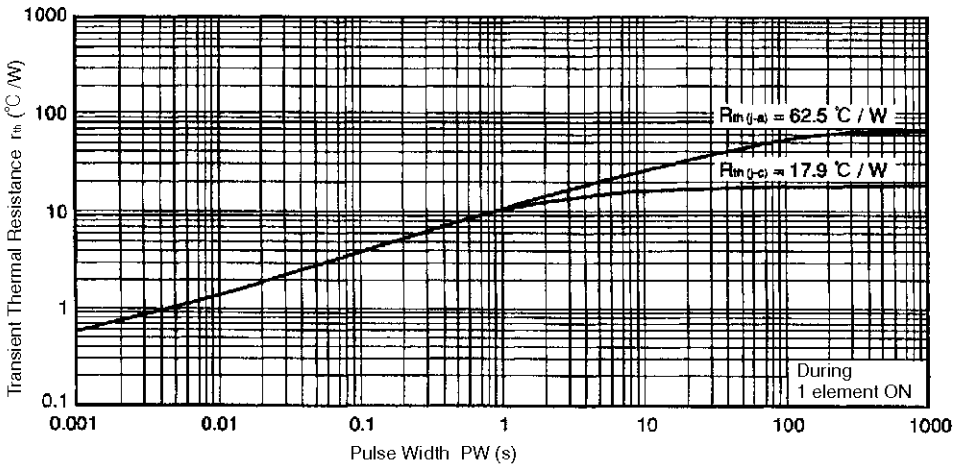
DRAIN CURRET vs. DRAIN TO SOURCE VOLTAGE



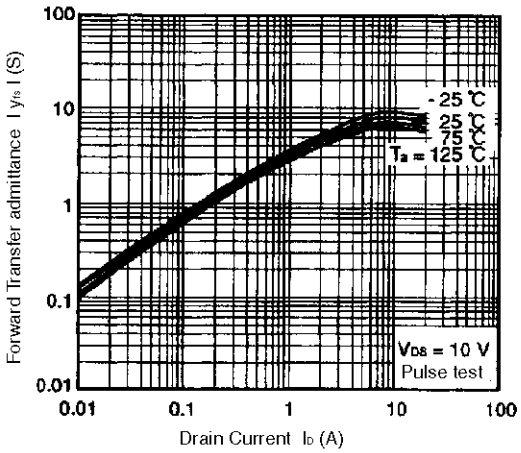
TRANSFER CHARACTERISTICS



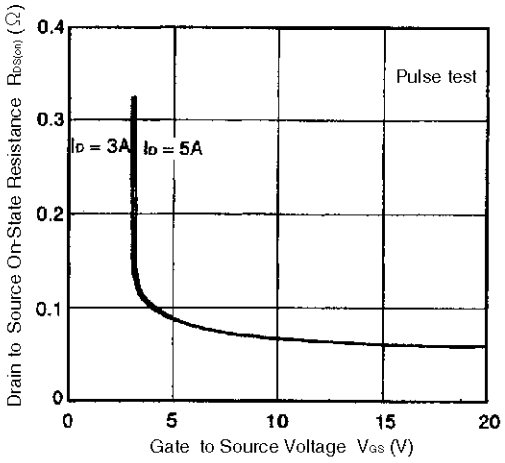
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



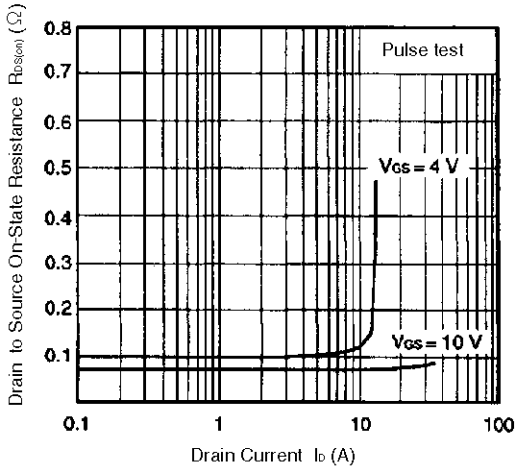
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



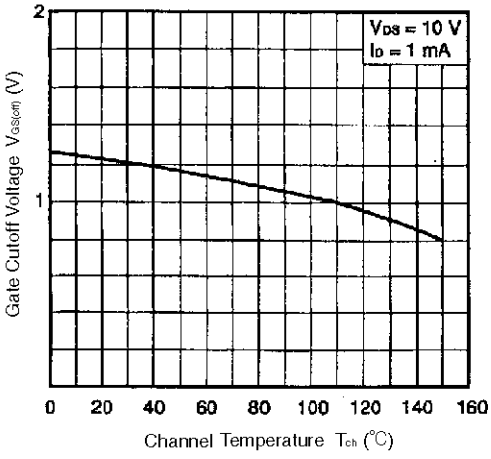
DRAIN TO SOURCE ON STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



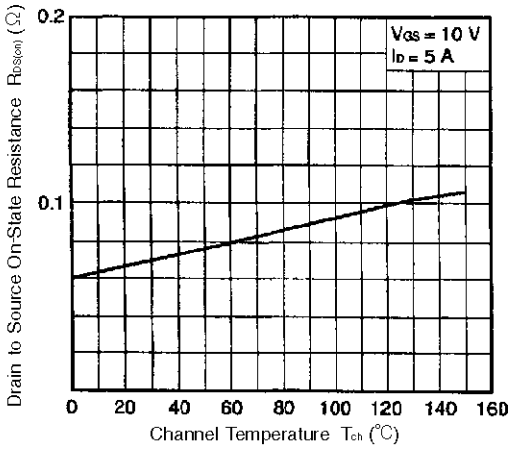
DRAIN TO SOURCE ON STATE RESISTANCE vs. DRAIN CURRENT



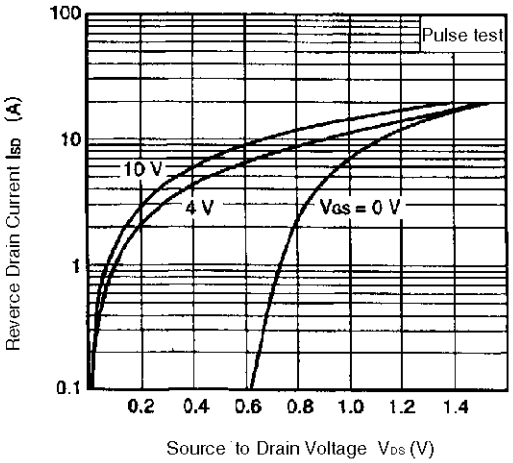
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



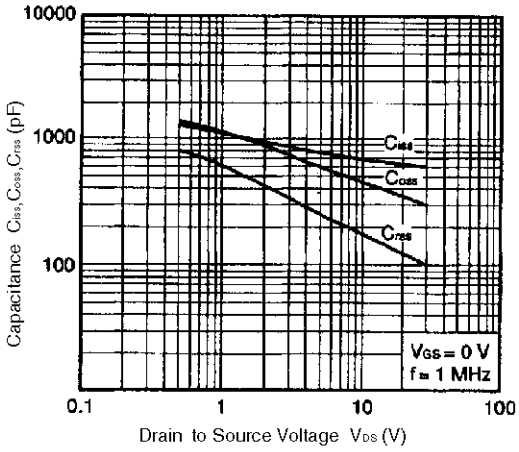
DRAIN TO SOURCE ON - STATE RESISTANCE vs. CHANNEL TEMPERATURE



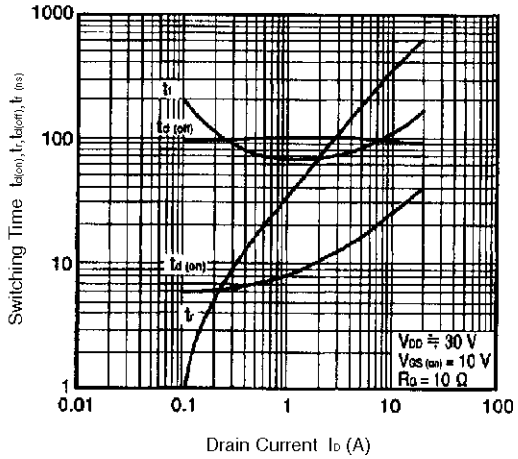
BODY DIODE FORWARD VOLTAGE



CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



SWITCHING CARACTERISTICS



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M8E 00.4