7480/7481 GROUP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 7480/7481 group is the single-chip microcomputer adopting the silicon gate CMOS process. In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed in the same memory space.

Having built-in serial I/O, A-D converter, and watchdog timer, this single-chip microcomputer is useful for control of automobiles, office automation equipment and home electric appliances.

The 7480/7481 group includes multiple types which differ in the memory type, size, and package.

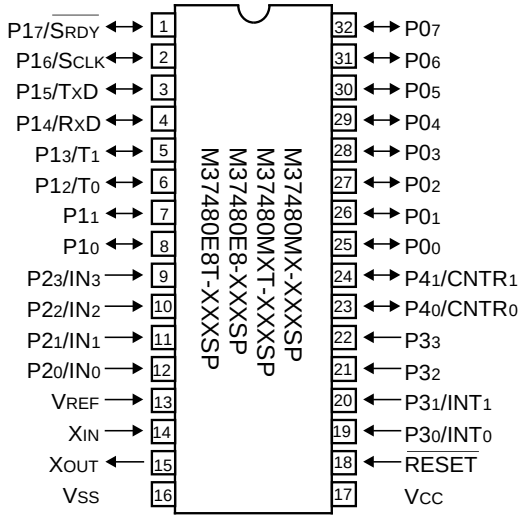
FEATURES

- Number of basic machine language instructions 71
- Minimum instruction execution time ..... 0.5 μs
  (at 8 MHz clock input oscillation frequency)
- Memory size ROM ..... 4 K to 16 K bytes
  RAM ..... 128 to 448 bytes
- Programmable I/O ports ..... 18 (7480 group)
  (P0, P1, P4, P5) 24 (7481 group)
- Input ports ..... 8 (7480 group)
  (P2, P3) 12 (7481 group)
- Built-in programmable pull-up transistors (P0, P1)
- Built-in clamp diodes ..... 2 (7480 group)
  (P4, P5) 8 (7481 group)
- Interrupt ..... 14 sources, 13 vectors
- Timer X, Y ..... 16-bit × 2
- Timer 1, 2 ..... 8-bit × 2
- Serial I/O ..... 8-bit x 1 (UART or clock-synchronized)
- A-D converter ..... 8-bit x 4 channels (7480 group)
  8-bit x 8 channels (7481 group)
- Built-in watchdog timer
- Power source voltage ..... 2.7 to 4.5 V
  (at [2.2 V_{CC}-2] MHz clock input oscillation frequency)
  4.5 to 5.5 V
  (at 8 MHz clock input oscillation frequency)
- Power dissipation ..... 35 mW
  (at 8 MHz clock input oscillation frequency and 5 V power source voltage)

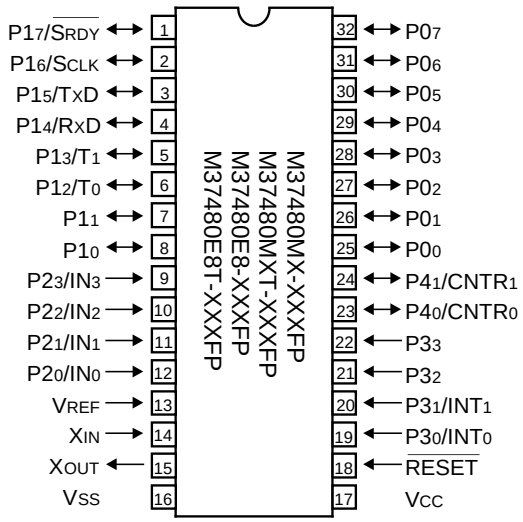
APPLICATIONS

Automobiles, office automation equipment, home electric appliances, etc.

PIN CONFIGURATION

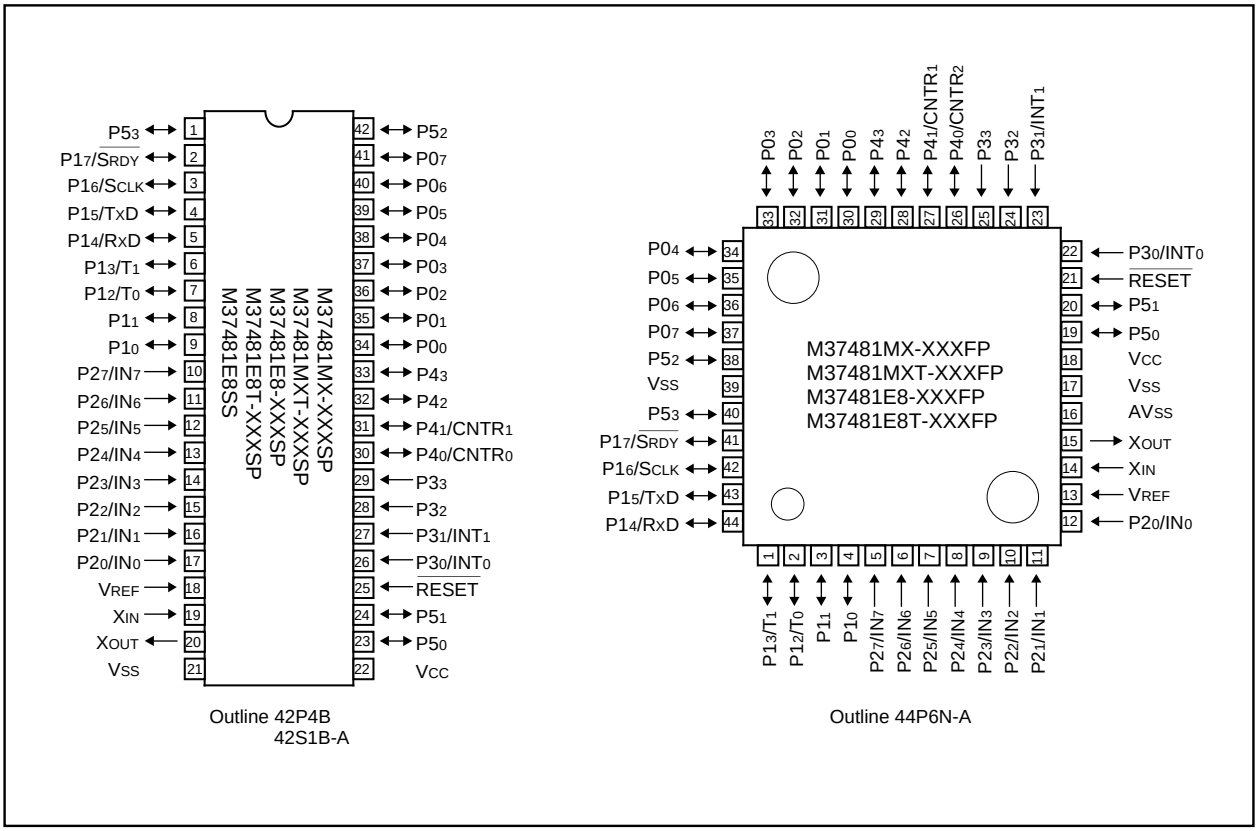


Outline 32P4B



Outline 32P2W-A

Fig. 1 Pin configuration (top view)



Outline 42P4B
42S1B-A

Outline 44P6N-A

Fig. 2 Pin configuration (top view)

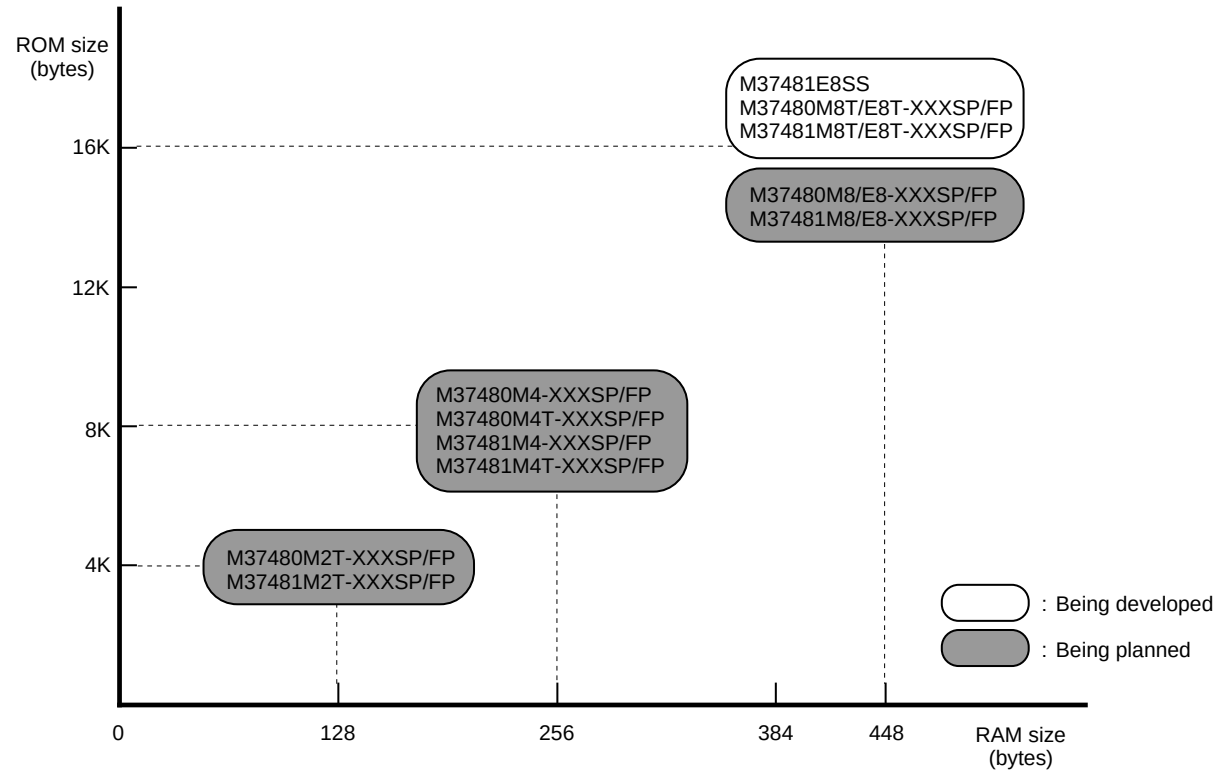
7480/7481 GROUP PRODUCT LIST

Table 1. 7480/7481 group product list

Product model name	ROM (bytes)	RAM (bytes)	I/O port	Package	Remarks
M37480M2T-XXXSP	4096	128	18 I/O ports 8 input ports (including 4 analog input ports)	32P4B	Mask ROM version*
M37480M2T-XXXFP				32P2W-A	
M37480M4-XXXSP	8192	256		32P4B	Mask ROM version
M37480M4-XXXFP				32P2W-A	
M37480M4T-XXXSP				32P4B	Mask ROM version*
M37480M4T-XXXFP				32P2W-A	
M37480M8-XXXSP	16384	448		32P4B	Mask ROM version
M37480M8-XXXFP				32P2W-A	
M37480M8T-XXXSP				32P4B	Mask ROM version*
M37480M8T-XXXFP				32P2W-A	
M37480E8SP				32P4B	One time PROM version (shipped in blank)
M37480E8FP				32P2W-A	
M37480E8-XXXSP				32P4B	One time PROM version
M37480E8-XXXFP				32P2W-A	
M37480E8T-XXXSP				32P4B	One time PROM version*
M37480E8T-XXXFP				32P2W-A	
M37481M2T-XXXSP	4096	128	24 I/O ports 12 input ports (including 8 analog input ports)	42P4B	Mask ROM version*
M37481M2T-XXXFP				44P6N-A	
M37481M4-XXXSP	8192	256		42P4B	Mask ROM version
M37481M4-XXXFP				44P6N-A	
M37481M4T-XXXSP				42P4B	Mask ROM version*
M37481M4T-XXXFP				44P6N-A	
M37481M8-XXXSP	16384	448		42P4B	Mask ROM version
M37481M8-XXXFP				44P6N-A	
M37481M8T-XXXSP				42P4B	Mask ROM version*
M37481M8T-XXXFP				44P6N-A	
M37481E8SP				42P4B	One time PROM version (shipped in blank)
M37481E8FP				44P6N-A	
M37481E8-XXXSP				42P4B	One time PROM version
M37481E8-XXXFP				44P6N-A	
M37481E8T-XXXSP				42P4B	One time PROM version*
M37481E8T-XXXFP				44P6N-A	
M37481E8SS				42S1B-A	Built-in EPROM version

*: Extended operating temperature range version

7480/7481 GROUP ROM/RAM DEVELOPMENT SCHEDULE



Note: Regarding the models being developed and planned, the development schedule may be reviewed. In case of the models being planned, the development of them may be stopped.

Fig. 3 ROM/RAM development schedule

FUNCTIONAL BLOCK DIAGRAM

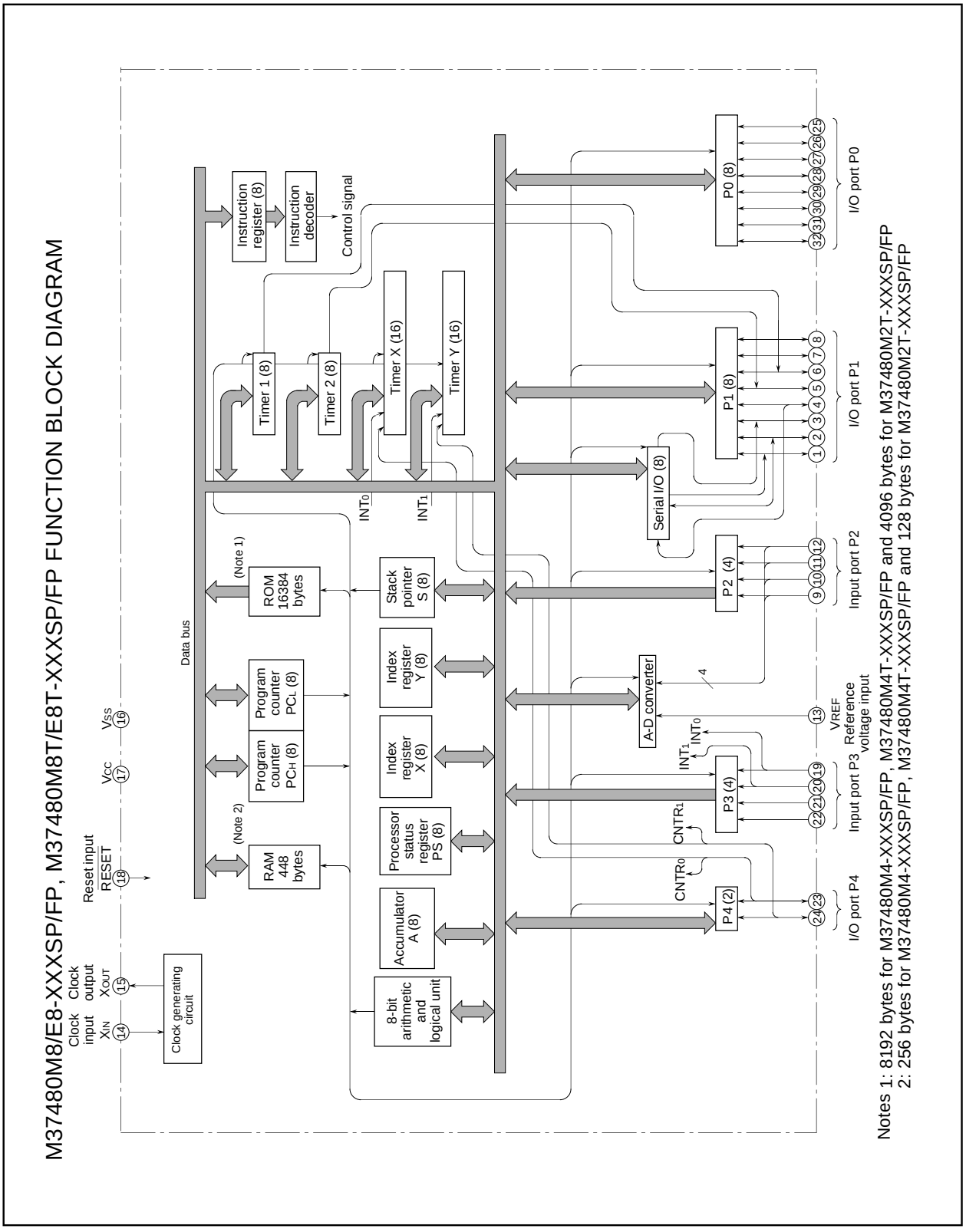


Fig. 4 Function block diagram (1)

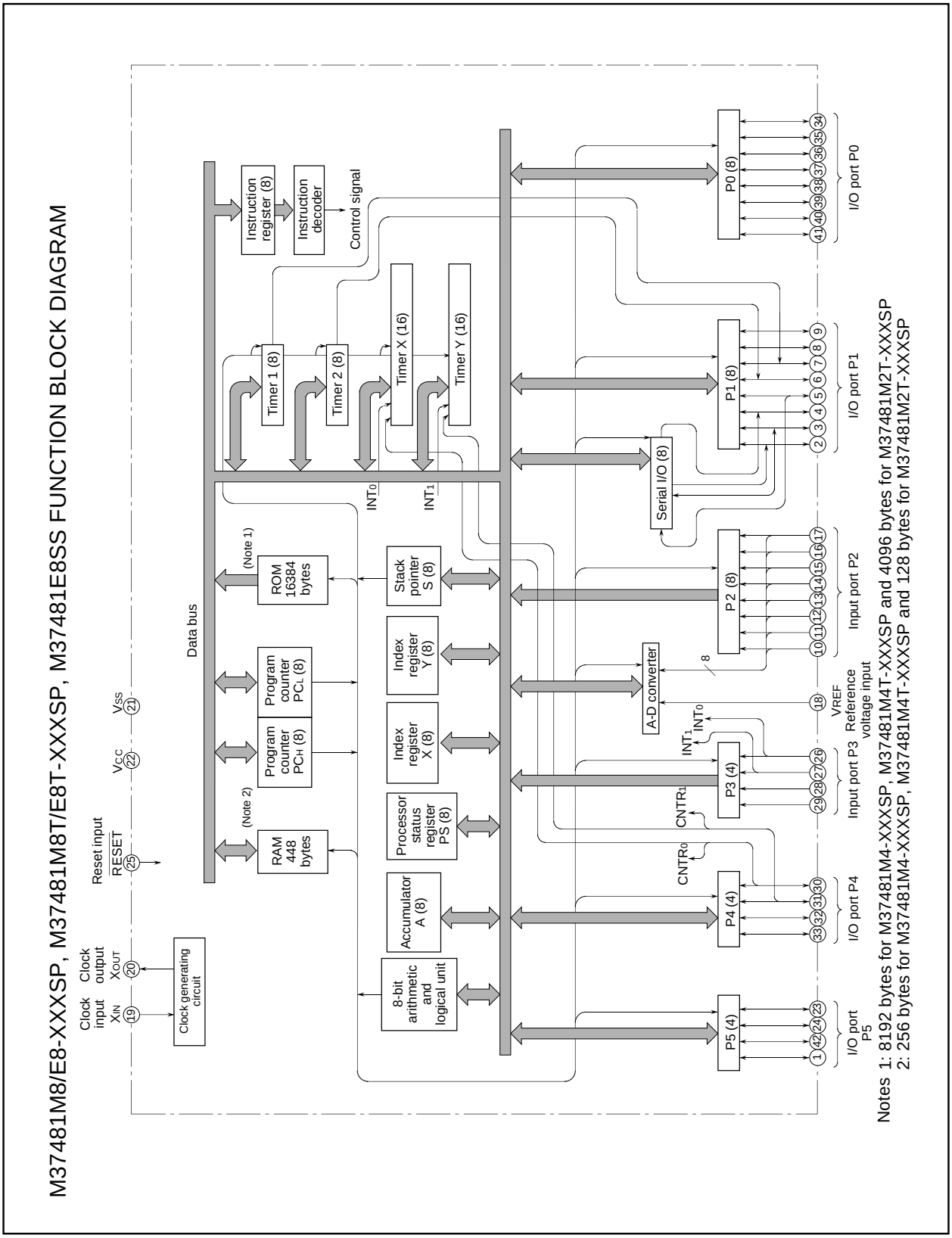


Fig. 5 Function block diagram (2)

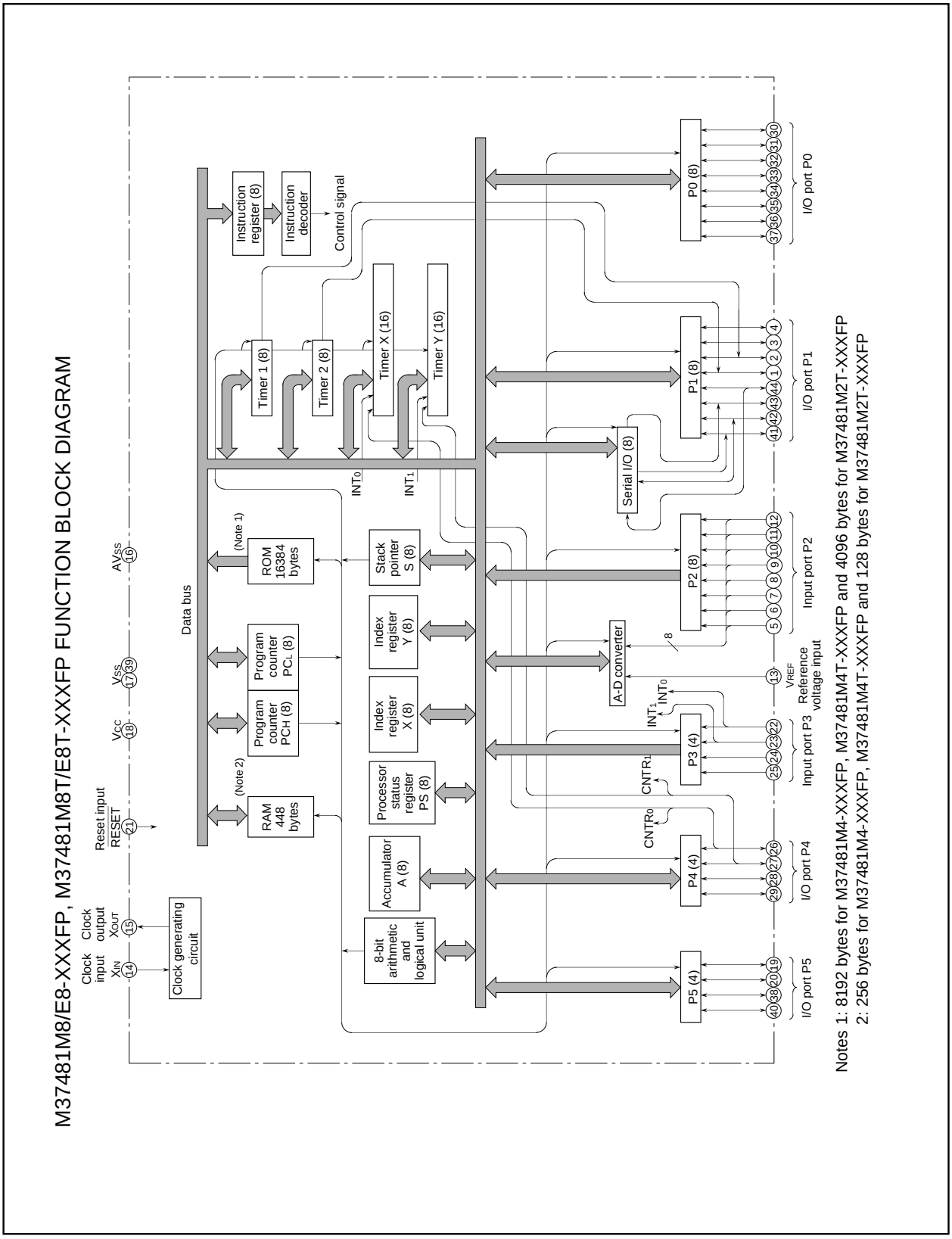


Fig. 6 Function block diagram (3)

FUNCTIONS OF 7480/7481 GROUP

Table 2. Functions of 7480/7481 group

Parameter			Functions	
			M37480M4/M8/E8-XXXSP/FP M37480M2T/M4T/M8T/E8T-XXXSP/FP	M37481M4/M8/E8-XXXSP/FP M37481M2T/M4T/M8T/E8T-XXXSP/FP
Number of basic instructions			71 (740 family 69 basic instructions + 2 multiplication/division instructions)	
Instruction execution time			0.5μs (Minimum instructions, at 8 MHz clock input oscillation frequency)	
Clock input oscillation frequency			8 MHz (max.)	
Memory size	ROM	M8/E8	16384 bytes	
		M4	8192 bytes	
		M2	4096 bytes	
	RAM	M8/E8	448 bytes	
		M4	256 bytes	
		M2	128 bytes	
I/O port	P0, P1	I/O	8 bits × 2	
	P2	Input	4 bits × 1	8 bits × 1
	P3	Input	4 bits × 1	
	P4	I/O	2 bits × 1	4 bits × 1
	P5	I/O	————	4 bits × 1
I/O characteristics	I/O withstand voltage		5 V	
	Output current		–5 to 10 mA (P0, P1: CMOS tri-states), 10 mA (P4, P5: N channel)	
Serial I/O			8 bits × 1	
Timers			16-bit timer x 2, 8-bit timer x 2	
Subroutine nesting		M8/E8	192 max.	
		M4	96 max.	
		M2	64 max.	
Interrupt			5 external interrupts, 8 internal interrupts, 1 software interrupt	
A-D converter (successive comparison method)			8 bits × 4 analog inputs (in common with P2)	8 bits × 8 analog inputs (in common with P2)
Clock generating circuit			Built-in circuit with feedback resistor (with external ceramic oscillator)	
Watchdog timer			Built-in circuit	
Power source voltage			2.7 to 4.5 V (at f(X_{IN}) = (2.2V_{CC} – 2) MHz) 4.5 to 5.5 V (at f(X_{IN})=8 MHz)	
Power dissipation			35 mW (standard, at 8 MHz clock input oscillation frequency)	
Operating temperature range			–20 to 85 °C (–40 to 85 °C for extended operating temperature range version)	
Device structure			CMOS silicon gate	
Package			32-pin SDIP/32-pin SOP	42-pin SDIP/44-pin OFP

PIN DESCRIPTION

Table 3. Pin description

Pin	Name	Input/ output	Functions
V_{CC}, V_{SS}	Power source		Apply a voltage of 2.7 to 5.5 V to V_{CC} and 0 V to V_{SS}.
AV_{SS}	Analog power source input		Ground level input pin for A-D converter. Apply the same voltage as Vss. (This pin is for 44P6N-A package only.)
V_{REF}	Reference voltage input	Input	Reference voltage input pin for A-D converter. (When the A-D converter is not used, connect it to V_{CC}.)
$\overline{RESET}$	Reset input	Input	Reset input pin active "L".
X_{IN}	Clock input	Input	These are I/O pins for the internal clock generating circuit of the main clock. To control the generating frequency, an external ceramic is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected to the X_{IN} pin, and the X_{OUT} pin should be left open. The feedback resistor is connected between X_{IN} and X_{OUT}.
X_{OUT}	Clock output	Output	
$P0_0$ – $P0_7$	I/O port P0	I/O	8-bit I/O port. The output structure is CMOS output. When this port is selected for input, pull-up transistors can be connected in units of 1 bit, and a key-on wake-up function is provided.
$P1_0$ – $P1_7$	I/O port P1	I/O	8-bit I/O port. The output structure is CMOS output. When this port is selected for input, pull-up transistors can be connected in units of 4 bits. $P1_2$ and $P1_3$ are in common with timer output pins T_0 and T_1. $P1_4$, $P1_5$, $P1_6$ and $P1_7$ are in common with serial I/O pins R_XD, T_XD, S_{CLK} and $\overline{S_{RDY}}$, respectively.
$P2_0$ – $P2_7$	Input port P2	Input	8-bit input port. (Only 4 bits of $P2_0$ to $P2_3$ for the 7480 group) or analog input pins IN_0 to IN_7 (IN_0 to IN_3 for the 7480 group).
$P3_0$ – $P3_3$	Input port P3	Input	4-bit input port. $P3_0$ and $P3_1$ can be configured to serve as external interrupt input pins INT_0 and INT_1.
$P4_0$ – $P4_3$	I/O port P4	I/O	4-bit I/O port. (2 bits of $P4_0$ and $P4_1$ for the 7480 group). The output structure is N-channel open drain output, having a built-in clamp diode. $P4_0$ and $P4_1$ can be configured to serve as timer I/O pins $CNTR_0$ and $CNTR_1$.
$P5_0$ – $P5_3$	I/O port P5	I/O	4-bit I/O port. (This port is not included in the 7480 group.) The output structure is N-channel open drain output, having built-in clamp diodes.

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The 7480/7481 group uses the standard 740 family CPU. Refer to the table of 740 family addressing modes and machine instructions or the MELPS 740 programming manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

1. The FST and SLW instructions are not available.
2. The MUL and DIV instructions are available.
3. The WIT instruction is available. (Note)
4. The STP instruction is available. (Note)

Note: When using these instructions, refer to the corresponding chapter “STP and WIT instruction control” below.

CPU Mode Register

The stack page selection bit is assigned to the CPU mode register. This register is allocated at address 00FB16.

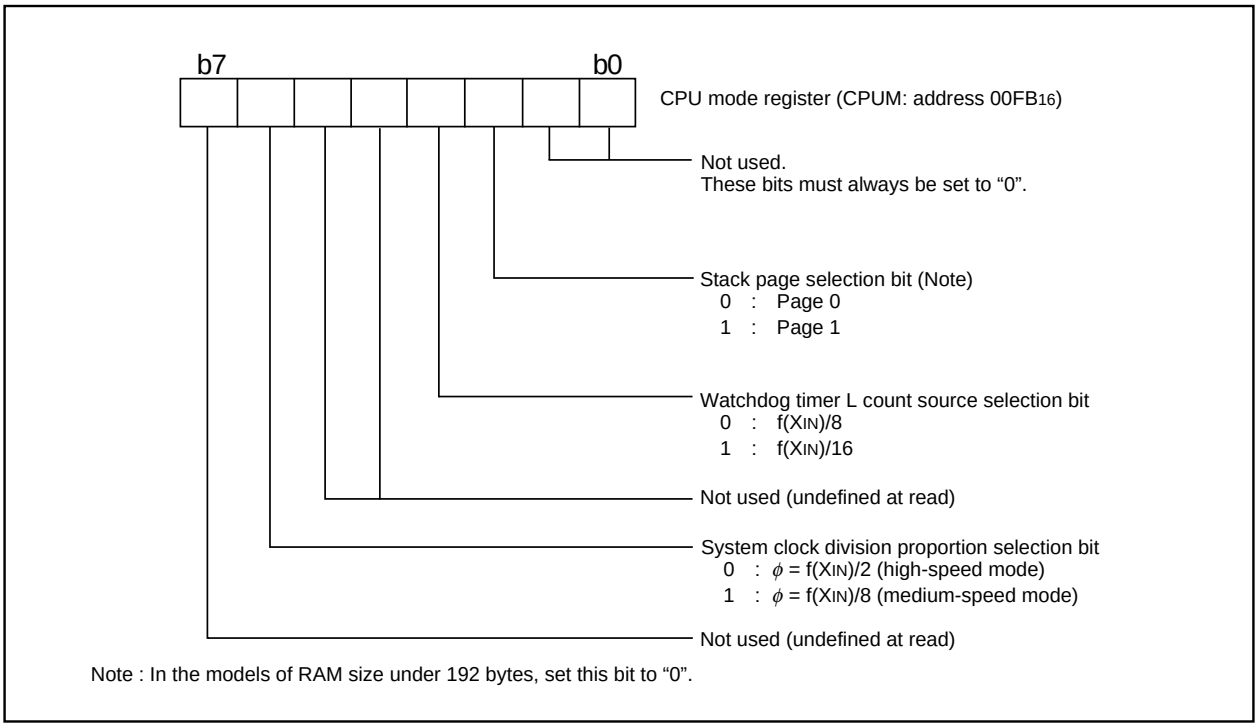


Fig. 7 Structure of CPU mode register

Memory

- SFR Area
  This SFR area is provided in the zero page and contains the registers for controlling I/O ports and timers.
- RAM
  RAM is used for data storage and for calling subroutines, as well as for a stack area for interrupts.
- ROM
  ROM is used for storing user programs and interrupt vectors.
- Interrupt Vector Area
  The interrupt vector area is used for storing vector addresses when an interrupt is generated or at reset.
- Zero Page
  This area can be accessed with 2 words when the zero page addressing mode is used.
- Special Page
  This area can be accessed with 2 words when the special page addressing mode is used.

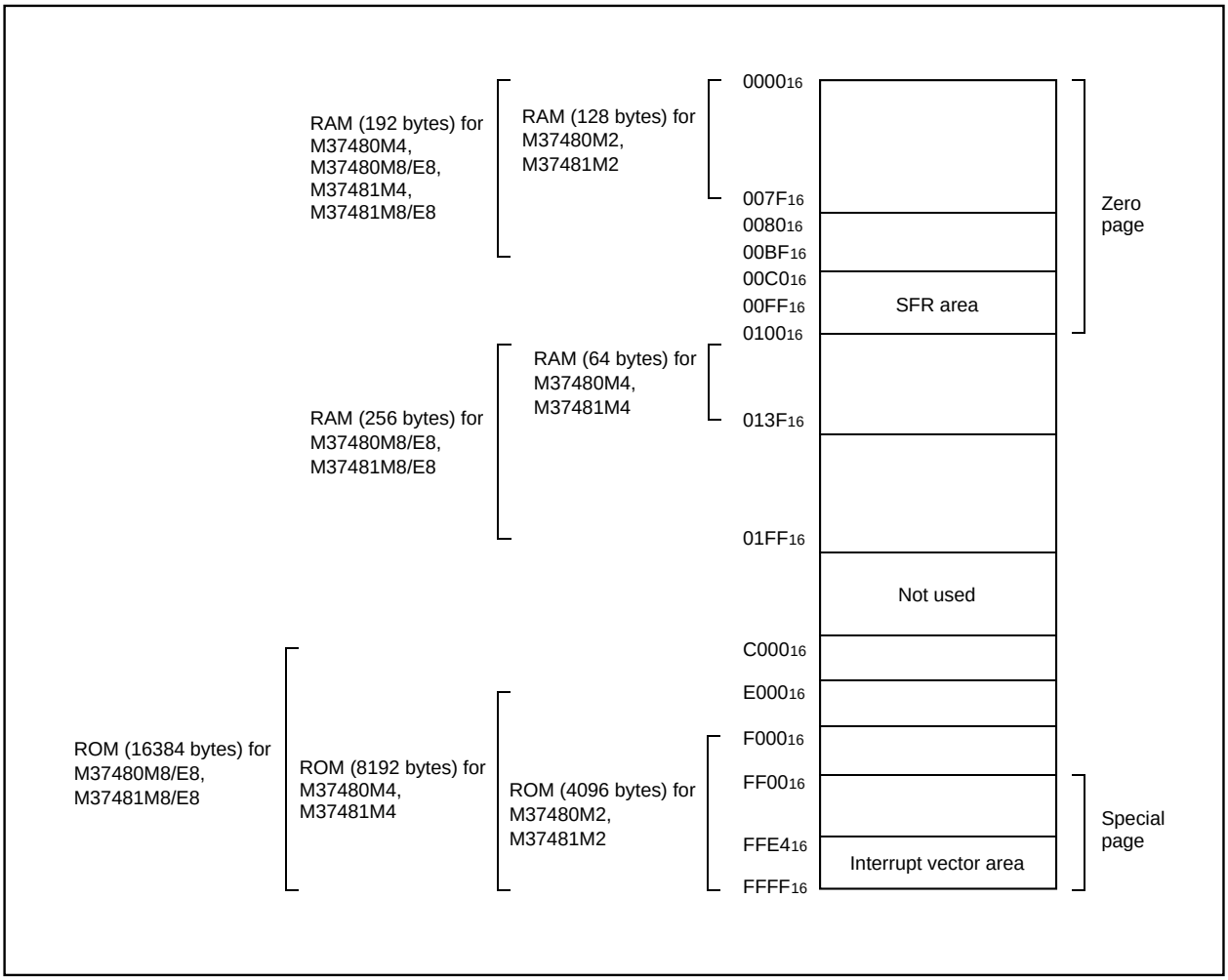


Fig. 8 Memory map

$00C0_{16}$	Port P0 (P0)	$00E0_{16}$	Transmit/receive buffer register (TB/RB)
$00C1_{16}$	Port P0 direction register (P0D)	$00E1_{16}$	Serial I/O status register (SIOSTS)
$00C2_{16}$	Port P1 (P1)	$00E2_{16}$	Serial I/O control register (SIOCON)
$00C3_{16}$	Port P1 direction register (P1D)	$00E3_{16}$	UART control register (UARTCON)
$00C4_{16}$	Port P2 (P2)	$00E4_{16}$	Baud rate generator (BRG)
$00C5_{16}$		$00E5_{16}$	Bus collision detection control register (BUSARBCON)
$00C6_{16}$	Port P3 (P3)	$00E6_{16}$	
$00C7_{16}$		$00E7_{16}$	
$00C9_{16}$	Port P4 (P4)	$00E8_{16}$	
$00C9_{16}$	Port P4 direction register (P4D)	$00E9_{16}$	
$00CA_{16}$	Port P5 (P5) (Note)	$00EA_{16}$	
$00CB_{16}$	Port P5 direction register (P5D) (Note)	$00EB_{16}$	
$00CC_{16}$		$00EC_{16}$	
$00CD_{16}$		$00ED_{16}$	
$00CE_{16}$		$00EE_{16}$	
$00CF_{16}$		$00EF_{16}$	Watchdog timer H (WDTH)
$00D0_{16}$	Port P0 pull-up control register (P0PCON)	$00F0_{16}$	Timer X low-order (TXL)
$00D1_{16}$	Port P1 pull-up control register (P1PCON)	$00F1_{16}$	Timer X high-order (TXH)
$00D2_{16}$	Port P4P5 input control register (P4P5CON)	$00F2_{16}$	Timer Y low-order (TYL)
$00D3_{16}$		$00F3_{16}$	Timer Y high-order (TYH)
$00D4_{16}$	Edge polarity selection register (EG)	$00F4_{16}$	Timer 1 (T1)
$00D5_{16}$		$00F5_{16}$	Timer 2 (T2)
$00D6_{16}$		$00F6_{16}$	Timer X mode register (TXM)
$00D7_{16}$		$00F7_{16}$	Timer Y mode register (TYM)
$00D8_{16}$		$00F8_{16}$	Timer XY control register (TXYCON)
$00D9_{16}$	A-D control register (ADCON)	$00F9_{16}$	Timer 1 mode register (T1M)
$00DA_{16}$	A-D conversion register (AD)	$00FA_{16}$	Timer 2 mode register (T2M)
$00DB_{16}$		$00FB_{16}$	CPU mode register (CPUM)
$00DC_{16}$		$00FC_{16}$	Interrupt request register 1 (IREQ1)
$00DD_{16}$		$00FD_{16}$	Interrupt request register 2 (IREQ2)
$00DE_{16}$	STP instruction operation control register (STPCON)	$00FE_{16}$	Interrupt control register 1 (ICON1)
$00DF_{16}$		$00FF_{16}$	Interrupt control register 2 (ICON2)

Fig. 9 SFR (Special Function Register) memory map

Note: This port is not allocated in the 7480 group.

I/O Ports

[Direction Registers]

The I/O ports have direction registers which determine the input/output direction of each pin in units of bit. When a bit of the direction register is set to "1", the corresponding pin becomes an output port. When the bit is cleared to "0", it becomes an input port.

If data is read from a pin configured as output, the value of the port latch is read rather than the value of this pin.

A pin configured as input becomes floating and its value can be read. If data is written to a pin, it is written to the port latch, but the pin remains floating.

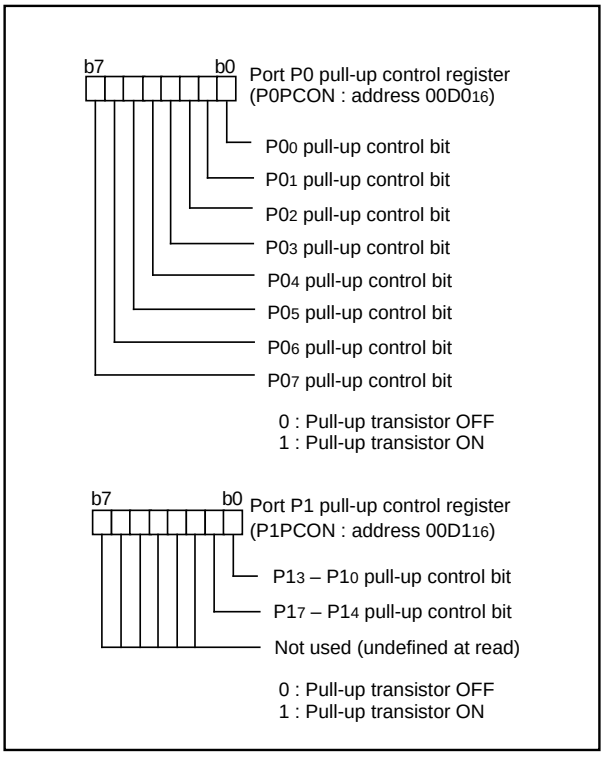


Fig. 10 Structure of pull-up control register

[Pull-up Control Registers]

Ports P0 and P1 are provided with a programmable pull-up transistor. When "1" is written to the pull-up control register and the direction register is in the input mode, the pull-up transistor turns on, and the port is pulled up.

■ Notes on Use for STP Instruction

When the 7480/7481 group is executing an STP instruction, apply 0 V or the same voltage as Vcc to the following pins.

If an intermediate voltage is applied to these pins, a through-current flows to the input gates and the power current increases.

P4, P5, P3, P16, P14

[Port P4P5 Input Control Register]

When ports P42, P43 and P5 of the 7481 group are selected for input, clear the corresponding direction register to "0" and set "1" to the corresponding bit of the port P4P5 input control register.

Ports P42, P43 and P5 are not included in the 7480 group. Fix each bit of the port P4P5 input control register to "0".

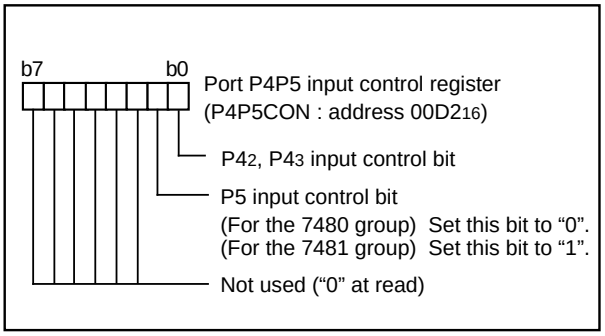
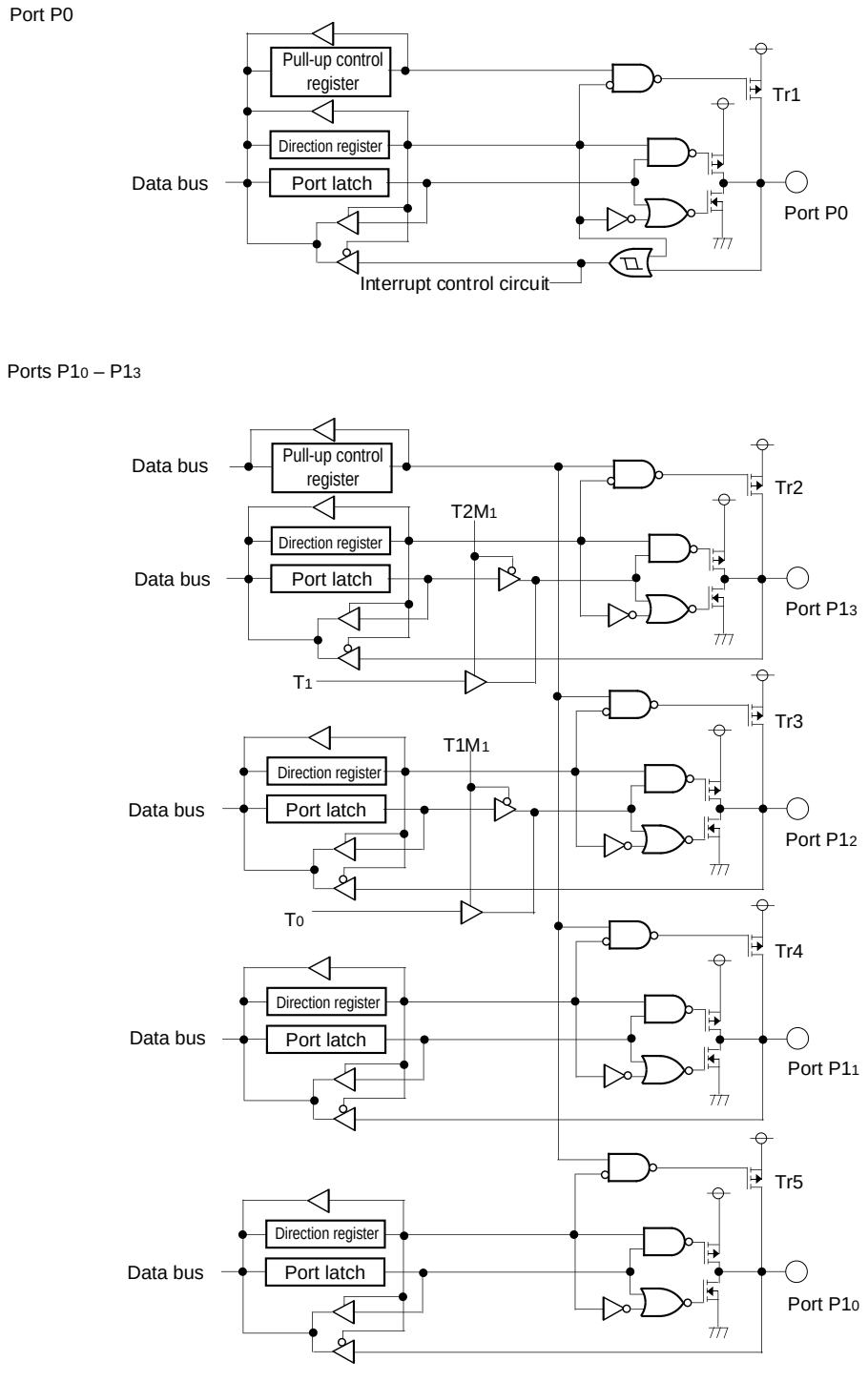
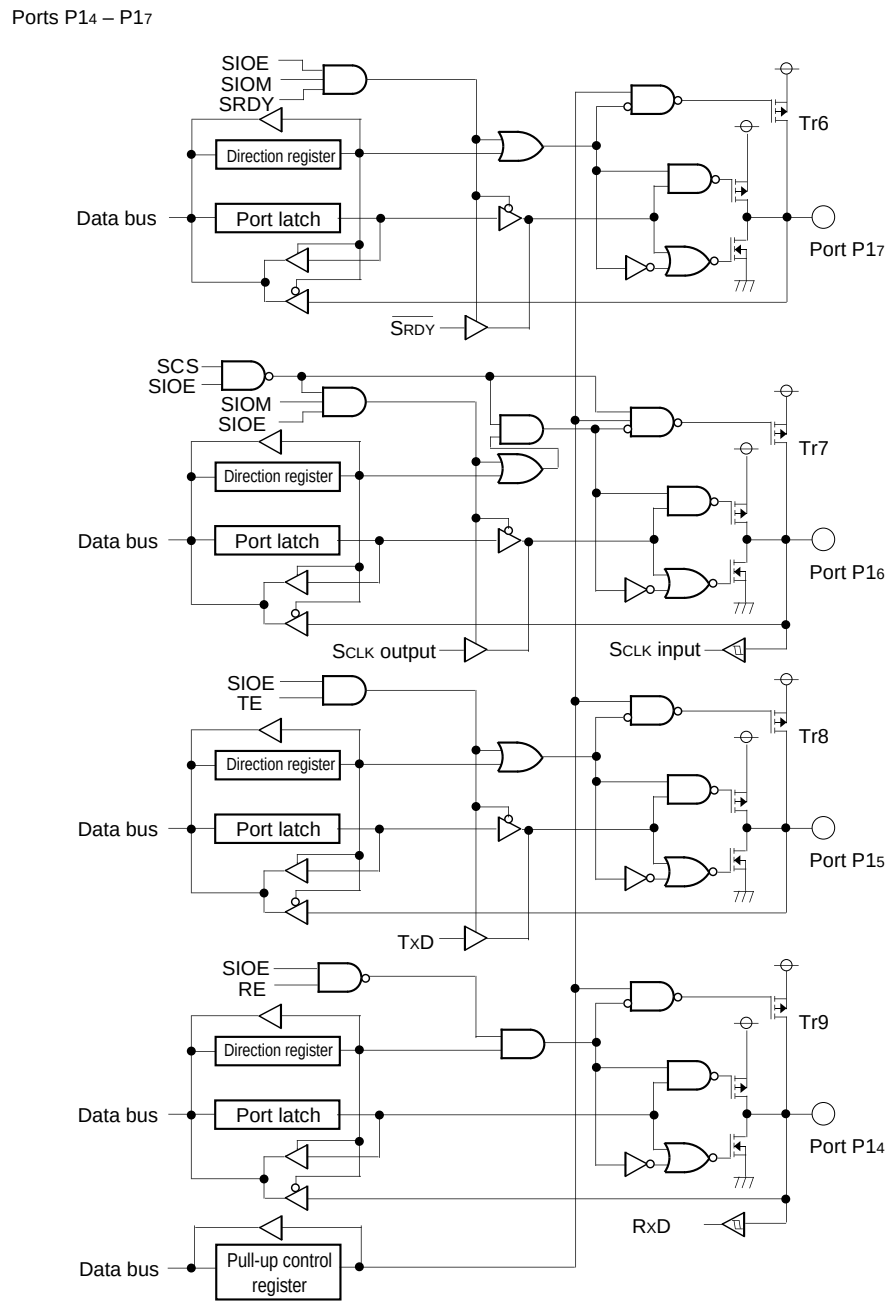


Fig. 11 Structure of port P4P5 input control register



Tr1 to Tr5 are pull-up transistors.

Fig. 12 Block diagram of ports (1)



Tr6 to Tr9 are pull-up transistors.

Fig. 13 Block diagram of ports (2)

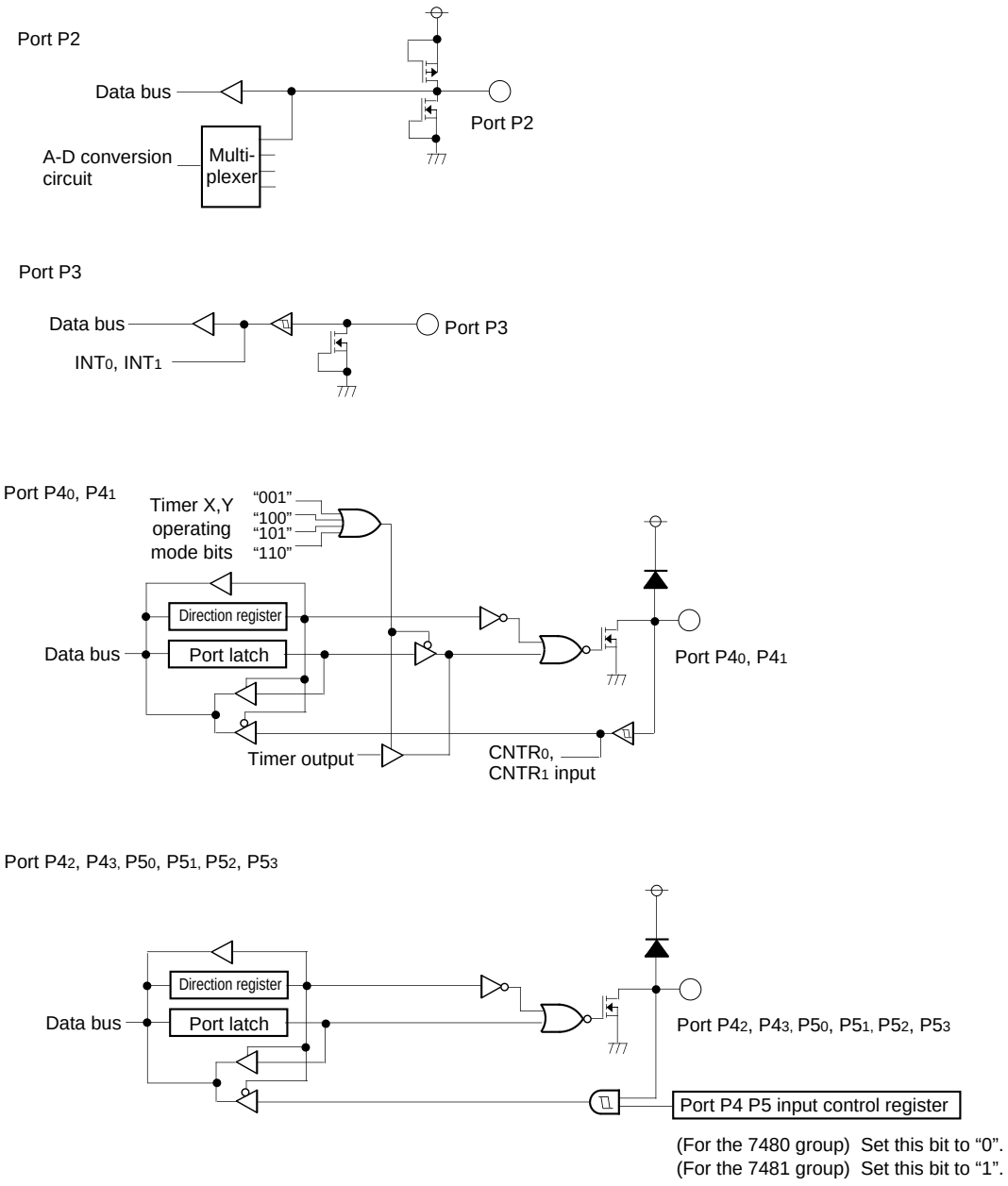


Fig. 14 Block diagram of ports (3)

Interrupts

Interrupts are vectored interrupts, and they can be caused by 14 different sources: 5 external sources, 8 internal sources, and 1 software source.

(1) Interrupt Control

All interrupts, except the BRK instruction interrupt, have an interrupt request bit and an interrupt enable bit. Additionally, a global interrupt disable flag affects them.

When the interrupt enable bit and the interrupt request bit are set to "1" and the interrupt disable flag is set to "0", an interrupt is accepted.

The interrupt request bits can be cleared by the program but cannot be set. The interrupt enable bit can be set and cleared by the program.

The reset and BRK instruction interrupt can never be disabled. Other interrupts are disabled when the interrupt disable flag is set.

(2) Interrupt Operation

When an interrupt request is accepted:

1. The contents of the program counter and the processor status register are automatically pushed into the stack.
2. The interrupt disable flag is set and the interrupt request bit is cleared.
3. The interrupt jump destination address is read into the program counter.

■ **Notes**

- When the active edge of an external interrupt (INT_0, INT_1, $CNTR_0$, $CNTR_1$) is set, the interrupt request bit may also be set. Therefore, disable the external interrupt and set the edge polarity selection register. Then clear the interrupt request bit and accept the external interrupt.
- Input a trigger width over 250 ns to the INT_0/INT_1 pin.

Table 4. Interrupt vector addresses and priority

Interrupt source	Priority	Vector address (Note 1)		Interrupt request generating conditions	Remarks
		High-order	Low-order		
RESET (Note 2)	1	FFFF16	FFFE16	At reset	Non-maskable
INT0	2	FFFD16	FFFC16	At detection of either rising edge or falling edge of INT0 input	External interrupt (active edge programmable)
INT1	3	FFFB16	FFFA16	At detection of either rising edge or falling edge of INT1 input	External interrupt (active edge programmable)
Key-on wake-up				At input "L" to port P0 in key-on wake-up mode	Validity after execution of STP/WIT instruction
CNTR0	4	FFF916	FFF816	At detection of either rising edge or falling edge of CNTR0 input	External interrupt (active edge programmable)
CNTR1	5	FFF716	FFF616	At detection of either rising edge or falling edge of CNTR1 input	External interrupt (active edge programmable)
Timer X	6	FFF516	FFF416	At timer X underflow	
Timer Y	7	FFF316	FFF216	At timer Y underflow	
Timer 1	8	FFF116	FFF016	At timer 1 underflow	
Timer 2	9	FFEF16	FFEE16	At timer 2 underflow	
Serial I/O reception	10	FFED16	FFEC16	At completion of serial I/O data reception	
Serial I/O transmission	11	FFEB16	FFEA16	At completion of serial I/O transfer shift or when transmission buffer is empty	
Bus arbitration	12	FFE916	FFE816	At detection of bus collision	
A-D conversion	13	FFE716	FFE616	At completion of A-D conversion	
BRK instruction	14	FFE516	FFE416	At execution of BRK instruction	Non-maskable software interrupt

Notes 1 : Vector addresses contain interrupt jump destination addresses.
2 : RESET is mentioned in the table because its operation is the same as an interrupt.

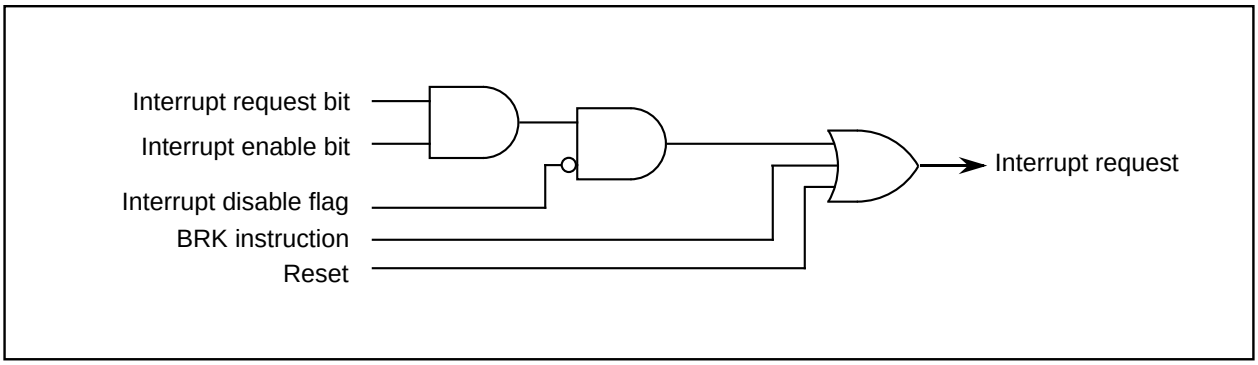


Fig. 15 Interrupt control diagram

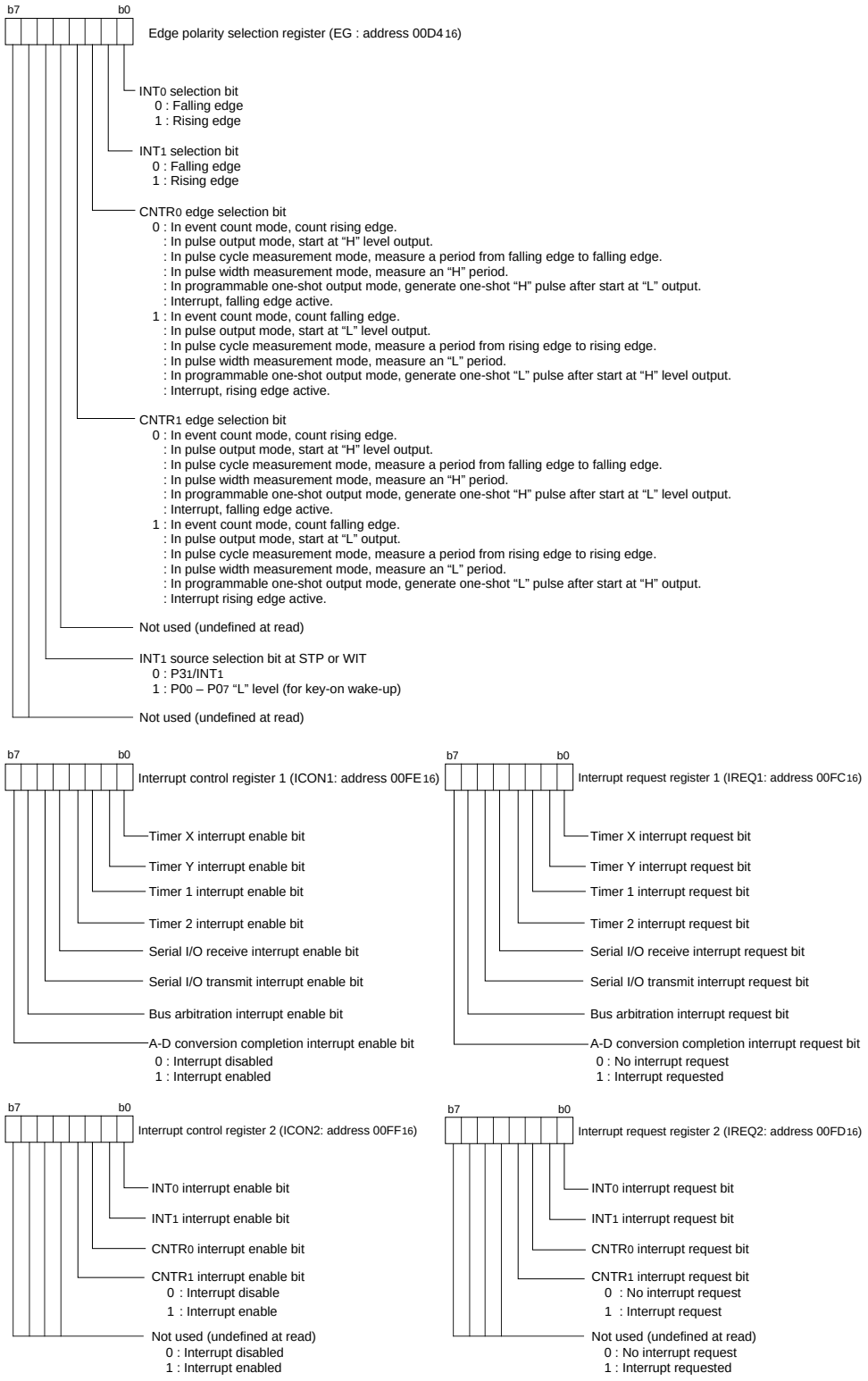


Fig. 16 Structure of registers related to interrupts

Timers

The 7480/7481 group has two 16-bit timers (timer X and timer Y), and two 8-bit timers (timer 1 and timer 2).

All the timers are of a count-down type. When the timer reaches "FF16" or "000016", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to this timer is set to "1".

At reading and setting the timer value to a 16-bit timer, be sure to read and set both high-order byte and low-order byte.

At reading the count value from a 16-bit timer, read the high-order byte and the low-order byte in this order. At setting the count value in a 16-bit timer, set the low-order byte and the high-order byte in this order.

The 16-bit timer cannot operate normally at reading during set operation or at setting during read operation.

● Timer X, Timer Y

Both timer X and timer Y are 16-bit timers independent from each other. They can select 7 operating modes by setting the mode registers. The registers related to timer X and timer Y are shown below. In the following, abbreviations will be used as register names.

- Timer XY control register (TXYCON: address 00F816)
- Port P4 direction register (P4D: address 00C916)
- Timer X low-order (TXL: address 00F016)
- Timer X high-order (TXH: address 00F116)
- Timer Y low-order (TYL: address 00F216)
- Timer Y high-order (TYH: address 00F316)
- Timer X mode register (TXM: address 00F616)
- Timer Y mode register (TYM: address 00F716)
- Edge polarity selection register (EG: address 00D416)
- Interrupt request register 1 (IREQ1: address 00FC16)
- Interrupt request register 2 (IREQ2: address 00FD16)
- Interrupt control register 1 (ICON1: address 00FE16)
- Interrupt control register 2 (ICON2: address 00FF16)

For register structures, refer to each register structural diagram.

In the following, each mode will be described.

(1) Timer Mode/Event Count Mode

① Timer Mode

● Mode Selection

This mode is selected by setting "000" in the timer X operating mode bits (b2b1b0) of TXM and the timer Y operating mode bits (b2b1b0) of TYM.

● Count Source Selection

The count source is f(XIN)/2, f(XIN)/8 or f(XIN)/16.

● Interrupt

When a timer underflows, the timer X interrupt request bit (b0) or timer Y interrupt request bit (b1) of IREQ1 is set to "1".

● Explanation of Operation

After reset release, the timer X stop control bit (b0) or timer Y stop control bit (b1) of TXYCON is "1", and the timer stops.

In the timer stop status, usually the timer value is set by writing the latch and timer at the same time. Timer operation is started by setting "0" in b0 or b1 of TXYCON.

When the timer reaches "000016", an underflow occurs at the next count pulse, the corresponding timer latch is reloaded into the timer, and the count is continued. To change the timer value during count operation, the latch value is changed by writing to the latch only. At the next underflow reloading, the timer value is changed.

② Event Count Mode

● Mode Selection

Select the timer event count mode. This mode is selected by inputting from the CNTR0 pin for timer X or from the CNTR1 pin for timer Y (setting "11" in b7 and b6 of TXM or "11" in b7 and b6 of TYM). The count operation active edge is selected by setting in the CNTR0 edge selection bit (b2) or the CNTR1 edge selection bit (b3) of EG. At "0", the rising edge is counted.

At "1", the falling edge is counted.

● Interrupt

The underflow interrupt is the same as the timer mode.

● Explanation of Operation

This operation is the same as that of the timer mode. In this mode, set the port in common with the CNTR0/CNTR1 pin as an input port.

Figure 19 shows a timing diagram in the timer event count mode.

(2) Pulse Output Mode

● Mode Selection

This mode is selected by setting b2, b1 and b0 of TXM or TYM to "001".

● Count Source Selection

The count source is f(XIN)/2, f(XIN)/8 or f(XIN)/16.

● Interrupt
The timer underflow interrupt is the same as the timer event count mode.

● Explanation of Operation
This operation is the same as the timer event count mode except that a timer outputs a pulse from the CNTR0/CNTR1 pin in which the polarity of output level is inverted at each timer underflow. When the CNTR0 edge selection bit (b2) or CNTR1 edge selection bit (b3) of EG is "0", the output of the CNTR0/CNTR1 pin is started with an "H" level output. When b2 or b3 of EG is "1", the output of this pin is started with an "L" level. In this mode, set the port in common with the CNTR0/CNTR1 pin as an output port.

■ **Note**

While a timer operation stops

The output level of the CNTR0/CNTR1 pin is initialized to the value set in the CNTR0 edge selection bit or CNTR1 edge selection bit by writing to the timer.

While a timer operation is enabled

The output level of the CNTR0/CNTR1 pin is inverted by changing the CNTR0 edge selection bit or CNTR1 edge selection bit.

Figure 20 shows a timing diagram in the pulse output mode.

(3) Pulse Cycle Measurement Mode

● Mode Selection
This mode is selected by setting b2, b1 and b0 of TXM or TYM to "010".

● Count Source Selection
The count source is f(XIN)/2, f(XIN)/8 or f(XIN)/16.

● Interrupt
The underflow interrupt is the same as the timer event count mode. Set b2 or b3 of IREQ2 to "1" as soon as the pulse cycle measurement is completed.

● Explanation of Operation

While a timer operation stops

Select a timer count source. Next, select a pulse cycle to be measured. When b2 or b3 of EG is "0", a timer counts a period from a falling edge to a falling edge of the CNTR0/CNTR1 pin input.

When b2 or b3 of EG is "1", a timer counts a period from a rising edge to a rising edge of the CNRT0/CNTR1 pin input.

While a timer operation is enabled

At setting b0 and b1 of TXYCON to "0", a timer starts to measure the pulse cycle, and starts to count down from the count value provided before measurement. When an active edge is detected at measurement completion or measurement start, 1's complement of the timer value is set to the timer latch and "FFFF16" is set in the timer.

When a timer underflows, a timer X or timer Y interrupt occurs, and "FFFF16" is set in the timer. A measurement value is held until the next measurement is completed. In this mode, set the port in common with the CNTR0/CNTR1 pin as an input port.

■ **Note**

The timer value cannot be read in this mode. A timer value can be set while a timer operation stops (no measurement).

Since the timer latch of this mode becomes read only, do not perform a write operation during measurement.

The timer is set to "FFFF16" only when the timer underflows or the active edge of pulse cycle measurement is detected.

Accordingly, the timer value at a start of measurement depends on the timer value provided before the start of measurement.

Figure 21 shows a timing diagram in the pulse cycle measurement mode.

(4) Pulse Width Measurement Mode

● Mode Selection
This mode is selected by setting b2, b1 and b0 of TXM or TYM to "011".

● Count Source Selection
The count source is f(XIN)/2, f(XIN)/8 or f(XIN)/16.

● Interrupt
The underflow interrupt is the same as the timer event count mode. Set b2 or b3 of IREQ2 to "1" as soon as pulse width measurement is completed.

● Explanation of Operation

While a timer operation stops

Select a timer count source. Next, select a pulse width to be measured. A timer counts a period from a falling edge to a rising edge of the CNTR0/CNTR1 pin input ("L" period) when b2 or b3 of EG is "1". A timer counts a period from a rising edge to a falling edge of the CNTR0/CNTR1 pin input ("H" period) when b2 or b3 of EG is set to "0".

While a timer operation is enabled

At setting b0 and b1 of TXYCON to "0", a timer starts to measure a pulse width, and starts to count down from the count value provided before measurement. When the active edge is detected at measurement completion, 1's complement of the timer value is set in the timer latch. When the active edge is detected at measurement completion or measurement start, "FFFF16" is set in the timer. When a timer underflows, a timer X or timer Y interrupt occurs, and "FFFF16" is set in the timer.

A measurement value is held until the next measurement is completed. In this mode, set the port in common with the CNTR0/CNTR1 pin as an input port.

■ **Note**

The timer value cannot be read in this mode. A timer value can be set while a timer operation stops (not under pulse width measurement).

Since the timer latch of this mode becomes read only, do not perform a write operation during measurement.

The timer is set to "FFFF$_{16}$" only when a timer underflows or when the active edge of pulse width measurement is detected.

Accordingly, the timer value at a start of measurement depends on the timer value provided before the start of measurement.

Figure 22 shows a timing diagram in the pulse width measurement mode.

(5) Programmable Waveform Generation Mode

● Mode Selection

This mode is selected by setting b2, b1 and b0 of TXM or TYM to "100".

● Count Source Selection

The count source is f(XIN)/2, f(XIN)/8 or f(XIN)/16.

● Interrupt

The underflow interrupt is the same as the timer event count mode. The INT0 interrupt request bit (b0) or INT1 interrupt request bit (b1) of IREQ2 is set to "1" by detecting an active edge of the INT pin.

● Explanation of Operation

This operation is the same as that of the timer event count mode, except that a timer outputs the level of the value set in the output level latch (b4) of TXM or TYM from the CNTR0/CNTR1 pin each time the timer underflows. After the timer underflows, if the values of the output level latch and timer latch are changed, the timer can output an optional waveform from the CNTR0/CNTR1 pin. In this mode, set the port in common with the CNTR0/CNTR1 pin as an output port.

In this mode, if the trigger selection bit of TXM or TYM is set to "1" and the count stop control bit of TXYCON is set to "0" (count operation), a timer can be started concurrently with the occurrence of a trigger (input signal of INT0/INT1 pin).

A timer starting trigger is set in the INT0 edge selection bit (b0) or INT1 edge selection bit (b1) of EG. At "0", the falling edge is active. At "1", the rising edge is active. When the count stop control bit is "1" (count status), a timer is not started at the occurrence of a trigger.

Figure 23 shows a timing diagram in the programmable waveform generation mode.

(6) Programmable One-Shot Output Mode

● Mode Selection

This mode is selected by setting b2, b1 and b0 of TXM or TYM to "101".

● Count Source Selection

The count source is f(XIN)/2, f(XIN)/8 or f(XIN)/16.

● Interrupt

The underflow interrupt is the same as the timer event count mode. One-shot output trigger is set in the INT0 edge selection bit (b0) or INT1 edge selection bit (b1) of EG. At "0", the falling edge is active. At "1", the rising edge is active. The INT0 interrupt request bit (b0) or INT1 interrupt request bit (b1) of IREQ2 is set to "1" by detecting an active edge of the INT pin.

● Explanation of Operation

① In case of One-shot Output "H"

(b2, b3 of EG = "0")

While a timer operation stops

The output level of the CNTR0/CNTR1 pin is initialized to "L" at mode selection. Set the one-shot width in TXH, TXL, TYH and TYL. While a timer operation stops, a trigger (input signal of INT0/INT1 pin) cannot occur.

While a timer operation is enabled

At detecting a trigger, a timer outputs "H" from the CNTR0/CNTR1 pin, and outputs "L" at a timer underflow.

② In Case of One-shot Output "L"

(b2, b3 of EG = "1")

While a timer operation stops

The output level of the CNTR0/CNTR1 pin is initialized to "H" at mode selection. Set the one-shot width in TXH, TXL, TYH and TYL. While a timer operation stops, a trigger (input signal of the INT0/INT1 pin) cannot occur.

While a timer operation is enabled

At the detection of a trigger, a timer outputs "L" from the CNTR0/CNTR1 pin and outputs "H" at a timer underflow.

In this mode, set the port in common with the CNTR0/CNTR1 pin as an output port.

■ **Note**

● Input a trigger width over 250 ns to the INT0/INT1 pin.

● If the value of the CNTR0 edge selection bit or CNTR1 edge selection bit is changed while one-shot output is enabled or one-shot output occurs, the output level from the CNTR0/CNTR1 pin changes.

Figure 24 shows a timing diagram in the programmable one-shot output mode.

(7) PWM Mode

● Mode Selection
This mode is selected by setting b2, b1 and b0 of TXM or TYM to "110".

● Count Source Selection
The count source is f(XIN)/2, f(XIN)/8 or f(XIN)/16.

● Interrupt
At the rising edge of the CNTR0/CNTR1 output, set the timer X interrupt request bit (b0) or timer Y interrupt request bit (b1) of IREQ1 to "1".

● Explanation of Operation
In the case of timer X, the PWM waveform is output from the CNTR0 pin. In the case of timer Y, the PWM waveform is output from the CNTR1 pin.
The PWM waveform "H" period is determined by the setting value n (n=0 to 255) of TXH or TYH. The "L" period is determined by the setting value m (m=0 to 255) of TXL or TYL.
The PWM cycle is as follows:

PWM cycle = (n + m) × ts

$$\text{PWM output duty} = \frac{n}{(n + m)}$$

ts: Timer X/timer Y count source cycle

While a timer operation stops
The timer value is set in TXL, TXH, TYL and TYH by writing to the timer and timer latch at the same time. The output of the CNTR0/CNTR1 pin is initialized to "H" by setting this timer value.

While a timer operation is enabled
When b1 and b0 of TXYCON are set to "0", "H" is output during the period of the setting value of TXH or TYH. After that, "L" is output during the period of the setting value of TXL or TYL.
Then, these operations will be repeated. The PWM output subsequent to an underflow can be changed by setting the timer value in TXL, TXH, TYL, TYH by writing only to the timer latch.
In this mode, set the port in common with the CNTR0/CNTR1 pin as an output port.

■ **Note**

● When the PWM "H" period is set to "00$_{16}$", the PWM output is always "L" level.

● When the PWM "L" period is set to "00$_{16}$", the PWM output is always "H" level.

● When the PWM "H" period is set to "00$_{16}$" and the "L" period is set to "00$_{16}$", the PWM output is always "L" level.

● When at least one of the PWM "H" period and "L" period is set to "00$_{16}$", a timer X interrupt request/timer Y interrupt request does not occur.

● When the timer latch is set at "00$_{16}$", the timer counts down, so its value is not constant.
Figure 25 shows a timing diagram in the PWM mode.

■ **Note on All Modes**

● Write Control for Timer X, Timer Y
Timer X and timer Y can select either writing to both timer latch and timer or writing only to the timer latch by b3 of TXM or TYM.
At writing only to the timer latch, a value is set in the timer latch by writing the value in the timer X/timer Y address, so the timer is updated at the next underflow. After reset release, writing to both the timer latch and timer is selected.
At this status, when a value is written in the timer X/timer Y address, the value is set in both the timer and timer latch at the same time.
At writing only to the timer latch, when the write timing for the timer latch is almost equal to the underflow timing, the value that is set in the timer may not be constant.

● Read Control for Timer X/Timer Y
When the pulse cycle measurement mode or pulse width measurement mode is selected, the timer value cannot be read out. In the other modes, the timer value can be read regardless of count operation and count stop. However, the timer latch value cannot be read out.

● Note on CNTR0, CNTR1, INT0, INT1 Interrupt Polarity Selection
When the CNTR0/CNTR1 edge selection bit or INT0/INT1 interrupt edge selection bit is set, this affects the respective interrupt polarity.

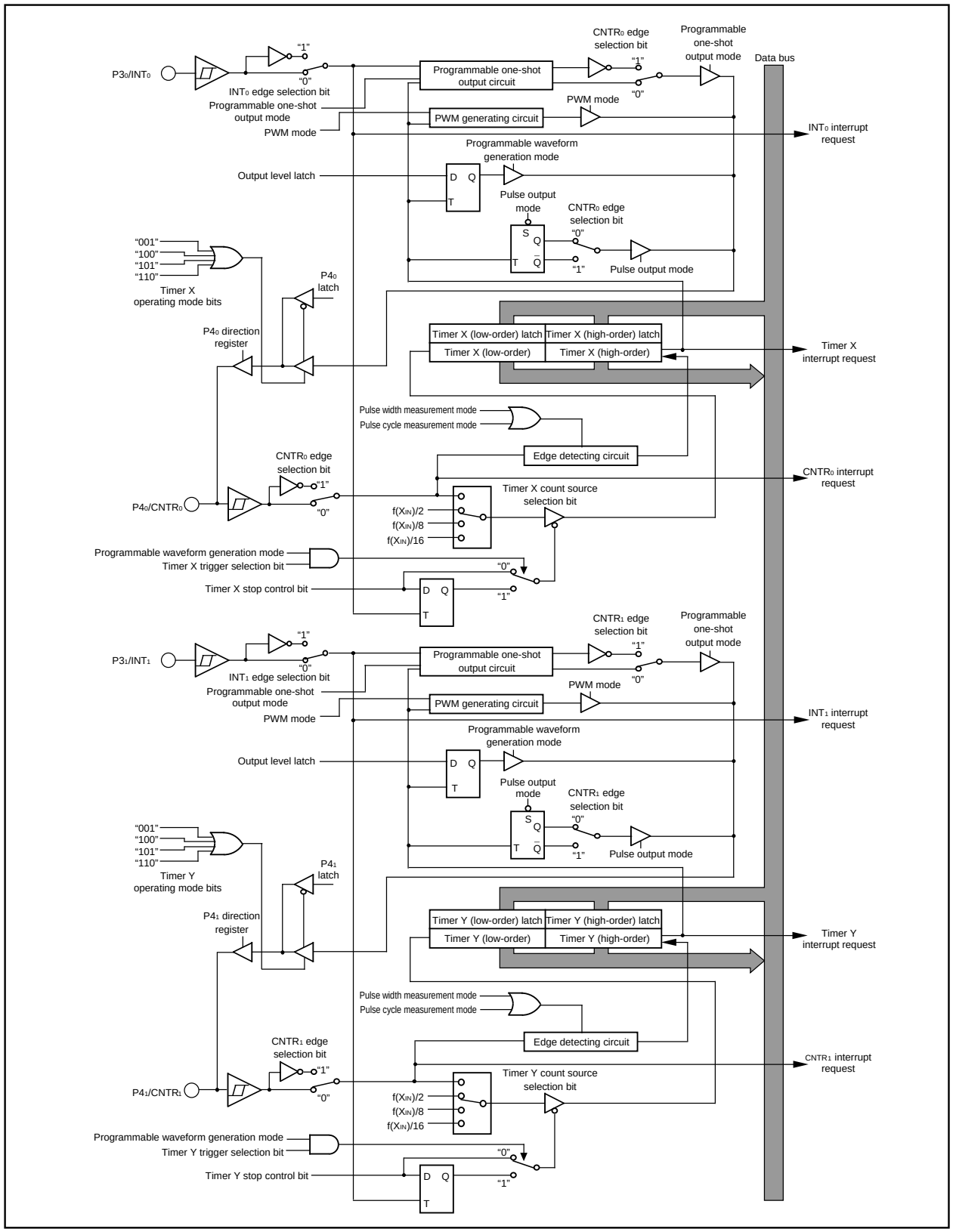


Fig. 17 Block diagram of timer X and timer Y

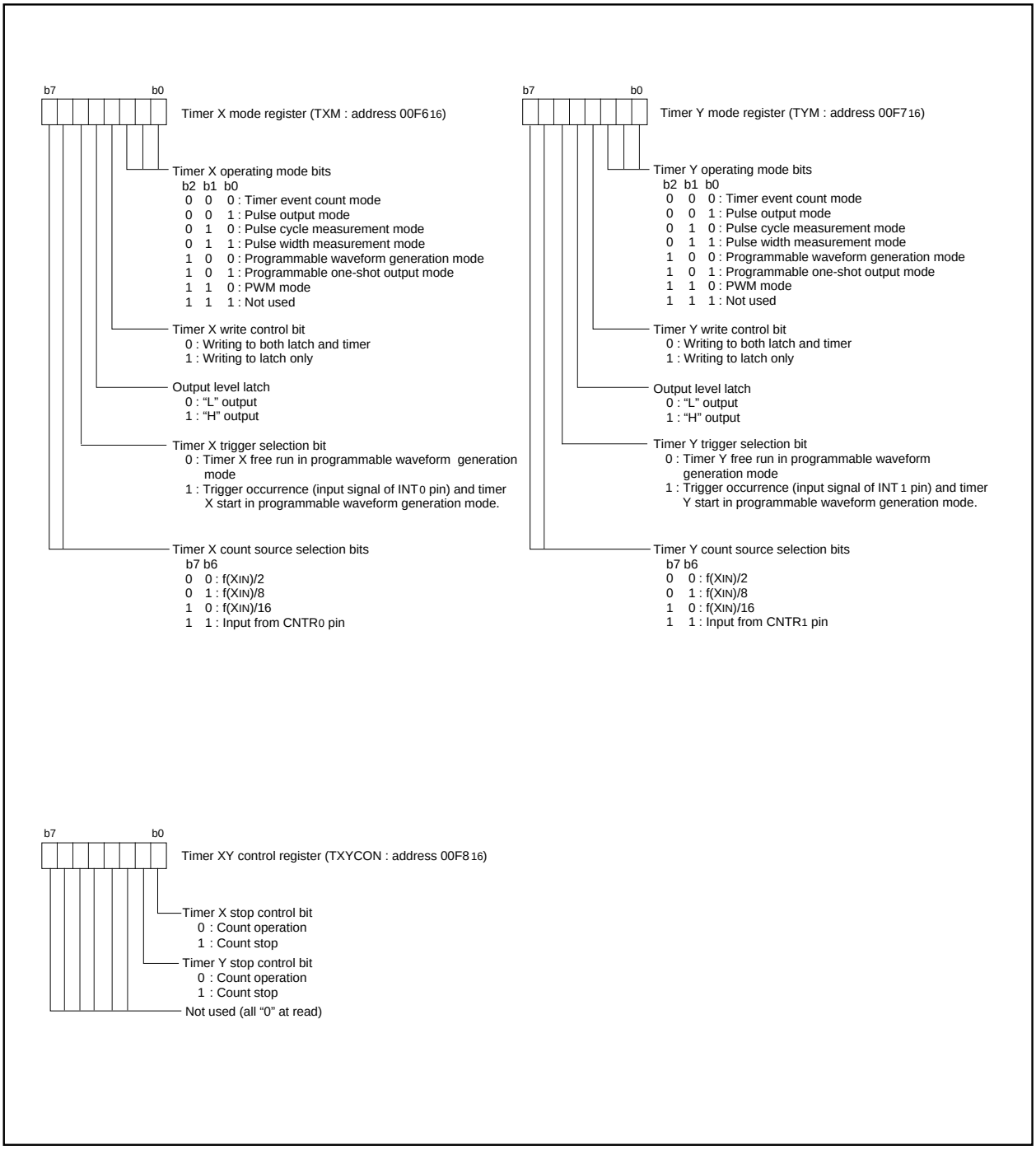


Fig. 18 Structure of timer X/timer Y mode register and timer XY control register

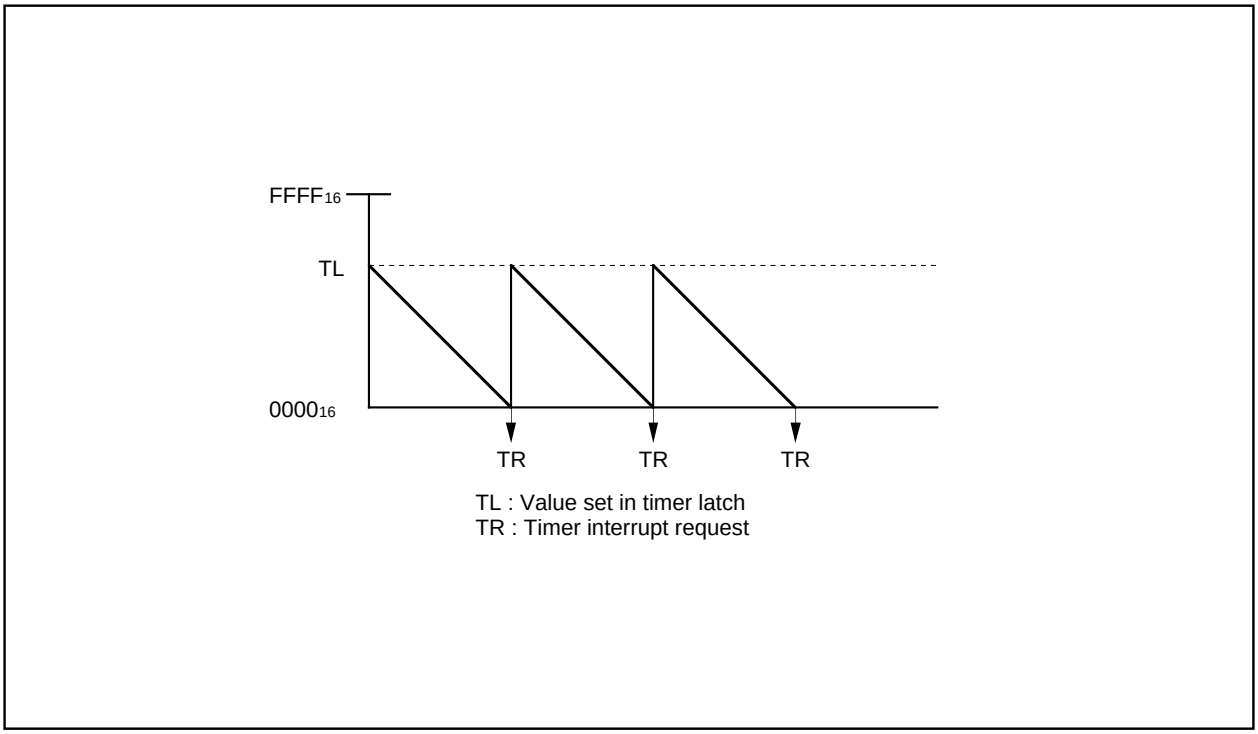


Fig. 19 Timing diagram in timer mode/event count mode

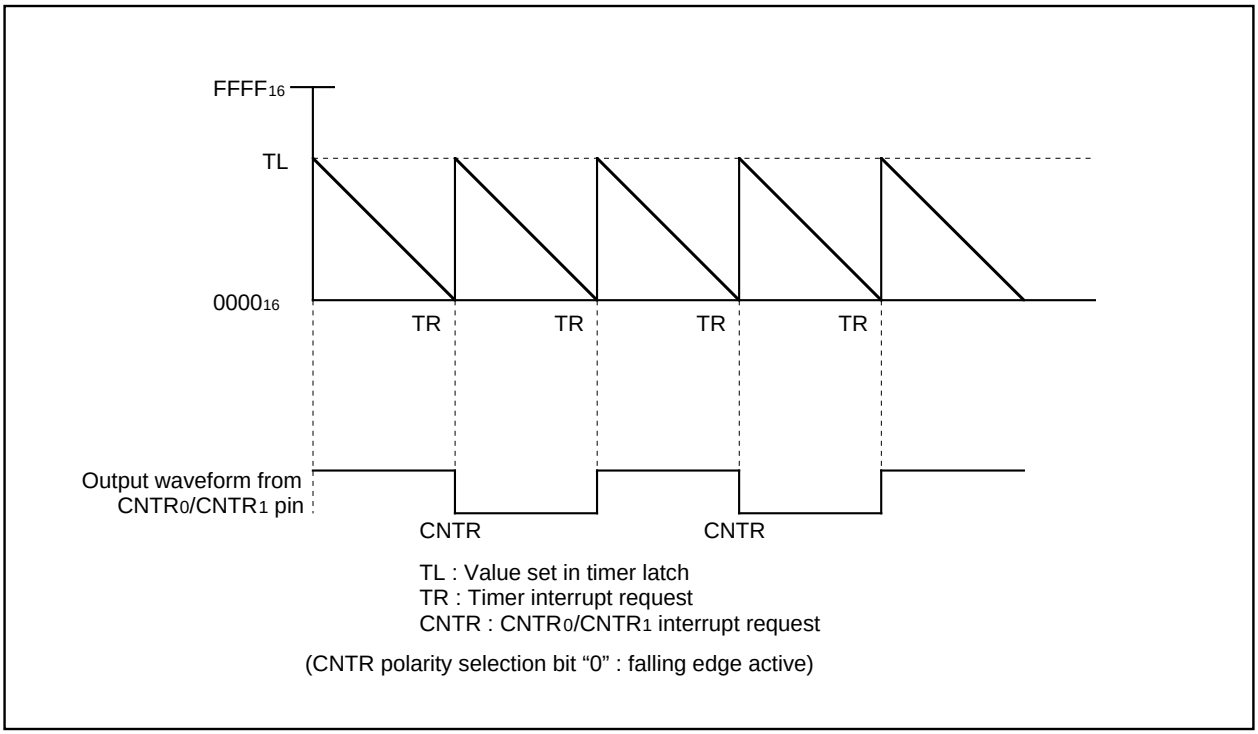


Fig. 20 Timing diagram in pulse output mode

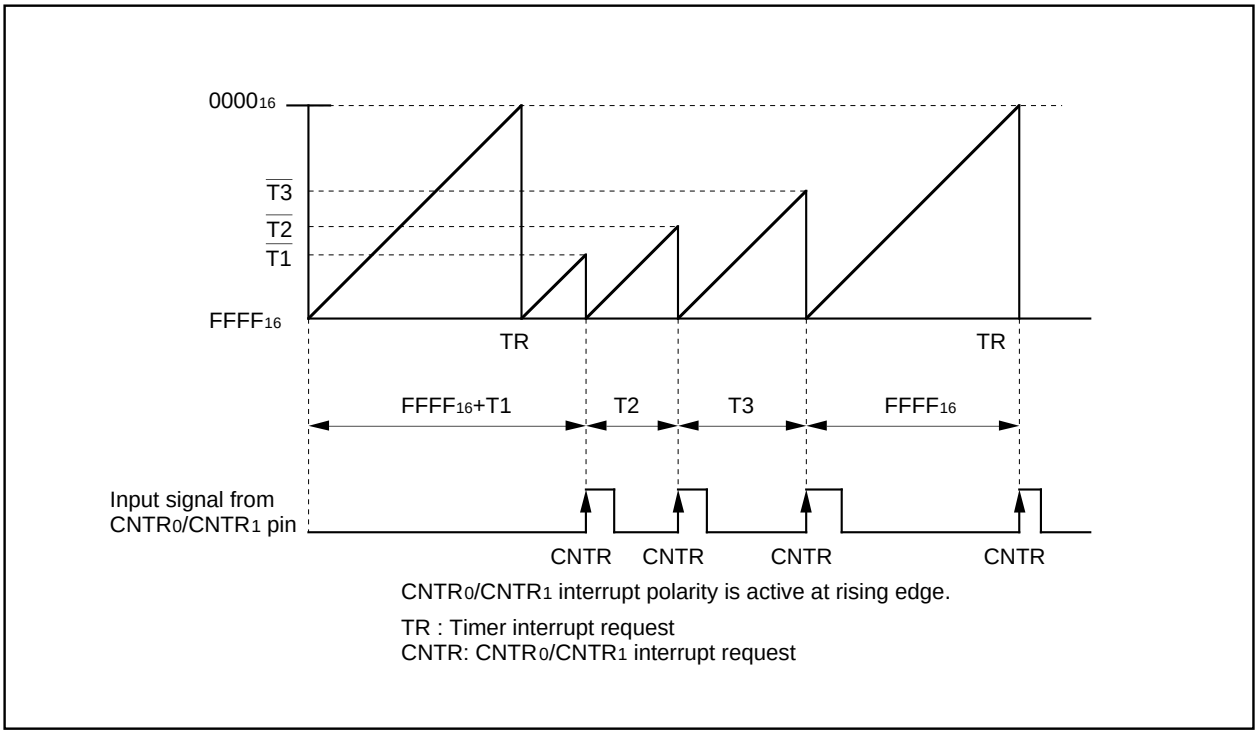


Fig. 21 Timing diagram in pulse cycle measurement mode (at "rising edge interval" measurement)

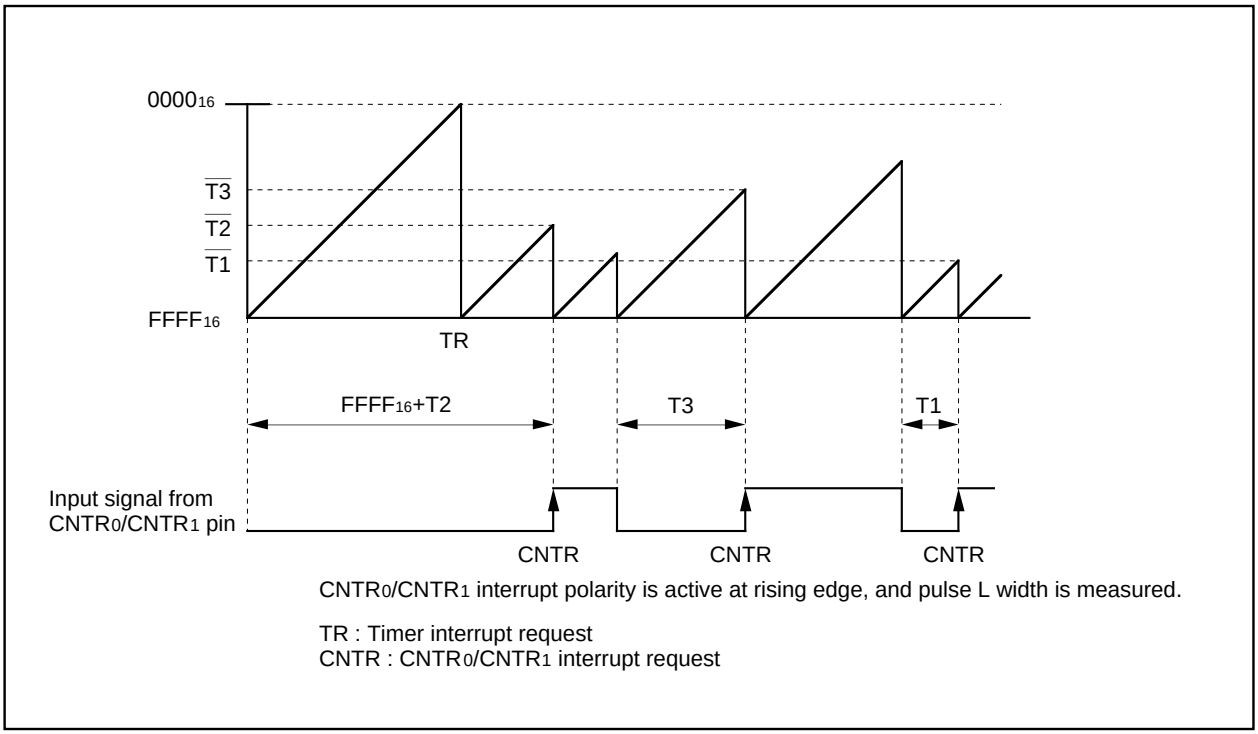
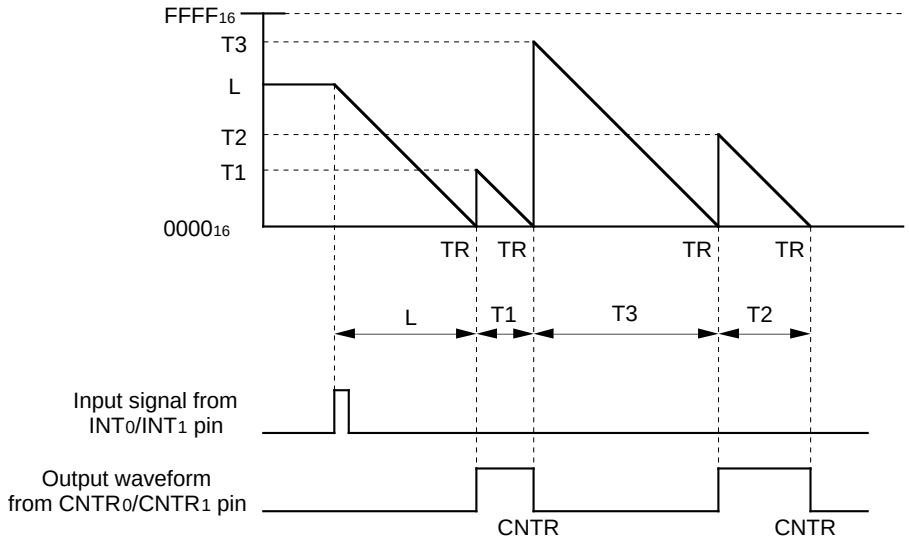


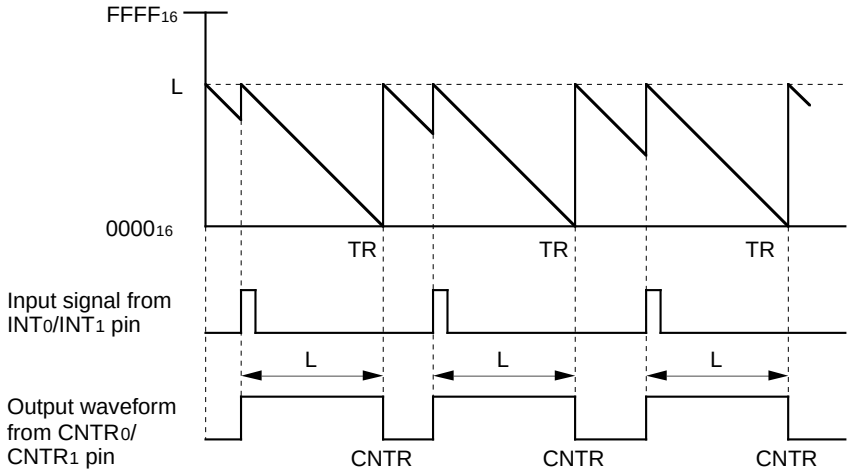
Fig. 22 Timing diagram in pulse width measurement mode (at "L section" measurement)



L : Initial value of TLH, TLL
TR : Timer interrupt request
CNTR : CNTR0/CNTR1 interrupt request

(CNTR polarity selection bit "0" : falling edge active)

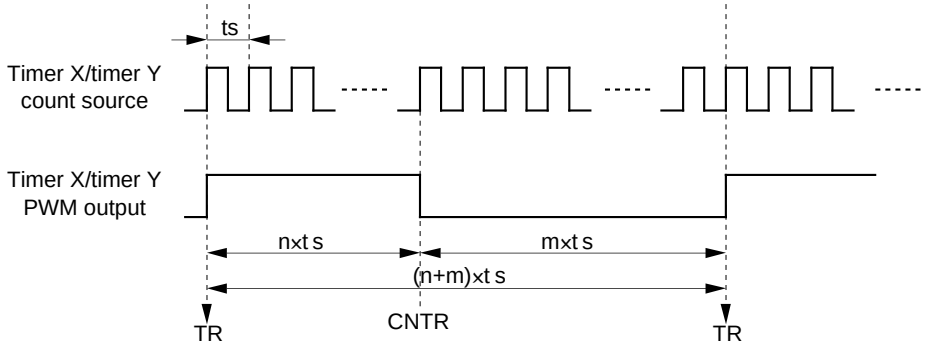
Fig. 23 Timing diagram in programmable waveform generation mode (when trigger selection bit = "1")



L : One-shot pulse width
TR : Timer interrupt request
CNTR : CNTR0/CNTR1 interrupt request

(CNTR polarity selection bit "0" : falling edge active)

Fig. 24 Timing diagram in programmable one-shot output mode



CNTR : CNTR0/CNTR1 interrupt request
(CNTR polarity selection bit "0" : falling edge active)

TR : Timer interrupt

Note : A PWM waveform with duty n/(n+m) and cycle (n+m) × ts is output.
- TXH/TYH setting value: n= 0 – 255
- TXL/TYL setting value: m = 0 – 255
- Timer X/timer Y count source cycle: ts
- n+m = 0 – 510

Fig. 25 Timing diagram in PWM mode

● Timers 1 and 2

Timer 1 and timer 2 are the 8-bit timers. They can select the following 2 modes by setting timer 1 mode register and timer 2 mode register.

- Timer mode
- Programmable waveform generation mode

When the count source is changed, set it again as the timer value may go wrong.

(1) Timer Mode

The frequency of f(XIN)/8, f(XIN)/64, f(XIN)/128 or f(XIN)/256 is counted.

(2) Programmable Waveform Generation Mode

This operation is the same as the timer mode, except that a timer outputs the level of the value set in the output level latch of the timer 1 mode register/timer 2 mode register from the T0 or T1 pin each time a timer underflows.

After the timer underflows, the timer can output an optional waveform from the T0 or T1 pin if the values of the output level latch and timer latch are changed.

In this mode, set the port in common with the T0/T1 pin as an output port.

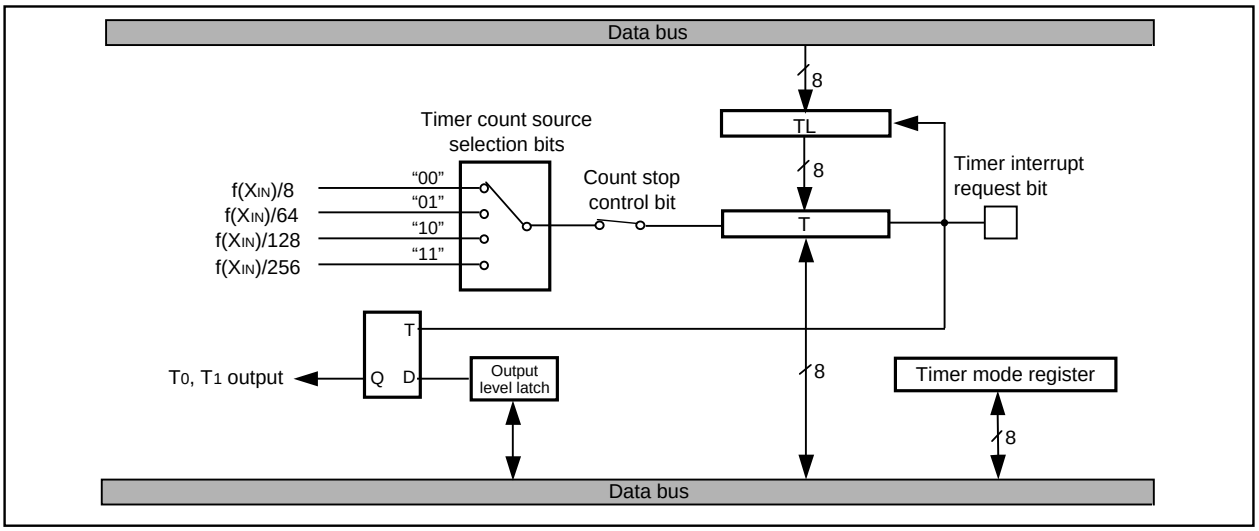


Fig. 26 Block diagram of timer 1, timer 2

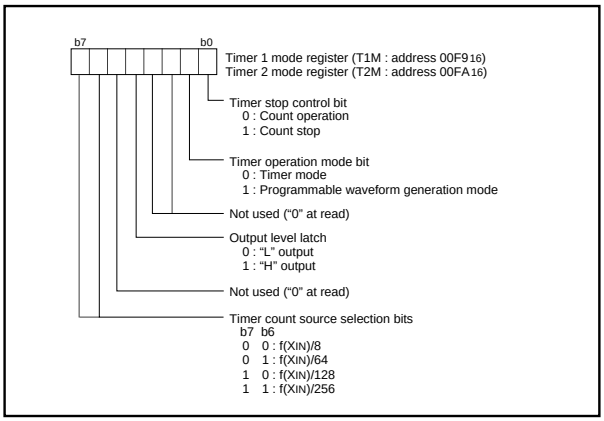


Fig. 27 Structure of timer 1/timer 2 mode register

Serial I/O

Serial I/O can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer (baud rate generator) is also provided for baud rate generation when serial I/O is in operation.

(1) Clock Synchronous Serial I/O Mode

The clock synchronous serial I/O mode can be selected by setting the serial I/O mode selection bit of the serial I/O control register (address $00E2_{16}$) to "1".

In the clock synchronous serial I/O, the transmitter-side microcomputer and the receiver-side microcomputer must use the same clock for serial I/O operation. If an internal clock is used as operating clock, a transfer is started by a write signal to the transmit/receive buffer register.

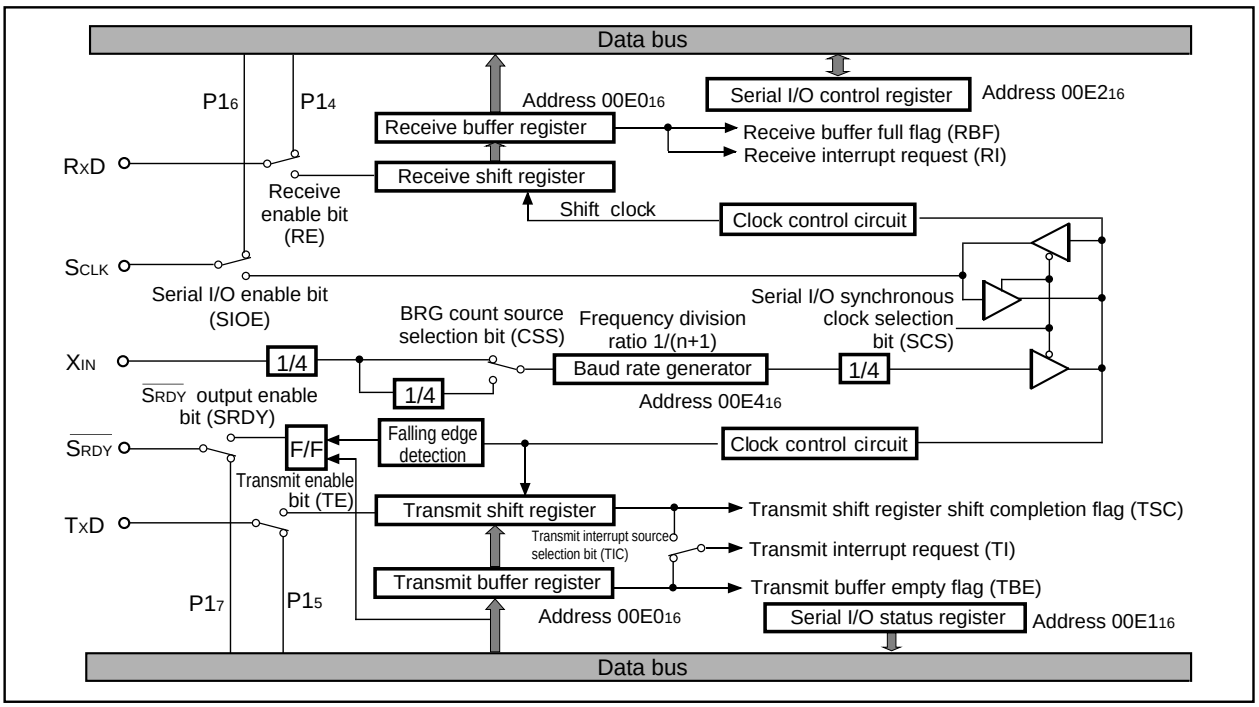
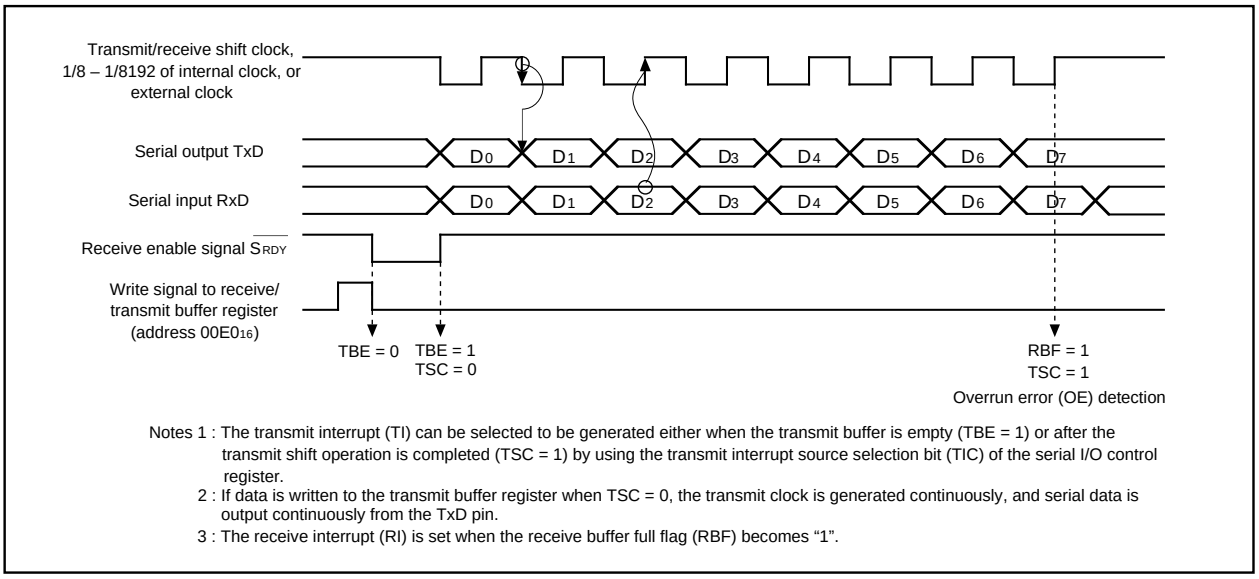


Fig. 28 Block diagram of clock synchronous serial I/O



Notes 1 : The transmit interrupt (TI) can be selected to be generated either when the transmit buffer is empty (TBE = 1) or after the transmit shift operation is completed (TSC = 1) by using the transmit interrupt source selection bit (TIC) of the serial I/O control register.
2 : If data is written to the transmit buffer register when TSC = 0, the transmit clock is generated continuously, and serial data is output continuously from the TxD pin.
3 : The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes "1".

Fig. 29 Operation of clock synchronous serial I/O function

(2) Asynchronous Serial I/O (UART) Mode

The UART mode can be selected by clearing the serial I/O mode selection bit of the serial I/O control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats to be used by a transmitter and a receiver must be identical.

Each of the transmit and receive registers has a buffer register (the same address on memory). Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register and receive data is read from the receive buffer register. These buffer registers can also hold the next data to be transmitted and receive 2-byte receive data in succession.

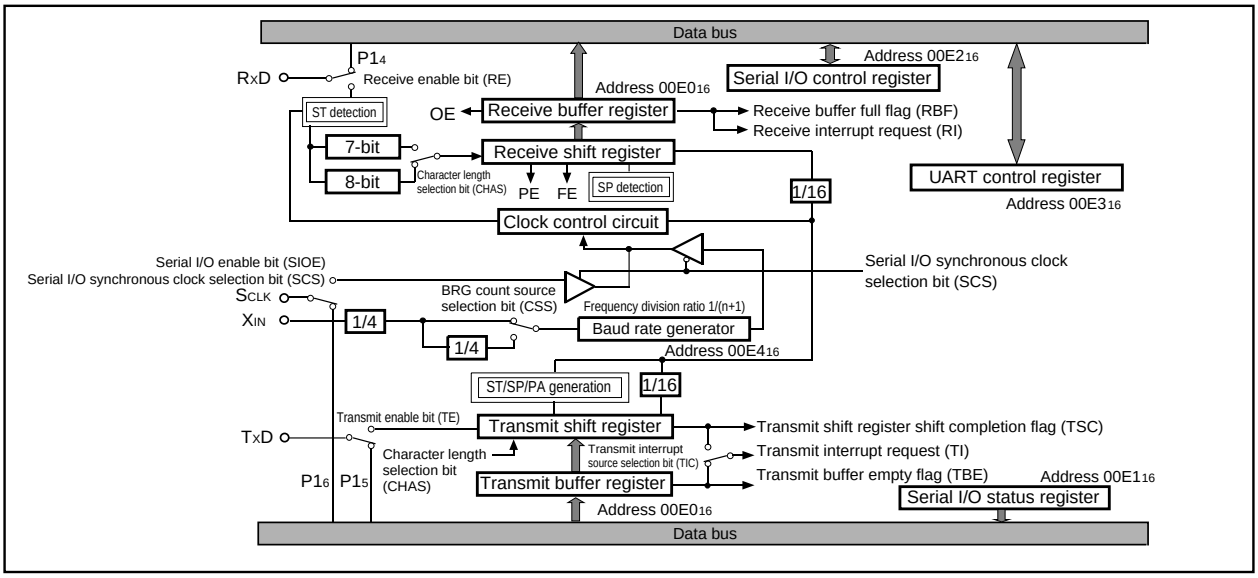
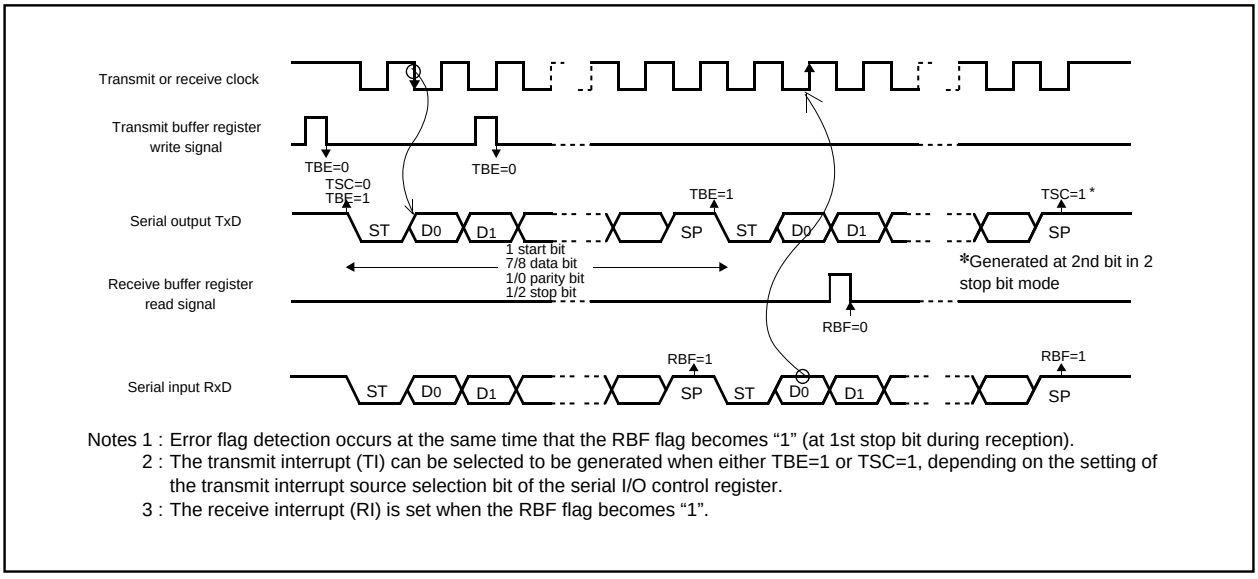


Fig. 30 Block diagram of UART serial I/O



Notes 1 : Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit during reception).
2 : The transmit interrupt (TI) can be selected to be generated when either TBE=1 or TSC=1, depending on the setting of the transmit interrupt source selection bit of the serial I/O control register.
3 : The receive interrupt (RI) is set when the RBF flag becomes "1".

Fig. 31 Operation of UART serial I/O function

[Serial I/O Control Register] SIOCON

The serial I/O control register consists of 8 control bits for control of the serial I/O.

[UART Control Register] UARTCON

The UART control register is a 4-bit control register which is valid when UART is selected. This 4-bit control register sets a data format for serial data transfer.

[Serial I/O Status Register] SIOSTS

This is a 7-bit read-only register consisting of flags that indicate the serial I/O operating status and different error flags. The 3 bits of bit 4 to bit 6 are valid only in the UART mode.

The receive buffer full flag is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set.

Writing to the serial I/O status register clears all the error flags (OE, PE, FE, SE).

All the bits of this register are initialized to "0" at reset.

However, if the transmit enable bit of the serial I/O control register is set to "1", bit 2 and bit 0 become "1".

[Transmit Buffer Register/Receive Buffer Register] TB/RG

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer register is a write-only type and the receive buffer register is a read-only type.

If a character bit length is 7 bits, the MSB of the receive data stored in the receive buffer is "0".

[Baud Rate Generator] BRG

The baud rate generator determines a baud rate for serial transfer. The baud rate generator, being an 8-bit counter with a reload register, divides the frequency of the count source by 1/(n+1), where n is the value written to the baud rate generator.

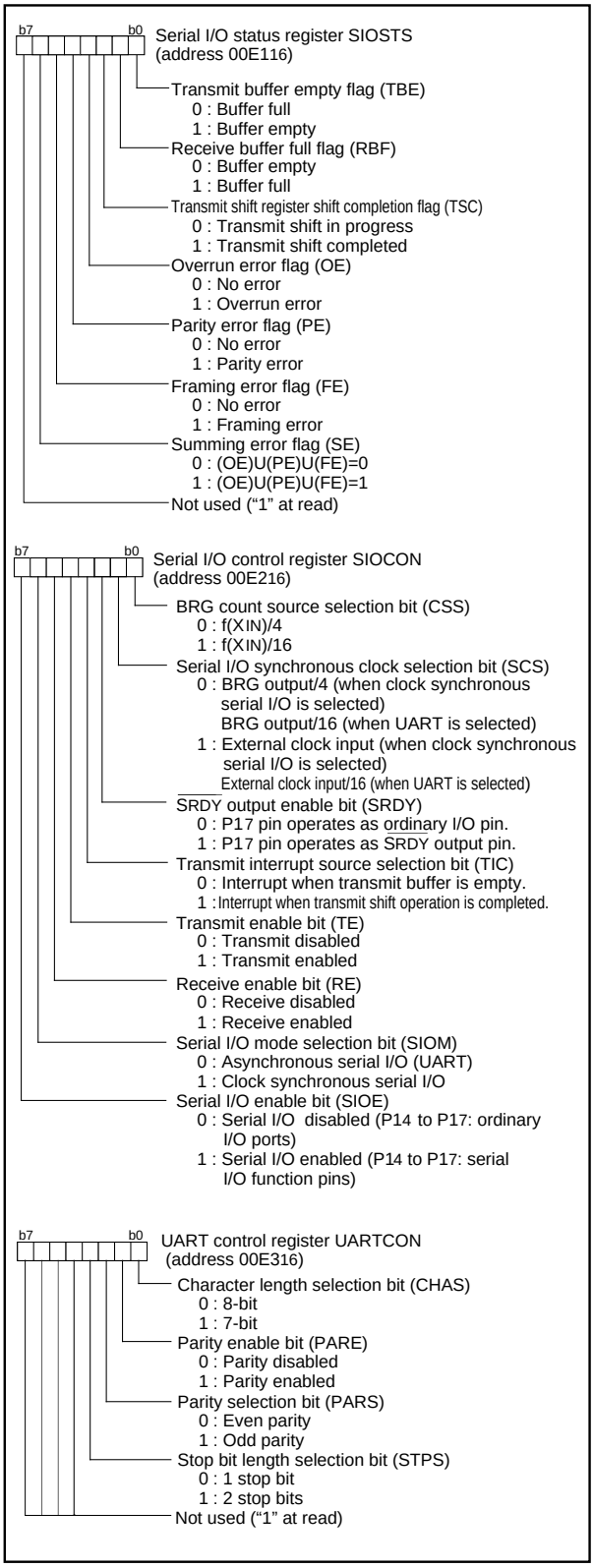


Fig. 32 Structure of serial I/O related registers (SIOSTS, UARTCON, SIOCON)

Bus Arbitration Interrupt

The 7480/7481 group is provided with a built-in bus arbitration interrupt as a function for bus conflict system communication.
At such bus conflict system communication, as shown in Figure 33, if transmit data cannot be transmitted to the LAN data bus due to a transmit data collision, the data collision can be detected by the bus arbitration interrupt.

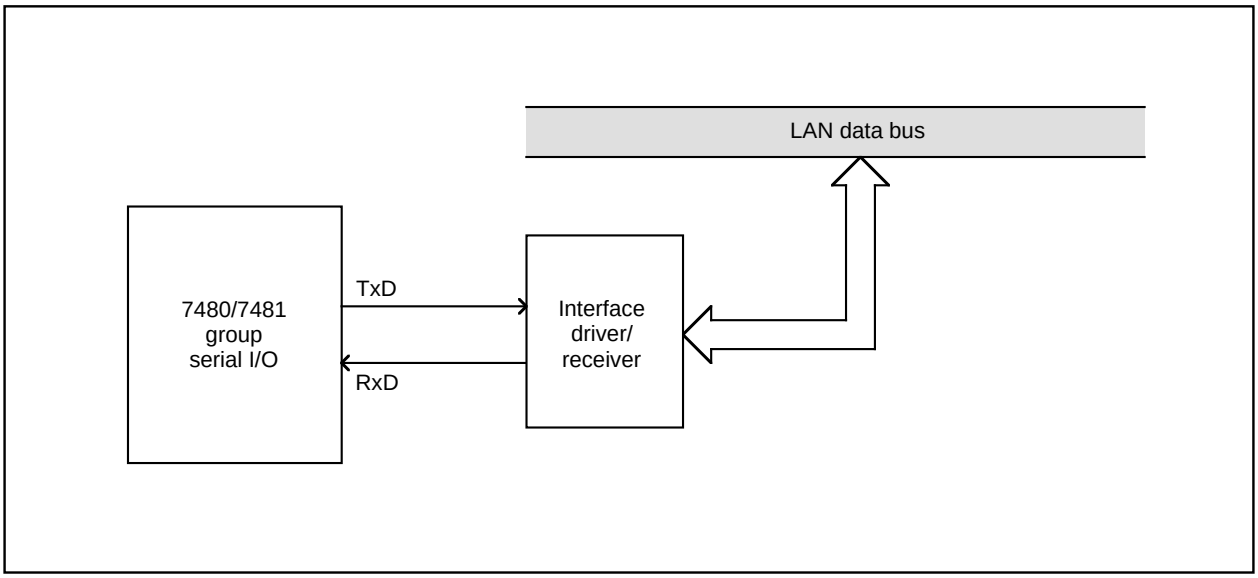


Fig. 33 Example of bus conflict system communication

Bus Collision Detection

The 7480/7481 group can detect a bus collision by setting the bus collision detection enable bit to “1”.

When transmission is started in the clock synchronous or asynchronous (UART) serial I/O mode, the transmit pin TxD is compared with the receive pin RxD in synchronization with a rising edge of transmit shift clock. If they do not coincide with each other, a bus arbitration interrupt request occurs (bus collision detection).

A transmit data collision is detected between LSB and MSB of transmit data in the clock synchronous serial I/O mode or between the start bit and stop bit of transmit data in the UART mode. Bus collision detection can be performed by both the internal clock and the external clock.

A block diagram is shown in Figure 34. A timing diagram is shown in Figure 35. A bus collision detection control register is shown in Figure 36.

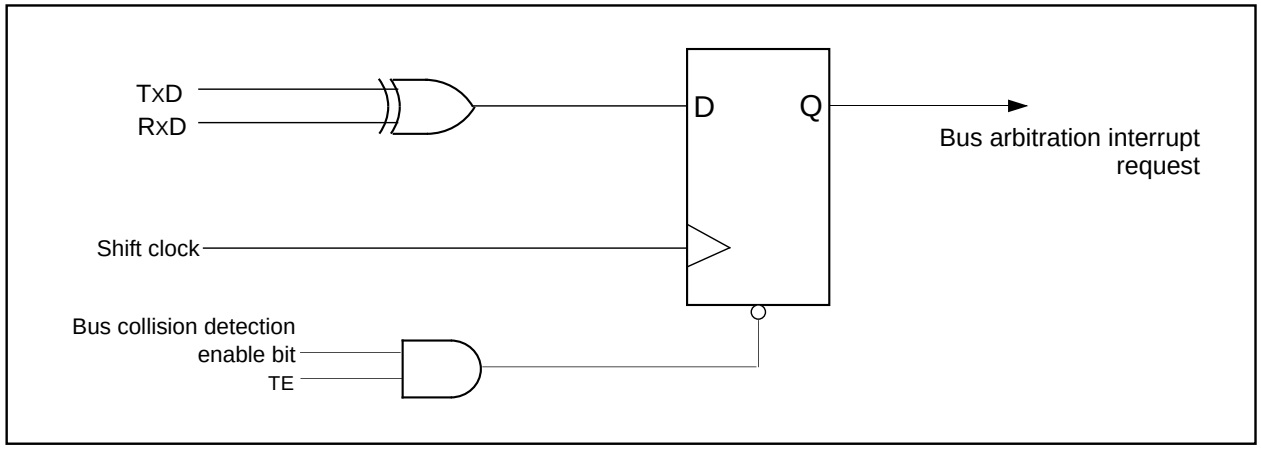


Fig. 34 Block diagram of bus arbitration interrupt circuit

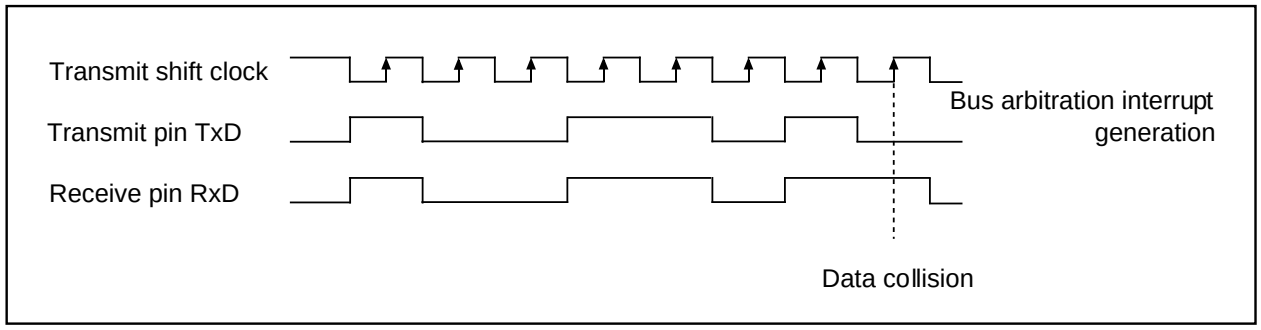


Fig. 35 Timing diagram of bus arbitration interrupt

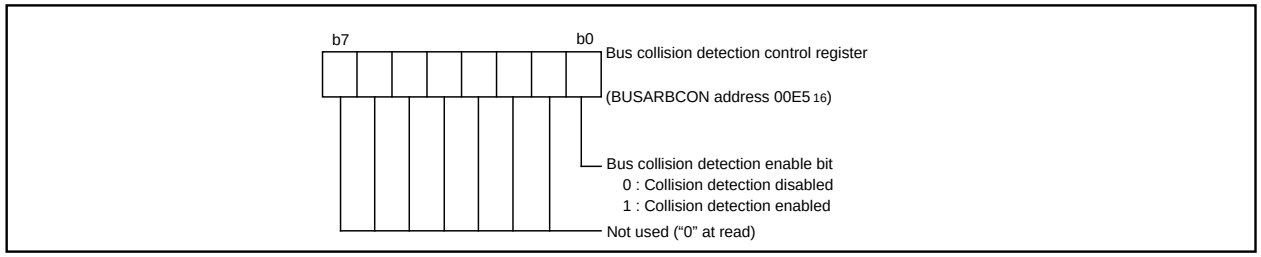


Fig. 36 Structure of bus collision detection control register

Application Example
Priority Control at Simplified SAEJ1850

At simplified SAEJ1850 communication, when multiple units start to transmit data at the same time, priority control is exerted.
On the LAN data bus, the “H” level has priority over the “L” level. When an “H” level collides with an “L” level, the LAN data bus status goes to the “H” level.
For example, when unit A outputs “H” and unit B outputs “L” at the same time in Figure 37, the LAN data bus goes to “H”. Accordingly, unit A takes priority of control and continues its transmission, and unit B stops its transmission immediately.
In this way, the 7480/7481 group exerts priority control for each bit and finally allows only the highest-priority unit to transmit data.

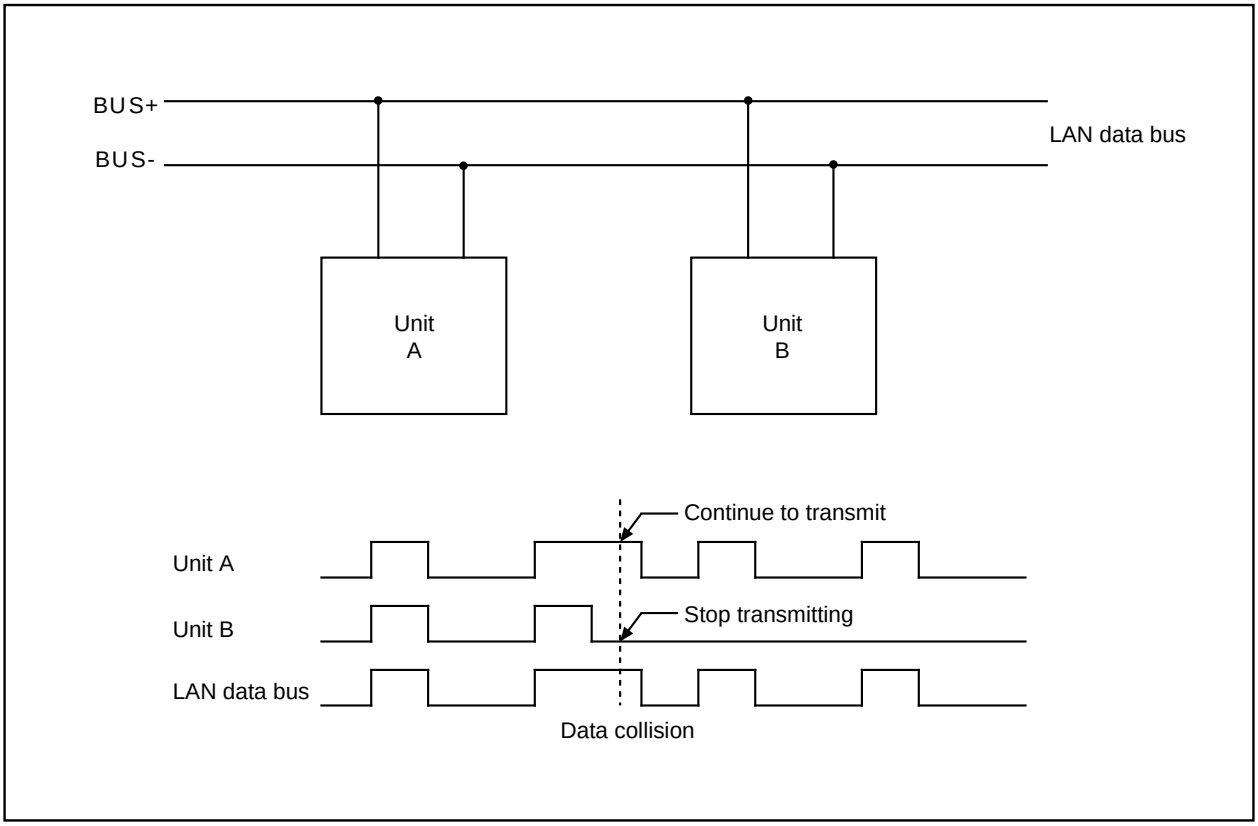


Fig. 37 Priority control at simplified SAEJ1850

A-D Converter

For A-D conversion, the 8-bit successive comparison method is used. Figure 38 shows a block diagram of A-D conversion. Conversion is automatically performed once started by the program.

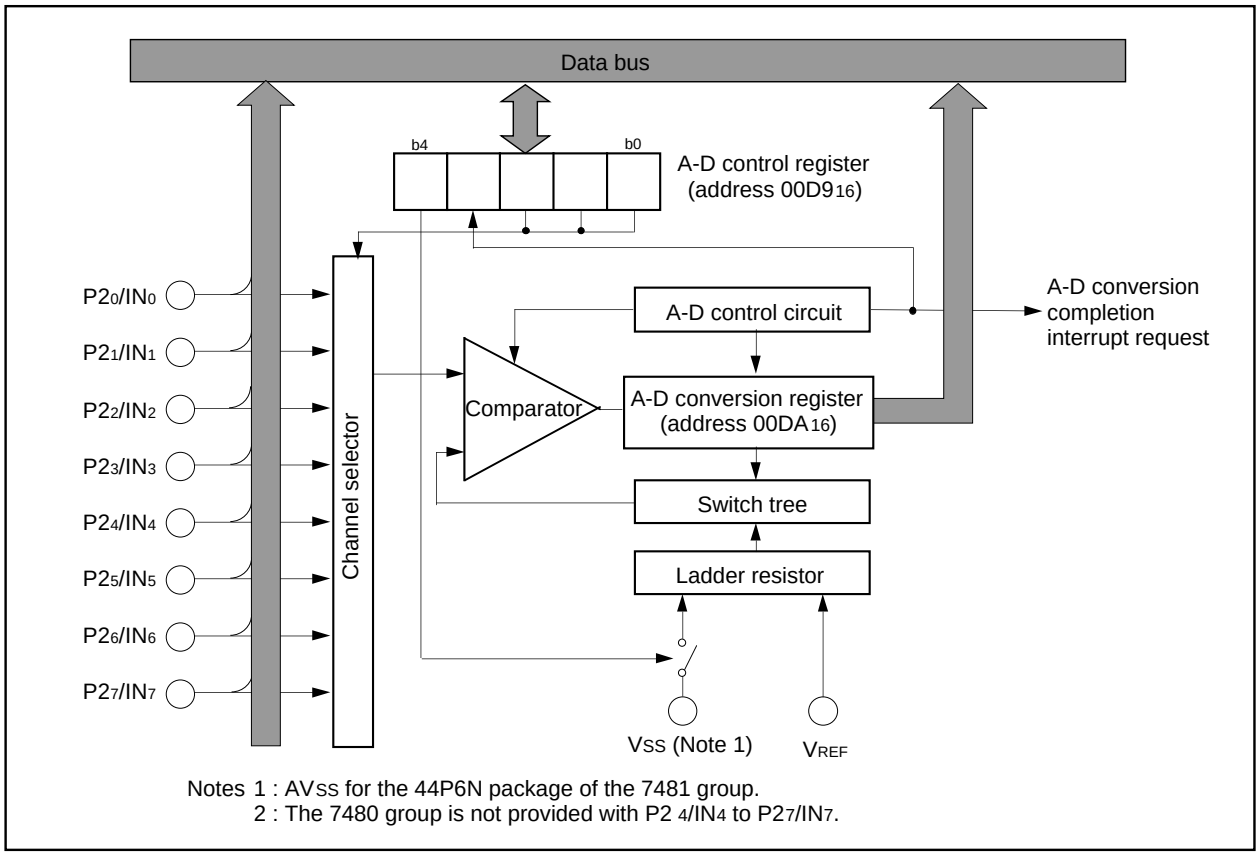
There are 8 analog input pins that are in common with $P2_7$ to $P2_0$ of port P2 (4 pins of $P2_3$ to $P2_0$ in the 7480 group).

Pin inputs to be A-D converted are selected by bit 2 to bit 0 of the A-D control register (address $00D9_{16}$). Bit 3 of the A-D control register is an A-D conversion completion bit. This bit is "0" during A-D conversion and "1" after completion of it. Accordingly, it is possible by checking this bit to know whether A-D conversion is completed or not. Figure 39 shows the relationship between the contents of the A-D control register and input pins to be selected.

The A-D conversion register (address $00DA_{16}$) stores conversion results, so it is possible to know them by reading the contents of this register.

Next, the procedure for executing A-D conversion will be explained below. First, set values in bit 2 to bit 0 of the A-D control register and select pins to be A-D converted.

Next, clear the A-D conversion completion bit to "0". With this write operation, A-D conversion is started. The A-D conversion is completed after the lapse of 50 machine cycles (12.5 μs at $f(X_{IN})$= 8 MHz), and the A-D conversion completion bit is set to "1". The A-D conversion interrupt request bit is also set to "1". Conversion results are stored in the A-D conversion register.



Notes 1 : AV_{SS} for the 44P6N package of the 7481 group.
2 : The 7480 group is not provided with $P2_4/IN_4$ to $P2_7/IN_7$.

Fig. 38 Block diagram of A-D converter circuit

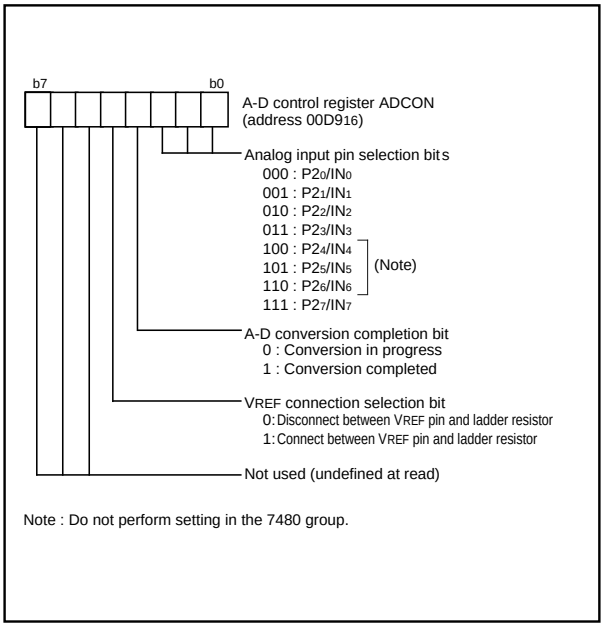


Fig. 39 Structure of A-D control register

Watchdog Timer

The watchdog timer gives a means for returning to a reset status when the program fails to run on its normal loop due to a runaway. The watchdog timer consists of a 7-bit watchdog timer L and an 8-bit watchdog timer H.

● Initial Value of Watchdog Timer

By a reset or writing to the watchdog timer H, the watchdog timer H is set to "FF16" and the watchdog timer L is set to "7F16". Any instruction that permits generating a write signal can be used; for example, STA, LDM, CLB, etc. Write data has no significance, so the above values are set regardless of that data.

● Operation of Watchdog Timer

The watchdog timer stops at reset, and writing a value in the watchdog timer H causes it to start to count down. When bit 7 of the watchdog timer H becomes "0", an internal reset occurs.
The reset status is released as soon as the release reset time is up. After that, the 7480/7481 group runs the program from the reset vector address. It is programmed that the watchdog timer H can be set before bit 7 of the watchdog timer H is cleared to "0". If the watchdog timer H is never written, the watchdog timer does not function. When the STP instruction is executed, the clock stops and the watchdog timer also stops. The count is restarted as soon as the stop mode is released. (Note) On the other hand, the watchdog timer does not stop after execution of the WIT instruction.

The timing from writing to the watchdog timer H to clearing bit 7 of the watchdog timer H to "0" is shown below. (f(XIN)=8 MHz)

- When bit 3 of the CPU mode register is "0" ..... 16.384 ms
- When bit 3 of the CPU mode register is "1" ..... 32.768 ms

Note: Since the watchdog timer still counts for the stop release waiting time (about 2048 cycles of XIN), bit 7 of the watchdog timer H should not be cleared to "0" in this period.

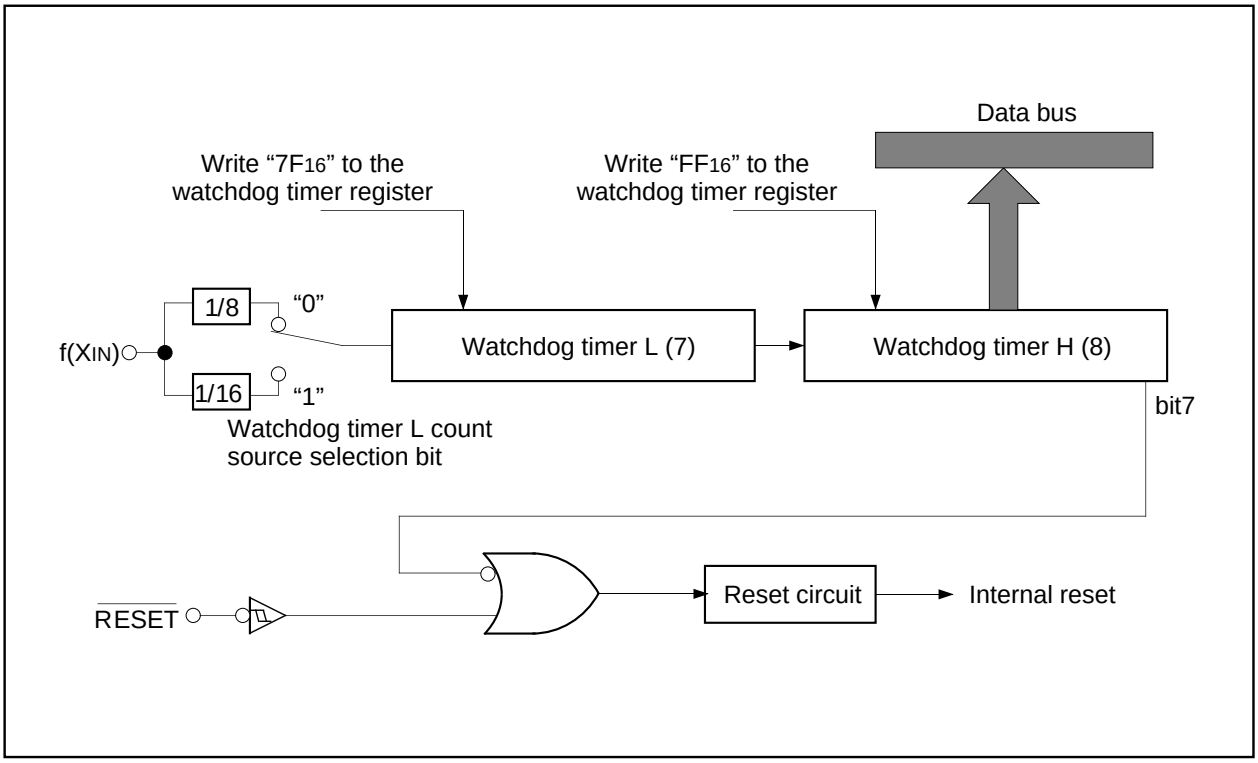


Fig. 40 Block diagram of watchdog timer

STP/WIT Instruction Control

The STP instruction and the WIT instruction can be enabled or disabled selectively by using the STP instruction operation control register. To cope with a program runaway after reset, the STP instruction and the WIT instruction are disabled in the initial status.

The STP and WIT instructions can be set as enable/disable only by writing to the STP instruction operation control register twice successively so as not to stop the oscillation clock even if a write data error is caused by program runaway. Figure 41 shows a structure of the STP instruction operation control register.

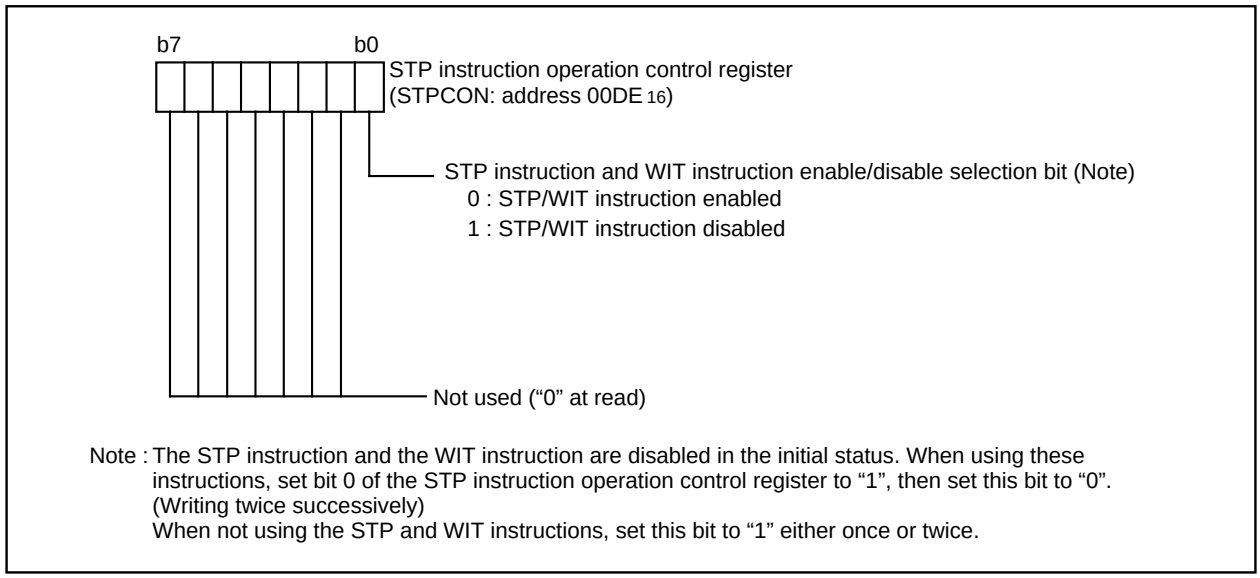


Fig. 41 Structure of STP instruction operation control register

Explanation of STP Instruction Operation Control Register

The STP instruction operation control register will be enabled by writing data to the same address twice successively. If data is not written in continuous form, the written data is not valid but the previous value is held.

If an interrupt is received while the same data is written twice, there is a possibility that the write instruction in the interrupt routine may be executed. For this reason, rewriting is required after interrupt disable. Figure 42 shows a reference example of data rewriting.

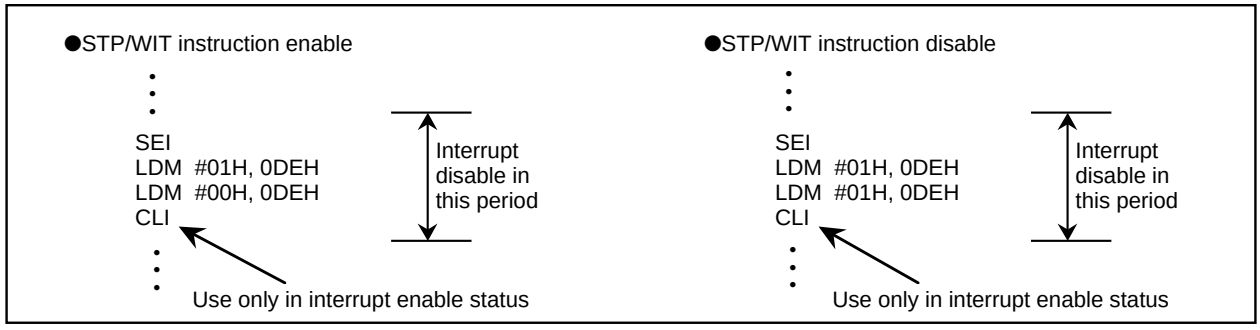


Fig. 42 Reference example of data rewriting

Recovery From Power-down Status By Key Input Interrupt (Key-on wake-up)

"Key-on wake-up" is one way of recovery from a power-down status by using the STP or WIT instruction.

If an "L" level voltage is input to any pin of port P0 when bit 5 of the edge polarity selection register is "1", an interrupt occurs, and a recovery can be made to the normal operating state. If a key matrix of active "L" with port P0 as an input port is constructed, a recovery can be made to the normal operating status by pressing a key.

The key input interrupt is in common with the INT_1 interrupt. When bit 5 of the edge polarity selection register is set to "1", the key input interrupt function is selected. If this bit is set to "1" except in the power-down status, both INT_1 and key-on wake-up are invalidated.

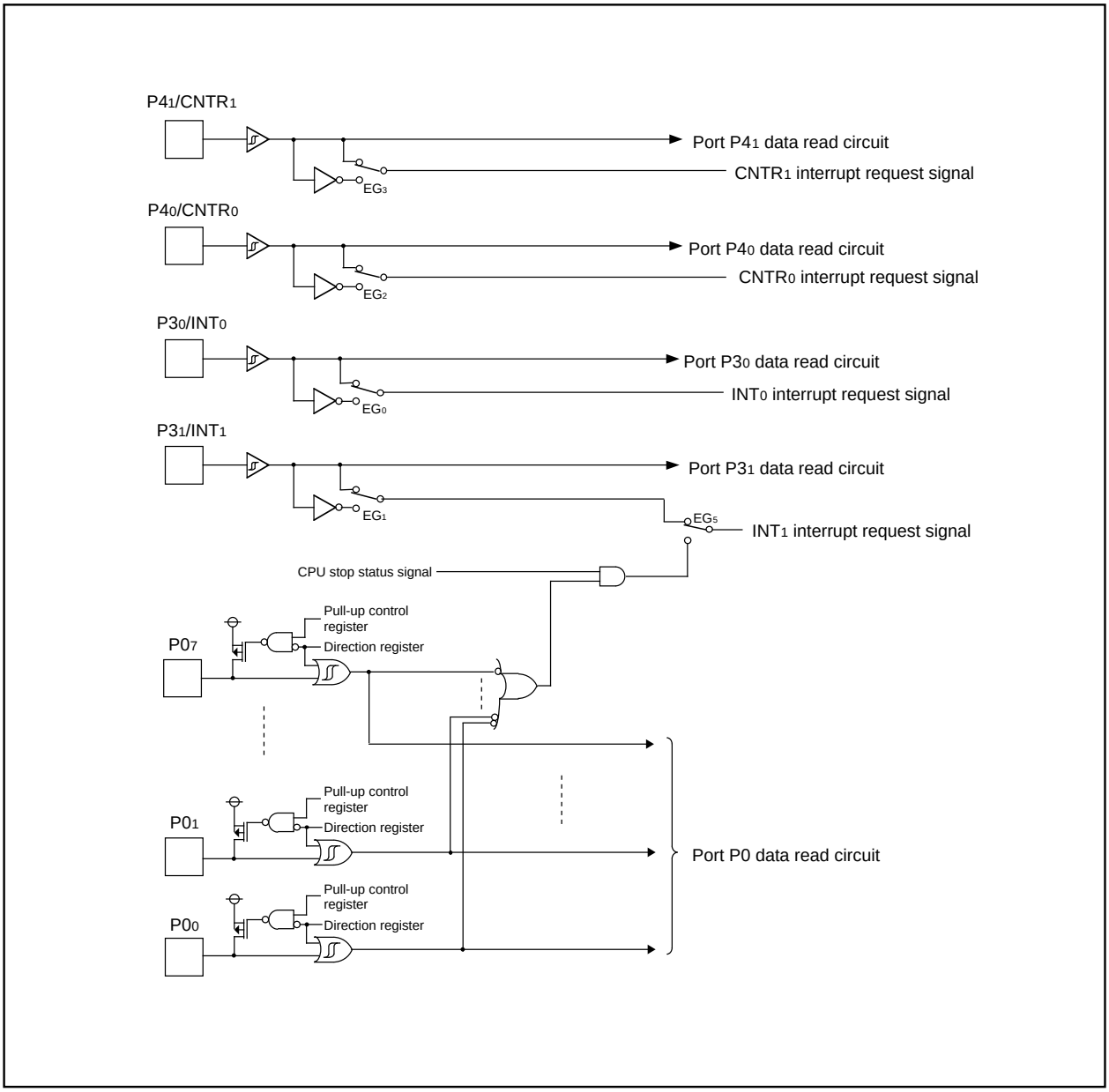


Fig. 43 Block diagram of interrupt input/key-on wake-up circuit

Clock Generating Circuit

The 7480/7481 group is provided with a built-in oscillation circuit. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT. Use the manufacturer's recommended values for constants such as capacitance, which will differ depending on each resonator. The 7480/7481 group has a built-in feedback resistor between the XIN and XOUT pins, so an external resistor can be omitted.

● Frequency Control

(1) High-speed Mode

The frequency applied to the clock input pin XIN divided by 2 is used as the internal clock ϕ. This mode is set after reset release.

(2) Medium-speed Mode

The frequency applied to the clock input pin XIN divided by 8 is used as the internal clock ϕ.

● Oscillation Frequency

(1) Stop Mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and the oscillator stops. At this time, timer 1 is set to "FF16," and f(XIN)/8 is forcibly connected to the count source of timer 1. Accordingly, set the timer 1 interrupt enable bit to the disable status ("0") before execution of the STP instruction.

When a reset or an external interrupt is accepted, oscillation is restarted, but the internal clock ϕ is supplied to the CPU after timer 1 underflows. This is because when an external resonator is used, some time is required until a start of oscillation.

(2) Wait Mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level. But, the oscillator does not stop. When a reset or interrupt is accepted, the stop status is released. The microcomputer can execute any instruction immediately, because the oscillator does not stop.

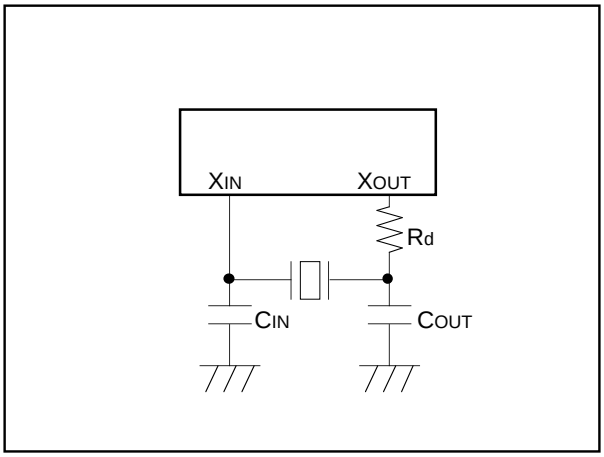


Fig. 44 External circuit of ceramic resonator

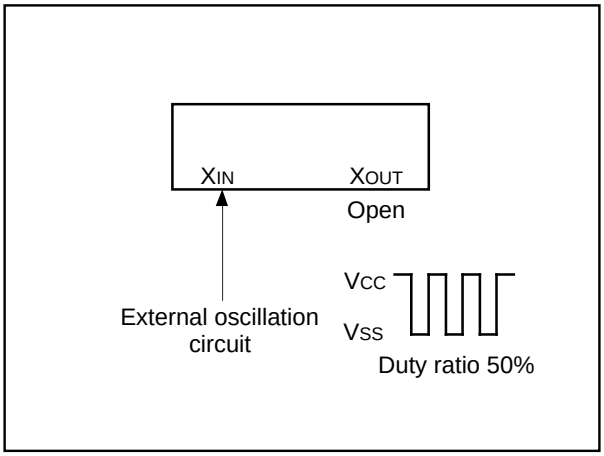


Fig. 45 External clock input circuit

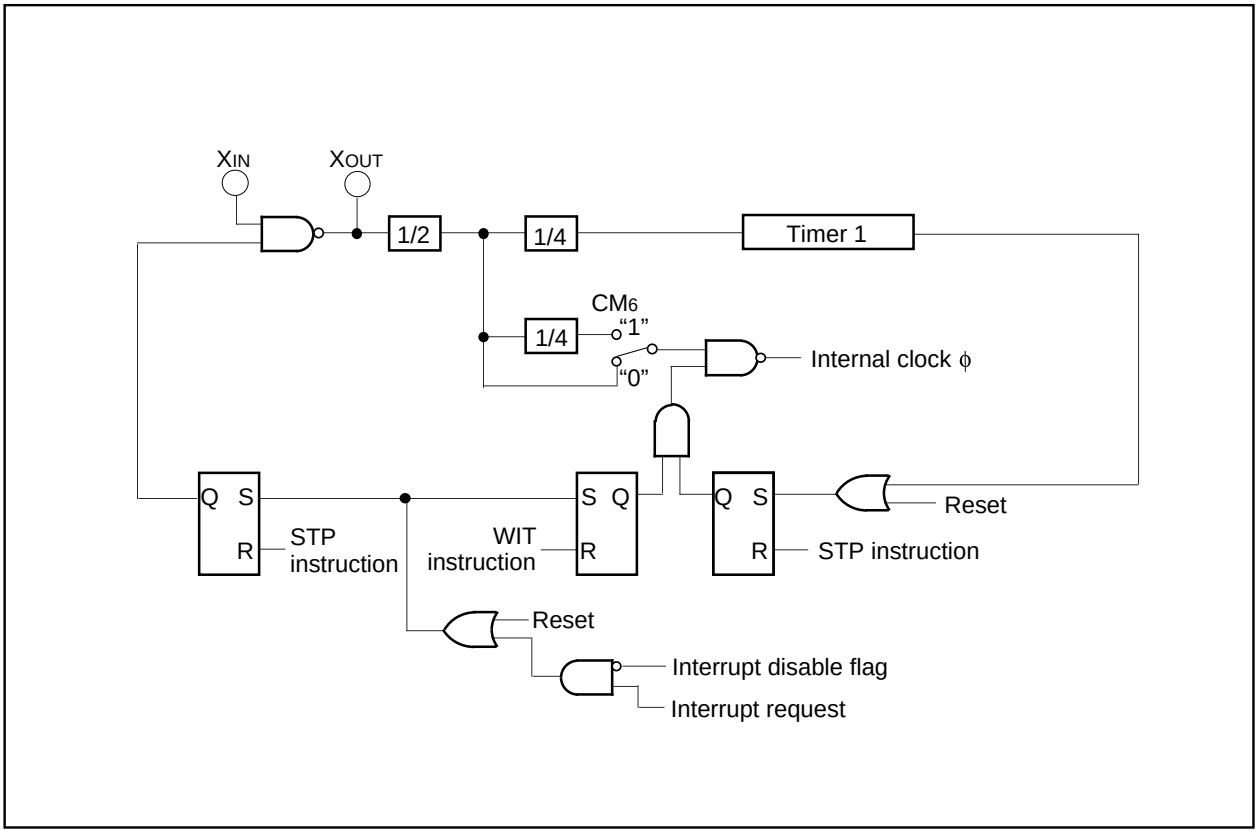


Fig. 46 Block diagram of clock generating circuit

Reset Circuit

The microcomputer is put into a reset status by holding the $\overline{RESET}$ pin at the "L" level for 2μs or more when the power source voltage is 2.7 to 5.5 V and X_{IN} is in stable oscillation.
After that, this reset status is released by returning the $\overline{RESET}$ pin to the "H" level. The program starts from the address having the contents of address FFFF16 as high-order address and the contents of address FFFE16 as low-order address.
Note that the reset input voltage should be 0.32 V or less when the power source voltage passes 2.7 V.

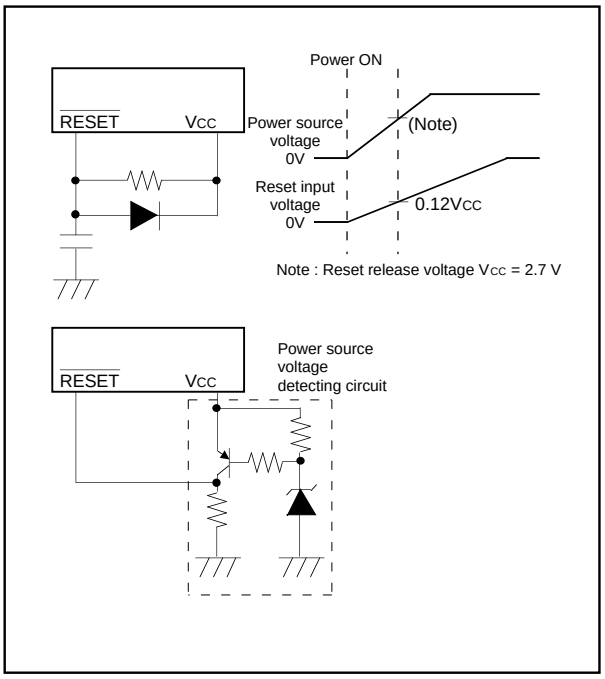


Fig. 47 Reset circuit diagram

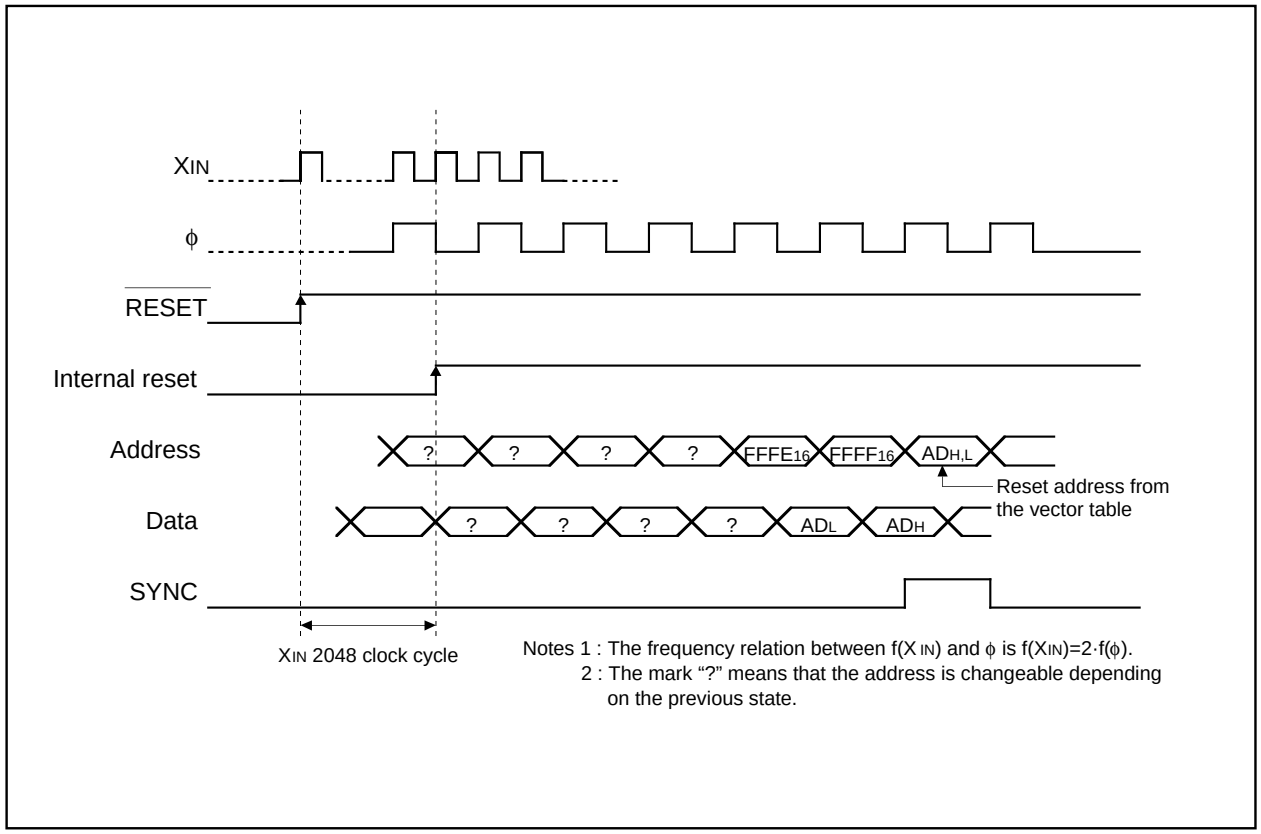


Fig. 48 Reset sequence

		Address	b7 b0
(1)	Port P0 direction register (P0D)	($C1_{16}$)	00
(2)	Port P1 direction register (P1D)	($C3_{16}$)	00
(3)	Port P4 direction register (P4D)	($C9_{16}$)	0 0 0 0
(4)	Port P5 direction register (P5D)	(CB_{16})	0 0 0 0
(5)	Port P0 pull-up control register (P0PCON)	($D0_{16}$)	00
(6)	Port P1 pull-up control register (P1PCON)	($D1_{16}$)	0 0
(7)	Port P4P5 input control register (P4P5CON)	($D2_{16}$)	00
(8)	Edge polarity selection register (EG)	($D4_{16}$)	0 0 0 0 0
(9)	A-D control register (ADCON)	($D9_{16}$)	0 1 0 0 0
(10)	STP instruction operation control register (STPCON)	(DE_{16})	0 0 0 0 0 0 0 1
(11)	Serial I/O status register (SIOSTS)	($E1_{16}$)	1 0 0 0 0 0 0 0
(12)	Serial I/O control register (SIOCON)	($E2_{16}$)	00
(13)	UART control register (UARTCON)	($E3_{16}$)	1 1 1 1 0 0 0 0
(14)	Bus collision detection control register (BUSARBCON)	($E5_{16}$)	00
(15)	Watchdog timer H (WDTH)	(EF_{16})	FF
(16)	Timer X low-order (TXL)	($F0_{16}$)	FF
(17)	Timer X high-order (TXH)	($F1_{16}$)	FF
(18)	Timer Y low-order (TYL)	($F2_{16}$)	FF
(19)	Timer Y high-order (TYH)	($F3_{16}$)	FF
(20)	Timer 1 (T1)	($F4_{16}$)	FF
(21)	Timer X mode register (TXM)	($F6_{16}$)	00
(22)	Timer Y mode register (TYM)	($F7_{16}$)	00
(23)	Timer XY control register (TXYCON)	($F8_{16}$)	0 0 0 0 0 0 1 1
(24)	Timer 1 mode register (T1M)	($F9_{16}$)	00
(25)	Timer 2 mode register (T2M)	(FA_{16})	00
(26)	CPU mode register (CPUM)	(FB_{16})	0 0 0 0 0
(27)	Interrupt request register 1 (IREQ1)	(FC_{16})	00
(28)	Interrupt request register 2 (IREQ2)	(FD_{16})	0 0 0 0
(29)	Interrupt control register 1 (ICON1)	(FE_{16})	00
(30)	Interrupt control register 2 (ICON2)	(FF_{16})	0 0 0 0
(31)	Program counter (PC_H)		Contents of address $FFFF_{16}$
	(PC_L)		Contents of address $FFFE_{16}$
(32)	Processor status register (PS)		1

□ : At reset release, the read value is undefined.

Note : Some kinds of microcomputers do not use some of these bits. Refer to the structure of each register.

Fig. 49 Internal state of microcomputer at reset

BUILT-IN PROGRAMMABLE ROM VERSIONS
M37480E8-XXXSP/FP, M37480E8T-XXXSP/FP, M37481E8-XXXSP/FP, M37481E8T-XXXSP/FP, M37481E8SS
PIN DESCRIPTION

Table 5. Pin description

Pin	Mode	Name	Input/ output	Function
VCC, VSS AVSS (Note 1)	Single-chip/ EPROM	Power source		Apply a voltage of 2.7 to 5.5 V to VCC and 0 V to VSS and AVSS.
VREF	Single-chip	Reference power input	Input	Reference voltage input pin for A-D converter.
	EPROM	Mode input	Input	Used as $\overline{CE}$ input pin.
$\overline{RESET}$	Single-chip	Reset input	Input	Reset input pin.
	EPROM	Reset input	Input	Connect to VSS.
XIN	Single-chip/ EPROM	Clock input	Input	These are I/O pins of internal clock generating circuit for the main clock. To control generating frequency, an external ceramic resonator is connected between XIN and XOUT pins. If an external clock is used, the clock oscillation source should be connected to the XIN pin, and the XOUT pin should be left open. Feedback resistor is connected between XIN and XOUT.
XOUT	Single-chip/ EPROM	Clock output	Output	
P00 – P07	Single-chip	I/O port P0	I/O	8-bit I/O port. The output structure is CMOS output. When this port is selected for input, a pull-up transistor can be connected in units of 1 bit, and a key-on wake-up function is provided.
	EPROM	Data I/O D0 – D7	I/O	Data 8-bit (D0 to D7) I/O pins
P10 – P17	Single-chip	I/O port P1	I/O	8-bit I/O port. The output structure is CMOS output. When this port is selected for input, a pull-up transistor can be connected in units of 4 bits. P12 and P13 are in common with timer output pins T0 and T1. P14, P15, P16 and P17 are in common with serial I/O pins RxD, TxD, SCLK and $\overline{SRDY}$.
	EPROM	Address input A4 – A10	Input	P11 to P17 are address (A4 to A10) input pins. Leave P10 open.
P20 – P27 (Note 2)	Single-chip	Input port P2	Input	8-bit input port. This port is in common with analog input pins IN0 to IN7 (IN0 to IN3 for the 7480 group).
	EPROM	Address input A0 – A3	Input	P20 to P23 are address (A0 to A3) input pins. Leave P24 to P27 open.
P30 – P33	Single-chip	Input port P3	Input	4-bit input port. P30 and P31 are in common with external interrupt input pins INT0 and INT1.
	EPROM	Address input A11, A12, mode input, VPP input	Input	P30 and P31 are address (A11, A12) input pins. P32 is used for $\overline{OE}$ input. P33 is VPP input. Apply VPP in the program and program verify modes.
P40 – P43 (Note 3)	Single-chip	I/O port P4	I/O	4-bit I/O port. The output structure is N-channel open drain output, having built-in clamp diode. P40 and P41 are in common with timer input pins CNTR0 and CNTR1.
	EPROM	Address input A13, A14	Input	P40 and P41 are address (A13, A14) input pins. Leave P42 and P43 open.
P50 – P53 (Note 4)	Single-chip	I/O port P5	I/O	4-bit I/O port. The output structure is N-channel open drain output, having a built-in clamp diode.
	EPROM	Input port P5	Input	Leave these pins open.

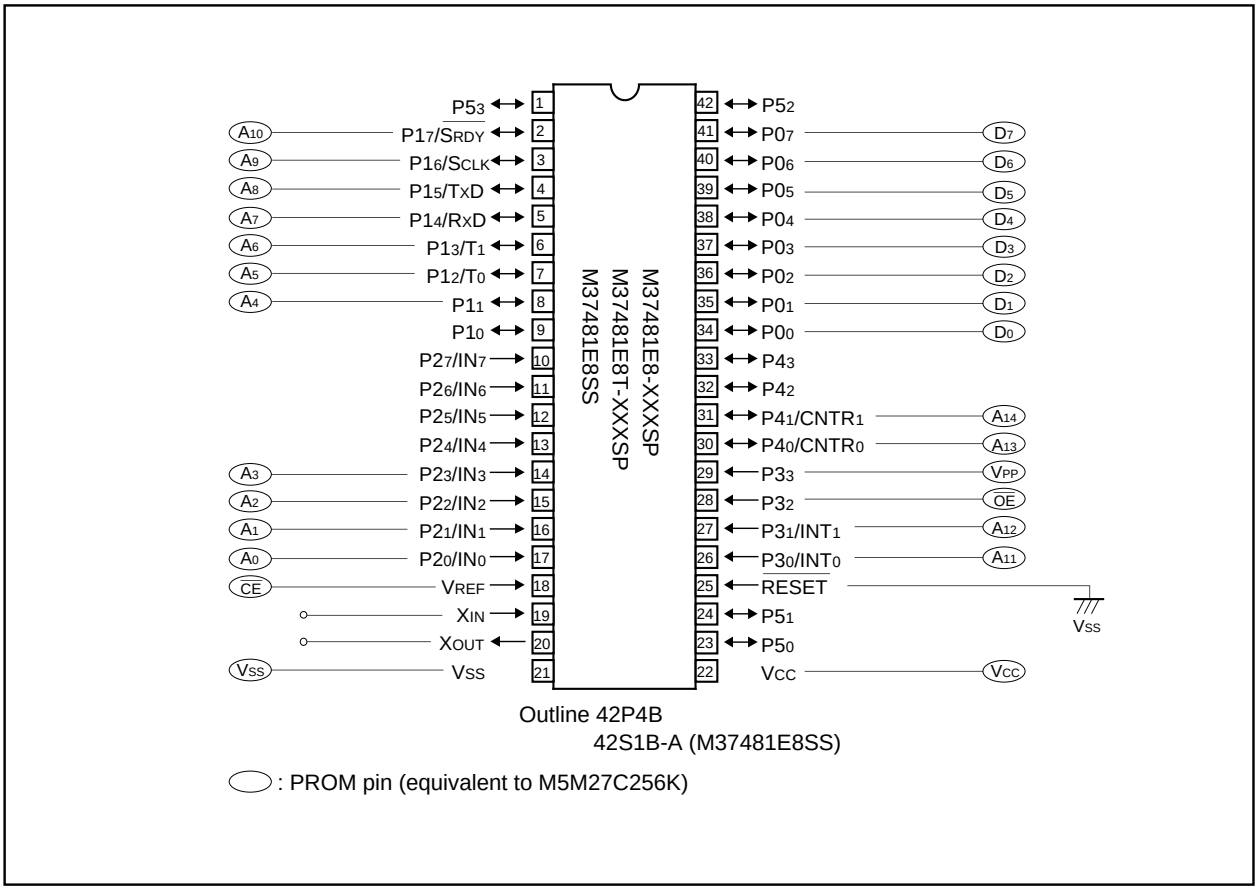
Notes 1 : This is a dedicated pin for the 44P6N-A package in the 7481 group.
2 : Only 4 bits of P20 to P23 (IN0 to IN3) for the 7480 group.
3 : Only 2 bits of P40 and P41 for the 7480 group.
4 : This is a dedicated pin for the 7481 group.

EPROM MODE

The built-in programmable ROM has the EPROM mode in addition to its normal operation modes. When the $\overline{\text{RESET}}$ level becomes "L", the chip automatically enters the EPROM mode. Table 6 shows a list of correspondence between pins and Figure 50 to Figure 52 show pin connection diagrams. In this status, each of ports P0, P11 to P17, P20 to P23, P3, P40, P41 and VREF are used for the PROM (equivalent to M5M27C256K). In this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5M27C256K. The clock should be connected to XIN and XOUT pins.

Table 6. Correspondence between pins in EPROM mode

	M37480E8, M37481E8	M5M27C256K
VCC	VCC	VCC
VPP	P33	VPP
VSS	VSS	VSS
Address input	Ports P11 – P17, P20 – P23, P30, P31, P40, P41	A0 – A14
Data I/O	Port P0	D0 – D7
$\overline{\text{CE}}$	VREF	$\overline{\text{CE}}$
$\overline{\text{OE}}$	P32	$\overline{\text{OE}}$



Outline 42P4B
42S1B-A (M37481E8SS)

: PROM pin (equivalent to M5M27C256K)

Fig. 50 Pin connection in EPROM mode (1)

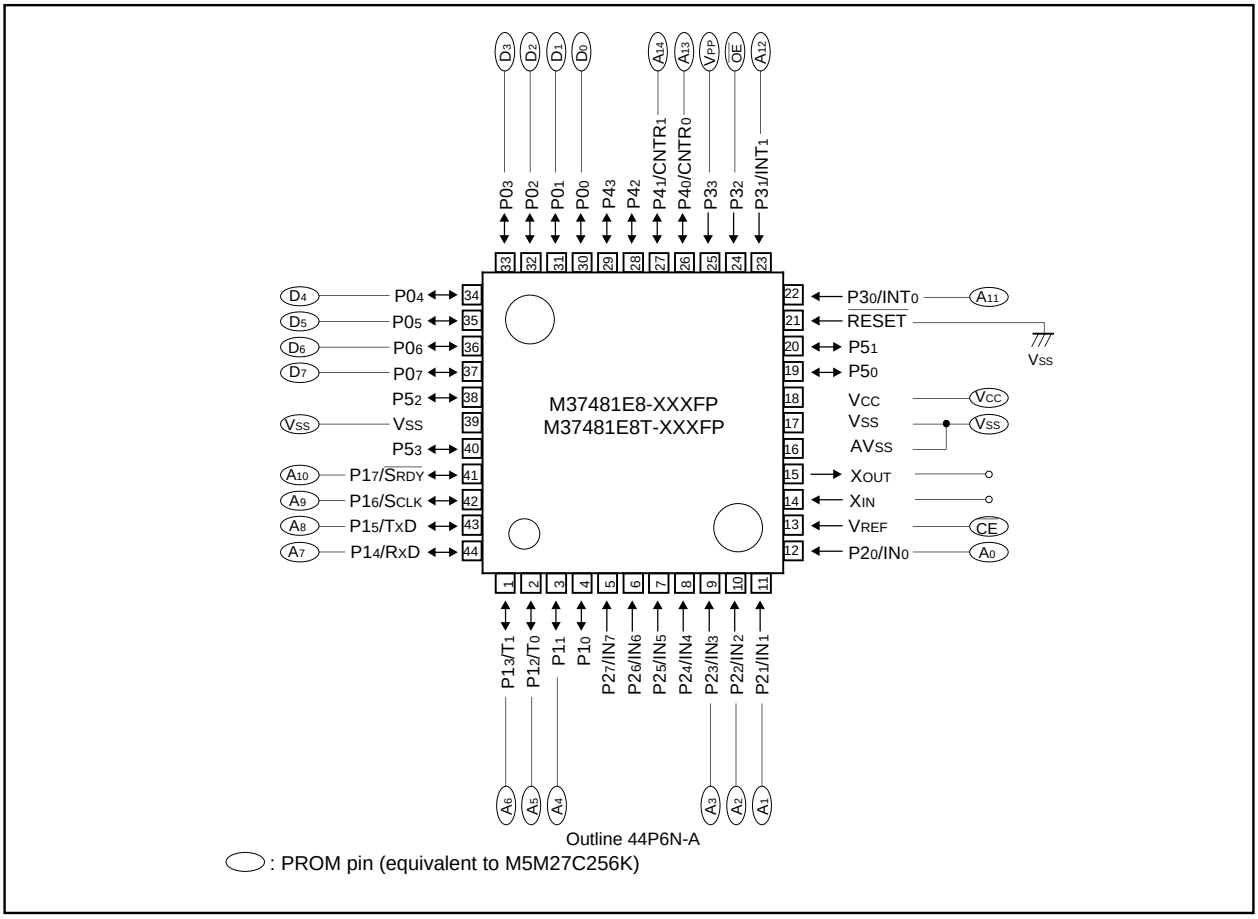


Fig. 51 Pin connection in EPROM mode (2)

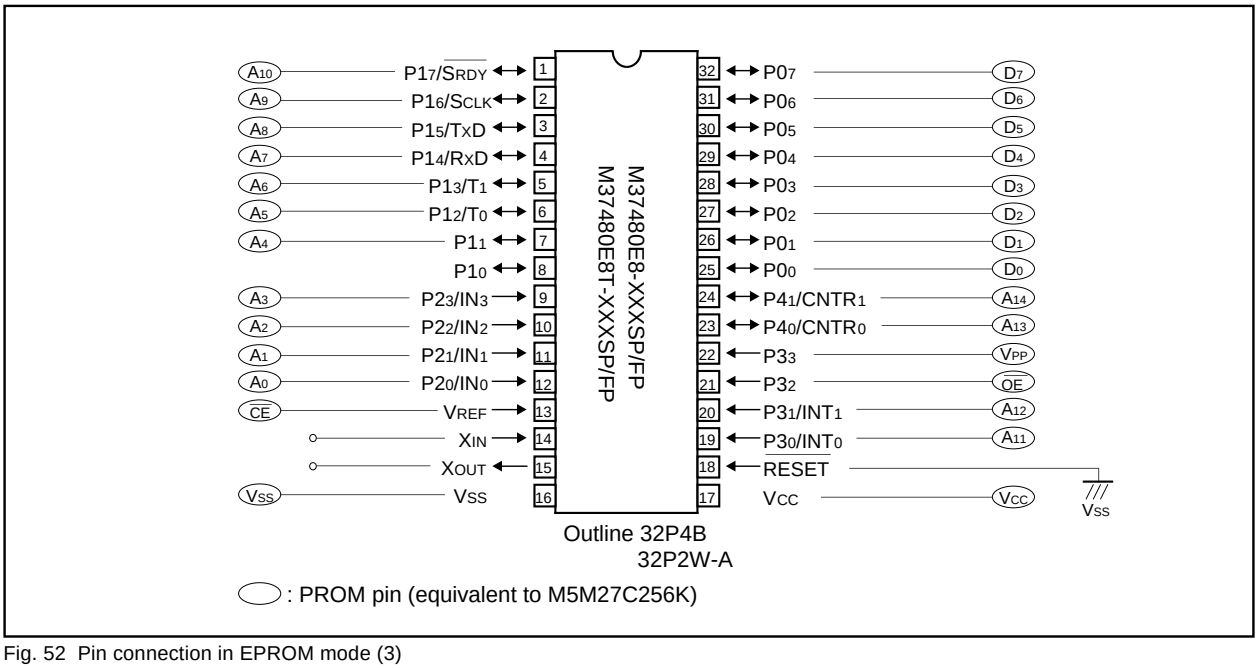


Fig. 52 Pin connection in EPROM mode (3)

FUNCTIONAL DESCRIPTION OF PROM VERSION

Reading

To read the PROM, set the $\overline{CE}$ and $\overline{OE}$ pins to "L" level, and set the address signal (A_0 to A_{14}). The stored contents will appear to data I/O pins (D_0 to D_7). When the $\overline{CE}$ and $\overline{OE}$ pins are set to "H" level, the data I/O pins will be put into a floating status.

Writing

To write to the PROM, apply "H" to the $\overline{OE}$ pin and V_{PP} to the V_{PP} pin to set the program mode. Select addresses to be written to with address input pins (A_0 to A_{14}) and give write data to the data input pins (D_0 to D_7) in 8-bit parallel form. In this status, when the $\overline{CE}$ pin becomes "L", writing will be started.

Notes on Writing

When using a PROM programmer, specify the address range to address 4000_{16} to address $7FFF_{16}$.
When data is written between address 0000_{16} and address $7FFF_{16}$, fill addresses 0000_{16} to $3FFF_{16}$ with "FF_{16}".

Erasing

Data can be erased only on the ceramic package with window M37481E8SS. To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power required for erasing is $15W \cdot s/cm^2$.

NOTES ON HANDLING

(1) Sunlight and fluorescent light contain wavelengths capable of erasing data. For use in the read mode, be sure to cover the transparent window with a seal. (Ceramic package type)
(2) We can supply the seal with which the transparent window is covered. Be careful not to allow the seal to contact the microcomputer lead pins. (Ceramic package type)
(3) Before erasing, clean the transparent glass. If the glass is smeared with greasy hands or paste, ultraviolet light transmission will be prevented, having a negative effect on erasing characteristics. (Ceramic package type)
(4) Since a high voltage is used for writing data, care should be taken not to apply an overvoltage when turning on the power source.
(5) For the programmable microcomputers (one-time programmable version, version shipped in blank), Mitsubishi does not perform PROM write testing and screening in the assembly process and subsequent processes. To improve reliability after writing, perform writing and testing according to the following operation flow before use.

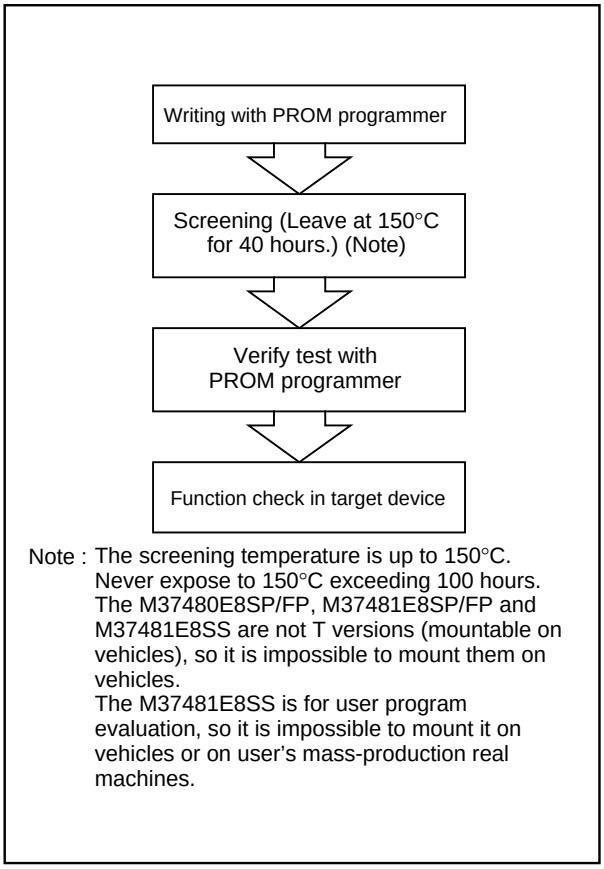


Fig. 53 Writing and testing for one-time programmable version

I/O SIGNALS IN EACH MODE

Table 7. I/O signals in each mode

Pin / Mode	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	Data I/O
Read-out	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Output
Output disable	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Floating
Programming	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Input
Programming verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	Output
Program disable	V_{IH}	V_{IH}	V_{PP}	V_{CC}	Floating

Note : V_{IL} and V_{IH} denote an “L” input voltage and an “H” input voltage, respectively.

ADDRESSING MODES

The 7480/7481 group has strong accessability, because it has 17 kinds of addressing modes. For details, refer to the 740 family addressing modes.

MACHINE-LANGUAGE INSTRUCTIONS

The 7480/7481 group has 71 machine-language instructions. For details, refer to the 740 family machine-language instruction list.

NOTES ON PROGRAMMING

(1) The frequency division ratio of the timer is 1/(n+1).
n: Timer setting value
However, n = 0 – 255 (for timer 1, timer 2)
n = 0 – 65535 (timer X, timer Y)

(2) The contents of the interrupt request bits can be changed by software, but the values will not change immediately after being overwritten.
After changing the value of the interrupt request bits, execute at least one instruction before executing a the BBC or BBS instruction.

(3) To calculate in decimal notation, set the decimal mode flag (D) to “1”. After executing the ADC or SBC instruction, execute another instruction before executing the SEC, CLC, or CLD instruction.

(4) A NOP instruction should be executed after every PLP instruction.

(5) Do not execute the STP instruction during A-D conversion.

(6) Multiplication and Division Instructions
The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instructions.
The execution of these instructions does not change the contents of the processor status register.

DATA REQUIRED FOR MASK ORDERING

Please submit the following data when placing mask orders.
(1) Mask ROM confirmation form
(2) Mark specification form
(3) ROM data ..... EPROM 3 sets

DATA REQUIRED FOR ROM WRITING ORDERING

Please submit the following data when placing ROM writing orders.
(1) ROM writing confirmation form
(2) Mark specification form
(3) ROM data ..... EPROM 3 sets

M37480M4/M8/E8-XXXSP/FP, M37480M2T/M4T/M8T/E8T-XXXSP/FP
ABSOLUTE MAXIMUM RATINGS (7480 Group)

Table 8. Absolute maximum ratings

Symbol	Parameter	Condition	Rated value	Unit
V_{CC}	Power source voltage	All voltages are measured on the basis of the V_{SS} pin. Output transistors are cut off.	–0.3 to 7	V
V_I	Input voltage		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	T_a = 25 °C	1000 (Note 1)	mW
T_{opr}	Operating temperature range		–20 to 85 (Note 2)	°C
T_{stg}	Storage temperature		–40 to 150 (Note 3)	°C

Notes 1 : 500 mW for 32P2W-A package type.
2 : –40 to 85 °C for extended operating temperature range version.
3 : –65 to 150 °C for extended operating temperature range version.

RECOMMENDED OPERATING CONDITIONS (7480 Group)

(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85°C (Note 1) unless otherwise specified)

Table 9. Recommended operating conditions

Symbol	Parameter		Standard values			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage	f(X_{IN}) = (2.2V_{CC} – 2) MHz	2.7	3	4.5	V
		f(X_{IN}) = 8 MHz	4.5	5	5.5	V
V_{SS}	Power source voltage			0		V
V_{IH}	"H" input voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$		0.8 V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P2_0$ – $P2_3$		0.7 V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P3_0$ – $P3_3$	V_{CC} = 4.5 to 5.5 V	0.8 V_{CC}		V_{CC}	V
		V_{CC} = 2.7 to 4.5 V	0.9 V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P4_0$ – $P4_1$ (Note 4)	V_{CC} = 4.5 to 5.5 V	0.8 V_{CC}		V_{CC}	V
		V_{CC} = 2.7 to 4.5 V	0.9 V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage X_{IN}, $\overline{RESET}$		0.8 V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$		0		0.2 V_{CC}	V
V_{IL}	"L" input voltage $P2_0$ – $P2_3$		0		0.25 V_{CC}	V
V_{IL}	"L" input voltage $P3_0$ – $P3_3$	V_{CC} = 4.5 to 5.5 V	0		0.4 V_{CC}	V
		V_{CC} = 2.7 to 4.5 V	0		0.3 V_{CC}	V
V_{IL}	"L" input voltage $P4_0$ – $P4_1$	V_{CC} = 4.5 to 5.5 V	0		0.4 V_{CC}	V
		V_{CC} = 2.7 to 4.5 V	0		0.3 V_{CC}	V
V_{IL}	"L" input voltage X_{IN}		0		0.16 V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0.12 V_{CC}	V
I_I	Input current $P4_0$ – $P4_1$ (Note 4) V_I > V_{CC}				1	mA
$I_{OH(sum)}$	"H" sum output current $P0_0$ – $P0_7$				– 30	mA
$I_{OH(sum)}$	"H" sum output current $P1_0$ – $P1_7$				– 30	mA
$I_{OL(sum)}$	"L" sum output current $P0_0$ – $P0_7$, $P4_0$ – $P4_1$				60	mA
$I_{OL(sum)}$	"L" sum output current $P1_0$ – $P1_7$				60	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$				– 10	mA
$I_{OL(peak)}$	"L" peak output current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P4_0$ – $P4_1$				20	mA
$I_{OH(avg)}$	"H" average output current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$ (Note 2)				– 5	mA
$I_{OL(avg)}$	"L" average output current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P4_0$ – $P4_1$ (Note 2)				10	mA

Table 9. Recommended operating conditions (cont.)

Symbol	Parameter			Standard values			Unit
				Min.	Typ.	Max.	
f(CNTR)	Timer input frequency CNTR0 (P40), CNTR1 (P41) (Note 3)		f(XIN) = 4 MHz			1	MHz
			f(XIN) = 8 MHz			2	
f(SCLK)	Serial I/O clock input frequency SCLK (P16) (Note 3)	Clock synchronous serial I/O mode	f(XIN) = 4 MHz			250	kHz
			f(XIN) = 8 MHz			500	
		UART mode	f(XIN) = 4 MHz			1	MHz
			f(XIN) = 8 MHz			2	
f(XIN)	Clock input oscillation frequency (Note 3)		VCC = 2.7 to 4.5 V			2.2VCC – 2	MHz
			VCC = 4.5 to 5.5 V			8	

Notes 1 : –40 to 85 °C for extended operating temperature range version.
2 : The average output currents IOH(avg) and IOL(avg) are the average values during 100 ms.
3 : The clock input oscillation frequency is at 50 % duty ratio.
4 : When applying a voltage through a resistor as shown in the figure 54, VI > VCC may be accepted if the current is 1 mA or less.

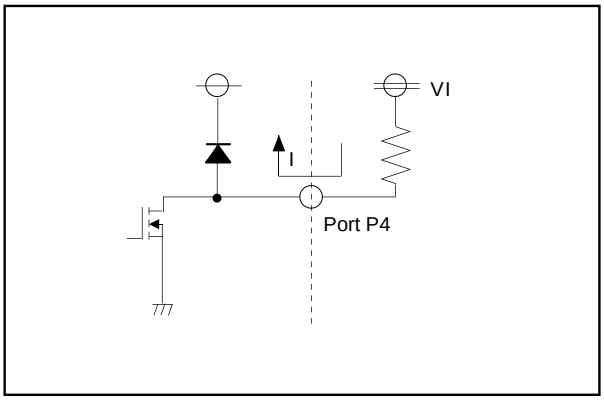


Fig. 54 Note on use of port P4

Notes on Clamp Diode (7480 Group)

(1) Total input current

The current of port P4 through the clamp diode can be drawn up to 1.0 mA per port. When a current that cannot be consumed by microcomputer is sent to the clamp diode, this may raise the power source pin voltage of the microcomputer.

The system power circuit must be designed so that the power source voltage of the microcomputer may be stabilized within standard values.

(2) Maximum input voltage

If the input voltage of a signal connected to port P4 is beyond VCC + 0.3 V, the input waveform should have a delay exceeding 2 μs/V from the moment that this waveform goes over the voltage.

For using a CR circuit for delay, calculate a proper delay value by the following expression:

$$\frac{dt}{dv} = \frac{t}{0.6 \times V_{IN}} \geq 2 \times 10^{-6} \ (s/V)$$

where VIN = Maximum input voltage amplitude margin and
t = C × R.

The clamp diode of the 7480/7481 group is designed for a level shift of DC signal unlike ordinary switching diodes. Do not apply sudden stress, such as rush current, directly to the diode.

Notes on Countermeasures for Noise and Latch-up (7480 Group)

(1) Connect a bypass capacitor (0.1μF) across the VCC pin and the VSS pin with the shortest possible wiring, using a relatively thick wire.
(2) Connect a bypass capacitor (0.01 μF) across the VREF pin and the VSS pin with the shortest possible wiring, using a relatively thick wire.
(3) In the oscillation circuit, connect across the XIN and XOUT pins with the shortest possible wiring. Connect the GND and VSS pins of the oscillation circuit with the shortest possible wiring, using a relatively thick wire.
(4) In the case of the P33/VPP pin of the built-in programmable ROM version, connect an approximately 5 kΩ resistor to the P33/VPP pin the shortest possible in series.

M37480M4/M8/E8-XXXSP/FP, M37480M2T/M4T/M8T/E8T-XXXSP/FP
ELECTRICAL CHARACTERISTICS (7480 Group)

(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C (Note 1) unless otherwise specified)

Table 10. Electrical characteristics

Symbol	Parameter	Test conditions		Standard values			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage	V_{CC} = 5 V, I_{OH} = –5 mA		3			V
	$P0_0$ – $P0_7$, $P1_0$ – $P1_7$	V_{CC} = 3 V, I_{OH} = –1.5 mA		2			
V_{OL}	"L" output voltage	V_{CC} = 5 V, I_{OL} = 10 mA				2	V
	$P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P4_0$ – $P4_1$	V_{CC} = 3 V, I_{OL} = 3 mA				1	
V_{T+} – V_{T-}	Hysteresis $P0_0$ – $P0_7$,	V_{CC} = 5 V			0.5		V
	$P3_0$ – $P3_3$, $P4_0$ – $P4_1$ (Note 2)	V_{CC} = 3 V			0.3		
V_{T+} – V_{T-}	Hysteresis $P1_6$/S_{CLK}, $P1_4$/RxD	When used as S_{CLK}, RxD	V_{CC} = 5 V		0.5		V
		input	V_{CC} = 3 V		0.3		
V_{T+} – V_{T-}	Hysteresis $\overline{RESET}$	V_{CC} = 5 V			0.5		V
		V_{CC} = 3 V			0.3		
I_{IH}	"H" input current	V_I = V_{CC} without pull-up	V_{CC} = 5 V			5	μA
	$P0_0$ – $P0_7$, $P1_0$ – $P1_7$	transistor	V_{CC} = 3 V			3	
I_{IH}	"H" input current	V_I = V_{CC} = 5 V				5	μA
	$P3_0$ – $P3_3$, $P4_0$ – $P4_1$	V_I = V_{CC} = 3 V				3	
I_{IH}	"H" input current $P2_0$ – $P2_3$	V_I = V_{CC} when analog	V_{CC} = 5 V			5	μA
		input is not selected	V_{CC} = 3 V			3	
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}	V_I = V_{CC}	V_{CC} = 5 V			5	μA
		(X_{IN} at stop)	V_{CC} = 3 V			3	
I_{IL}	"L" input current	V_I = 0 V without pull-up	V_{CC} = 5 V			–5	μA
	$P0_0$ – $P0_7$, $P1_0$ – $P1_7$	transistor	V_{CC} = 3 V			–3	
		V_I = 0 V with pull-up	V_{CC} = 5 V	–0.25	–0.5	–1.0	mA
		transistor (Note 3)	V_{CC} = 3 V	–0.08	–0.18	–0.35	
I_{IL}	"L" input current	V_I = 0 V	V_{CC} = 5 V			–5	μA
	$P3_0$ – $P3_3$, $P4_0$ – $P4_1$		V_{CC} = 3 V			–3	
I_{IL}	"L" input current $P2_0$ – $P2_3$	V_I = 0 V when analog input	V_{CC} = 5 V			–5	μA
		is not selected	V_{CC} = 3 V			–3	
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}	V_I = 0 V	V_{CC} = 5 V			–5	μA
		(X_{IN} at stop)	V_{CC} = 3 V			–3	

Notes 1 : –40 to 85 °C for extended operating temperature range version.

2 : At using P0 for key-on wake-up function.

3 : Can be indicated in resistance value as shown below:
When V_{CC} = 5 V: 5 kΩ (min.), 10 kΩ (typ.), 20 kΩ (max.).
When V_{CC} = 3 V: 8.6 kΩ (min.), 16.7 kΩ (typ.), 37.5 kΩ (max.).

M37480M4/M8/E8-XXXSP/FP, M37480M2T/M4T/M8T/E8T-XXXSP/FP

Table 10. Electrical characteristics (cont.)

Symbol	Parameter	Test conditions			Standard values			Unit
					Min.	Typ.	Max.	
V_{RAM}	RAM retention voltage	At clock stop mode			2			V
I_{CC}	Power source current	In operating mode	In high-speed mode, $f(X_{IN})$ = 4 MHz, V_{CC} = 5 V	A-D conversion not executed		3.5	7	mA
				A-D conversion in progress		4	8	mA
			In high-speed mode, $f(X_{IN})$ = 4 MHz, V_{CC} = 3 V	A-D conversion not executed		1.8	3.6	mA
				A-D conversion in progress		2	4	mA
			In high-speed mode, $f(X_{IN})$ = 8 MHz, V_{CC} = 5 V	A-D conversion not executed		7	14	mA
				A-D conversion in progress		7.5	15	mA
			In medium-speed mode, $f(X_{IN})$ = 4 MHz, V_{CC} = 5 V	A-D conversion not executed		1.75	3.5	mA
				A-D conversion in progress		2	4	mA
			In medium-speed mode, $f(X_{IN})$ = 4 MHz, V_{CC} = 3 V	A-D conversion not executed		0.9	1.8	mA
				A-D conversion in progress		1	2	mA
			In medium-speed mode, $f(X_{IN})$ = 8 MHz, V_{CC} = 5 V	A-D conversion not executed		3.5	7	mA
				A-D conversion in progress		3.75	7.5	mA
		In wait mode	In high-speed mode, $f(X_{IN})$ = 4 MHz	V_{CC} = 5 V		1	2	mA
				V_{CC} = 3 V		0.5	1	
			In high-speed mode, $f(X_{IN})$ = 8 MHz	V_{CC} = 5 V		2	4	
			In medium-speed mode, $f(X_{IN})$ = 4 MHz	V_{CC} = 5 V		0.9	1.8	mA
				V_{CC} = 3 V		0.45	0.9	
			In medium-speed mode, $f(X_{IN})$ = 8 MHz	V_{CC} = 5 V		1.8	3.6	
		In stop mode	$f(X_{IN})$ = 0 V_{CC} = 5 V	T_a = 25 °C		0.1	1	μA
				T_a = 85 °C		1	10	μA

M37480M4/M8/E8-XXXSP/FP, M37480M2T/M4T/M8T/E8T-XXXSP/FP
A-D CONVERSION CHARACTERISTICS (7480 Group)

(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C (Note) unless otherwise specified)

Table 11. A-D conversion characteristics

Symbol	Parameter	Test conditions	Standard values			Unit
			Min.	Typ.	Max.	
——	Resolution				8	bits
——	Absolute accuracy (except quantization error)	V_{CC} = V_{REF} = 5.0 V			±2	LSB
T_{CONV}	Conversion time	V_{CC} = 2.7 to 5.5 V, f(X_{IN}) = 4 MHz			25	μs
		V_{CC} = 4.5 to 5.5 V, f(X_{IN}) = 8 MHz			12.5	
V_{VREF}	Reference voltage	V_{CC} = 2.7 to 4.0 V	2		V_{CC}	V
		V_{CC} = 4.0 to 5.5 V	0.5 V_{CC}		V_{CC}	
R_{LADDER}	Ladder resistance		12	35	100	kΩ
V_{IA}	Analog input voltage		0		V_{REF}	V
I_{VREF}	Reference input current	V_{REF} = 5.0 V	50	143	416	μA

Note: –40 to 85 °C for extended operating temperature range version.

M37481M4/M8/E8-XXXSP/FP, M37481M2T/M4T/M8T/E8T-XXXSP/FP, M37481E8SS ABSOLUTE MAXIMUM RATINGS (7481 Group)

Table 12. Absolute maximum ratings

Symbol	Parameter	Condition	Rated value	Unit
V_{CC}	Power source voltage	All voltages are measured on the basis of the V_{SS} pin. Output transistors are cut off.	–0.3 to 7	V
V_I	Input voltage		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	T_a = 25 °C	1000 (Note 1)	mW
T_{opr}	Operating temperature range		–20 to 85 (Note 2)	°C
T_{stg}	Storage temperature		–40 to 150 (Note 3)	°C

Notes 1 : 500 mW for 44P6N-A package type.
2 : –40 to 85 °C for extended operating temperature range version.
3 : –65 to 150 °C for extended operating temperature range version.

RECOMMENDED OPERATING CONDITIONS (7481 Group)

(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85°C (Note 1) unless otherwise specified)

Table 13. Recommended operating conditions

Symbol	Parameter		Standard values			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage	f(X_{IN}) = (2.2V_{CC} – 2) MHz	2.7	3	4.5	V
		f(X_{IN}) = 8 MHz	4.5	5	5.5	V
V_{SS}	Power source voltage			0		V
V_{IH}	"H" input voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$		0.8 V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P2_0$ – $P2_7$		0.7 V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P3_0$ – $P3_3$	V_{CC} = 4.5 to 5.5 V	0.8 V_{CC}		V_{CC}	V
		V_{CC} = 2.7 to 4.5 V	0.9 V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P4_0$ – $P4_3$, $P5_0$ – $P5_3$ (Note 4)	V_{CC} = 4.5 to 5.5 V	0.8 V_{CC}		V_{CC}	V
		V_{CC} = 2.7 to 4.5 V	0.9 V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage X_{IN}, $\overline{RESET}$		0.8 V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$		0		0.2 V_{CC}	V
V_{IL}	"L" input voltage $P2_0$ – $P2_7$		0		0.25 V_{CC}	V
V_{IL}	"L" input voltage $P3_0$ – $P3_3$	V_{CC} = 4.5 to 5.5 V	0		0.4 V_{CC}	V
		V_{CC} = 2.7 to 4.5 V	0		0.3 V_{CC}	V
V_{IL}	"L" input voltage $P4_0$ – $P4_3$, $P5_0$ – $P5_3$	V_{CC} = 4.5 to 5.5 V	0		0.4 V_{CC}	V
		V_{CC} = 2.7 to 4.5 V	0		0.3 V_{CC}	V
V_{IL}	"L" input voltage X_{IN}		0		0.16 V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0.12 V_{CC}	V
I_I	Input current $P4_0$ – $P4_3$, $P5_0$ – $P5_3$ (Note 4) V_I > V_{CC}				1	mA
$I_{OH(sum)}$	"H" sum output current $P0_0$ – $P0_7$				–30	mA
$I_{OH(sum)}$	"H" sum output current $P1_0$ – $P1_7$				–30	mA
$I_{OL(sum)}$	"L" sum output current $P0_0$ – $P0_7$, $P4_0$ – $P4_3$, $P5_0$ – $P5_2$				60	mA
$I_{OL(sum)}$	"L" sum output current $P1_0$ – $P1_7$, $P5_3$				60	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$				–10	mA
$I_{OL(peak)}$	"L" peak output current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P4_0$ – $P4_3$, $P5_0$ – $P5_3$				20	mA
$I_{OH(avg)}$	"H" average output current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$ (Note 2)				–5	mA
$I_{OL(avg)}$	"L" average output current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P4_0$ – $P4_3$, $P5_0$ – $P5_3$ (Note 2)				10	mA

Table 13. Recommended operating conditions (cont.)

Symbol	Parameter			Standard values			Unit
				Min.	Typ.	Max.	
f(CNTR)	Timer input frequency CNTR0 (P40), CNTR1 (P41) (Note 3)		f(XIN) = 4 MHz			1	MHz
			f(XIN) = 8 MHz			2	
f(SCLK)	Serial I/O clock input frequency SCLK (P16) (Note 3)	Clock synchronous serial I/O mode	f(XIN) = 4 MHz			250	kHz
			f(XIN) = 8 MHz			500	
		UART mode	f(XIN) = 4 MHz			1	MHz
			f(XIN) = 8 MHz			2	
f(XIN)	Clock input oscillation frequency (Note 3)		VCC = 2.7 to 4.5 V			2.2VCC – 2	MHz
			VCC = 4.5 to 5.5 V			8	

Notes 1 : –40 to 85 °C for extended operating temperature range version.
2 : The average output currents IOH(avg) and IOL(avg) are the average values during 100 ms.
3 : The clock input oscillation frequency is at 50 % duty ratio.
4 : When applying a voltage through a resistor as shown in the figure 55, VI > VCC may be accepted if the current is 1 mA or less.

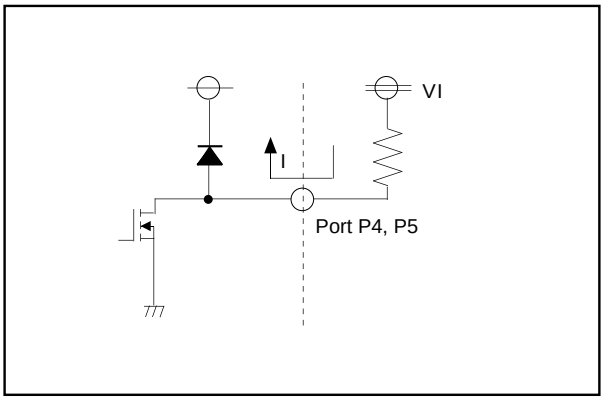


Fig. 55 Notes on use of ports P4 and P5

Notes on Clamp Diode (7481 Group)

(1) Total input current

The current of ports P4 and P5 through the clamp diode can be drawn up to 1.0 mA per port. When a current that cannot be consumed by microcomputer is sent flow to the clamp diode, this may raise the power source pin voltage of the microcomputer.

The system power circuit must be designed so that the power source voltage of the microcomputer may be stabilized within the standard values.

(2) Maximum input voltage

If the input voltage of a signal connected to ports P4 and P5 is beyond VCC + 0.3 V, the input waveform should have a delay exceeding 2 μs/V from the moment that this waveform goes over the voltage.

For using a CR circuit for delay, calculate a proper delay value by the following expression:

$$\frac{dt}{dv} = \frac{t}{0.6 \times V_{IN}} \geq 2 \times 10^{-6} \ (s/V)$$

where VIN = Maximum input voltage amplitude margin and
t = C × R.

The clamp diode of the 7480/7481 group is designed for a level shift of DC signal unlike ordinary switching diodes. Do not apply sudden stress, such as rush current, directly to the diode.

Notes on Countermeasures for Noise and Latch-up (7481 Group)

(1) Connect a bypass capacitor (0.1μF) across the VCC pin and the VSS pin with the shortest possible wiring, using a relatively thick wire.

(2) Connect a bypass capacitor (0.01 μF) across the VREF pin and the VSS pin with the shortest possible wiring, using a relatively thick wire.

(3) In the oscillation circuit, connect across the XIN and XOUT pins with the shortest possible wiring. Connect the GND and VSS pins of the oscillation circuit with the shortest possible wiring, using a relatively thick wire.

(4) In the case of the P33/VPP pin of the built-in programmable ROM version, connect an approximately 5 kΩ resistor to the P33/VPP pin the shortest possible in series.

M37481M4/M8/E8-XXXSP/FP, M37481M2T/M4T/M8T/E8T-XXXSP/FP, M37481E8SS
ELECTRICAL CHARACTERISTICS (7481 Group)

(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C (Note 1) unless otherwise specified)

Table 14. Electrical characteristics

Symbol	Parameter	Test conditions		Standard values			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage	V_{CC} = 5 V, I_{OH} = –5 mA		3			V
	$P0_0$ – $P0_7$, $P1_0$ – $P1_7$	V_{CC} = 3 V, I_{OH} = –1.5 mA		2			
V_{OL}	"L" output voltage $P0_0$ – $P0_7$,	V_{CC} = 5 V, I_{OL} = 10 mA				2	V
	$P1_0$ – $P1_7$, $P4_0$ – $P4_3$, $P5_0$ – $P5_3$	V_{CC} = 3 V, I_{OL} = 3 mA				1	
$V_{T+} - V_{T-}$	Hysteresis $P0_0$ – $P0_7$, (Note 2)	V_{CC} = 5 V			0.5		V
	$P3_0$ – $P3_3$, $P4_0$ – $P4_3$, $P5_0$ – $P5_3$	V_{CC} = 3 V			0.3		
$V_{T+} - V_{T-}$	Hysteresis $P1_6$/S_{CLK}, $P1_4$/RxD	When used as S_{CLK}, RxD	V_{CC} = 5 V		0.5		V
		input	V_{CC} = 3 V		0.3		
$V_{T+} - V_{T-}$	Hysteresis $\overline{RESET}$	V_{CC} = 5 V			0.5		V
		V_{CC} = 3 V			0.3		
I_{IH}	"H" input current	V_I = V_{CC} without pull-up	V_{CC} = 5 V			5	μA
	$P0_0$ – $P0_7$, $P1_0$ – $P1_7$	transistor	V_{CC} = 3 V			3	
I_{IH}	"H" input current	V_I = V_{CC} = 5 V				5	μA
	$P3_0$ – $P3_3$, $P4_0$ – $P4_3$, $P5_0$ – $P5_3$	V_I = V_{CC} = 3 V				3	
I_{IH}	"H" input current $P2_0$ – $P2_7$	V_I = V_{CC} when analog	V_{CC} = 5 V			5	μA
		input is not selected	V_{CC} = 3 V			3	
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}	V_I = V_{CC}	V_{CC} = 5 V			5	μA
		(X_{IN} at stop)	V_{CC} = 3 V			3	
I_{IL}	"L" input current $P0_0$ – $P0_7$,	V_I = 0 V without pull-up	V_{CC} = 5 V			–5	μA
	$P1_0$ – $P1_7$	transistor	V_{CC} = 3 V			–3	
		V_I = 0 V with pull-up	V_{CC} = 5 V	–0.25	–0.5	–1.0	mA
		transistor (Note 3)	V_{CC} = 3 V	–0.08	–0.18	–0.35	
I_{IL}	"L" input current $P3_0$ – $P3_3$,	V_I = 0 V	V_{CC} = 5 V			–5	μA
	$P4_0$ – $P4_3$, $P5_0$ – $P5_3$		V_{CC} = 3 V			–3	
I_{IL}	"L" input current $P2_0$ – $P2_7$	V_I = 0 V when analog input	V_{CC} = 5 V			–5	μA
		is not selected	V_{CC} = 3 V			–3	
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}	V_I = 0 V	V_{CC} = 5 V			–5	μA
		(X_{IN} at stop)	V_{CC} = 3 V			–3	

Notes 1 : –40 to 85 °C for extended operating temperature range version.

2 : Using P0 for key-on wake-up function.

3 : Can be indicated in resistance value as shown below:
When V_{CC} = 5 V: 5 kΩ (min.), 10 kΩ (typ.), 20 kΩ (max.).
When V_{CC} = 3 V: 8.6 kΩ (min.), 16.7 kΩ (typ.), 37.5 kΩ (max.).

M37481M4/M8/E8-XXXSP/FP, M37481M2T/M4T/M8T/E8T-XXXSP/FP, M37481E8SS

Table 14. Electrical characteristics (cont.)

Symbol	Parameter	Test conditions			Standard values			Unit
					Min.	Typ.	Max.	
V_{RAM}	RAM retention voltage	At clock stop mode			2			V
I_{CC}	Power source current	In operating mode	In high-speed mode, $f(X_{IN})$ = 4 MHz, V_{CC} = 5 V	A-D conversion not executed		3.5	7	mA
				A-D conversion in progress		4	8	mA
			In high-speed mode, $f(X_{IN})$ = 4 MHz, V_{CC} = 3 V	A-D conversion not executed		1.8	3.6	mA
				A-D conversion in progress		2	4	mA
			In high-speed mode, $f(X_{IN})$ = 8 MHz, V_{CC} = 5 V	A-D conversion not executed		7	14	mA
				A-D conversion in progress		7.5	15	mA
			In medium-speed mode, $f(X_{IN})$ = 4 MHz, V_{CC} = 5 V	A-D conversion not executed		1.75	3.5	mA
				A-D conversion in progress		2	4	mA
			In medium-speed mode, $f(X_{IN})$ = 4 MHz, V_{CC} = 3 V	A-D conversion not executed		0.9	1.8	mA
				A-D conversion in progress		1	2	mA
			In medium-speed mode, $f(X_{IN})$ = 8 MHz, V_{CC} = 5 V	A-D conversion not executed		3.5	7	mA
				A-D conversion in progress		3.75	7.5	mA
		In wait mode	In high-speed mode, $f(X_{IN})$ = 4 MHz	V_{CC} = 5 V		1	2	mA
				V_{CC} = 3 V		0.5	1	
			In high-speed mode, $f(X_{IN})$ = 8 MHz	V_{CC} = 5 V		2	4	
			In medium-speed mode, $f(X_{IN})$ = 4 MHz	V_{CC} = 5 V		0.9	1.8	mA
				V_{CC} = 3 V		0.45	0.9	
			In medium-speed mode, $f(X_{IN})$ = 8 MHz	V_{CC} = 5 V		1.8	3.6	
		In stop mode	$f(X_{IN})$ = 0 V_{CC} = 5 V	T_a = 25 °C		0.1	1	μA
				T_a = 85 °C		1	10	μA

M37481M4/M8/E8-XXXSP/FP, M37481M2T/M4T/M8T/E8T-XXXSP/FP, M37481E8SS
A-D CONVERSION CHARACTERISTICS (7481 Group)

(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85°C (Note) unless otherwise specified)

Table 15. A-D conversion characteristics

Symbol	Parameter	Test conditions	Standard values			Unit
			Min.	Typ.	Max.	
——	Resolution				8	bits
——	Absolute accuracy (except quantization error)	V_{CC} = V_{REF} = 5.0 V			±2	LSB
T_{CONV}	Conversion time	V_{CC} = 2.7 to 5.5 V, f(X_{IN}) = 4 MHz			25	μs
		V_{CC} = 4.5 to 5.5 V, f(X_{IN}) = 8 MHz			12.5	
V_{VREF}	Reference voltage	V_{CC} = 2.7 to 4.0 V	2		V_{CC}	V
		V_{CC} = 4.0 to 5.5 V	0.5 V_{CC}		V_{CC}	
R_{LADDER}	Ladder resistance		12	35	100	kΩ
V_{IA}	Analog input voltage		0		V_{REF}	V
I_{VREF}	Reference input current	V_{REF} = 5.0 V	50	143	416	μA

Note: –40 to 85 °C for extended operating temperature range version.

MASK ROM CONFIRMATION FORM

GZZ-SH09-84B<56A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37480M2T-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ✵.

✵	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date:			

✵ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M37480M2T-XXXSP ☐ M37480M2T-XXXFP

Checksum code for entire EPROM [ ][ ][ ][ ] (hexadecimal notation)

EPROM type (indicate the type used)

☐ 27128	☐ 27256	☐ 27512
EPROM address	EPROM address	EPROM address
0000_{16} Area for ASCII codes of the name of the product 'M37480M2T–'	0000_{16} Area for ASCII codes of the name of the product 'M37480M2T-'	0000_{16} Area for ASCII codes of the name of the product 'M37480M2T–'
$000F_{16}$	$000F_{16}$	$000F_{16}$
0010_{16}	0010_{16}	0010_{16}
$2FFF_{16}$	$6FFF_{16}$	$EFFF_{16}$
3000_{16} ROM (4K)	7000_{16} ROM (4K)	$F000_{16}$ ROM (4K)
$3FFF_{16}$	$7FFF_{16}$	$FFFF_{16}$

(1) Set "FF_{16}" in the shaded area.
(2) Write the ASCII codes that indicates the name of the product 'M37480M2T–' to addresses 0000_{16} to $000F_{16}$. ASCII codes 'M37480M2T–' are listed on the right. The addresses and data are in hexadecimal notation.

Address	
0000_{16}	'M' = $4D_{16}$
0001_{16}	'3' = 33_{16}
0002_{16}	'7' = 37_{16}
0003_{16}	'4' = 34_{16}
0004_{16}	'8' = 38_{16}
0005_{16}	'0' = 30_{16}
0006_{16}	'M' = $4D_{16}$
0007_{16}	'2' = 32_{16}

Address	
0008_{16}	' T ' = 54_{16}
0009_{16}	' – ' = $2D_{16}$
$000A_{16}$	FF_{16}
$000B_{16}$	FF_{16}
$000C_{16}$	FF_{16}
$000D_{16}$	FF_{16}
$000E_{16}$	FF_{16}
$000F_{16}$	FF_{16}

GZZ-SH09-84B<56A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37480M2T-XXXSP/FP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the start address of the assembler source program.

EPROM type	27128	27256	27512
The pseudo-command	✻=△$C000 △.BYTE△'M37480M2T–'	✻=△$8000 △.BYTE△'M37480M2T–'	✻=△$0000 △.BYTE△'M37480M2T–'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

✵ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered fill out the appropriate mark specification form (32P4B for M37480M2T-XXXSP, 32P2W-A for M37480M2T-XXXFP) and attach to the mask ROM confirmation form.

✵ 3. Comments

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

GZZ-SH09-85B<56A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37480M4-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ✵.

✵	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date:			

✵ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M37480M4-XXXSP ☐ M37480M4-XXXFP

Checksum code for entire EPROM | | | | | (hexadecimal notation)

EPROM type (indicate the type used)

☐ 27128	☐ 27256	☐ 27512
EPROM address	EPROM address	EPROM address
0000_{16} Area for ASCII codes of the name of the product 'M37480M4–'	0000_{16} Area for ASCII codes of the name of the product 'M37480M4-'	0000_{16} Area for ASCII codes of the name of the product 'M37480M4–'
$000F_{16}$	$000F_{16}$	$000F_{16}$
0010_{16}	0010_{16}	0010_{16}
$1FFF_{16}$	$5FFF_{16}$	$DFFF_{16}$
2000_{16} ROM (8K)	6000_{16} ROM (8K)	$E000_{16}$ ROM (8K)
$3FFF_{16}$	$7FFF_{16}$	$FFFF_{16}$

(1) Set "FF_{16}" in the shaded area.
(2) Write the ASCII codes that indicates the name of the product 'M37480M4–' to addresses 0000_{16} to $000F_{16}$. ASCII codes 'M37480M4–' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	' – ' = $2D_{16}$
0001_{16}	'3' = 33_{16}	0009_{16}	FF_{16}
0002_{16}	'7' = 37_{16}	$000A_{16}$	FF_{16}
0003_{16}	'4' = 34_{16}	$000B_{16}$	FF_{16}
0004_{16}	'8' = 38_{16}	$000C_{16}$	FF_{16}
0005_{16}	'0' = 30_{16}	$000D_{16}$	FF_{16}
0006_{16}	'M' = $4D_{16}$	$000E_{16}$	FF_{16}
0007_{16}	'4' = 34_{16}	$000F_{16}$	FF_{16}

MITSUBISHI ELECTRIC

GZZ-SH09-85B<56A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37480M4-XXXSP/FP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the start address of the assembler source program.

EPROM type	27128	27256	27512
The pseudo-command	✻=△$C000 △.BYTE△'M37480M4–'	✻=△$8000 △BYTE △'M37480M4–'	✻=△$0000 △.BYTE△'M37480M4–'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

✵ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered fill out the appropriate mark specification form (32P4B for M37480M4-XXXSP, 32P2W-A for M37480M4-XXXFP) and attach to the mask ROM confirmation form.

✵ 3. Comments

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

GZZ-SH09-86B<56A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37480M4T-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ✵.

✵	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date:			

✵ 1. Confirmation

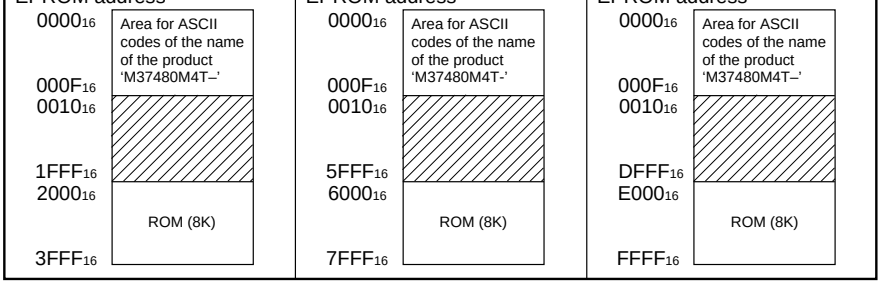
Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M37480M4T-XXXSP ☐ M37480M4T-XXXFP

Checksum code for entire EPROM [ ][ ][ ][ ] (hexadecimal notation)

EPROM type (indicate the type used)

☐ 27128	☐ 27256	☐ 27512
EPROM address	EPROM address	EPROM address



(1) Set "FF$_{16}$" in the shaded area.
(2) Write the ASCII codes that indicates the name of the product 'M37480M4T–' to addresses 0000$_{16}$ to 000F$_{16}$. ASCII codes 'M37480M4T–' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000$_{16}$	'M' = 4D$_{16}$	0008$_{16}$	' T ' = 54$_{16}$
0001$_{16}$	'3' = 33$_{16}$	0009$_{16}$	' – ' = 2D$_{16}$
0002$_{16}$	'7' = 37$_{16}$	000A$_{16}$	FF$_{16}$
0003$_{16}$	'4' = 34$_{16}$	000B$_{16}$	FF$_{16}$
0004$_{16}$	'8' = 38$_{16}$	000C$_{16}$	FF$_{16}$
0005$_{16}$	'0' = 30$_{16}$	000D$_{16}$	FF$_{16}$
0006$_{16}$	'M' = 4D$_{16}$	000E$_{16}$	FF$_{16}$
0007$_{16}$	'4' = 34$_{16}$	000F$_{16}$	FF$_{16}$

GZZ-SH09-86B<56A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37480M4T-XXXSP/FP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the start address of the assembler source program.

EPROM type	27128	27256	27512
The pseudo-command	✻= △$C000 △.BYTE△'M37480M4T–'	✻= △$8000 △.BYTE△'M37480M4T–'	✻= △$0000 △.BYTE△'M37480M4T–'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

✵ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered fill out the appropriate mark specification form (32P4B for M37480M4T-XXXSP, 32P2W-A for M37480M4T-XXXFP) and attach to the mask ROM confirmation form.

✵ 3. Comments

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

GZZ-SH09-87B<56A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37480M8-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ✵.

✵	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date:			

✵ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M37480M8-XXXSP ☐ M37480M8-XXXFP

Checksum code for entire EPROM | | | | | (hexadecimal notation)

EPROM type (indicate the type used)

☐ 27256	☐ 27512
EPROM address	EPROM address
0000_{16} Area for ASCII codes of the name of the product 'M37480M8–'	0000_{16} Area for ASCII codes of the name of the product 'M37480M8–'
$000F_{16}$	$000F_{16}$
0010_{16}	0010_{16}
$3FFF_{16}$ ROM (16K)	$BFFF_{16}$ ROM (16K)
4000_{16}	$C000_{16}$
$7FFF_{16}$	$FFFF_{16}$

(1) Set "FF_{16}" in the shaded area.
(2) Write the ASCII codes that indicates the name of the product 'M37480M8–' to addresses 0000_{16} to $000F_{16}$. ASCII codes 'M37480M8–' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	' – ' = $2D_{16}$
0001_{16}	'3' = 33_{16}	0009_{16}	FF_{16}
0002_{16}	'7' = 37_{16}	$000A_{16}$	FF_{16}
0003_{16}	'4' = 34_{16}	$000B_{16}$	FF_{16}
0004_{16}	'8' = 38_{16}	$000C_{16}$	FF_{16}
0005_{16}	'0' = 30_{16}	$000D_{16}$	FF_{16}
0006_{16}	'M' = $4D_{16}$	$000E_{16}$	FF_{16}
0007_{16}	'8' = 38_{16}	$000F_{16}$	FF_{16}

MITSUBISHI ELECTRIC

GZZ-SH09-87B<56A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37480M8-XXXSP/FP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27256	27512
The pseudo-command	✻=△$8000 △BYTE△'M37480M8-'	✻=△$0000 △BYTE△'M37480M8-'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

✵ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered fill out the appropriate mark specification form (32P4B for M37480M8-XXXSP, 32P2W-A for M37480M8-XXXFP) and attach to the mask ROM confirmation form.

✵ 3. Comments

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

GZZ-SH09-88B<56A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37480M8T-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ✵.

✵ Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
	Date issued	Date:			

✵ 1. Confirmation

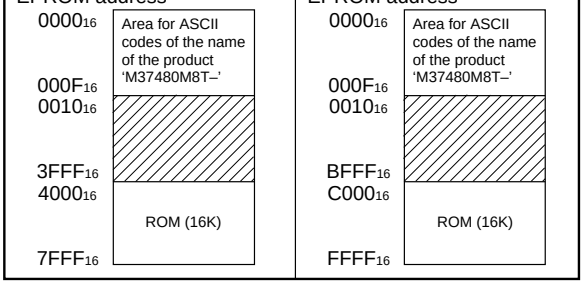
Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M37480M8T-XXXSP ☐ M37480M8T-XXXFP

Checksum code for entire EPROM [ ][ ][ ][ ] (hexadecimal notation)

EPROM type (indicate the type used)

☐ 27256	☐ 27512
EPROM address	EPROM address



(1) Set "FF$_{16}$" in the shaded area.
(2) Write the ASCII codes that indicates the name of the product 'M37480M8T–' to addresses 0000$_{16}$ to 000F$_{16}$. ASCII codes 'M37480M8T–' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000$_{16}$	'M' = 4D$_{16}$	0008$_{16}$	' T ' = 54$_{16}$
0001$_{16}$	'3' = 33$_{16}$	0009$_{16}$	' – ' = 2D$_{16}$
0002$_{16}$	'7' = 37$_{16}$	000A$_{16}$	FF$_{16}$
0003$_{16}$	'4' = 34$_{16}$	000B$_{16}$	FF$_{16}$
0004$_{16}$	'8' = 38$_{16}$	000C$_{16}$	FF$_{16}$
0005$_{16}$	'0' = 30$_{16}$	000D$_{16}$	FF$_{16}$
0006$_{16}$	'M' = 4D$_{16}$	000E$_{16}$	FF$_{16}$
0007$_{16}$	'8' = 38$_{16}$	000F$_{16}$	FF$_{16}$

GZZ-SH09-88B<56A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37480M8T-XXXSP/FP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27256	27512
The pseudo-command	✻=△ $8000 △.BYTE △'M37480M8T-'	✻=△ $0000 △.BYTE △'M37480M8T-'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

✵ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered fill out the appropriate mark specification form (32P4B for M37480M8T-XXXSP, 32P2W-A for M37480M8T-XXXFP) and attach to the mask ROM confirmation form.

✵ 3. Comments

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

GZZ-SH09-78B<56A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37481M2T-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ✵.

✵ Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
	Date issued	Date:			

✵ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M37481M2T-XXXSP ☐ M37481M2T-XXXFP

Checksum code for entire EPROM | | | | | (hexadecimal notation)

EPROM type (indicate the type used)

☐ 27128	☐ 27256	☐ 27512
EPROM address	EPROM address	EPROM address
0000_{16} Area for ASCII codes of the name of the product 'M37481M2T–'	0000_{16} Area for ASCII codes of the name of the product 'M37481M2T-'	0000_{16} Area for ASCII codes of the name of the product 'M37481M2T–'
$000F_{16}$	$000F_{16}$	$000F_{16}$
0010_{16}	0010_{16}	0010_{16}
$2FFF_{16}$	$6FFF_{16}$	$EFFF_{16}$
3000_{16} ROM (4K)	7000_{16} ROM (4K)	$F000_{16}$ ROM (4K)
$3FFF_{16}$	$7FFF_{16}$	$FFFF_{16}$

(1) Set "FF_{16}" in the shaded area.
(2) Write the ASCII codes that indicates the name of the product 'M37481M2T–' to addresses 0000_{16} to $000F_{16}$. ASCII codes 'M37481M2T–' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	' T ' = 54_{16}
0001_{16}	'3' = 33_{16}	0009_{16}	' – ' = $2D_{16}$
0002_{16}	'7' = 37_{16}	$000A_{16}$	FF_{16}
0003_{16}	'4' = 34_{16}	$000B_{16}$	FF_{16}
0004_{16}	'8' = 38_{16}	$000C_{16}$	FF_{16}
0005_{16}	'1' = 31_{16}	$000D_{16}$	FF_{16}
0006_{16}	'M' = $4D_{16}$	$000E_{16}$	FF_{16}
0007_{16}	'2' = 32_{16}	$000F_{16}$	FF_{16}

GZZ-SH09-78B<56A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37481M2T-XXXSP/FP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the start address of the assembler source program.

EPROM type	27128	27256	27512
The pseudo-command	✻=△$C000 △BYTE△'M37481M2T–'	✻=△$8000 △BYTE△'M37481M2T–'	✻=△$0000 △BYTE△ 'M37481M2T–'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

✵ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered fill out the appropriate mark specification form (42P4B for M37481M2T-XXXSP, 44P6N-A for M37481M2T-XXXFP) and attach to the mask ROM confirmation form.

✵ 3. Comments

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

GZZ-SH09-79B<56A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37481M4-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ✵.

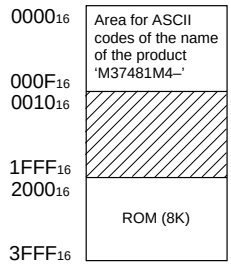
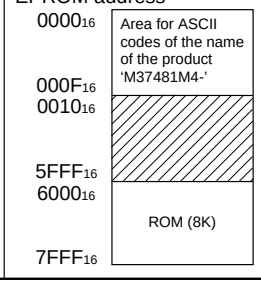
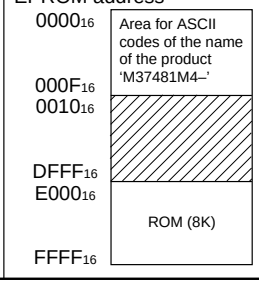
✵	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date:			

✵ 1. Confirmation
Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M37481M4-XXXSP ☐ M37481M4-XXXFP

Checksum code for entire EPROM | | | | | (hexadecimal notation)

EPROM type (indicate the type used)

☐ 27128	☐ 27256	☐ 27512
EPROM address	EPROM address	EPROM address
		

(1) Set "FF$_{16}$" in the shaded area.
(2) Write the ASCII codes that indicates the name of the product 'M37481M4–' to addresses 0000$_{16}$ to 000F$_{16}$. ASCII codes 'M37481M4–' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000$_{16}$	'M' = 4D$_{16}$	0008$_{16}$	' – ' = 2D$_{16}$
0001$_{16}$	'3' = 33$_{16}$	0009$_{16}$	FF$_{16}$
0002$_{16}$	'7' = 37$_{16}$	000A$_{16}$	FF$_{16}$
0003$_{16}$	'4' = 34$_{16}$	000B$_{16}$	FF$_{16}$
0004$_{16}$	'8' = 38$_{16}$	000C$_{16}$	FF$_{16}$
0005$_{16}$	'1' = 31$_{16}$	000D$_{16}$	FF$_{16}$
0006$_{16}$	'M' = 4D$_{16}$	000E$_{16}$	FF$_{16}$
0007$_{16}$	'4' = 34$_{16}$	000F$_{16}$	FF$_{16}$

GZZ-SH09-79B<56A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37481M4-XXXSP/FP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the start address of the assembler source program.

EPROM type	27128	27256	27512
The pseudo-command	✻=△$C000 △.BYTE△'M37481M4–'	✻=△$8000 △.BYTE△'M37481M4–'	✻=△$0000 △.BYTE△'M37481M4–'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

✵ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered fill out the appropriate mark specification form (42P4B for M37481M4-XXXSP, 44P6N-A for M37481M4-XXXFP) and attach to the mask ROM confirmation form.

✵ 3. Comments

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

GZZ-SH09-80B<56A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37481M4T-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ✵.

✵ Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
	Date issued	Date:			

✵ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M37481M4T-XXXSP ☐ M37481M4T-XXXFP

Checksum code for entire EPROM | | | | | (hexadecimal notation)

EPROM type (indicate the type used)

☐ 27128	☐ 27256	☐ 27512
EPROM address	EPROM address	EPROM address
0000_{16} Area for ASCII codes of the name of the product 'M37481M4T–'	0000_{16} Area for ASCII codes of the name of the product 'M37481M4T-'	0000_{16} Area for ASCII codes of the name of the product 'M37481M4T–'
$000F_{16}$	$000F_{16}$	$000F_{16}$
0010_{16}	0010_{16}	0010_{16}
$1FFF_{16}$	$5FFF_{16}$	$DFFF_{16}$
2000_{16} ROM (8K)	6000_{16} ROM (8K)	$E000_{16}$ ROM (8K)
$3FFF_{16}$	$7FFF_{16}$	$FFFF_{16}$

(1) Set "FF_{16}" in the shaded area.
(2) Write the ASCII codes that indicates the name of the product 'M37481M4T–' to addresses 0000_{16} to $000F_{16}$. ASCII codes 'M37481M4T–' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	' T ' = 54_{16}
0001_{16}	'3' = 33_{16}	0009_{16}	' – ' = $2D_{16}$
0002_{16}	'7' = 37_{16}	$000A_{16}$	FF_{16}
0003_{16}	'4' = 34_{16}	$000B_{16}$	FF_{16}
0004_{16}	'8' = 38_{16}	$000C_{16}$	FF_{16}
0005_{16}	'1' = 31_{16}	$000D_{16}$	FF_{16}
0006_{16}	'M' = $4D_{16}$	$000E_{16}$	FF_{16}
0007_{16}	'4' = 34_{16}	$000F_{16}$	FF_{16}

GZZ-SH09-80B<56A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37481M4T-XXXSP/FP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the start address of the assembler source program.

EPROM type	27128	27256	27512
The pseudo-command	✻=△$C000 △.BYTE △'M37481M4T–'	✻=△$8000 △.BYTE △'M37481M4T–'	✻=△$0000 △.BYTE△'M37481M4T–'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

✵ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered fill out the appropriate mark specification form (42P4B for M37481M4T-XXXSP, 44P6N-A for M37481M4T-XXXFP) and attach to the mask ROM confirmation form.

✵ 3. Comments

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

GZZ-SH09-81B<56A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37481M8-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ✵.

✵	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date:			

✵ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M37481M8-XXXSP ☐ M37481M8-XXXFP

Checksum code for entire EPROM [ ][ ][ ][ ] (hexadecimal notation)

EPROM type (indicate the type used)

☐ 27256	☐ 27512
EPROM address	EPROM address
0000_{16} Area for ASCII codes of the name of the product 'M37481M8–'	0000_{16} Area for ASCII codes of the name of the product 'M37481M8–'
$000F_{16}$	$000F_{16}$
0010_{16}	0010_{16}
$3FFF_{16}$ ROM (16K)	$BFFF_{16}$ ROM (16K)
4000_{16}	$C000_{16}$
$7FFF_{16}$	$FFFF_{16}$

(1) Set "FF_{16}" in the shaded area.
(2) Write the ASCII codes that indicates the name of the product 'M37481M8–' to addresses 0000_{16} to $000F_{16}$. ASCII codes 'M37481M8–' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	' – ' = $2D_{16}$
0001_{16}	'3' = 33_{16}	0009_{16}	FF_{16}
0002_{16}	'7' = 37_{16}	$000A_{16}$	FF_{16}
0003_{16}	'4' = 34_{16}	$000B_{16}$	FF_{16}
0004_{16}	'8' = 38_{16}	$000C_{16}$	FF_{16}
0005_{16}	'1' = 31_{16}	$000D_{16}$	FF_{16}
0006_{16}	'M' = $4D_{16}$	$000E_{16}$	FF_{16}
0007_{16}	'8' = 38_{16}	$000F_{16}$	FF_{16}

GZZ-SH09-81B<56A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37481M8-XXXSP/FP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27256	27512
The pseudo-command	✻= △$8000 △.BYTE△ 'M37481M8-'	✻= △$0000 △.BYTE△ 'M37481M8-'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

✵ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered fill out the appropriate mark specification form (42P4B for M37481M8-XXXSP, 44P6N-A for M37481M8-XXXFP) and attach to the mask ROM confirmation form.

✵ 3. Comments

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

GZZ-SH09-82B<56A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37481M8T-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ✵.

✵	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date:			

✵ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M37481M8T-XXXSP ☐ M37481M8T-XXXFP

Checksum code for entire EPROM [ ][ ][ ][ ] (hexadecimal notation)

EPROM type (indicate the type used)

☐ 27256	☐ 27512
EPROM address	EPROM address
0000_{16} Area for ASCII codes of the name of the product 'M37481M8T–'	0000_{16} Area for ASCII codes of the name of the product 'M37481M8T–'
$000F_{16}$	$000F_{16}$
0010_{16}	0010_{16}
$3FFF_{16}$ ROM (16K)	$BFFF_{16}$ ROM (16K)
4000_{16}	$C000_{16}$
$7FFF_{16}$	$FFFF_{16}$

(1) Set "FF_{16}" in the shaded area.
(2) Write the ASCII codes that indicates the name of the product 'M37481M8T–' to addresses 0000_{16} to $000F_{16}$. ASCII codes 'M37481M8T–' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	' T ' = 54_{16}
0001_{16}	'3' = 33_{16}	0009_{16}	' – ' = $2D_{16}$
0002_{16}	'7' = 37_{16}	$000A_{16}$	FF_{16}
0003_{16}	'4' = 34_{16}	$000B_{16}$	FF_{16}
0004_{16}	'8' = 38_{16}	$000C_{16}$	FF_{16}
0005_{16}	'1' = 31_{16}	$000D_{16}$	FF_{16}
0006_{16}	'M' = $4D_{16}$	$000E_{16}$	FF_{16}
0007_{16}	'8' = 38_{16}	$000F_{16}$	FF_{16}

MITSUBISHI ELECTRIC

GZZ-SH09-82B<56A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37481M8T-XXXSP/FP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27256	27512
The pseudo-command	✻=△$8000 △.BYTE △'M37481M8T-'	✻=△$0000 △.BYTE △ 'M37481M8T-'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

✵ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered fill out the appropriate mark specification form (42P4B for M37481M8T-XXXSP, 44P6N-A for M37481M8T-XXXFP) and attach to the mask ROM confirmation form.

✵ 3. Comments

ROM PROGRAMMING CONFIRMATION FORM

GZZ-SH09-91B<56A0>

ROM number	

740 FAMILY ROM PROGRAMMING CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37480E8-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ✵.

✵	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date:			

✵ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce ROM programming based on this data. We shall assume the responsibility for errors only if the ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M37480E8-XXXSP ☐ M37480E8-XXXFP

Checksum code for entire EPROM [ ][ ][ ][ ] (hexadecimal notation)

EPROM type (indicate the type used)

☐ 27256	☐ 27512
EPROM address	EPROM address
0000_{16} Area for ASCII codes of the name of the product 'M37480E8–' $000F_{16}$	0000_{16} Area for ASCII codes of the name of the product 'M37480E8–' $000F_{16}$
0010_{16} ▨ $3FFF_{16}$	0010_{16} ▨ $BFFF_{16}$
4000_{16} ROM (16K) $7FFF_{16}$	$C000_{16}$ ROM (16K) $FFFF_{16}$

(1) Set "FF_{16}" in the shaded area.
(2) Write the ASCII codes that indicates the name of the product 'M37480E8–' to addresses 0000_{16} to $000F_{16}$. ASCII codes 'M37480E8–' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	' – ' = $2D_{16}$
0001_{16}	'3' = 33_{16}	0009_{16}	FF_{16}
0002_{16}	'7' = 37_{16}	$000A_{16}$	FF_{16}
0003_{16}	'4' = 34_{16}	$000B_{16}$	FF_{16}
0004_{16}	'8' = 38_{16}	$000C_{16}$	FF_{16}
0005_{16}	'0' = 30_{16}	$000D_{16}$	FF_{16}
0006_{16}	'E' = 45_{16}	$000E_{16}$	FF_{16}
0007_{16}	'8' = 38_{16}	$000F_{16}$	FF_{16}

GZZ-SH09-91B<56A0>

ROM number	

740 FAMILY ROM PROGRAMMING CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37480E8-XXXSP/FP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27256	27512
The pseudo-command	✻=△$8000 △BYTE△'M37480E8-'	✻=△$0000 △BYTE△'M37480E8-'

Note : If the name of the product written to the EPROMs does not match the name of the ROM programming confirmation form, the ROM processing is disabled. Write the data correctly.

✵ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered. Please submit the shrink DIP package Mark Specification Form (only for built-in One Time PROM microcomputer) for the M37480E8-XXXSP or the 32P2W-A Mark Specification Form for the M37480E8-XXXFP.

✵ 3. Comments

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

GZZ-SH09-92B<56A0>

ROM number	

740 FAMILY ROM PROGRAMMING CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37480E8T-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ✵.

✵	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date:			

✵ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce ROM programming based on this data. We shall assume the responsibility for errors only if the ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M37480E8T-XXXSP ☐ M37480E8T-XXXFP

Checksum code for entire EPROM [ ][ ][ ][ ] (hexadecimal notation)

EPROM type (indicate the type used)

☐ 27256	☐ 27512
EPROM address	EPROM address
0000_{16} Area for ASCII codes of the name of the product 'M37480E8T–'	0000_{16} Area for ASCII codes of the name of the product 'M37480E8T–'
$000F_{16}$	$000F_{16}$
0010_{16}	0010_{16}
$3FFF_{16}$ ROM (16K)	$BFFF_{16}$ ROM (16K)
4000_{16}	$C000_{16}$
$7FFF_{16}$	$FFFF_{16}$

(1) Set "FF_{16}" in the shaded area.
(2) Write the ASCII codes that indicates the name of the product 'M37480E8T–' to addresses 0000_{16} to $000F_{16}$. ASCII codes 'M37480E8T–' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	' T ' = 54_{16}
0001_{16}	'3' = 33_{16}	0009_{16}	' – ' = $2D_{16}$
0002_{16}	'7' = 37_{16}	$000A_{16}$	FF_{16}
0003_{16}	'4' = 34_{16}	$000B_{16}$	FF_{16}
0004_{16}	'8' = 38_{16}	$000C_{16}$	FF_{16}
0005_{16}	'0' = 30_{16}	$000D_{16}$	FF_{16}
0006_{16}	'E' = 45_{16}	$000E_{16}$	FF_{16}
0007_{16}	'8' = 38_{16}	$000F_{16}$	FF_{16}

MITSUBISHI ELECTRIC

GZZ-SH09-92B<56A0>

ROM number	

740 FAMILY ROM PROGRAMMING CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37480E8T-XXXSP/FP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27256	27512
The pseudo-command	✻= △$8000 △.BYTE △'M37480E8T-'	✻= △$0000 △.BYTE △'M37480E8T-'

Note : If the name of the product written to the EPROMs does not match the name of the ROM programming confirmation form, the ROM processing is disabled. Write the data correctly.

✺ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered. Please submit the shrink DIP package Mark Specification Form (only for built-in One Time PROM microcomputer) for the M37480E8T-XXXSP or the 32P2W-A Mark Specification Form for the M37480E8T-XXXFP.

✺ 3. Comments

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

GZZ-SH09-89B<56A0>

ROM number	

740 FAMILY ROM PROGRAMMING CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37481E8-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ✵.

✵	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date:			

✵ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce ROM programming based on this data. We shall assume the responsibility for errors only if the ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M37481E8-XXXSP ☐ M37481E8-XXXFP

Checksum code for entire EPROM [ ][ ][ ][ ] (hexadecimal notation)

EPROM type (indicate the type used)

☐ 27256	☐ 27512
EPROM address	EPROM address
0000_{16} Area for ASCII codes of the name of the product 'M37481E8–'	0000_{16} Area for ASCII codes of the name of the product 'M37481E8–'
$000F_{16}$	$000F_{16}$
0010_{16}	0010_{16}
$3FFF_{16}$	$BFFF_{16}$
4000_{16} ROM (16K)	$C000_{16}$ ROM (16K)
$7FFF_{16}$	$FFFF_{16}$

(1) Set "FF_{16}" in the shaded area.
(2) Write the ASCII codes that indicates the name of the product 'M37481E8–' to addresses 0000_{16} to $000F_{16}$. ASCII codes 'M37481E8–' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	' – ' = $2D_{16}$
0001_{16}	'3' = 33_{16}	0009_{16}	FF_{16}
0002_{16}	'7' = 37_{16}	$000A_{16}$	FF_{16}
0003_{16}	'4' = 34_{16}	$000B_{16}$	FF_{16}
0004_{16}	'8' = 38_{16}	$000C_{16}$	FF_{16}
0005_{16}	'1' = 31_{16}	$000D_{16}$	FF_{16}
0006_{16}	'E' = 45_{16}	$000E_{16}$	FF_{16}
0007_{16}	'8' = 38_{16}	$000F_{16}$	FF_{16}

GZZ-SH09-89B<56A0>

ROM number	

740 FAMILY ROM PROGRAMMING CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37481E8-XXXSP/FP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27256	27512
The pseudo-command	✻=△$8000 △BYTE△'M37481E8-'	✻=△$0000 △BYTE△'M37481E8-'

Note : If the name of the product written to the EPROMs does not match the name of the ROM programming confirmation form, the ROM processing is disabled. Write the data correctly.

✵ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered. Please submit the shrink DIP package Mark Specification Form (only for built-in One Time PROM microcomputer) for the M37481E8-XXXSP or the 44P6N-A Mark Specification Form for the M37481E8-XXXFP.

✵ 3. Comments

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

GZZ-SH09-90B<56A0>

ROM number	

740 FAMILY ROM PROGRAMMING CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37481E8T-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ✵.

✵	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date:			

✵ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce ROM programming based on this data. We shall assume the responsibility for errors only if the ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M37481E8T-XXXSP ☐ M37481E8T-XXXFP

Checksum code for entire EPROM [ ][ ][ ][ ] (hexadecimal notation)

EPROM type (indicate the type used)

☐ 27256	☐ 27512
EPROM address	EPROM address
0000_{16} Area for ASCII codes of the name of the product 'M37481E8T–'	0000_{16} Area for ASCII codes of the name of the product 'M37481E8T–'
$000F_{16}$	$000F_{16}$
0010_{16}	0010_{16}
$3FFF_{16}$	$BFFF_{16}$
4000_{16} ROM (16K)	$C000_{16}$ ROM (16K)
$7FFF_{16}$	$FFFF_{16}$

(1) Set "FF_{16}" in the shaded area.
(2) Write the ASCII codes that indicates the name of the product 'M37481E8T–' to addresses 0000_{16} to $000F_{16}$. ASCII codes 'M37481E8T–' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	' T ' = 54_{16}
0001_{16}	'3' = 33_{16}	0009_{16}	' – ' = $2D_{16}$
0002_{16}	'7' = 37_{16}	$000A_{16}$	FF_{16}
0003_{16}	'4' = 34_{16}	$000B_{16}$	FF_{16}
0004_{16}	'8' = 38_{16}	$000C_{16}$	FF_{16}
0005_{16}	'1' = 31_{16}	$000D_{16}$	FF_{16}
0006_{16}	'E' = 45_{16}	$000E_{16}$	FF_{16}
0007_{16}	'8' = 38_{16}	$000F_{16}$	FF_{16}

MITSUBISHI ELECTRIC

GZZ-SH09-90B<56A0>

ROM number	

740 FAMILY ROM PROGRAMMING CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37481E8T-XXXSP/FP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27256	27512
The pseudo-command	✻= △$8000 △BYTE △'M37481E8T-'	✻=△$0000 △BYTE △'M37481E8T-'

Note : If the name of the product written to the EPROMs does not match the name of the ROM programming confirmation form, the ROM processing is disabled. Write the data correctly.

✺ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered. Please submit the shrink DIP package Mark Specification Form (only for built-in One Time PROM microcomputer) for the M37481E8T-XXXSP or the 44P6N-A Mark Specification Form for the M37481E8T-XXXFP.

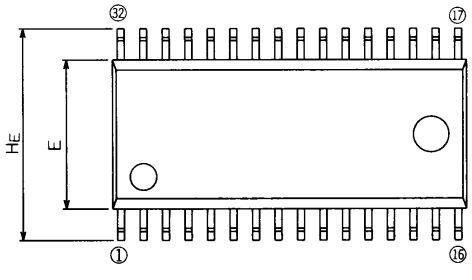
✺ 3. Comments

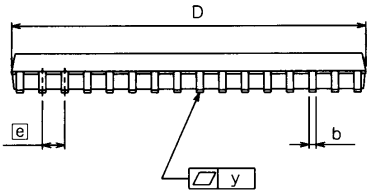
PACKAGE OUTLINE

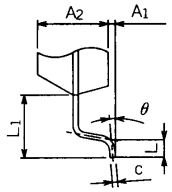
32P2W-A — Plastic 32pin 450mil SOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SOP32-P-450-1.27	—	0.67	Alloy 42

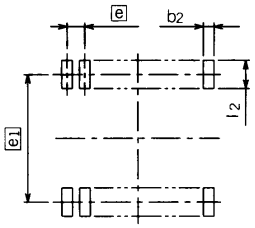
Scale : 2.5/1







Detail F



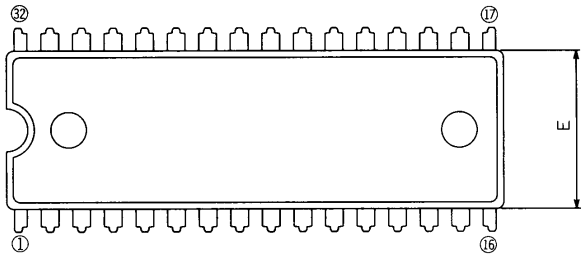
Recommended Mount Pad

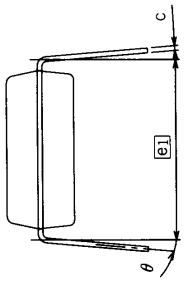
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.4
A_1	0.05	—	—
A_2	—	2.0	—
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	19.8	20.0	20.2
E	8.2	8.4	8.6
e	—	1.27	—
H_E	11.63	11.93	12.23
L	0.3	0.5	0.7
L_1	—	1.765	—
y	—	—	0.15
θ	0°	—	10°
b_2	—	0.76	—
e_1	—	11.43	—
l_2	1.27	—	—

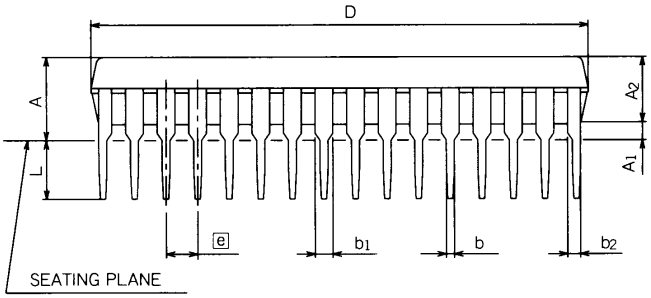
32P4B — Plastic 32pin 400mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP32-P-400-1.78	—	2.2	Alloy 42/Cu Alloy

Scale : 2.5/1







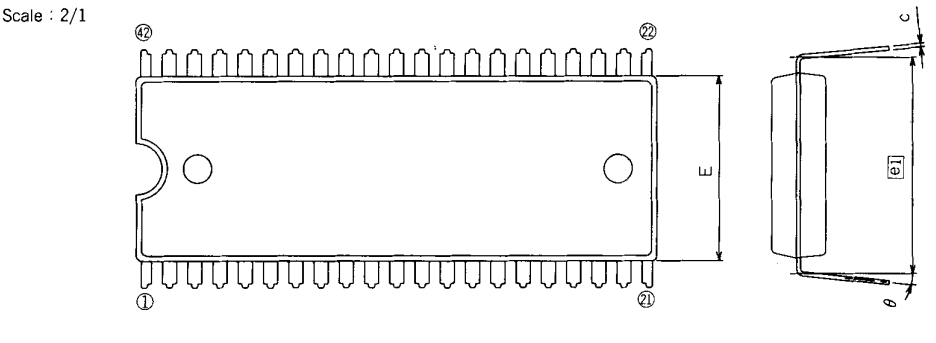
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	5.08
A_1	0.51	—	—
A_2	—	3.8	—
b	0.35	0.45	0.55
b_1	0.9	1.0	1.3
b_2	0.63	0.73	1.03
c	0.22	0.27	0.34
D	27.8	28.0	28.2
E	8.75	8.9	9.05
e	—	1.778	—
e_1	—	10.16	—
L	3.0	—	—
θ	0°	—	15°

42P4B

Plastic 42pin 600mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP42-P-600-1.78	—	4.1	Alloy 42/Cu Alloy

Scale : 2/1



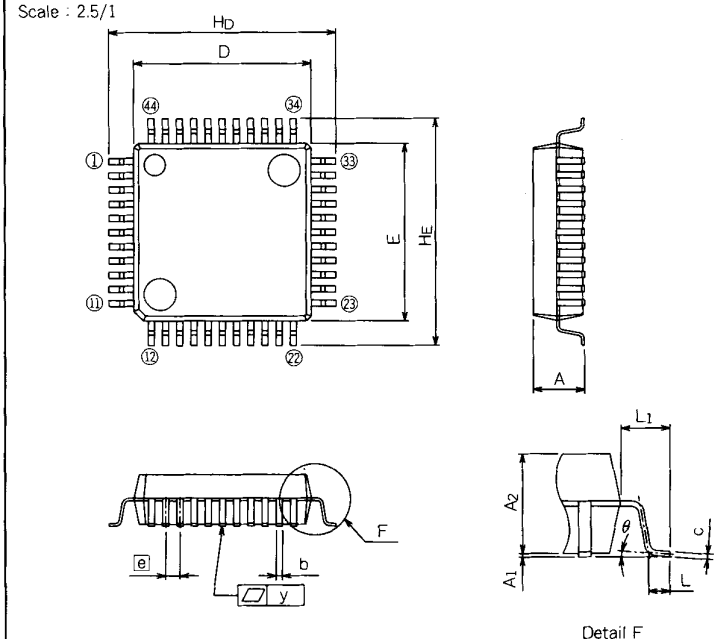
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	5.5
A_1	0.51	—	—
A_2	—	3.8	—
b	0.35	0.45	0.55
b_1	0.9	1.0	1.3
b_2	0.63	0.73	1.03
c	0.22	0.27	0.34
D	36.5	36.7	36.9
E	12.85	13.0	13.15
e	—	1.778	—
e1	—	15.24	—
L	3.0	—	—
θ	0°	—	15°

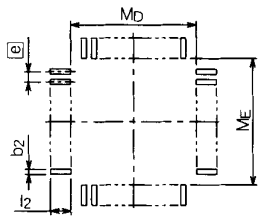
44P6N-A

Plastic 44pin 10×10mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP44-P-1010-0.80	—	0.59	Alloy 42

Scale : 2.5/1





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	3.05
A_1	0	0.1	0.2
A_2	—	2.8	—
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	9.8	10.0	10.2
E	9.8	10.0	10.2
e	—	0.8	—
HD	12.5	12.8	13.1
HE	12.5	12.8	13.1
L	0.4	0.6	0.8
L_1	—	1.4	—
y	—	—	0.1
θ	0°	—	10°
b_2	—	0.5	—
l_2	1.3	—	—
MD	—	10.6	—
ME	—	10.6	—

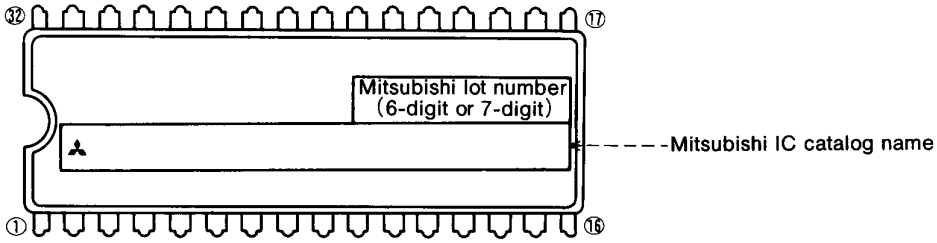
MARK SPECIFICATION FORM

32P4B (32-PIN SHRINK DIP) MARK SPECIFICATION FORM

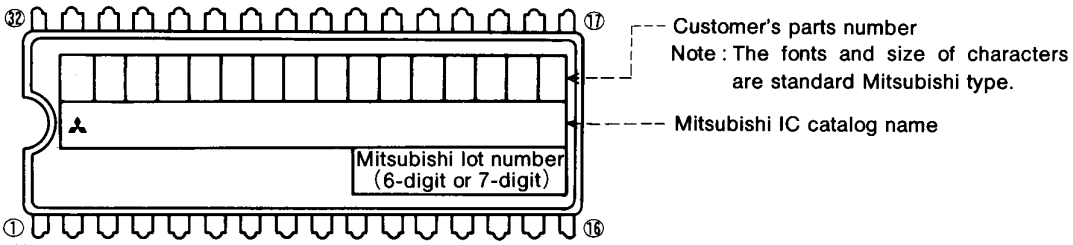
Mitsubishi IC catalog name ☐

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark

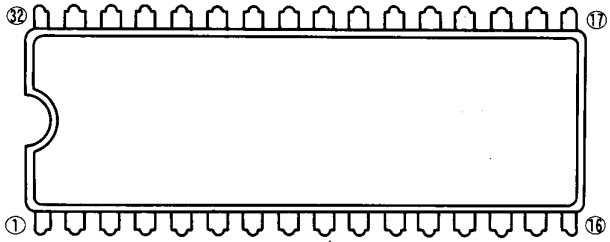


B. Customer's Parts Number + Mitsubishi Catalog Name



Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's parts number can be up to 16 characters :
Only 0~9, A~Z, +, −, /, (,), &, ©, .(period), and ,(comma) are usable.
4 : If the Mitsubishi logo is not required, check the box on the right. Mitsubishi logo is not required ☐

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the upper figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit or 7-digit) and mask ROM number (3-digit) are always marked.
2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.
Special logo required ☐

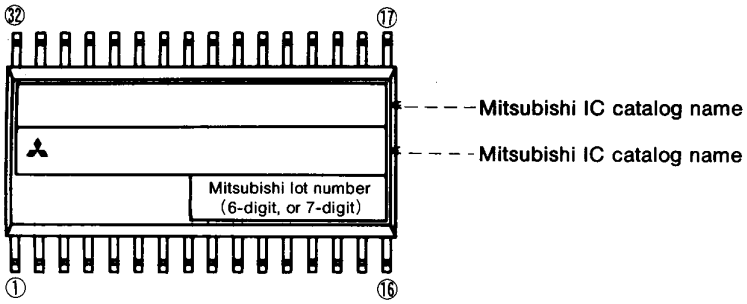
The standard Mitsubishi font is used for all characters except for a logo.

32P2W (32-PIN SOP) MARK SPECIFICATION FORM

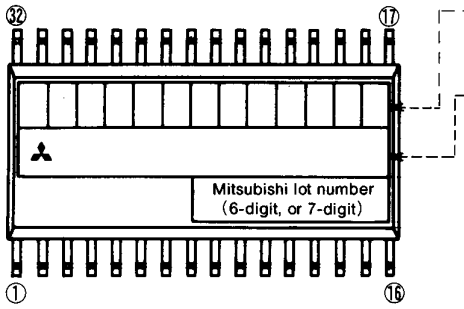
Mitsubishi IC catalog name ☐

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



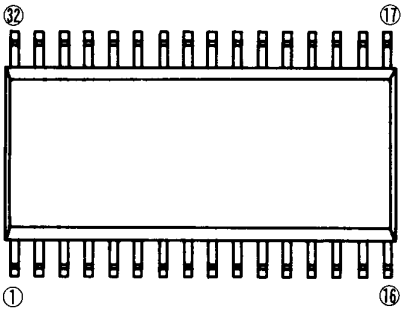
B. Customer's Parts Number + Mitsubishi catalog name



Customer's Parts Number
Note : The fonts and size of characters are standard Mitsubishi type.
Mitsubishi IC catalog name
Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's Parts Number can be up to 13 characters : Only 0~9, A~Z, +, −, /, (,), &, ©, ・ (periods), , (commas) are usable.
4 : If the Mitsubishi logo ⅄ is not required, check the box below.

⅄ Mitsubishi logo is not required ☐

C. Special Mark Required



Note1 : If the Special Mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit, or 7-digit) and Mask ROM number (3-digit) are always marked.
2 : If the customer's trade mark logo must be used in the Special Mark, check the box below. Please submit a clean original of the logo. For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required ☐

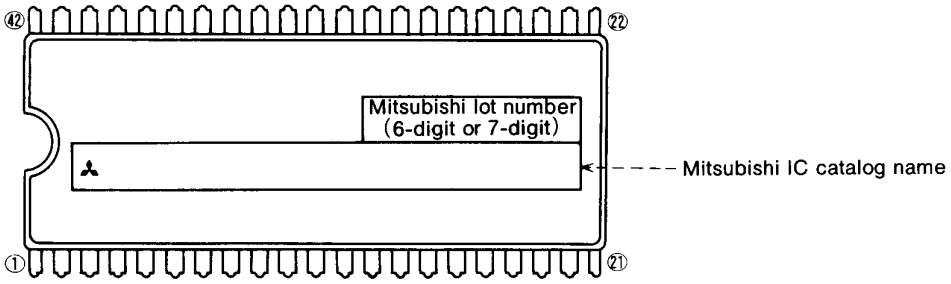
3 : The standard Mitsubishi font is used for all characters except for a logo.

42P4B (42-PIN SHRINK DIP) MARK SPECIFICATION FORM

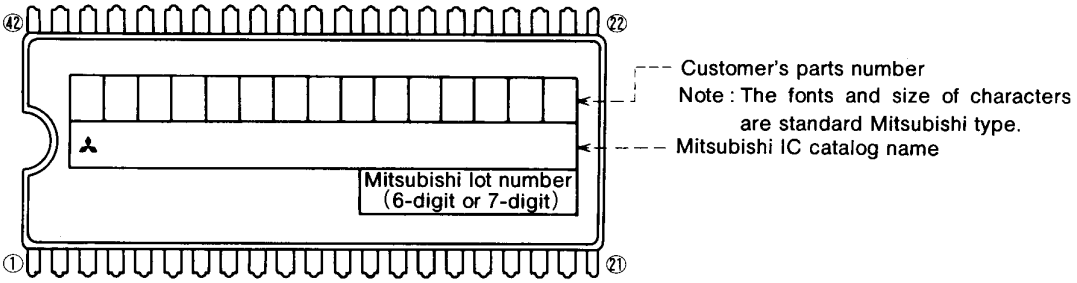
Mitsubishi IC catalog name ☐

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark

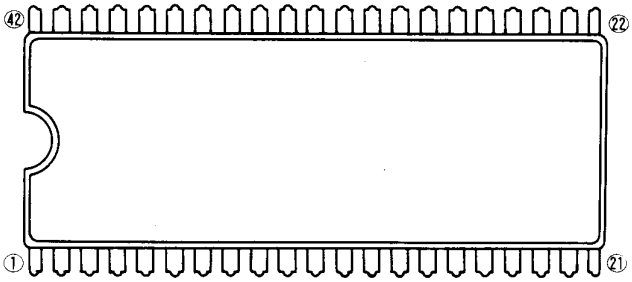


B. Customer's Parts Number + Mitsubishi Catalog Name



Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's parts number can be up to 15 characters :
Only 0~9, A~Z, +, −, /, (,), &, ©, . (period), and , (comma) are usable.
4 : If the Mitsubishi logo ⅄ is not required, check the box on the right. ⅄Mitsubishi logo is not required ☐

C. Special Mark Required



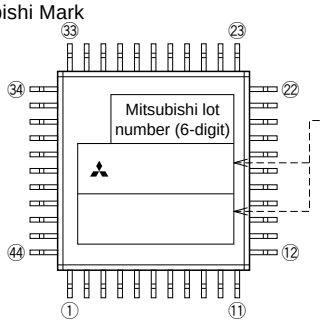
Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the upper figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit or 7-digit) and mask ROM number (3-digit) are always marked.
2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.
Special logo required
The standard Mitsubishi font is used for all characters except for a logo. ☐

44P6N (44-PIN QFP) MARK SPECIFICATION FORM

Mitsubishi IC catalog name

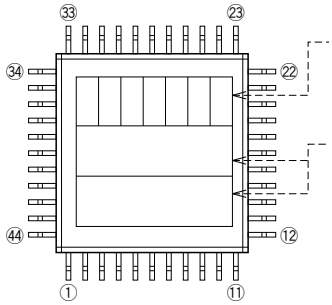
Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



Mitsubishi IC catalog name

B. Customer's Parts Number + Mitsubishi Catalog Name



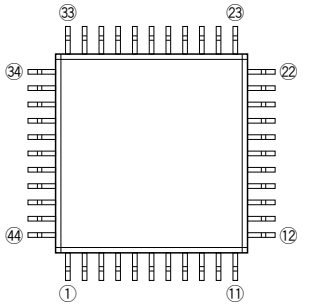
Customer's parts number
Note : The fonts and size of characters are standard Mitsubishi type.

Mitsubishi IC catalog name and Mitsubishi lot number

Note4 : If the Mitsubishi logo is not required, check the box below.
Mitsubishi logo is not required. ☐

Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's parts number can be up to 7 characters : Only 0 ~ 9, A ~ Z,+,–,/, (,), &, ©, . (period), and , (comma) are usable.

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.
2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo. For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required ☐

The standard Mitsubishi font is used for all characters except for a logo.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

MITSUBISHI MICROCOMPUTERS

7480/7481 GROUP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

KI-9711 Printed in Japan (ROD) II
New publication, effective Nov. 1997.
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MITSUBISHI ELECTRIC

REVISION DESCRIPTION LIST	7480/7481 GROUP DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	971130