M52001SP

SYNC SIGNAL PROCESSOR

DESCRIPTION

The M52001SP is a semiconductor integrated circuit that allows automatic selection and waveform shaping of 3 types of sync signal input: separate sync (positive/negative polarities 1~5V_{P-P}), composite sync (positive/negative polarities 1~5V_{P-P}) and sync video (sync negative).
This IC is best suited to sync signal processing in auto tracking type display monitors.

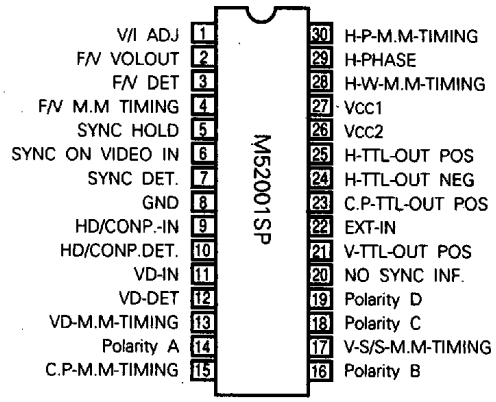
FEATURES

- Sync input presence or absence and polarity information output is available.
- Output amplitude can be varied by the power supply pin only for the output stage.
- A clamping pulse output is available: it is switched to external pulse output automatically in the absence of sync input.
- With F→V conversion function, H_D output, V_D output, clamping pulse timing and pulse width follow the input sync frequency.
- Vertical sync separation by the mono/multi system makes it possible to produce V_D output with more speedy timing than in the integral system.

APPLICATION

Display monitor

PIN CONFIGURATION (TOP VIEW)



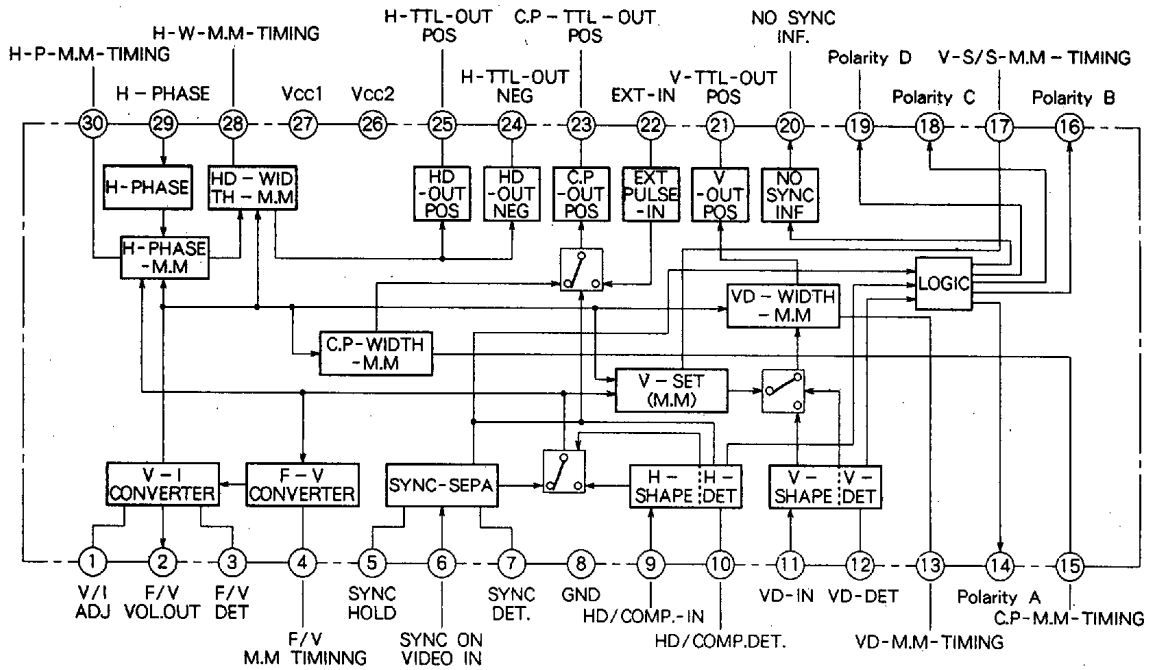
Outline 30P4B

NC: No connection

RECOMMENDED OPERATING CONDITION

Supply voltage range ..... 11.2~13V
Rated supply voltage ..... 12V, 5V (Output stage)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	14	V
P_d	Power dissipation	1333	mW
T_{opr}	Operating temperature	−20~75	℃
T_{stg}	Storage temperature	−40~125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions: Switch setting S1	S2	S3	S4	S5	S6	S7	Input Pin	Input Conditions	Output Pin	Output Waveform	Limits: Min.	Typ.	Max.	Unit
I_{CC1}	Circuit current 1*1	2	2	2	2	1	2	2	27		A1		33.0	44.0	55.0	mA
I_{CC2}	Circuit current 2*2	2	2	2	2	2	1	2	28		A2		6.41	8.55	10.7	mA
SS-HV	Input signal – maximum amplitude voltage*3	1	2	2	2	1	1	2	6	16kHz 2.2VP-P, 1.5 μs	6	(Pin⑥ open voltage) ---- OPEN V-0.1V No pulse should be produced below--- OPEN V - 0.1V.			2.20	V
SS-LV	Input signal – minimum amplitude voltage.*4	1	2	2	2	1	1	2	6	16kHz 0.2VP-P, 1.5 μs	25	16kHz No pulse should be output in this section.	0.2			V
SS-NV	Input signal – maximum noise amplitude voltage*5	1	2	2	2	1	1	2	6	16kHz 0.1VP-P, 1.5 μs	25	No pulse should be output.			0.1	V
14_{OH}	Pin ⑭ output – ON level*6	2	1	1	2	1	1	2	9	16kHz 1VP-P, 7.5 μs	14	DC	4.5	4.8	5.0	V
									11	16kHz 1VP-P, 7.5 μs						
14_{OL}	Pin ⑭ output – OFF level*7	2	1	1	2	1	1	2	9	16kHz 0.7VP-P, 7.5 μs	14	DC			0.4	V
									11	16kHz 0.7VP-P, 7.5 μs						
16_{OH}	Pin ⑯ output – ON level*8	2	1	1	2	1	1	2	9	16kHz 1.0VP-P, 7.5 μs	16	DC	4.5	4.8	5.0	V
									11	16kHz 1.0VP-P, 7.5 μs						

* 1. * 2 : Pins ⑥, ⑨, ⑪ input is not applied.
The Input pin should be connected to GND in C cut.
* 3. The input waveform is free from VIDEO = 2.0Vp − p, SYNC = 0.2 Vp − p front porch and back porch, and VIDEO is completely wehite. The input amplitude voltage is as shown in Table 3. * 4. Make sure that nomalfunction caused by noise is found.
* 5. The input signal (0.1 Vp = p − p) is a dummy noise signal.
* 6. The truth value table is as per Table 1.
* 7. The input signal 0.7VP-P is same as in NO SYNC.
* 8. The truth value table is as per Table 1.

ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test conditions: Switch setting S1	S2	S3	S4	S5	S6	S7	Input Pin	Input Condition	Output Pin	Output Waveform	Limits: Min.	Typ.	Max.	Unit
16_{OL}	Pin ⑯ output – OFF level	2	1	1	2	1	1	2	9	16kHz 1.0Vp-p, 7.5 μs	16	DC			0.4	V
									11	16kHz 1.0Vp-p, 7.5 μs						
18_{OH}	Pin ⑱ output – ON level	2	1	1	2	1	1	2	9	16kHz 1.0Vp-p, 7.5 μs	18	DC	4.5	4.8	5.0	V
									11	16kHz 1.0Vp-p, 7.5 μs						
18_{OL}	Pin ⑱ output – OFF level	2	1	1	2	1	1	2	9	16kHz 1.0Vp-p, 7.5 μs	18	DC			0.4	V
									11	16kHz 1.0Vp-p, 7.5 μs						
19_{OH}	Pin ⑲ output – ON level	2	1	1	2	1	1	2	9	16kHz 1.0Vp-p, 7.5 μs	19	DC	4.5	4.8	5.0	V
									11	16kHz 1.0Vp-p, 7.5 μs						
19_{OL}	Pin ⑲ output – OFF level	2	1	1	2	1	1	2	9	16kHz 1.0Vp-p, 7.5 μs	19	DC			0.4	V
									11	16kHz 1.0Vp-p, 7.5 μs						
20_{OH}	Pin ⑳ output – ON level*9	1	1	2	2	1	1	2	6	16kHz 0.05Vp-p, 7.5 μs	20	DC	4.5	4.8	5.0	V
									9	16kHz 0.7Vp-p, 7.5 μs						
20_{OL}	Pin ⑳ output – OFF level*10	1	2	1	2	1	1	2	6	16kHz 0.2Vp-p, 7.5 μs	20	DC			0.4	V
									11	16kHz 0.7Vp-p, 7.5 μs						

* 9. : The truth value table is as per Table 2.
* 10 : Pins ⑨, ⑪ input 0.7 Vp – p is the same as in NO INPUT.

ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test conditions: Switch setting S1	S2	S3	S4	S5	S6	S7	Input Pin	Input Condition	Output Pin	Output Waveform	Limits: Min.	Typ.	Max.	Unit
24OH	Pin ㉔ HD POS-output – ON peak value	2	1	2	2	1	1	2	9	16kHz 1.0VP-P 7.5 µs	24	Meas V	3.3	3.7		V
24OL	Pin ㉔ HD POS-output – OFF peak value	2	1	2	2	1	1	2	9	16kHz 1.0VP-P 7.5 µs	24	Meas V			0.4	V
25OH	Pin ㉕ HD NEG output – ON peak value	2	1	2	2	1	1	2	9	16kHz 1.0VP-P 7.5 µs	25	Meas V	3.3	3.7		V
25OL	Pin ㉕ HD NEG output – OFF peak value	2	1	2	2	1	1	2	9	16kHz 1.0VP-P 7.5 µs	25	Meas V			0.4	V
HD-HPT-1	HD-H.P-TIME 1	2	1	2	2	1	1	2	9	16kHz 1.0VP-P 7.5 µs	25	input/output Meas Time	2.05	2.63	3.21	µs
									29	Open						
HD-HPT-2	HD-H.P-TIME 2*11	2	1	2	2	1	1	1	9	16kHz 1.0VP-P 7.5 µs	25	input/output Meas Time	0.99	1.52	2.05	µs
									29	DC 12.0V						
HD-PW	HD-PULSE-WIDTH	2	1	2	2	1	1	2	9	16kHz 1.0VP-P 7.5 µs	25	Meas Time	1.13	1.41	1.69	µs
CP-HV1	CP-output peak value 1	2	1	2	2	1	1	2	9	16kHz 1.0VP-P 7.5 µs	23	Meas V	3.3	3.8		V
CP-HV2	CP-output peak value 2	2	1	2	2	1	1	2	9	16kHz 1.0VP-P 7.5 µs	23	Meas V			0.4	V
CP-DT	CP-delay time	2	1	2	2	1	1	2	9	16kHz 1.0VP-P 7.5 µs	23	input/output Meas Time			0.2	µs
CP-PW	CP-PULSE-WIDTH	2	1	2	2	1	1	2	9	16kHz 1.0VP-P 7.5 µs	23	Meas Time	6.02	7.52	9.02	µs
V-S/S-HV1	V-s/s output peak value 1	1	2	2	2	1	1	2	6	NTSC signal	21	Meas V	3.3	3.8		V

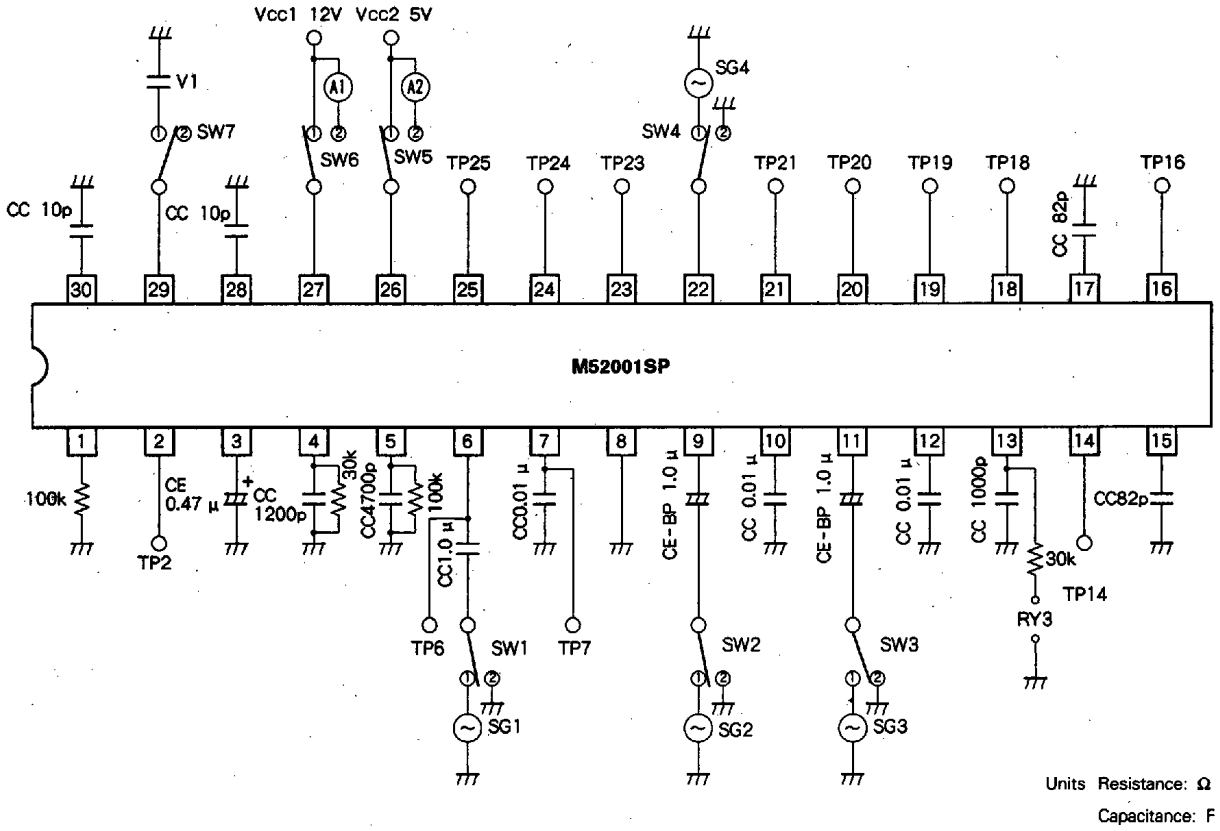
* 11. Pins ⑨, ⑪ input 0.7VP-P is the same as in NO INPUT.

ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test conditions: Switch setting S1	S2	S3	S4	S5	S6	S7	Input Pin	Input Condition	Output Pin	Output Waveform	Limits: Min.	Typ.	Max.	Unit
V-S/S -HV2	V-S/S output peak value 2	1	2	2	2	1	1	2	6	NTSC signal	21	Meas V			0.4	V
V-S/S -DT	V-S/S input delay time	1	2	2	2	1	1	2	6	NTSC signal	21	input/output, Meas Time	6.00	7.50	9.00	μs
V-S/S -PW	V-S/S output pulse width	1	2	2	2	1	1	2	6	NTSC signal	21	Meas Time	213	266	319	μs
F/V -VOL1	F/V voltage-1	2	1	2	2	1	1	2	9	16kHz 1.0VP-P ⇔ 7.5 μs	2	DC	1.47	1.63	1.79	V
F/V -VOL2	F/V voltage-2	2	1	2	2	1	1	2	9	16kHz 1.0VP-P ⇔ 1.5 μs	2	DC	6.09	6.77	7.45	V
H-SW -AC	H-SW operation check*12.	1	1	2	2	1	1	2	6	16kHz 1.0VP-P	25	Meas Time	15.1	15.6	16.1	μs
									9	64kHz 1.0VP-P ⇔ 1.5 μs						
22SL	Pin ㉒ input threshold level*13	2	1	2	1	1	1	2	9	16kHz 0.7VP-P	23	Meas Time	2.2	2.5	2.8	V
									22	64kHz 2.7V / 2.3V ⇔ 1.5 μs						

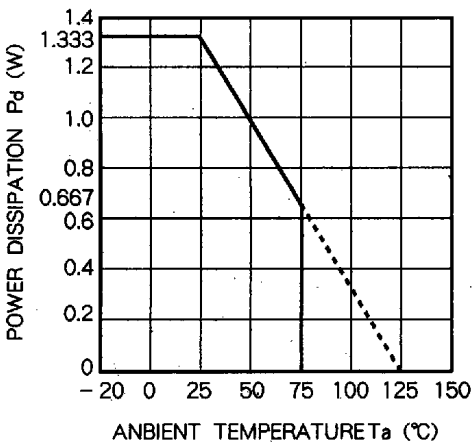
* 12. Check to see if either pin ⑥ or ⑨ input takes precedence, and pin⑨ input takes preocedence. The output priority order is as per Tables 4 and 5.
* 13. Check to see if pin ㉒ input takes precedence.

TEST CIRCUIT

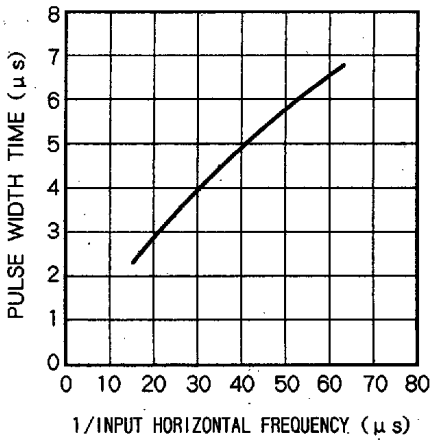


TYPICAL CHARACTERISTICS

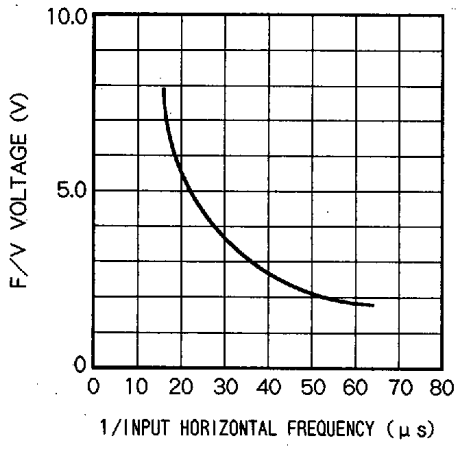
THERMAL DERATING (MAXIMUM RATING)



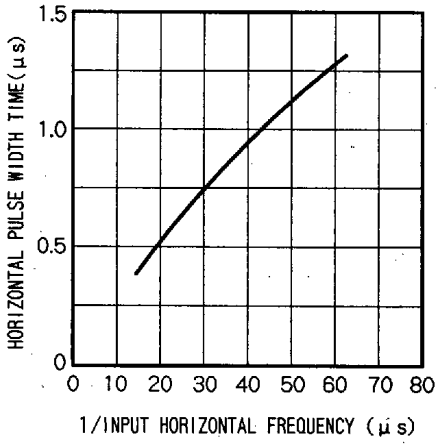
CLAMPING PULSE WIDTH – INPUT HORIZONTAL FREQUENCY CHARACTERISTICS



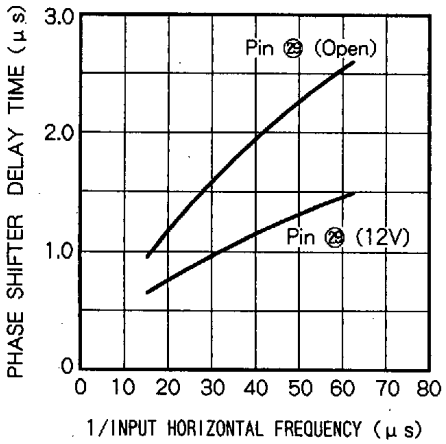
F/V VOLTAGE – INPUT HORIZONTAL FREQUENCYCHARACTERISTICS



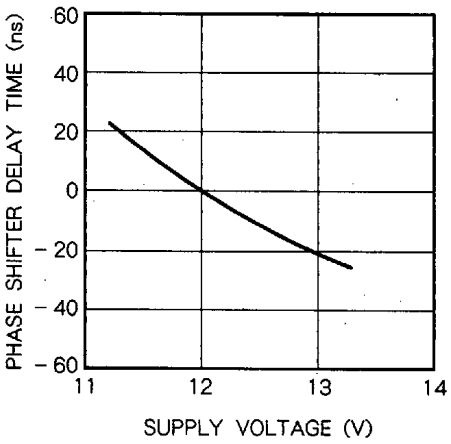
HORIZONTAL PULSE WIDTH – INPUT HORIZONTAL FREQUENCY CHARACTERISTICS



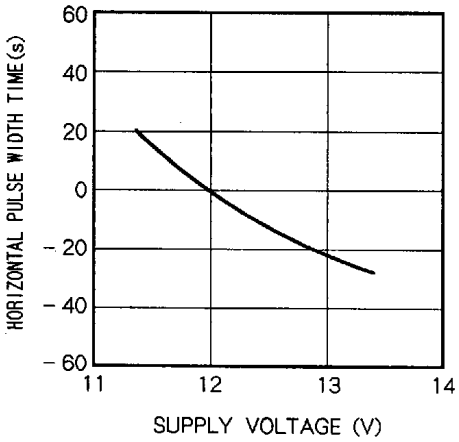
PHASE SHIFTER DELAY TIME – INPUT HORIZONTAL FREQUENCY CHARACTERISTICS



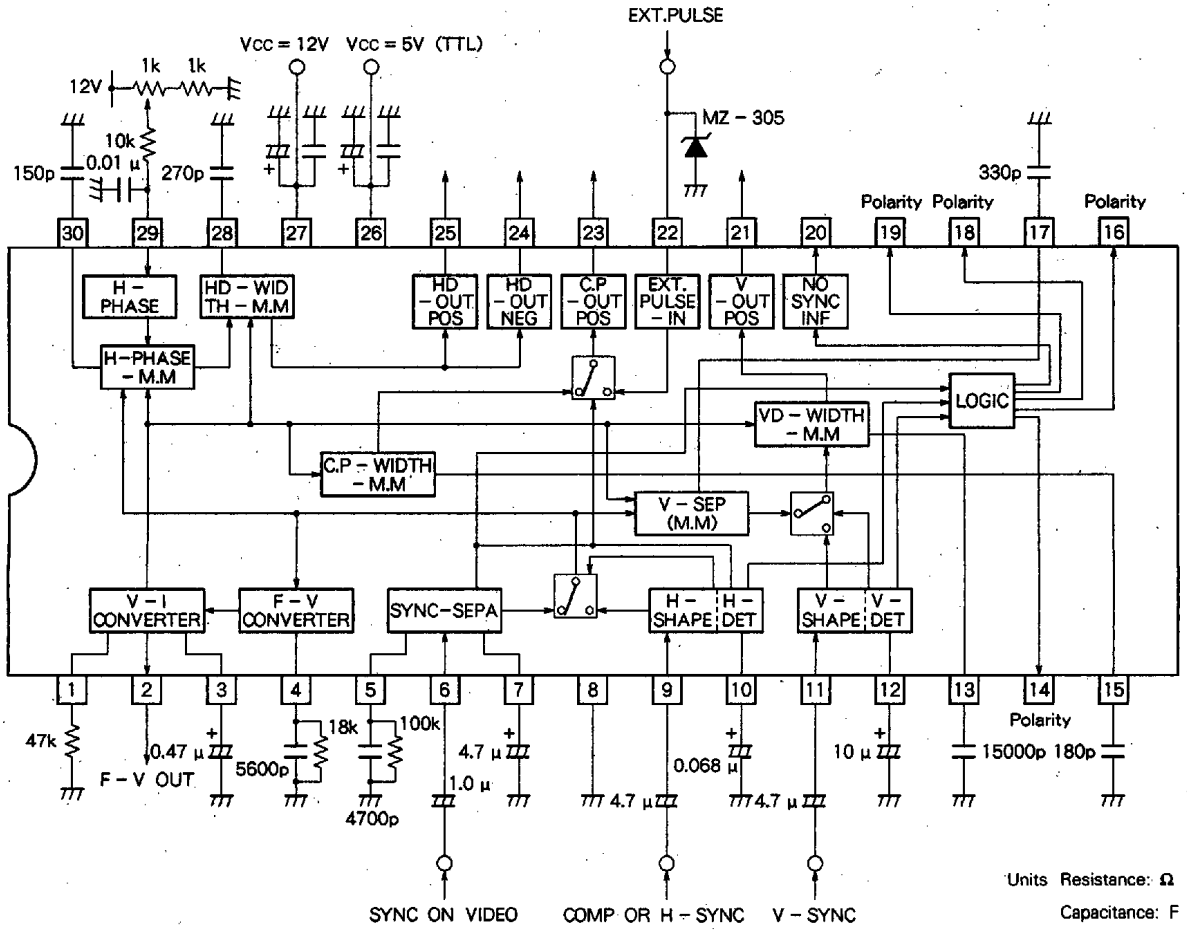
PHASE SHIFTER DELAY TIME – SUPPLY VOLTAGE CHARACTERISTICS



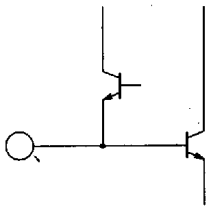
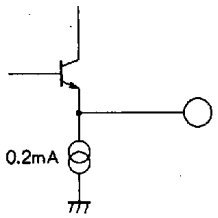
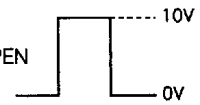
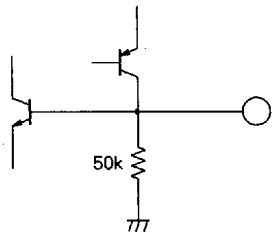
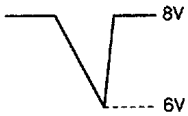
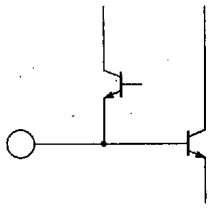
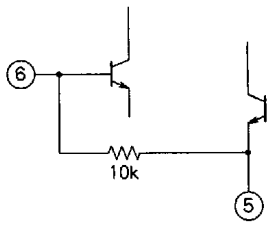
HORIZONTAL PULSE WIDTH VS. SUPPLY VOLTAGE CHARACTERISTICS



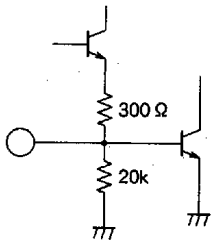
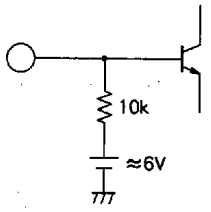
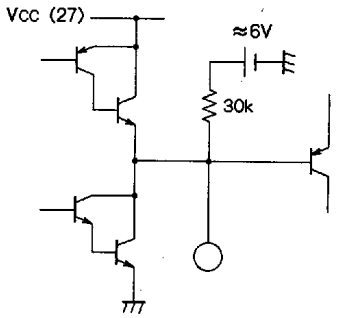
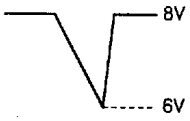
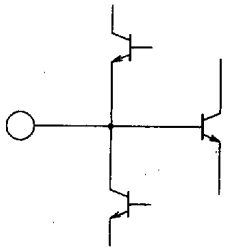
APPLICATION EXAMPLE(fH=1.5kHz, fV=60Hz)



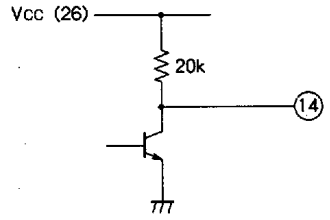
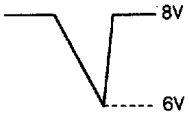
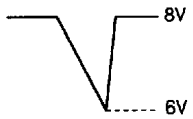
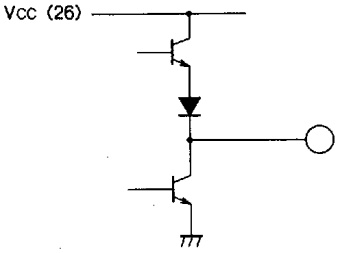
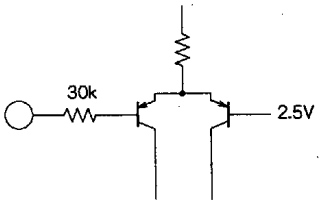
DESCRIPTION OF PIN

Pin No.	Symbol	Pin Voltage	Equivalent Circuit
①	V/I Adj	1.5 to 10 V (DC voltage varies within the above range, depending on the conditions.)	
②	F/V Out	1.5 to 10 V (DC voltage varies within the above range, depending on the conditions.)	
③	F/V Det	At OPEN 	
④	F/V MM TIMING		
⑤	Sync Hold	At OPEN ≈4V	
⑥	Sync On Video In	At OPEN ≈4V	

DESCRIPTION OF PIN (cont.)

Pin No.	Symbol	Pin Voltage	Equivalent Circuit
⑦	Sync Det.	At OPEN 0.8V / 0V	
⑧	GND	—	—
⑨	HD/ Comp. In	At OPEN ≈6V	
⑩	HD/ Comp. Det	At OPEN ≈6V (No signal)	
⑪	V_D In	At OPEN ≈6V	Same as pin ⑨
⑫	V_D Det.	At OPEN ≈6V (No signal)	Same as pin ⑩
⑬	V_D – M.M. TIMING		

DESCRIPTION OF PIN (cont.)

Pin No.	Symbol	Pin Voltage	Equivalent Circuit
⑭	Polarity A	0VDC or 5VDC	
⑮	C.P.– M.M. TIMING		Same as pin ⑬
⑯	Polarity B	0VDC or 5VDC	Same as pin ⑭
⑰	Vert S/S M.M.TIMING	8V 6V 	Same as pin ⑬
⑱	Polarity C	0 VDC or 5 VDC	Same as pin ⑭
⑲	Polarity D		
⑳	NO Sync Inf.		
㉑	Vert Out (Posi)	TTL output	
㉒	Ext Pulse In	Max. 0 to 5 VDC pulse (V_{TH} = 2.5 VDC)	
㉓	C.P. Out	TTL output	Same as pin ㉑
㉔	HD Out (Neg.)		
㉕	HD Out (Posii)		
㉖	Vcc – 2	5V	—
㉗	Vcc – 1	12V	—

DESCRIPTION OF PIN (cont.)

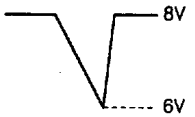
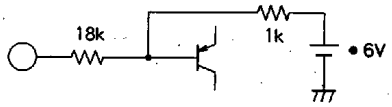
Pin No.	Symbol	Pin Voltage	Equivalent Circuit
㉘	H.W. – M.M. TIMING		Same as pin ⑬
㉙	H – Phase – Adj	At OPEN ≈6V	
㉚	H – Phase – M.M. TIMING		Sam as pin ⑬

Table 1. DECODER IOGIC OUTPUT

Pin ⑨ input HD,COMP.	Pin ⑪ input VD	Output pin ⑭	⑯	⑱	⑲
HD, COMP.(POS.)	NON	H	L	L	L
HD, COMP.(POS.)	VD (POS.)	H	L	L	L
HD, COMP.(POS.)	VD (NEG.)	L	H	L	L
HD, COMP.(NEG.)	NON	L	L	L	H
HD, COMP.(NEG.)	VD (POS.)	L	L	H	L
HD, COMP.(NEG.)	VD (NEG.)	L	L	L	H
NON	NON	L	L	L	H
NON	VD (POS.)	L	L	L	L
NON	VD (NEG.)	L	L	L	H

Table 2.

Pin ⑨ input HD, COMP.	Pin ⑥ input Synvc on Video	Output pin Pin ⑳
HD, COMP.(POS.NEG.)	ON	L
HD, COMP.(NEG.NEG.)	OFF	L
NON	ON	L
	OFF	H

Table 3 ALLOWABLE INPUT AMPLITUDE VOLTAGE

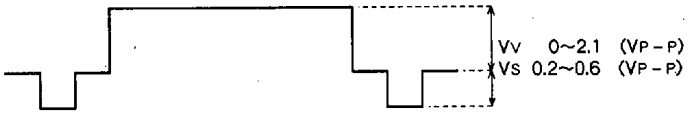
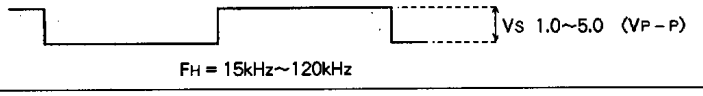
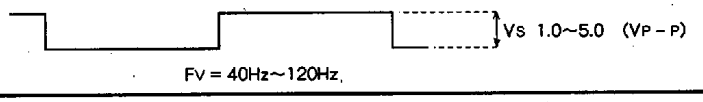
Pin ⑥ input amplitude	
Pin ⑨ input amplitude	
Pin ⑪ input amplitude	

Table 4 OUTPUT PRIORITY PRDER

Input signal (Pin) Pin ⑥	Pin ⑨ COMP.	Pin ⑨ HD	Pin ⑪	Output signal HD Pin ㉔ Pin ㉕	VD Pin ㉑
○	X	X	X	6	6
○	○	X	X	9COMP.	9COMP.
○	X	○	X	9HD	X
○	X	X	○	6	11
○	○	X	○	9COMP.	11
○	X	○	○	9HD	11
X	X	X	X	X	X
X	○	X	X	9COMP.	9COMP.
X	X	○	X	9HD	X
X	X	X	○	X	11
X	○	X	○	9COMP.	11
X	X	○	○	9HD	11

Table 5.

Input signal (Pin) Pin ⑥	Pin ⑨ COMP.	Pin ⑨ HD	Pin ㉒	Output signal CP Pin ㉓
○	X	X	X	6
○	○	X	X	9COMP.
○	X	○	X	9HD
○	X	X	○	6
○	○	X	○	9COMP.
○	X	○	○	9HD
X	X	X	X	X
X	○	X	X	9COMP.
X	X	○	X	9HD
X	X	X	○	22
X	○	X	○	9COMP.
X	X	○	○	9HD

ALLOWABLE MAXIMUM INPUT SIGNAL PULSE DUTY RATIO

Table 6 PIN ⑨ INPUT PULSE(HD, COMP.) fH = 16kHz

Maximum Amaplitude Voltage		1.0	3.3	4.0	5.0
POS.	(%)	15.0	13.8	11.2	9.0
	Time (us)	9.38	8.63	7.00	5.63
NEG.	(%)	15.0	13.0	10.5	8.8
	Time (us)	9.38	8.13	6.56	5.50

Table 7 PIN ⑪ INPUT PULSE (VD) fv = 60Hz

Mximum Amplitude Voltage (VP-P)		1.0	3.3	4.0	5.0
POS.	(%)	14.1	12.1	9.8	7.7
	Time (ms)	2.35	2.02	1.63	1.28
NEG.	(%)	14.8	11.3	9.2	7.5
	Time (ms)	2.47	1.88	1.53	1.25

PRECAUTIONS FOR APPLICATION

1. Input Section

1) Sync on Video input (Pins ⑤, ⑥, ⑦)

Input this signal with sync negative polarity. For sync separation, the sync tip ramping system by external capacitor of pin ⑥ and capacitor/resistor of pin ⑤ is used, and the resistance value of pin ⑤ makes it possible to change the slice level.

The voltage at the sync tip on pin ⑥ is approx. 4V. A filter for judging the presence or absence of Sync on Video input is connected to pin ⑦.

2) Comp Sync/H Sync, V Sync input

Connect composite sync input to pin ⑨, separate sync input "H" and "V" to pins ⑨ and ⑪ respectively.

The bias at pins ⑨, ⑪ is 6V, and the impedance is 10kΩ.

The waveform is shaped and polarity is detected by internal double threshold comparator.

The internal circuit is as shown in Fig. B below, and the average DC voltage of input signal is V_2. Each threshold voltage is set to this V_2 voltage approx. ±0.7V apart. Accordingly, if the duty ratio is small as shown in Fig. A below, operation is performed at approx. $0.7V_{P\text{-}P}$ or more, and if this duty ratio is large, approx. $1.4V_{P\text{-}P}$ is the optimum voltage.

Fig. C shows the standard test value for the allowable input duty.

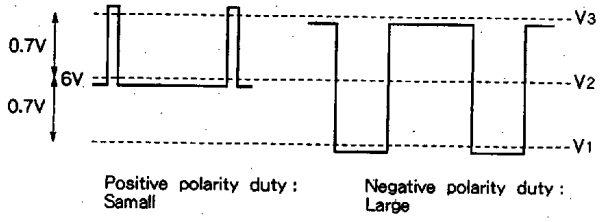
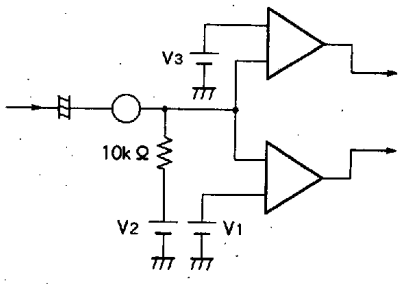


Fig. A



$V_3 - V_2 = V_2 - V_1 = 0.7$
$V_2 \approx 6V_{DC}$

Fig. B

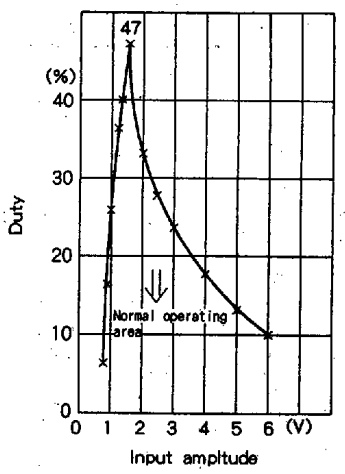


Fig. C

One example for enhancing a real allowable duty ratio at input amplitude $1.4V_{P\text{-}P}$ or more is shown in Fig. D below.

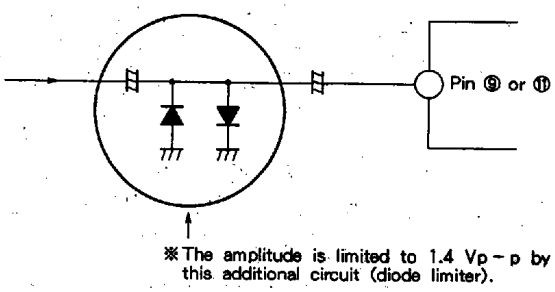


Fig. D

If this circuit is used at other than the specified value, remove the filters at pins ⑩, ⑫, and observe the waveform to make sure that it is shown in Fig. E below.

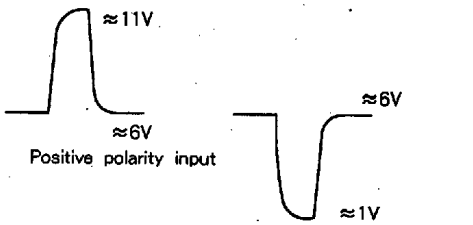


Fig. E

3) Polarity detection and no-input detection (Pins ⑩, ⑫)

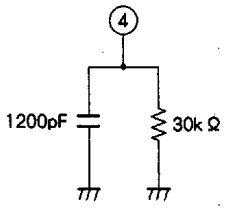
As a filter for detection of polarity or non-input, external capacitance is required. The larger the value is, the smaller the ripple is, and the fewer the malfunctions are. However, the detection response speed becomes low. The capacitance is sufficient if it is 0.05μF or more and 10 μF or more at 15kHz input and 60Hz input respectively, but if this capacitance is made smaller, check

the filter pin waveform under the conditions of the minimum frequency of input sync signal used and the minimum duty ratio, and make sure that 7.5V is exceeded (actually 6.6V) at positive polarity input and 4.5V is not exceeded (actually 5.5V) at negative polarity input.

2.F to V Conversion

1) M/M timing pin for F to V conversion (pin ④)

A pulse of approx. 10 width is obtained with the following constant. Use this resistor and capacitor for setting so that the period is shorter than the maximum horizontal frequency period.



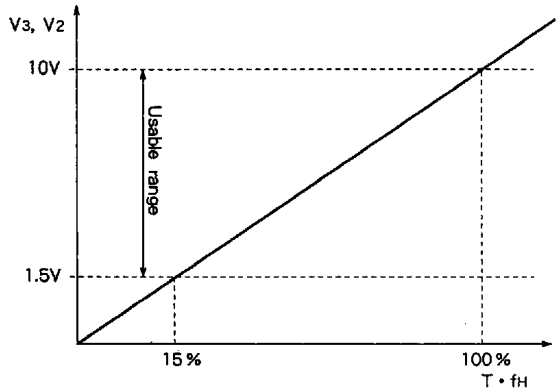
2) F to V converting filter (pin ③)

This filter is used for M/M output smoothing, which is set for 10V and 0V at duty 100% and 0% respectively. The larger the capacitance is, the better it is so long as the response at the unit side is allowed.

3) F to V conversion output (pin ②)

The same voltage as pin ③ voltage is output with the buffer. However, since the D range of buffer amplifier input (pin ③) exceeds 1.5VDC, it is necessary to set a resistor and capacitor on pin ④ so that pin ③ voltage is more than 1.5VDC even at the minimum horizontal frequency.

Consequently, the figure on the right shows the usable frequency range. For example, this is determined by a resistor and capacitor on pin ④. If T=10μs with the pulse width as T, f_H is 15~100kHz, and if T is 5μs, f_H=30~200kHz.

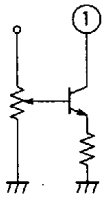


3.H-Phase, H-Width, CP-Width, V-Set & V-Width

1) Timing pin (Pins ①, ㉚, ㉘, ⑰, ⑮, ⑬)

All pins are the same M/M timing ones, and the time constant is determined by the current flowing from pin ① and the capacitance of each timing pin. Pin ① outflow current is normally determined by pin voltage and external resistance value, and since the pin voltage is quite equal to pins ②, ③ voltage, it is dependent on horizontal frequency. At V_1=6V, external resistance 100=kΩ (that is, 60μA) and external capacitance 3,300pF of timing pin, the pulse width of 90μs is obtained.

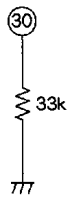
The outflow current at pin ① should preferably be 100μA or less, but it should be noted that if it is 10μA or less, it is vulnerable to the influence of noise. If the current is determined independently of the horizontal frequency, connect pin ① at constant current as shown below or insert a resistor across the earth in parallel to external capacitance of each timing pin with pin ① open. In this case, the usage is quite the same as in pin ④.



2) H-Phase (Pin ㉙)

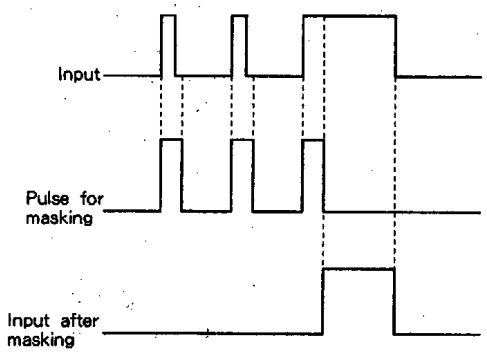
When pin ㉙ voltage is 9V or more, 100% of pin ① current becomes effective, and the delay amount is the smallest. When pin ㉙ voltage is 6V, the effective current is approx. 50%, and the delay amount is double. At 6V or less voltage, the current becomes small, which is liable to become unstable. Since the curve of changes in delay in relation to changes in applied voltage becomes large, be sure to use this at 6V or more.

When the H-phase amount is fixed to the minimum, pin ㉙ is pulled up to Vcc and for pin ㉚, the capacitance may be changed to resistance as shown below.



3) V-Sep (Pin ⑰)

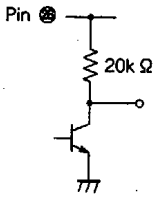
A slightly longer pulse than H sync is produced here, and this pulse masks input for V-Sep. Accordingly, to obtain as early V output as possible, it is necessary to reduce external capacitance at pin ⑰ within the range in which it can be masked.



4. Output Stage

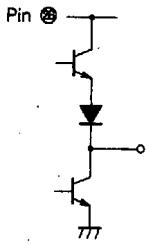
1) Logic output (Pins ⑭, ⑯, ⑱, ⑲, ⑳)

This output is of a collector output type as shown below.



2) Pulse output (Pins ㉑, ㉓, ㉔, ㉕)

This output is of a totem pole type as shown below.



3) Clamping pulse switching

If no input is applied to pins ⑥, ⑨, ⑪, no clamping pulse can be generated inside. In this IC, if a pulse is input to pin ㉒ from the outside in this case, this pulse is output from pin ㉓.

It is necessary to apply pin ㉒ input between 0V and Vcc-2, which is compared at the reference voltage of 1/2(Vcc-2) of the interior.

4) Power supply

The output stage, Ext pulse input unit and internal logic are supplied with Vcc-2 at pin ㉖.

5. Recommended Circuit Example

Shown on the following page is a recommended circuit example nearly when f_H=15kHz and f_V=60Hz. Also, the output at f_H=15.7kHz input with this constant is shown below.