HN27C101A Series

1M (128K x 8-bit) UV and OTP EPROM

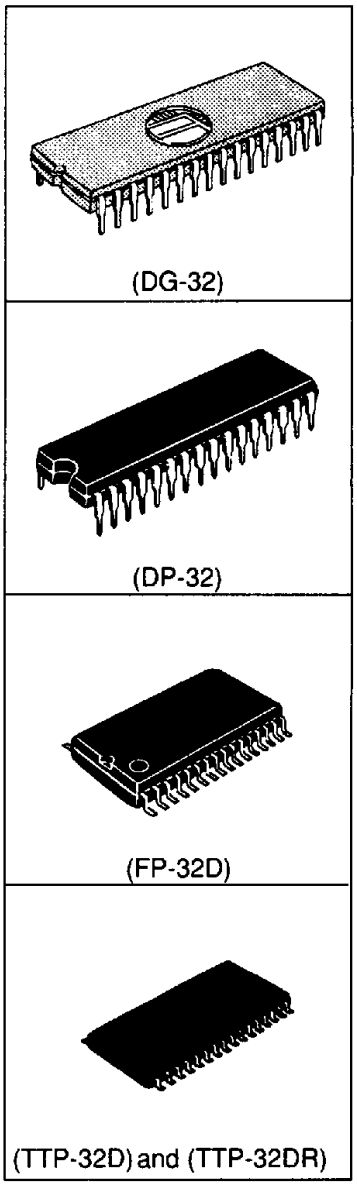
■ DESCRIPTION

The Hitachi HN27C101A is a 1-Megabit Ultraviolet Erasable and One-Time Programmable Electrically Programmable Read Only Memory organized as 131,072 x 8-bits.

The HN27C101A features fast address access times and low power dissipation. This combination makes the HN27C101A suitable for high speed microcomputer systems. The HN27C101A offers high speed programming using page programming mode.

Hitachi's HN27C101A is offered in JEDEC-Standard Byte-Wide EPROM pinouts in 32-pin Ceramic and Plastic DIP and 32-lead Plastic SOP and TSOP packages. This allows socket replacement with Flash Memory and Mask ROMs. The HN27C101A TSOP package is offered in both standard and reverse bend pinouts.

The Ceramic DIP package is erasable by exposure to Ultraviolet light. The Plastic DIP, SOP and TSOP packaged devices are One-Time Programmable and once programmed, can not be rewritten.



■ FEATURES

- Fast Access Times:
  100 ns/120 ns/150 ns/200 ns (max)
- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Low Power Dissipation:
  Active Mode: 50 mW/MHz (typ)
  Standby Mode: 5 µW (typ)
- High Speed Page and Word Programming:
  Page Programming Time: 14 sec (typ)
- Programming Power Supply:
  V_{PP} = 12.5 V ± 0.3 V
- Pin Arrangement:
  JEDEC Standard Byte-Wide EPROM
  Flash Memory and Mask ROM Compatible
- Packages:
  32-pin Ceramic DIP
  32-pin Plastic DIP
  32-lead Plastic SOP
  32-lead Plastic TSOP (Type II)

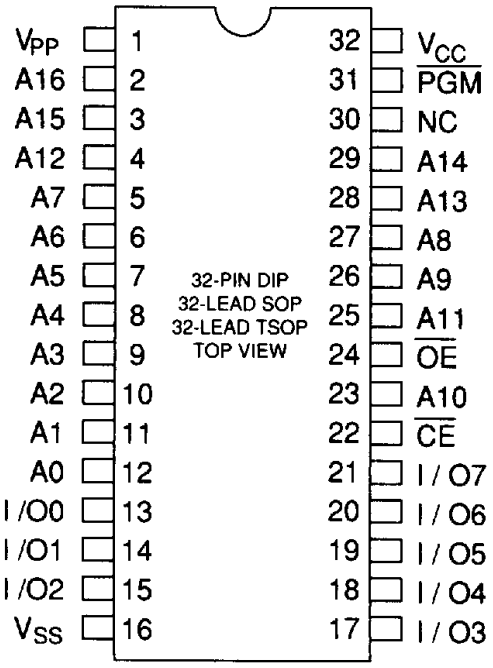
Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN27C101AG-10	100 ns	32-pin Ceramic DIP (DG-32)
HN27C101AG-12	120 ns	
HN27C101AG-15	150 ns	
HN27C101AG-20	200 ns	
HN27C101AP-12	120 ns	32-pin Plastic DIP (DP-32)
HN27C101AP-15	150 ns	
HN27C101AP-20	200 ns	
HN27C101AFP-12	120 ns	32-lead Plastic SOP (FP-32D)
HN27C101AFP-15	150 ns	
HN27C101AFP-20	200 ns	
HN27C101ATT-12	120 ns	32-lead Plastic TSOP (TTP-32D)
HN27C101ATT-15	150 ns	
HN27C101ATT-20	200 ns	
HN27C101ARR-12	120 ns	32-lead Plastic TSOP (TTP-32DR) Reverse bend
HN27C101ARR-15	150 ns	
HN27C101ARR-20	200 ns	

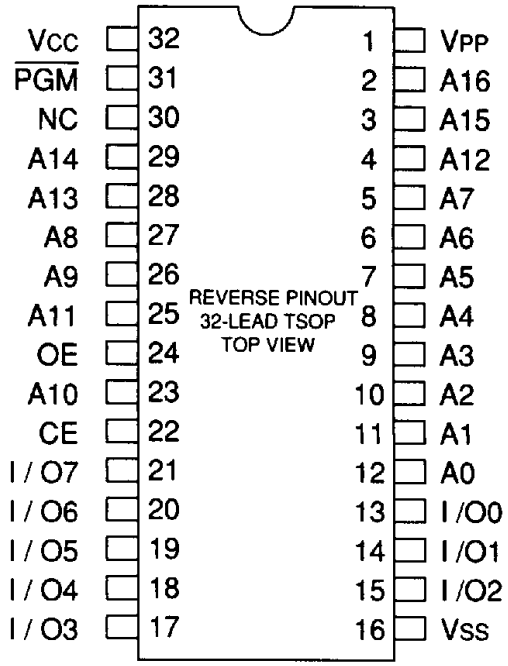
■ PIN ARRANGEMENT

HN27C101AG/P Series
HN27C101AFP Series
HN27C101ATT Series



(PinD32.HN27C101A)

HN27C101ARR Series



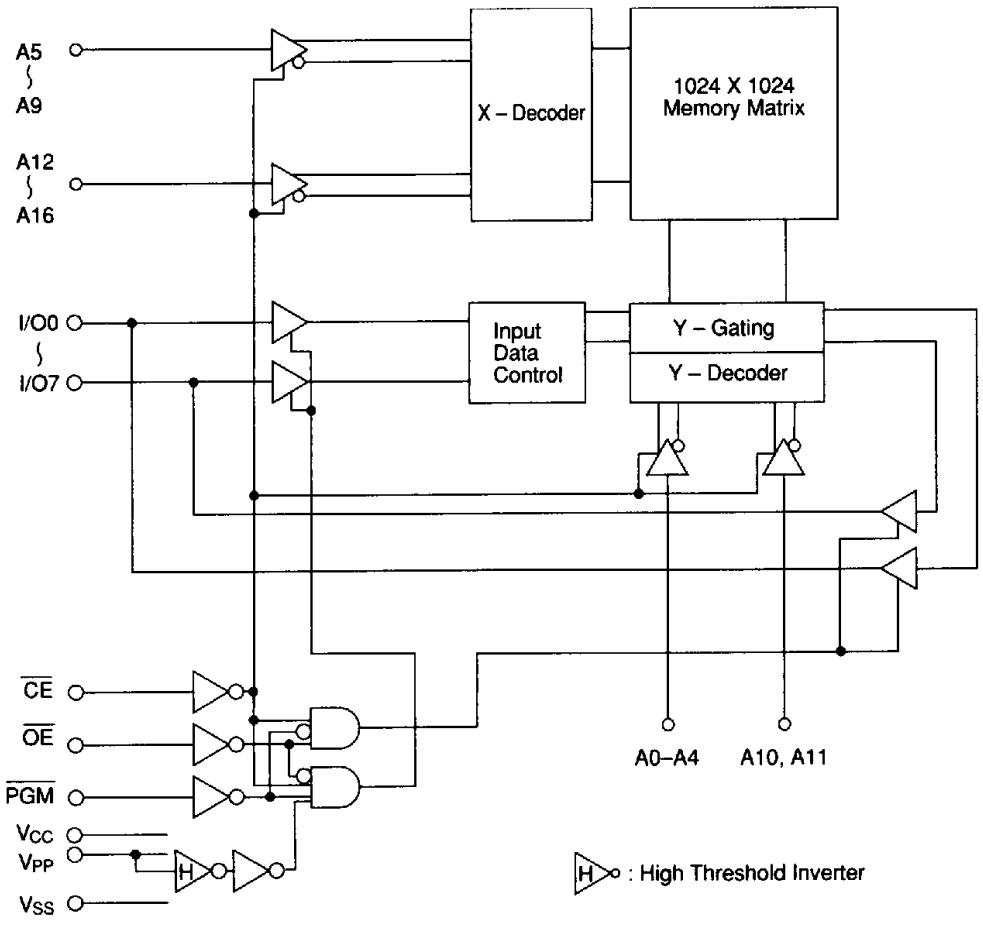
(PinT2.HN27C101A)

4

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{16}	Address
I/O_0 - I/O_7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Programming Supply
V_{SS}	Ground
$\overline{PGM}$	Programming Enable
NC	No Connection

■ BLOCK DIAGRAM



(BD.HN27C101A)

■ MODE SELECTION

Mode	V_{PP}	V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	I/O
Read	V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_{IH}	X[1]	D_{OUT}
Output Disable	V_{CC}	V_{CC}	V_{IL}	V_{IH}	V_{IH}	X	High-Z
Standby	V_{CC}	V_{CC}	V_{IH}	X	X	X	High-Z
Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}
Program Verify	V_{PP}	V_{CC}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}
Page Data Latch	V_{PP}	V_{CC}	V_{IH}	V_{IL}	V_{IH}	X	D_{IN}
Page Program	V_{PP}	V_{CC}	V_{IH}	V_{IH}	V_{IL}	X	High-Z
Program Inhibit	V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_{IL}	X	High-Z
	V_{PP}	V_{CC}	V_{IL}	V_{IH}	V_{IH}	X	High-Z
	V_{PP}	V_{CC}	V_{IH}	V_{IL}	V_{IL}	X	High-Z
	V_{PP}	V_{CC}	V_{IH}	V_{IH}	V_{IH}	X	High-Z
Identifier	V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_{IH}	V_H	ID

Notes: 1. X = Don't Care. $V_{PP} = 0$ V to V_{CC}.
2. $11.5\ V \leq V_H \leq 12.5\ V$

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Programming Voltage [1]	V_{PP}	-0.6 to +13.5	V
All Input and Output Voltage [1,2]	V_{IN}, V_{OUT}	-0.6 to +7.0	V
A_9 and $\overline{OE}$ Voltage [2]	V_{ID}	-0.6 to +13.0	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-65 to +125 [3] -55 to +125 [4]	°C
Storage Temperature Under Bias	T_{BIAS}	0 to +80	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN}, V_{OUT}, and V_{ID} min = -1.0V for pulse width ≤ 20 ns.
3. HN27C101AG.
4. HN27C101AP, HN27C101AFP, HN27C101ATT and HN27C101ARR.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	10	pF	$V_{IN} = 0V$
Output Capacitance	C_{OUT}	-	15	pF	$V_{OUT} = 0V$

4

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 5.5 V
Output Leakage Current	I_{LO}	-	-	2	µA	V_{OUT} = 5.5 V/0.45 V
Operating V_{CC} Current	I_{CC1}	-	-	30	mA	I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}
	I_{CC2}	-	-	30	mA	I_{OUT} = 0 mA, f = 5 MHz
	I_{CC3}	-	-	50	mA	I_{OUT} = 0 mA, f = 10 MHz
Standby V_{CC} Current	I_{SB}	-	-	1	mA	$\overline{CE}$ = V_{IH}
V_{PP} Current	I_{PP1}	-	1	20	µA	V_{PP} = 5.5 V
Input Voltage	V_{IH}	2.2	-	V_{CC} + 1 [2]	V	
	V_{IL}	-0.3 [1]	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.45	V	I_{OL} = 2.1 mA

Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns.
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns.
If V_{IH} is over the specified maximum value, Read operation can not be guaranteed.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

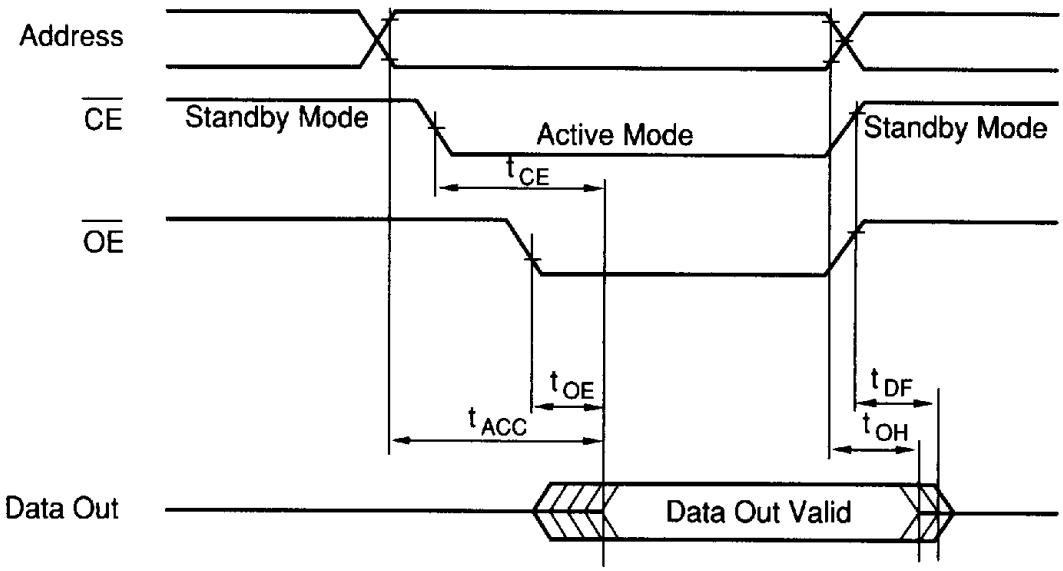
Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V/2.0 V

Item	Symbol	-10		-12		-15		-20		Unit	Test Condition
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Address Access Time	t_{ACC}	-	100	-	120	-	150	-	200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Chip Enable Access Time	t_{CE}	-	100	-	120	-	150	-	200	ns	$\overline{OE}$ = V_{IL}
Output Enable Access Time	t_{OE}	-	60	-	60	-	70	-	70	ns	$\overline{CE}$ = V_{IL}
Output Disable to High-Z [1]	t_{DF}	0	50	0	50	0	50	0	50	ns	$\overline{CE}$ = V_{IL}
Output Hold to Address Change	t_{OH}	0	-	0	-	0	-	0	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(TD.R.HN27C101A)

■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_a = 25 °C ± 5 °C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 0 V to V_{CC}
Operating V_{CC} Current	I_{CC}	-	-	30	mA	
Operating V_{PP} Current	I_{PP}	-	-	40	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}
Input Voltage [3]	V_{IH}	2.2	-	V_{CC} +.5 [6]	V	
	V_{IL}	- 0.1[5]	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.45	V	I_{OH} = 2.1 mA

Notes:
1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13 V, including overshoot.
3. Device reliability may be adversely affected if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not change V_{PP} from V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = low.
5. V_{IL} min = -0.6 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation can not be guaranteed.

4

■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.5 v ± 0.3 V, T_a = 25°C ± 5°C)

Test Conditions

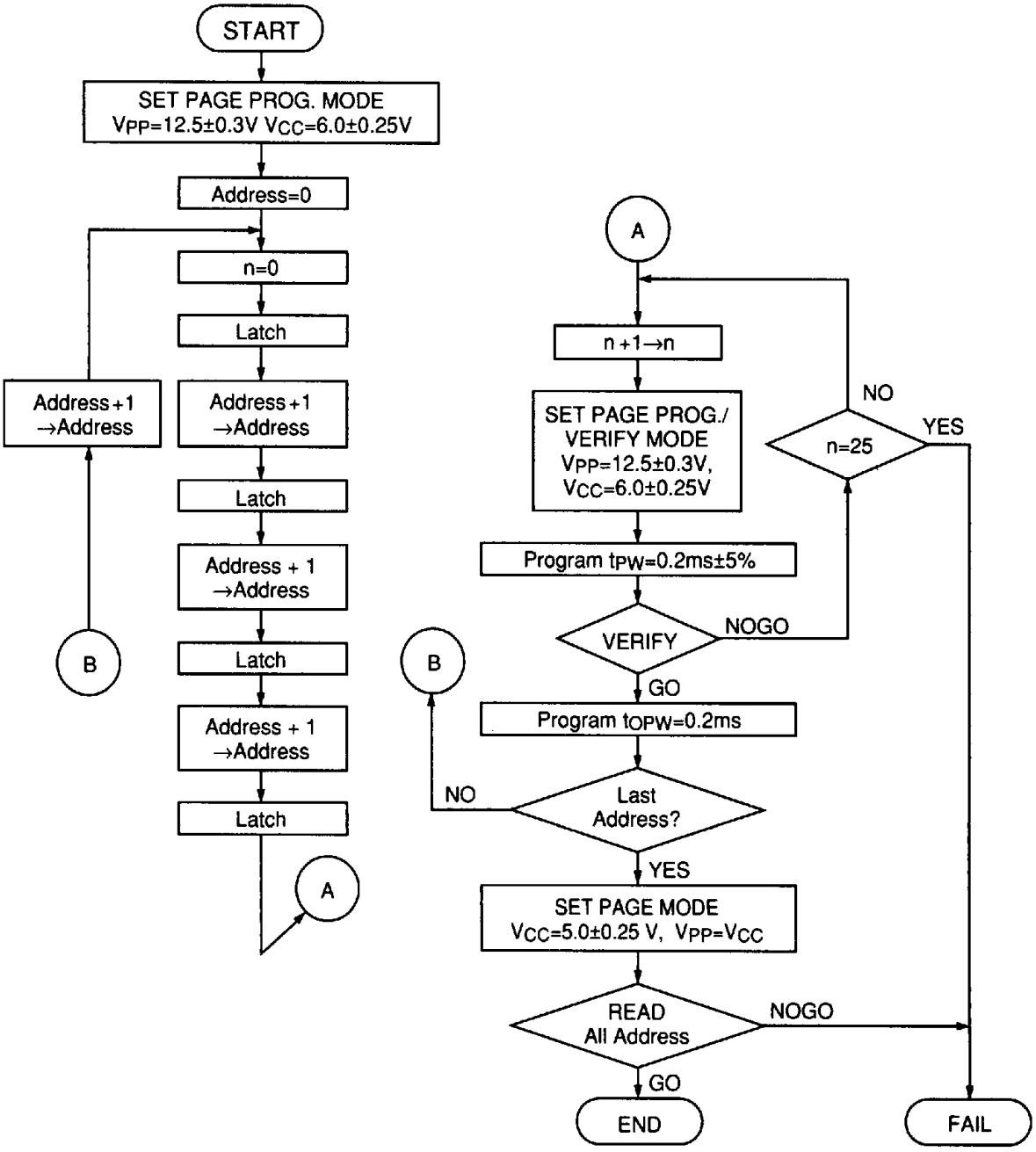
- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timing: 0.8 V / 2.0V

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	2	-	-	µs	
Address Hold Time	t_{AH}	0	-	-	µs	
Data Setup Time	t_{DS}	2	-	-	µs	
Data Hold Time	t_{DH}	2	-	-	µs	
Chip Enable Setup Time	t_{CES}	2	-	-	µs	
V_{PP} Setup Time	t_{VPS}	2	-	-	µs	
V_{CC} Setup Time	t_{VCS}	2	-	-	µs	
Output Enable Setup Time	t_{OES}	2	-	-	µs	
Output Disable Time	t_{DF}	0	-	130	ns	
$\overline{PGM}$ Initial Programming Pulse Width	t_{PW}	0.19	0.20	0.21	ms	
$\overline{PGM}$ Overprogramming Pulse Width	t_{OPW}	0.19	-	5.25	ms	
Data Valid from Output Enable Time	t_{OE}	0	-	150	ns	
Output Enable Pulse During Data Latch	t_{LW}	1	-	-	µs	
Output Enable Hold Time	t_{OEH}	2	-	-	µs	
Chip Enable Hold Time	t_{CEH}	2	-	-	µs	
$\overline{PGM}$ Setup Time	t_{PGMS}	2	-	-	µs	

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ PAGE PROGRAMMING FLOWCHART

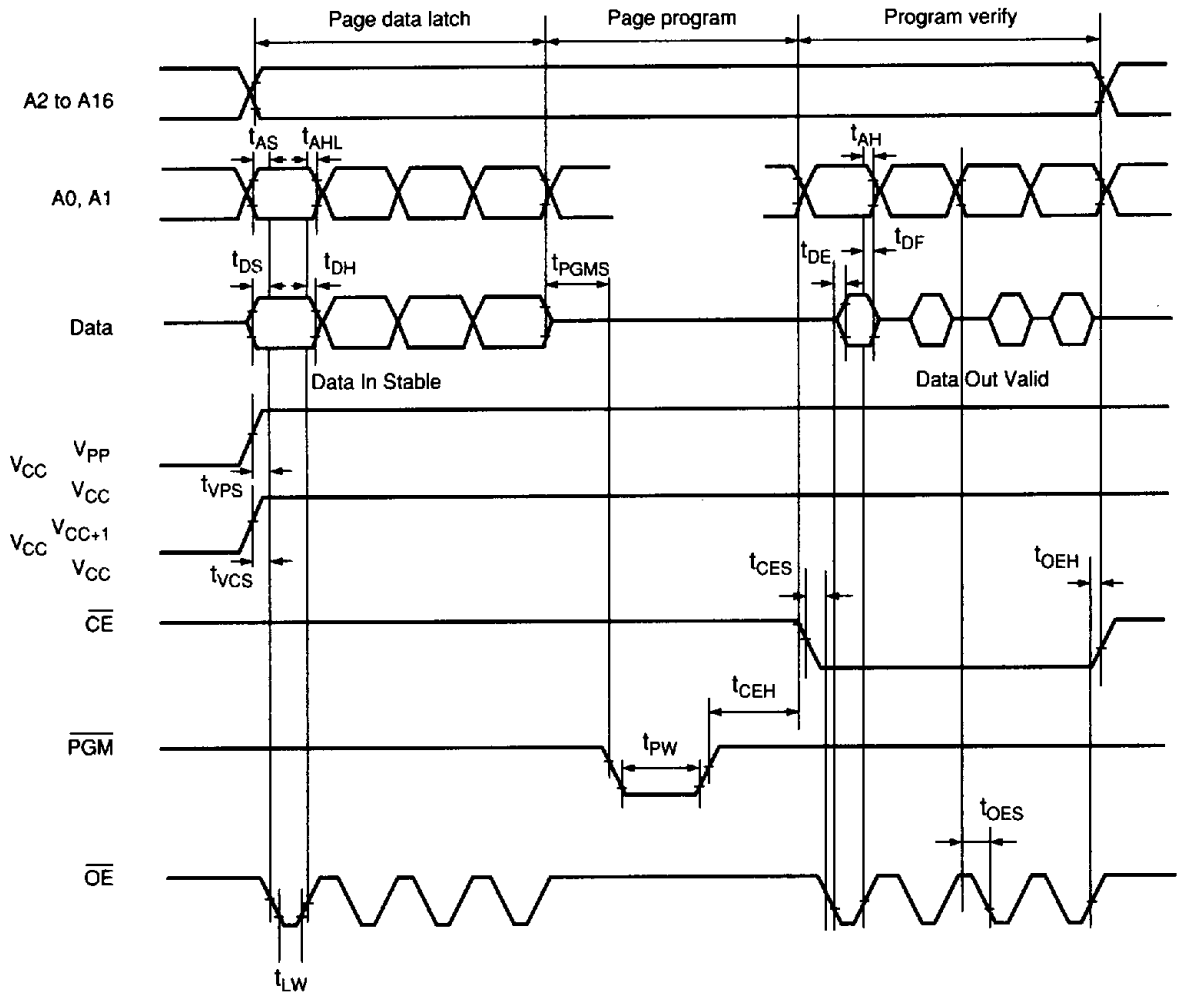
The Hitachi HN27C101A can be programmed with the high performance Page Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.



(FC.PP.HN27C101A)

4

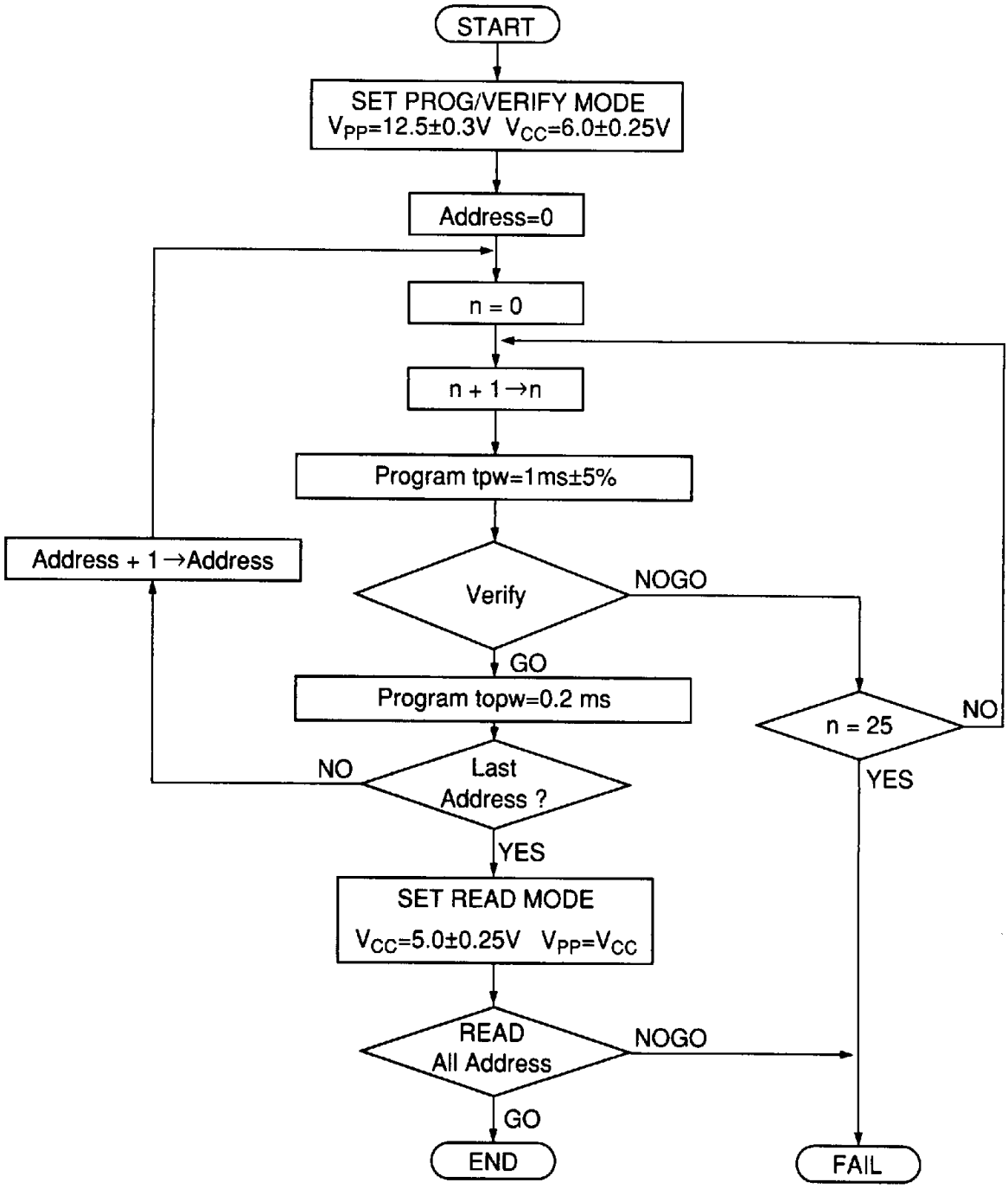
■ PAGE PROGRAMMING TIMING WAVEFORM



(TD.PP.HN27C101A)

■ BYTE PROGRAMMING FLOWCHART

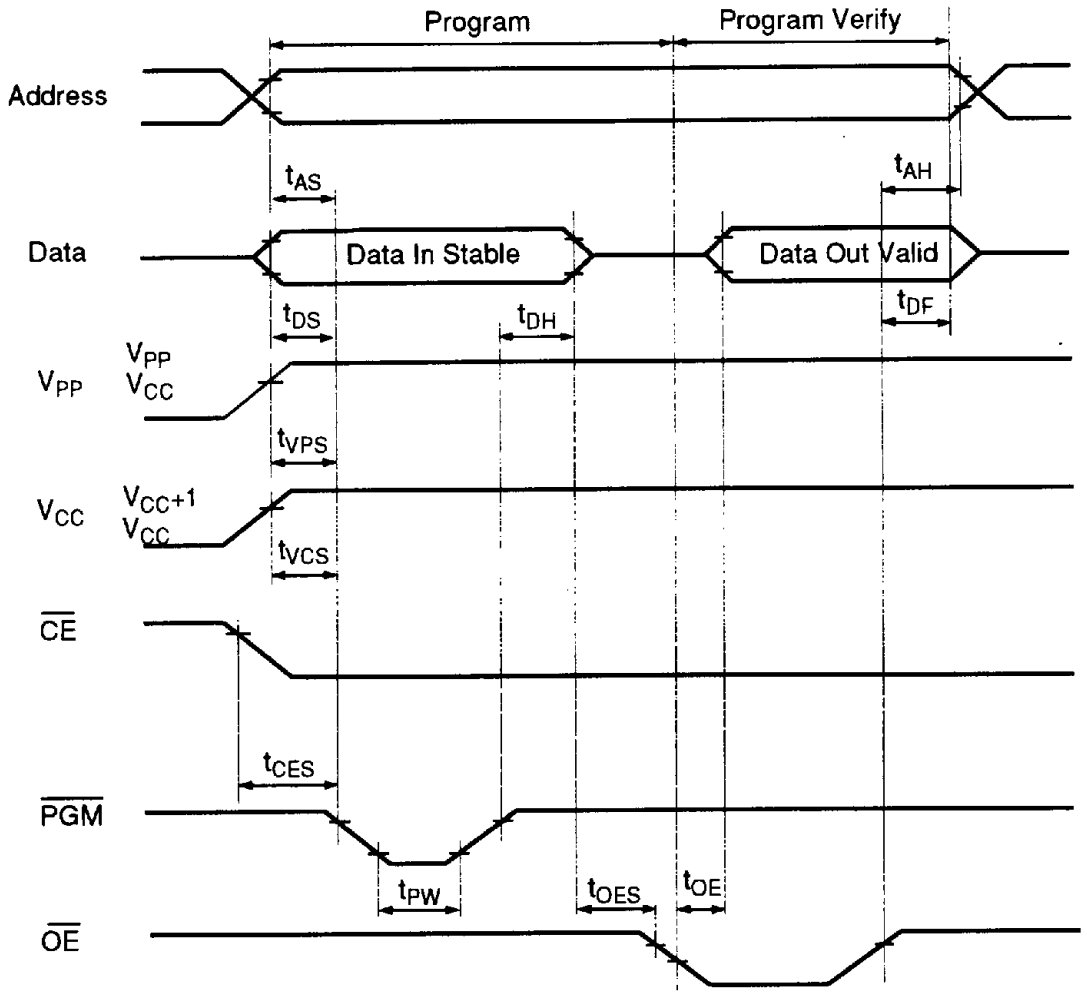
The Hitachi HN27C101A can be programmed with the high performance Byte Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.



(FC.P.HN27C101A)

4

■ BYTE PROGRAMMING TIMING WAVEFORM



(TD.P.HN27C101A)

■ ERASING THE HN27C101A

The Hitachi HN27C101A Ceramic DIP package allow the device to be erased by exposure to ultraviolet light of 2537Å. All of the data is changed to "1" after this erasure procedure. The minimum integrated dose (UV intensity x exposure time) for erasure is 15 W-sec/cm^2.

■ DEVICE IDENTIFIER MODE DESCRIPTION

The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

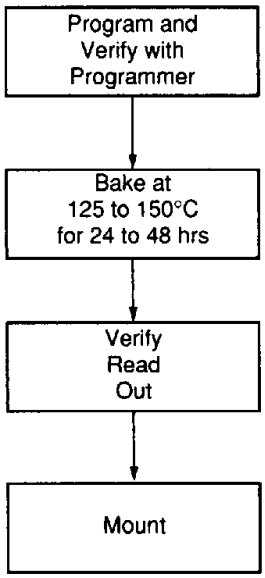
■ HN27C101A SERIES IDENTIFIER CODE

Identifier	A_0	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	0	0	1	1	1	0	0	0	38

Notes: 1. V_{CC} = 5.0 V ± 10%
2. A_9 = 12.0 V ± 0.5V
3. A_1-A_8, A_{10}-A_{16}, $\overline{CE}$, $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}
4. X = Don't Care

■ HN27C101AP/FP/TT/RR RECOMMENDED SCREENING CONDITIONS

Before mounting the HN27C101A plastic packages, please make the following screening (baking without bias) shown below:



(RSC.EPROM)

4