NEC

MOS INTEGRATED CIRCUIT

μPD75P3018A

4-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD75P3018A replaces the μPD753017A's internal mask ROM with a one-time PROM, and features expanded ROM capacity. The μPD75P3018A inherits the function of the μPD75P3018, and enables high-speed operation at a low supply voltage of 1.8 V.

Because the μPD75P3018A supports programming by users, it is suitable for use in evaluation of systems in development stages using the μPD753012A, 753016A, or 753017A, and for use in small-scale production.

The following document describes further details of the functions. Please make sure to read this document before starting design.

μPD753017 User's Manual : U11282E

FEATURES

○ Compatible with μPD753017A

○ Memory capacity:

- PROM : 32768 × 8 bits
- RAM : 1024 × 4 bits

○ Can operate in the same power supply voltage as the mask version μPD753017A

- V_{DD} = 1.8 to 5.5 V

○ LCD controller/driver

ORDERING INFORMATION

	Part Number	Package
	μPD75P3018AGC-3B9	80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm)
★	μPD75P3018AGC-8BT	80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm)
	μPD75P3018AGK-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.05 mm)
★	μPD75P3018AGK-9EU	80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.00 mm)

Caution Mask-option pull-up resistors are not provided in this device.

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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The mark ★ shows major revised points.

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FUNCTION OUTLINE

Item		Function	
Instruction execution time		• 0.95, 1.91, 3.81, 15.3 μs (main system clock: at 4.19 MHz operation) • 0.67, 1.33, 2.67, 10.7 μs (main system clock: at 6.0 MHz operation) • 122 μs (subsystem clock: at 32.768 kHz operation)	
Internal memory	PROM	32768 × 8 bits	
	RAM	1024 × 4 bits	
General-purpose register		• 4-bit operation: 8 × 4 banks • 8-bit operation: 4 × 4 banks	
Input/output port	CMOS input	8	On-chip pull-up resistor connection can be specified by using software: 23
	CMOS input/output	16	
	CMOS output	8	Also used for segment pins
	N-ch open-drain input/output	8	13 V breakdown voltage
	Total	40	
LCD controller/driver		• Segment number selection : 24/28/32 segments (can be changed to CMOS output port in unit of 4; max. 8) • Display mode selection : Static, 1/2 duty (1/2 bias), 1/3 duty (1/2 bias) 1/3 duty (1/3 bias), 1/4 duty (1/3 bias)	
Timer		5 channels: • 8-bit timer/event counter: 3 channels (can be used for 16-bit timer/event counter, carrier generator, timer with gate) • Basic interval timer/watchdog timer: 1 channel • Watch timer: 1 channel	
Serial interface		• 3-wire serial I/O mode ... MSB or LSB can be selected for transferring first bit • 2-wire serial I/O mode • SBI mode	
Bit sequential buffer (BSB)		16 bits	
Clock output (PCL)		• Φ, 524, 262, 65.5 kHz (main system clock: at 4.19 MHz operation) • Φ, 750, 375, 93.8 kHz (main system clock: at 6.0 MHz operation)	
Buzzer output (BUZ)		• 2, 4, 32 kHz (main system clock: at 4.19 MHz operation or subsystem clock: at 32.768 kHz operation) • 2.93, 5.86, 46.9 kHz (main system clock: at 6.0 MHz operation)	
Vectored interrupt		• External : 3 • Internal : 5	
Test input		• External : 1 • Internal : 1	
System clock oscillator		• Ceramic or crystal oscillator for main system clock oscillation • Crystal oscillator for subsystem clock oscillation	
Standby function		STOP/HALT mode	
Power supply voltage		V_{DD} = 1.8 to 5.5 V	
Package		• 80-pin plastic QFP (14 × 14 mm) • 80-pin plastic TQFP (fine pitch) (12 × 12 mm)	

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CONTENTS

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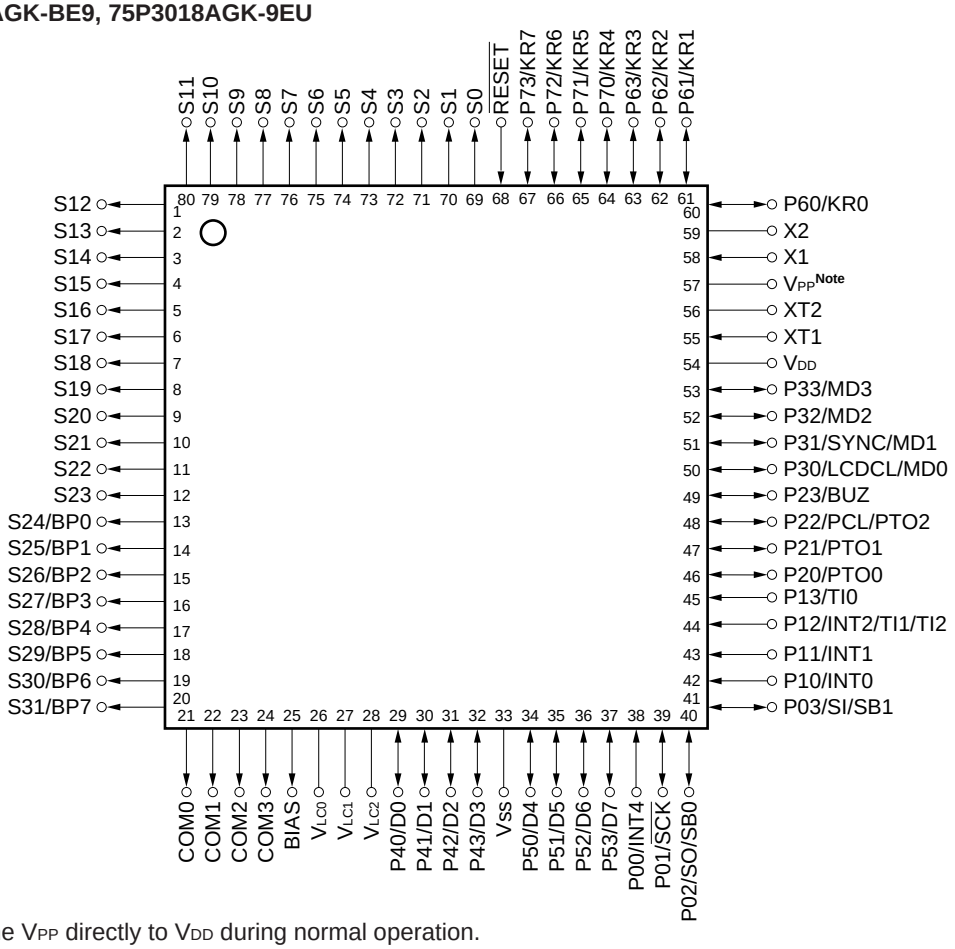
1. PIN CONFIGURATION (Top View)

- **80-pin plastic QFP (14 × 14 mm)**

★ **μPD75P3018AGC-3B9, 75P3018AGC-8BT**

- **80-pin plastic TQFP (fine pitch) (12 × 12 mm)**

★ **μPD75P3018AGK-BE9, 75P3018AGK-9EU**



Note Connect the V_{PP} directly to V_{DD} during normal operation.

PIN IDENTIFICATIONS

BIAS	: LCD Power Supply Bias Control	P70-P73	: Port7
BP0-BP7	: Bit Port 0-7	PCL	: Programmable Clock
BUZ	: Buzzer Clock	PTO0-PTO2	: Programmable Timer Output 0-2
COM0-COM3	: Common Output 0-3	$\overline{\text{RESET}}$	: Reset
D0-D7	: Data Bus 0-7	S0-S31	: Segment Output 0-31
INT0, 1, 4	: External Vectored Interrupt 0, 1, 4	SB0, SB1	: Serial Bus 0,1
INT2	: External Test Input 2	$\overline{\text{SCK}}$	: Serial Clock
KR0-KR7	: Key Return 0-7	SI	: Serial Input
LCDCL	: LCD Clock	SO	: Serial Output
MD0-MD3	: Mode Selection 0-3	SYNC	: LCD Synchronization
P00-P03	: Port0	TI0-TI2	: Timer Input 0-2
P10-P13	: Port1	V_{DD}	: Positive Power Supply
P20-P23	: Port2	V_{LC0}-V_{LC2}	: LCD Power Supply 0-2
P30-P33	: Port3	V_{PP}	: Programming Power Supply
P40-P43	: Port4	Vss	: Ground
P50-P53	: Port5	X1, X2	: Main System Clock Oscillation 1, 2
P60-P63	: Port6	XT1, XT2	: Subsystem Clock Oscillation 1, 2

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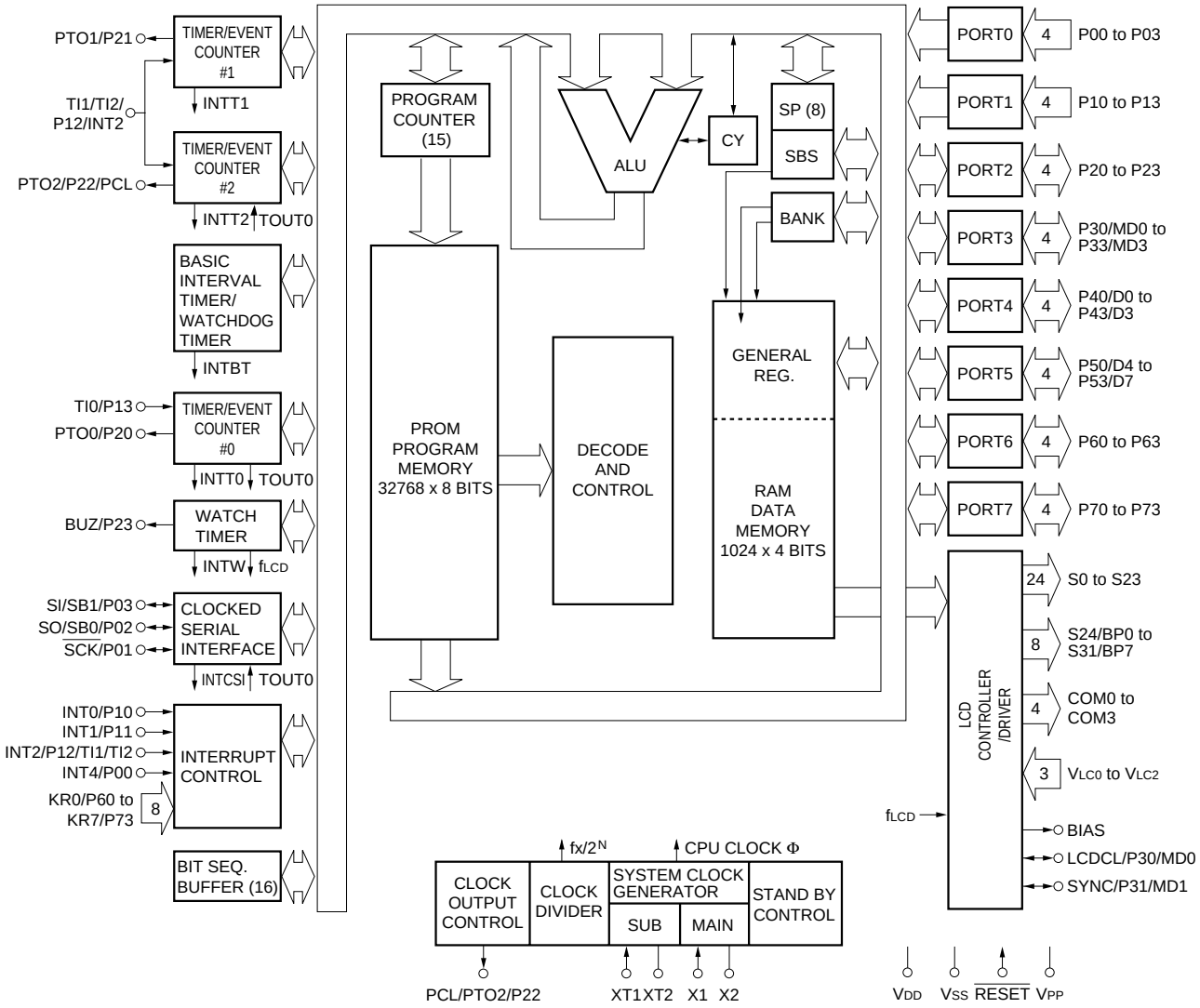
2. BLOCK DIAGRAM



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3. PIN FUNCTIONS

3.1 Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function	8-bit I/O	After Reset	I/O Circuit Type[Note 1]
P00	Input	INT4	This is a 4-bit input port (PORT0). P01 to P03 are 3-bit pins for which an internal pull-up resistor connection can be specified by software.	—	Input	<B>
P01		$\overline{\text{SCK}}$				<F>-A
P02		SO/SB0				<F>-B
P03		SI/SB1				<M>-C
P10	Input	INT0	This is a 4-bit input port (PORT1). These are 4-bit pins for which an internal pull-up resistor connection can be specified by software. P10/INT0 can select noise elimination circuit.	—	Input	<B>-C
P11		INT1				
P12		TI1/TI2/INT2				
P13		TI0				
P20	I/O	PTO0	This is a 4-bit I/O port (PORT2). These are 4-bit pins for which an internal pull-up resistor connection can be specified by software.	—	Input	E-B
P21		PTO1				
P22		PCL/PTO2				
P23		BUZ				
P30	I/O	LCDCL/MD0	This is a programmable 4-bit I/O port (PORT3). Input and output in single-bit units can be specified. When set for 4-bit units, an internal pull-up resistor connection can be specified by software.	—	Input	E-B
P31		SYNC/MD1				
P32		MD2				
P33		MD3				
P40[Note 2]	I/O	D0	This is an N-ch open-drain 4-bit I/O port (PORT4). When set to open-drain, voltage is 13 V. Also functions as data I/O pin (low-order 4 bits) for program memory (PROM) write/verify.	√	High impedance	M-E
P41[Note 2]		D1				
P42[Note 2]		D2				
P43[Note 2]		D3				
P50[Note 2]	I/O	D4	This is an N-ch open-drain 4-bit I/O port (PORT5). When set to open-drain, voltage is 13 V. Also functions as data I/O pin (high-order 4 bits) for program memory (PROM) write/verify.		High impedance	M-E
P51[Note 2]		D5				
P52[Note 2]		D6				
P53[Note 2]		D7				

Notes 1. Circuit types enclosed in brackets indicate Schmitt trigger input.

2. Low-level input leakage current increases when input instructions or bit manipulation instructions are executed.

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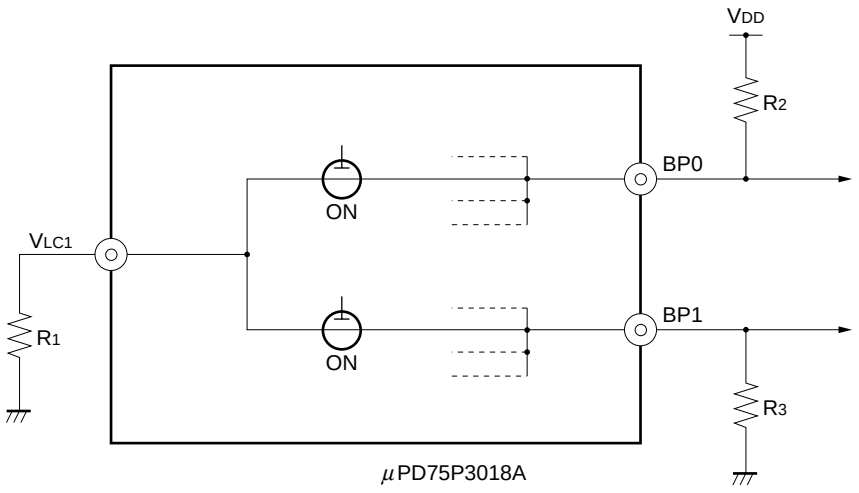
3.1 Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function	8-bit I/O	After Reset	I/O Circuit Type[Note 1]
P60	I/O	KR0	This is a programmable 4-bit I/O port (PORT6). Input and output in single-bit units can be specified. When set for 4-bit units, an internal pull-up resistor connection can be specified by software.	√	Input	<F>-A
P61		KR1				
P62		KR2				
P63		KR3				
P70	I/O	KR4	This is a 4-bit I/O port (PORT7). When set for 4-bit units, an internal pull-up resistor connection can be specified by software.		Input	<F>-A
P71		KR5				
P72		KR6				
P73		KR7				
BP0	Output	S24	1-bit output port (BIT PORT). These pins are also used as segment output pin.	—	**Note 2**	H-A
BP1		S25				
BP2		S26				
BP3		S27				
BP4	Output	S28				
BP5		S29				
BP6		S30				
BP7		S31				

Notes 1. Circuit types enclosed in brackets indicate Schmitt trigger input.

2. V_{LC1} is selected as the input source for BP0 to BP7. The output level varies depending on the external circuit for BP0 to BP7 and V_{LC1}.

Example: As shown below, BP0 to BP7 are mutually connected via the μPD75P3018A, so the output levels of BP0 to BP7 are determined by the sizes of R_1, R_2, and R_3.



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3.2 Non-port Pins (1/2)

Pin Name	I/O	Alternate Function	Function		After Reset	I/O Circuit Type[Note 1]
TI0	Input	P13	External event pulse input to timer/event counter		Input	<B>-C
TI1, TI2		P12/INT2				
PTO0	Output	P20	Timer/event counter output		Input	E-B
PTO1		P21				
PTO2		P22				
PCL		P22	Clock output			
BUZ		P23	Optional frequency output (for buzzer or system clock trimming)			
$\overline{SCK}$	I/O	P01	Serial clock I/O		Input	<F>-A
SO/SB0		P02	Serial data output Serial data bus I/O			<F>-B
SI/SB1		P03	Serial data input Serial data bus I/O			<M>-C
INT4	Input	P00	Edge detection vectored interrupt input (both rising and falling edges detection)			<B>
INT0	Input	P10	Edge detection vectored interrupt input (detected edge is selectable)	Noise elimination circuit/ asynchronous is selectable	Input	<B>-C
INT1		P11	INT0/P10 can select noise elimination circuit.	Asynchronous		
INT2		P12/TI1/TI2	Rising edge detection testable input	Asynchronous		
KR0-KR3	Input	P60-P63	Falling edge detection testable input		Input	<F>-A
KR4-KR7	Input	P70-P73	Falling edge detection testable input		Input	<F>-A
X1	Input	—	Ceramic/crystal oscillation circuit connection for main system clock. If using an external clock, input to X1 and input inverted phase to X2.		—	—
X2	—					
XT1	Input	—	Crystal oscillation circuit connection for subsystem clock. If using an external clock, input to XT1 and input inverted phase to XT2. XT1 can be used as a 1-bit (test) input.		—	—
XT2	—					
$\overline{RESET}$	Input	—	System reset input (low level active)		—	<B>
MD0	Input	P30/LCDCL	Mode selection for program memory (PROM) write/verify		Input	E-B
MD1		P31/SYNC				
MD2, MD3		P32, P33				
D0-D3	I/O	P40-P43	Data bus for program memory (PROM) write/verify		Input	M-E
D4-D7		P50-P53				
V_{PP}[Note 2]	—	—	Program power supply voltage for program memory (PROM) write/verify. For normal operation, connect directly to V_{DD}. Apply +12.5 V for PROM write/verify.		—	—
V_{DD}	—	—	Positive power supply		—	—
Vss	—	—	Ground		—	—

Notes 1. Circuit types enclosed in brackets indicate Schmitt trigger input.

2. The V_{PP} pin does not operate correctly during normal operation unless connected to the V_{DD} pin.

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3.2 Non-port Pins (2/2)

Pin Name	I/O	Alternate Function	Function	After Reset	I/O Circuit Type
S0-S23	Output	—	Segment signal output	**Note 1**	G-A
S24-S31	Output	BP0-BP7	Segment signal output	**Note 1**	H-A
COM0-COM3	Output	—	Common signal output	**Note 1**	G-B
V_{LC0}-V_{LC2}	—	—	Power source for LCD driver	—	—
BIAS	Output	—	Output for external split resistor cut	High impedance	—
LCDCL Note 2	I/O	P30/MD0	Clock output for driving external expansion driver	Input	E-B
SYNC Note 2	I/O	P31/MD1	Clock output for synchronization of external expansion driver	Input	E-B

Notes 1. The V_{LCX} (X = 0, 1, 2) shown below are selected as the input source for the display outputs.
S0-S31: V_{LC1}, COM0-COM2: V_{LC2}, COM3: V_{LC0}

2. These pins are provided for future system expansion. Currently, only P30 and P31 are used.

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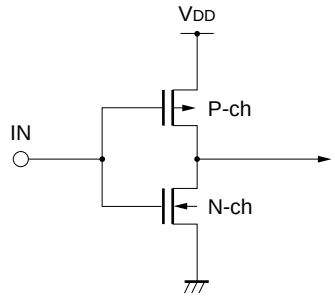
3.3 Pin Input/Output Circuits

The input/output circuits for the μPD75P3018A's pins are shown in abbreviated form below.

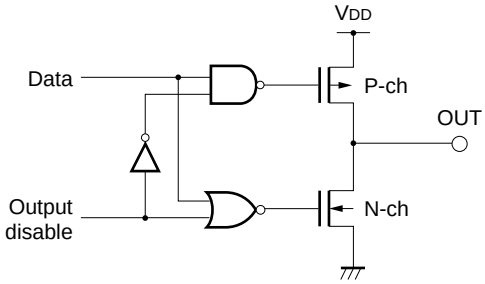
(1/2)

TYPE A



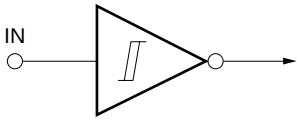
CMOS standard input buffer

TYPE D



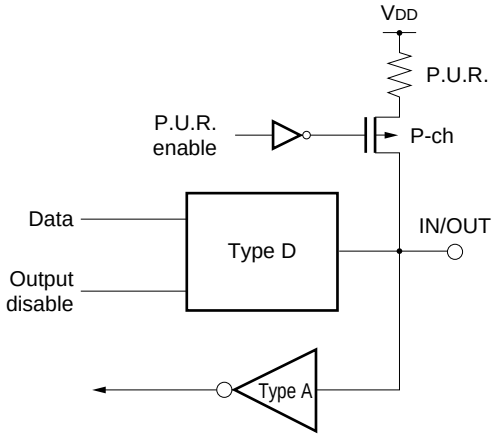
Push-pull output that can be set to high impedance output (with both P-ch and N-ch OFF).

TYPE B



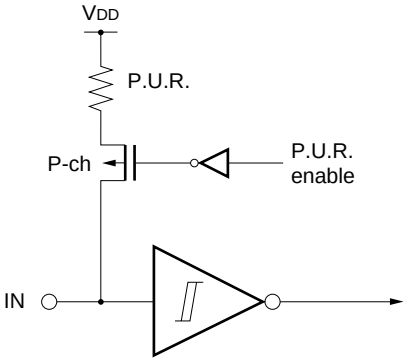
Schmitt trigger input with hysteresis characteristics.

TYPE E-B



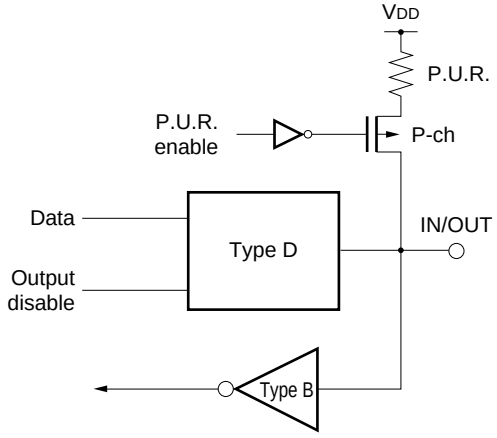
P.U.R. : Pull-Up Resistor

TYPE B-C



P.U.R. : Pull-Up Resistor

TYPE F-A



P.U.R. : Pull-Up Resistor

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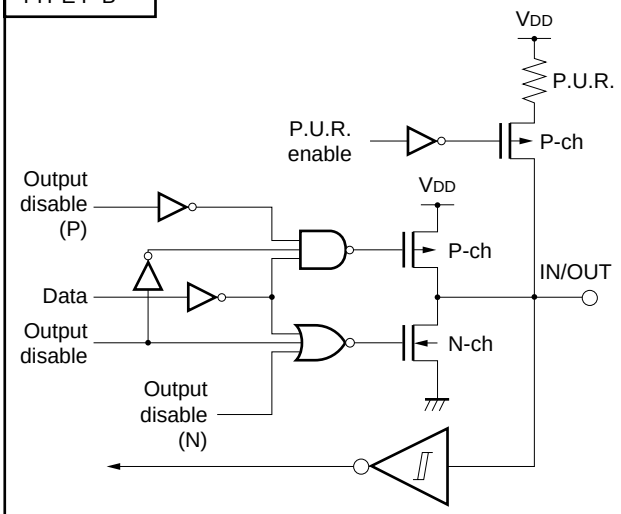
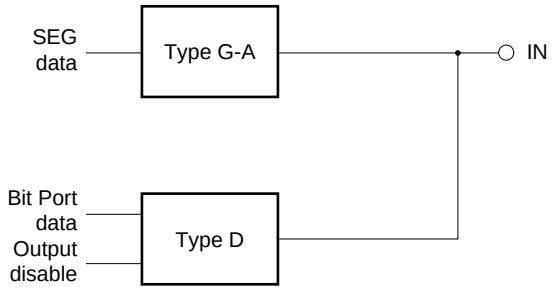
(2/2)

TYPE F-B

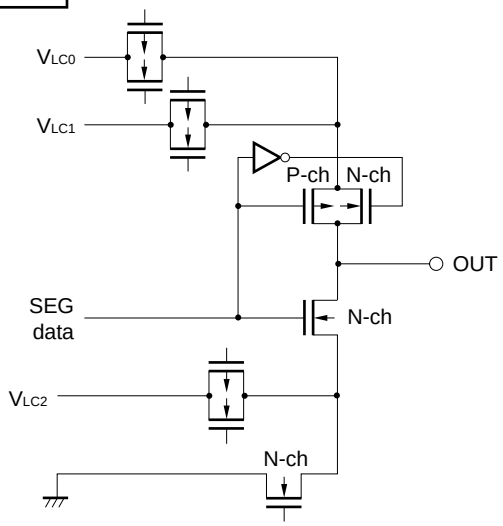


P.U.R. : Pull-Up Resistor

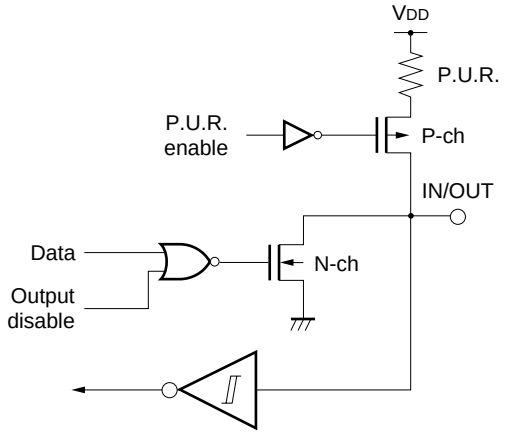
TYPE H-A★



TYPE G-A

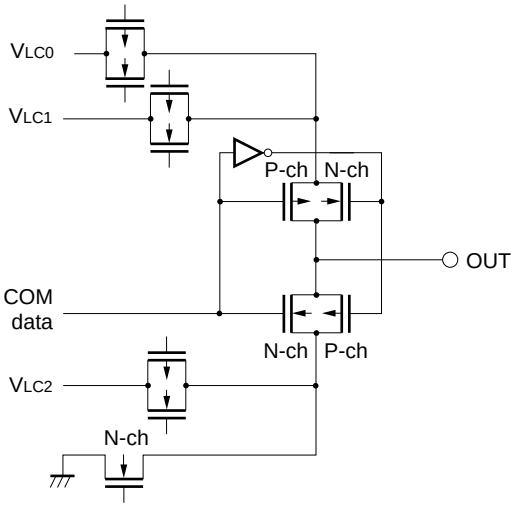


TYPE M-C

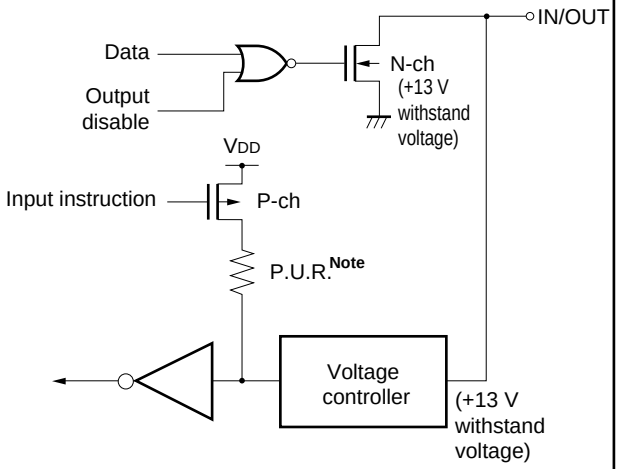


P.U.R. : Pull-Up Resistor

TYPE G-B



TYPE M-E



Note Pull-up resistor operated only when executing input instructions (when pins are low level, current flows from V_{DD} to pins).

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3.4 Recommended Connection for Unused Pins

Pin	Recommended Connection
P00/INT4	Connect to V_{SS} or V_{DD}
P01/$\overline{SCK}$	Connect to V_{SS} or V_{DD} via a resistor individually
P02/SO/SB0	
P03/SI/SB1	Connect to V_{SS}
P10/INT0, P11/INT1	Connect to V_{SS} or V_{DD}
P12/TI1/TI2/INT2	
P13/TI0	
P20/PTO0	Input : Connect to V_{SS} or V_{DD} via a resistor individually
P21/PTO1	Output : Leave open
P22/PTO2/PCL	
P23/BUZ	
P30/LCDCL/MD0	
P31/SYNC/MD1	
P32/MD2, P33/MD3	
P40/D0-P43/D3	Connect to V_{SS}
P50/D4-P53/D7	
P60/KR0-P63/KR3	Input : Connect to V_{SS} or V_{DD} via a resistor individually
P70/KR4-P73/KR7	Output : Leave open
S0-S23	Leave open
S24/BP0-S31/BP7	
COM0-COM3	
V_{LC0}-V_{LC2}	Connect to V_{SS}
BIAS	Connect to V_{SS} only when V_{LC0} to V_{LC2} are all not used. In other cases, leave open.
★ XT1[Note]	Connect to V_{SS}
XT2[Note]	Leave open

Note When subsystem clock is not used, specify SOS.0 = 1 (indicates that internal feedback resistor is disconnected).

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4. SWITCHING FUNCTION BETWEEN Mk I MODE AND Mk II MODE

Setting a stack bank selection (SBS) register for the μPD75P3018A enables the program memory to be switched between Mk I mode and Mk II mode. This function is applicable when using the μPD75P3018A to evaluate the μPD753012A, 753016A, or 753017A.

When the SBS bit 3 is set to 1 : sets Mk I mode (supports Mk I mode for μPD753012A, 753016A, and 753017A)
When the SBS bit 3 is set to 0 : sets Mk II mode (supports Mk II mode for μPD753012A, 753016A, and 753017A)

4.1 Difference between Mk I Mode and Mk II Mode

Table 4-1 lists points of difference between the Mk I mode and the Mk II mode for the μPD75P3018A.

Table 4-1. Difference between Mk I Mode and Mk II Mode

Item		Mk I Mode	Mk II Mode
Program counter		PC_{13-0} PC_{14} is fixed at 0	PC_{14-0}
Program memory (bytes)		16384	32768
Data memory (bits)		1024 × 4	
Stack	Stack bank	Selectable via memory banks 0 to 3	
	No. of stack bytes	2 bytes	3 bytes
Instruction	BRA !addr1 instruction CALLA !addr1 instruction	Not available	Available
Instruction execution time	CALL !addr instruction	3 machine cycles	4 machine cycles
	CALLF !faddr instruction	2 machine cycles	3 machine cycles
Supported mask ROMs		When set to Mk I mode: μPD753012A, 753016A, and 753017A	When set to Mk II mode: μPD753012A, 753016A, and 753017A

Caution The Mk II mode supports a program area exceeding 16 Kbytes for the 75X and 75XL series. Therefore, this mode is effective for enhancing software compatibility with products that have a program area of more than 16 Kbytes.
With regard to the number of stack bytes during execution of subroutine call instructions, the usable area increases by 1 byte per stack compared to the Mk I mode when the Mk II mode is selected. However, when the CALL !addr and CALLF !faddr instructions are used, the machine cycle becomes longer by 1 machine cycle. Therefore, if more emphasis is placed on RAM use efficiency and processing performance than on software compatibility, the Mk I mode should be used.

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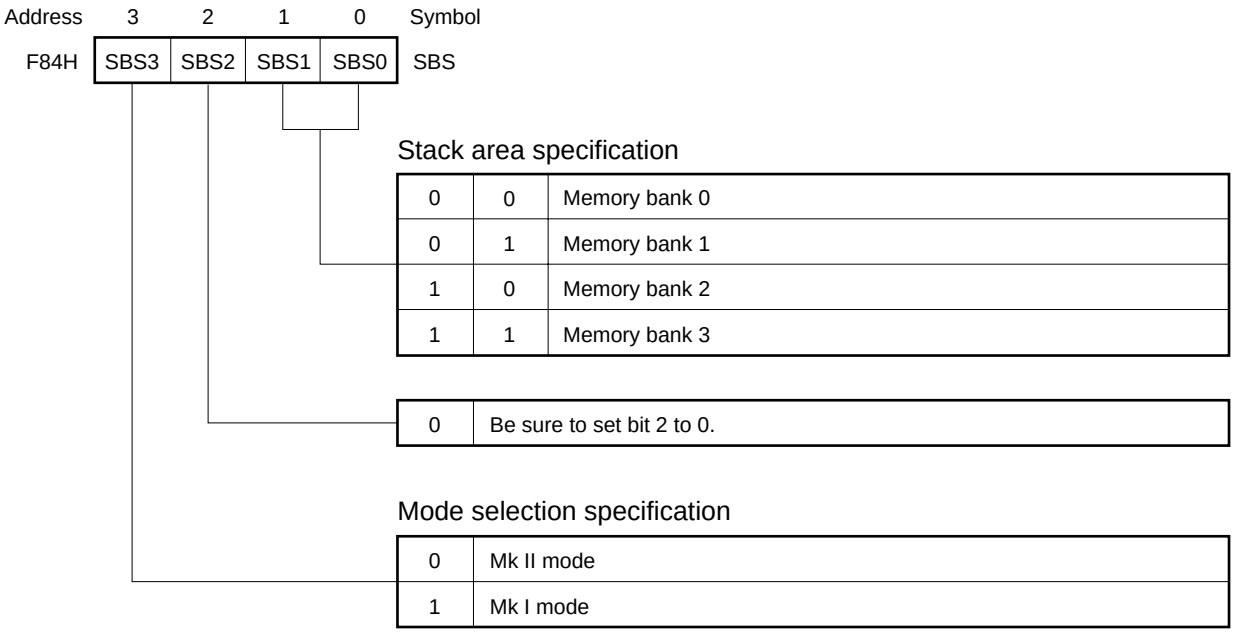
4.2 Setting of Stack Bank Selection Register (SBS)

Use the stack bank selection register to switch between Mk I mode and Mk II mode. Figure 4-1 shows the format for doing this.

The stack bank selection register is set using a 4-bit memory manipulation instruction. When using the Mk I mode, be sure to initialize the stack bank selection register to 10XXB[Note] at the beginning of the program. When using the Mk II mode, be sure to initialize it to 00XXB[Note].

Note Set the desired value for XX.

Figure 4-1. Format of Stack Bank Selection Register



Cautions 1. SBS3 is set to "1" after $\overline{\text{RESET}}$ input, and consequently the CPU operates in Mk I mode. When using instructions for Mk II mode, set SBS3 to "0" and set Mk II mode before using the instructions.

2. When using Mk II mode, execute a subroutine call instruction and an interrupt instruction after $\overline{\text{RESET}}$ input and after setting the stack bank selection register.

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5. DIFFERENCES BETWEEN μPD75P3018A AND μPD753012A, 753016A, AND 753017A

The μPD75P3018A replaces the internal mask ROM in the μPD753012A, 753016A, and 753017A with a one-time PROM and features expanded ROM capacity. The μPD75P3018A's Mk I mode supports the Mk I mode in the μPD753012A, 753016A, and 753017A and the μPD75P3018A's Mk II mode supports the Mk II mode in the μPD753012A, 753016A, and 753017A.

Table 5-1 lists differences among the μPD75P3018A and the μPD753012A, 753016A, and 753017A. Be sure to check the differences among these products before using them with PROMs for debugging or prototype testing of application systems or, later, when using them with a mask ROM for full-scale production.

For the CPU functions and internal hardwares, refer to **μPD753017 User's Manual (U11282E)**.

Table 5-1. Differences between μPD75P3018A and μPD753012A, 753016A, and 753017A

Item		μPD753012A	μPD753016A	μPD753017A	μPD75P3018A
Program counter		14 bits		15 bits	
Program memory (bytes)		Mask ROM			One-time PROM
	During Mk I mode	12288	16384	16384	16384
	During Mk II mode	12288	16384	24576	32768
Data memory (× 4 bits)		1024			
Mask options	Pull-up resistor for PORT4 and PORT5	Yes (Can be specified whether to incorporate or not)			No (Cannot incorporate)
	LCD split resistor				
	Feedback resistor for subsystem clock	Yes (Can be specified whether to use or not)			No (used)
	Wait time during $\overline{\text{RESET}}$	Yes (Can be specified either $2^{17}/f_X$ or $2^{15}/f_X$)Note			No (Fixed at $2^{15}/f_X$)Note
Pin configuration	Pin Nos. 29 to 32	P40 to P43			P40/D0 to P43/D3
	Pin Nos. 34 to 37	P50 to P53			P50/D4 to P53/D7
	Pin No. 50	P30/LCDCL			P30/LCDCL/MD0
	Pin No. 51	P31/SYNC			P31/SYNC/MD1
	Pin Nos. 52 and 53	P32, P33			P32/MD2, P33/MD3
	Pin No. 57	IC			V_{PP}
Other		Noise resistance and noise radiation may differ due to the different circuit sizes and mask layouts.			

Note For $2^{17}/f_X$, during 6.0 MHz operation is 21.8 ms, and during 4.19 MHz operation is 31.3 ms.
For $2^{15}/f_X$, during 6.0 MHz operation is 5.46 ms, and during 4.19 MHz operation is 7.81 ms.

Caution Noise resistance and noise radiation are different in PROM and mask ROMs. In transferring to mask ROM version from the PROM version in a process between prototype development and full production, be sure to fully evaluate the mask ROM version's CS (not ES).

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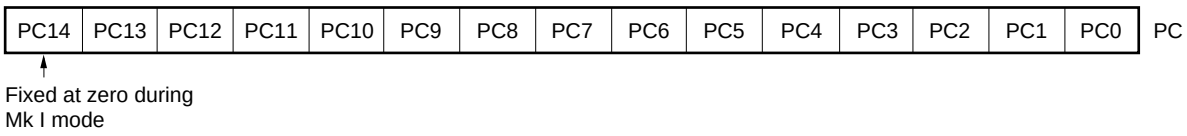
6. MEMORY CONFIGURATION

6.1 Program Counter (PC) ... 15 bits

This is a 15-bit binary counter that stores program memory address data.

Bit 15 is valid during Mk II mode. But PC14 is fixed at zero during Mk I mode, and the lower 14 bits are all valid.

Figure 6-1. Configuration of Program Counter



6.2 Program Memory (PROM) ... 32768 × 8 bits

The program memory consists of 32768 × 8-bit one-time PROM. The program memory address can be selected as shown below by setting the stack bank selection (SBS) register.

	Mk I Mode	Mk II Mode
Usable address	0000H to 3FFFH	0000H to 7FFFH

Figures 6-2 and 6-3 show the addressing ranges for the program memory and branch instruction and the subroutine call instruction, during Mk I and Mk II modes.

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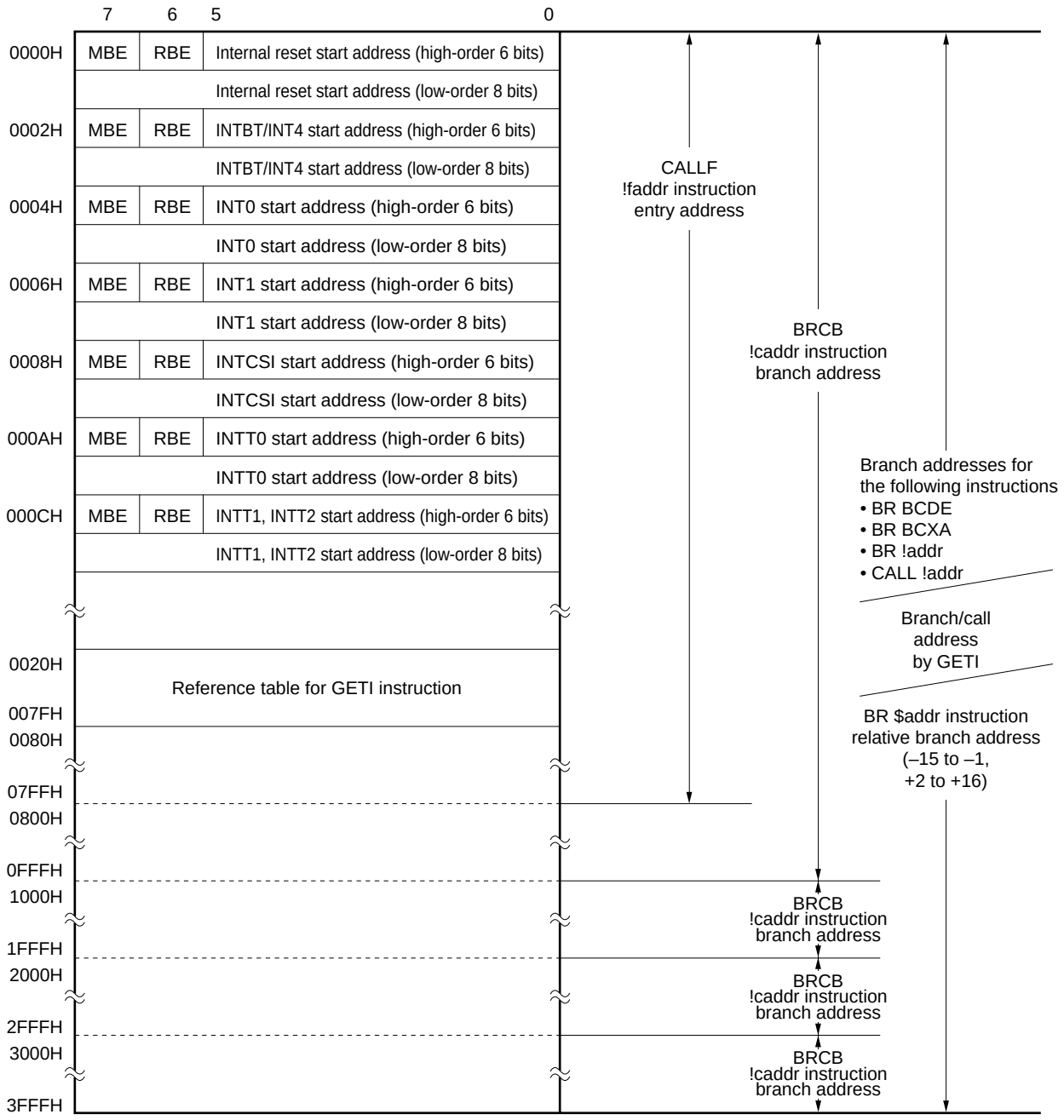
Figure 6-2. Program Memory Map (Mk I mode)



Remark For instructions other than those noted above, the BR PCDE and BR PCXA instructions can be used to branch to addresses with changes in the PC's low-order 8 bits only.

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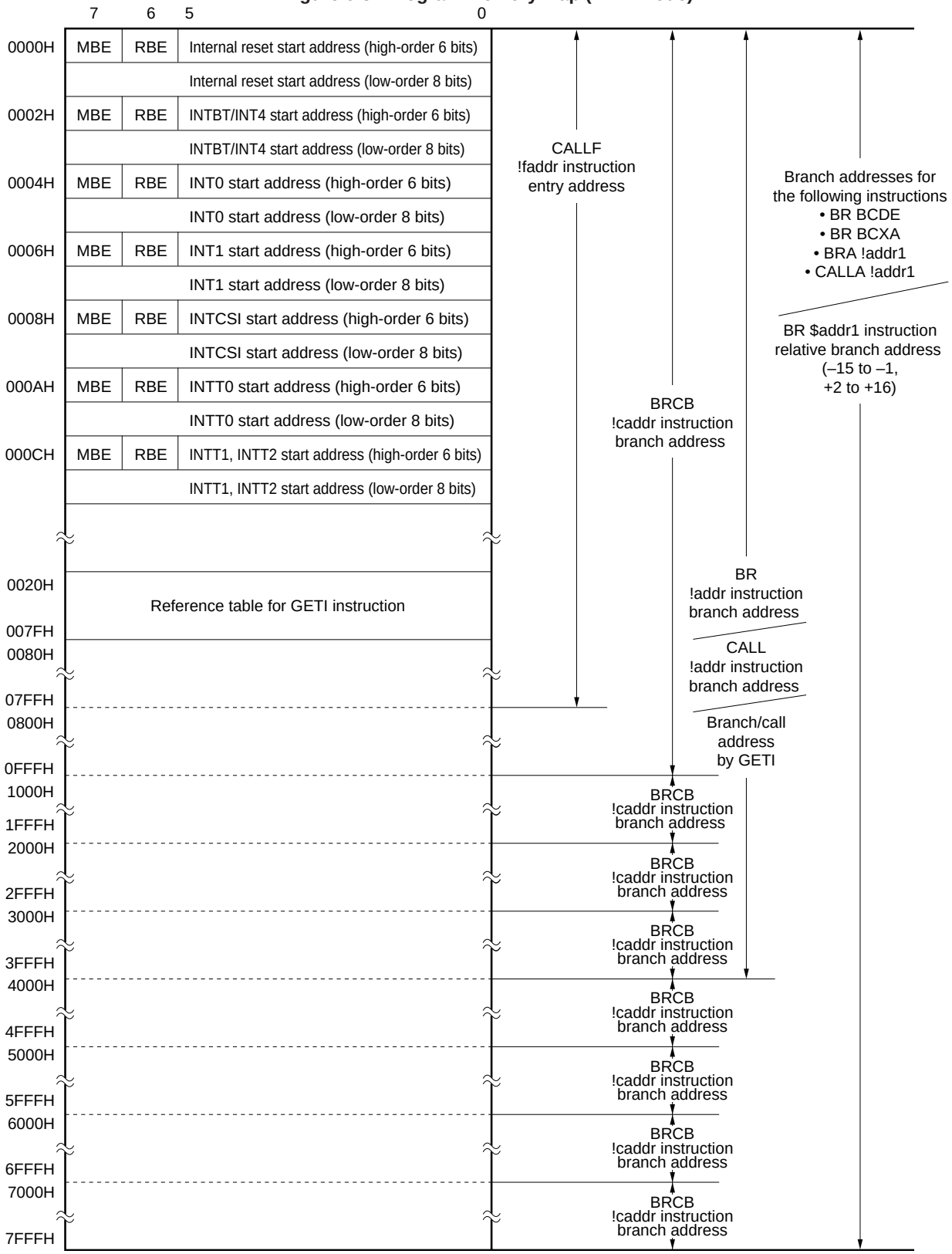
Figure 6-3. Program Memory Map (Mk II mode)



Caution To allow the vectored interrupt's 14-bit start address (noted above), set the address within a 16K area (0000H to 3FFFH).

Remark For instructions other than those noted above, the BR PCDE and BR PCXA instructions can be used to branch to addresses with changes in the PC's low-order 8 bits only.

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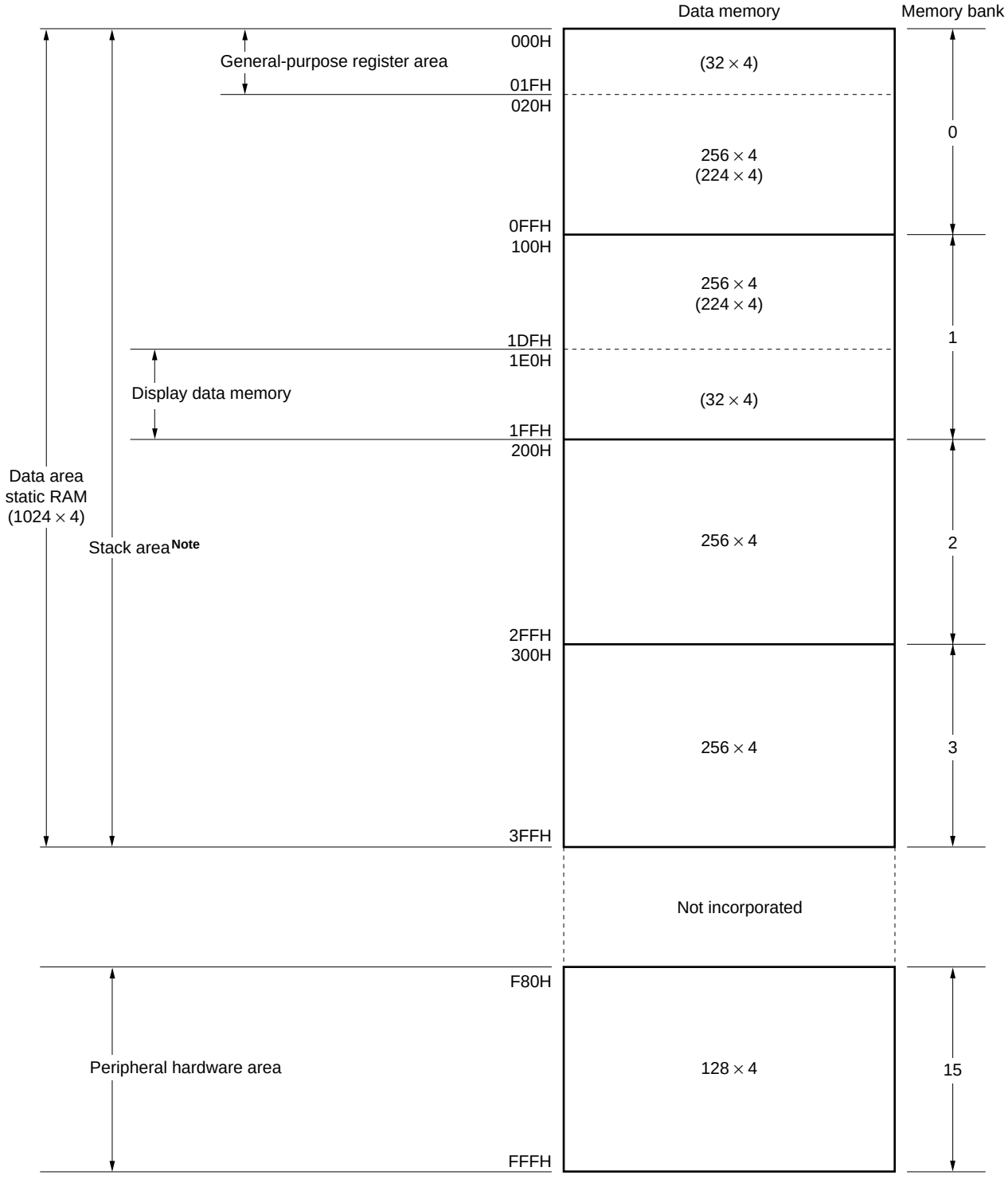
6.3 Data Memory (RAM) ... 1024 × 4 bits

Figure 6-4 shows the data memory configuration.

Data memory consists of a data area and a peripheral hardware area. The data area consists of 1024 × 4-bit static RAM.

Figure 6-4. Data Memory Map



Note Memory bank 0, 1, 2, or 3 can be selected as the stack area.

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7. INSTRUCTION SET

(1) Representation and coding formats for operands

In the instruction's operand area, use the following coding format to describe operands corresponding to the instruction's operand representations (for further description, see the **RA75X Assembler Package User's Manual Language ★ (U12385E)**). When there are several codes, select and use just one. Codes that consist of uppercase letters and + or – symbols are key words that should be entered as they are.

For immediate data, enter an appropriate numerical value or label.

Enter register flag symbols as label descriptors instead of mem, fmem, pmem, bit, etc. (For details, refer to the **μPD753017 User's Manual (U11282E)**). The number of labels that can be entered for fmem and pmem are restricted.

Representation	Coding Format
reg	X, A, B, C, D, E, H, L
reg1	X, B, C, D, E, H, L
rp	XA, BC, DE, HL
rp1	BC, DE, HL
rp2	BC, DE
rp'	XA, BC, DE, HL, XA', BC', DE', HL'
rp'1	BC, DE, HL, XA', BC', DE', HL'
rpa	HL, HL+, HL–, DE, DL
rpa1	DE, DL
n4	4-bit immediate data or label
n8	8-bit immediate data or label
mem	8-bit immediate data or label[Note]
bit	2-bit immediate data or label
fmem	FB0H-FBFH, FF0H-FFFH immediate data or label
pmem	FC0H-FFFH immediate data or label
addr	0000H-3FFFH immediate data or label
addr1	0000H-7FFFH immediate data or label (Mk II mode only)
caddr	12-bit immediate data or label
faddr	11-bit immediate data or label
taddr	20H-7FH immediate data (however, bit0 = 0) or label
PORTn	PORT0-PORT7
IEXXX	IEBT, IECSI, IET0, IET1, IET2, IE0-IE2, IE4, IEW
RBn	RB0-RB3
MBn	MB0-MB3, MB15

Note When processing 8-bit data, only even-numbered addresses can be specified.

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(2) Operation legend

A	: A register; 4-bit accumulator
B	: B register
C	: C register
D	: D register
E	: E register
H	: H register
L	: L register
X	: X register
XA	: Register pair (XA); 8-bit accumulator
BC	: Register pair (BC)
DE	: Register pair (DE)
HL	: Register pair (HL)
XA'	: Expansion register pair (XA')
BC'	: Expansion register pair (BC')
DE'	: Expansion register pair (DE')
HL'	: Expansion register pair (HL')
PC	: Program counter
SP	: Stack pointer
CY	: Carry flag; bit accumulator
PSW	: Program status word
MBE	: Memory bank enable flag
RBE	: Register bank enable flag
PORTn	: Port n (n = 0 to 7)
IME	: Interrupt master enable flag
IPS	: Interrupt priority selection register
IEXXX	: Interrupt enable flag
RBS	: Register bank selection register
MBS	: Memory bank selection register
PCC	: Processor clock control register
.	: Delimiter for address and bit
(XX)	: Addressed data
XXH	: Hexadecimal data

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(3) Description of symbols used in addressing area

*1	MB = MBE • MBS MBS = 0-3, 15	Data memory addressing
*2	MB = 0	
*3	MBE = 0 : MB = 0 (000H-07FH) MB = 15 (F80H-FFFH) MBE = 1 : MB = MBS MBS = 0-3, 15	
*4	MB = 15, fmem = FB0H-FBFH, FF0H-FFFH	
*5	MB = 15, pmem = FC0H-FFFH	
*6	addr = 0000H-3FFFH	Program memory addressing
*7	addr, addr1 = (Current PC) –15 to (Current PC) –1 (Current PC) +2 to (Current PC) +16	
*8	caddr = 0000H-0FFFH ($PC_{14, 13, 12}$ = 000B) or 1000H-1FFFH ($PC_{14, 13, 12}$ = 001B) or 2000H-2FFFH ($PC_{14, 13, 12}$ = 010B) or 3000H-3FFFH ($PC_{14, 13, 12}$ = 011B) or 4000H-4FFFH ($PC_{14, 13, 12}$ = 100B: Mk II mode only) or 5000H-5FFFH ($PC_{14, 13, 12}$ = 101B: Mk II mode only) or 6000H-6FFFH ($PC_{14, 13, 12}$ = 110B: Mk II mode only) or 7000H-7F7FH ($PC_{14, 13, 12}$ = 111B: Mk II mode only)	
*9	faddr = 0000H-07FFH	
*10	taddr = 0020H-007FH	
*11	addr1 = 0000H-7FFFH (Mk II mode only)	

Remarks 1. MB indicates access-enabled memory banks.

2. In area *2, MB = 0 for both MBE and MBS.

3. In areas *4 and *5, MB = 15 for both MBE and MBS.

4. Areas *6 to *11 indicate corresponding address-enabled areas.

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(4) Description of machine cycles

S indicates the number of machine cycles required for skipping of skip-specified instructions. The value of S varies as shown below.

- No skip ..... S = 0
- Skipped instruction is 1-byte or 2-byte instruction .... S = 1
- Skipped instruction is 3-byte instruction[Note] ..... S = 2

Note 3-byte instructions: BR !addr, BRA !addr1, CALL !addr, CALLA !addr1

Caution The GETI instruction is skipped for one machine cycle.

One machine cycle equals one cycle (= t_{CY}) of the CPU clock Φ. Use the PCC setting to select among four cycle times.

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Instruction Group	Mnemonic	Operand	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Transfer	MOV	A, #n4	1	1	A ← n4		String-effect A
		reg1, #n4	2	2	reg1← n4		
		XA, #n8	2	2	XA ← n8		String-effect A
		HL, #n8	2	2	HL ← n8		String-effect B
		rp2, #n8	2	2	rp2 ← n8		
		A, @HL	1	1	A ← (HL)	*1	
		A, @HL+	1	2+S	A ← (HL), then L ← L+1	*1	L=0
		A, @HL–	1	2+S	A ← (HL), then L ← L–1	*1	L=FH
		A, @rpa1	1	1	A ← (rpa1)	*2	
		XA, @HL	2	2	XA ← (HL)	*1	
		@HL, A	1	1	(HL) ← A	*1	
		@HL, XA	2	2	(HL) ← XA	*1	
		A, mem	2	2	A ← (mem)	*3	
		XA, mem	2	2	XA ← (mem)	*3	
		mem, A	2	2	(mem) ← A	*3	
		mem, XA	2	2	(mem) ← XA	*3	
		A, reg	2	2	A ← reg		
		XA, rp’	2	2	XA ← rp’		
		reg1, A	2	2	reg1 ← A		
		rp’1, XA	2	2	rp’1 ← XA		
	XCH	A, @HL	1	1	A ↔ (HL)	*1	
		A, @HL+	1	2+S	A ↔ (HL), then L ← L+1	*1	L=0
		A, @HL–	1	2+S	A ↔ (HL), then L ← L–1	*1	L=FH
		A, @rpa1	1	1	A ↔ (rpa1)	*2	
		XA, @HL	2	2	XA ↔ (HL)	*1	
		A, mem	2	2	A ↔ (mem)	*3	
		XA, mem	2	2	XA ↔ (mem)	*3	
		A, reg1	1	1	A ↔ reg1		
		XA, rp’	2	2	XA ↔ rp’		
Table reference	MOVT[Note 1]	XA, @PCDE	1	3	XA ← $(PC_{13-8}+DE)_{ROM}$		
					XA ← $(PC_{14-8}+DE)_{ROM}$		
		XA, @PCXA	1	3	XA ← $(PC_{13-8}+XA)_{ROM}$		
					XA ← $(PC_{14-8}+XA)_{ROM}$		
		XA, @BCDE	1	3	XA ← $(BCDE)_{ROM}$[Note 2]	*6	
					XA ← $(BCDE)_{ROM}$[Note 2]	*11	
		XA, @BCXA	1	3	XA ← $(BCXA)_{ROM}$[Note 2]	*6	
					XA ← $(BCXA)_{ROM}$[Note 2]	*11	

Notes 1. Shaded areas indicate support for Mk II mode only. Other areas indicate support for Mk I mode only.

2. Only the low-order 3 bits in the B register are valid.

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Instruction Group	Mnemonic	Operand	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Bit transfer	MOV1	CY, fmem.bit	2	2	CY← (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY ← (H+mem$_{3-0}$.bit)	*1	
		fmem.bit, CY	2	2	(fmem.bit) ← CY	*4	
		pmem.@L, CY	2	2	(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) ← CY	*5	
		@H+mem.bit, CY	2	2	(H+mem$_{3-0}$.bit) ← CY	*1	
Arithmetic	ADDS	A, #n4	1	1+S	A ← A+n4		carry
		XA, #n8	2	2+S	XA ← XA+n8		carry
		A, @HL	1	1+S	A ← A+(HL)	*1	carry
		XA, rp'	2	2+S	XA ← XA+rp'		carry
		rp'1, XA	2	2+S	rp'1 ← rp'1+XA		carry
	ADDC	A, @HL	1	1	A, CY ← A+(HL)+CY	*1	
		XA, rp'	2	2	XA, CY ← XA+rp'+CY		
		rp'1, XA	2	2	rp'1, CY ← rp'1+XA+CY		
	SUBS	A, @HL	1	1+S	A ← A–(HL)	*1	borrow
		XA, rp'	2	2+S	XA ← XA–rp'		borrow
		rp'1, XA	2	2+S	rp'1 ← rp'1–XA		borrow
	SUBC	A, @HL	1	1	A, CY ← A–(HL)–CY	*1	
		XA, rp'	2	2	XA, CY ← XA–rp'–CY		
		rp'1, XA	2	2	rp'1, CY ← rp'1–XA–CY		
	AND	A, #n4	2	2	A ← A ∧ n4		
		A, @HL	1	1	A ← A ∧ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∧ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ∧ XA		
	OR	A, #n4	2	2	A ← A ∨ n4		
		A, @HL	1	1	A ← A ∨ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∨ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ∨ XA		
	XOR	A, #n4	2	2	A ← A ⊻ n4		
		A, @HL	1	1	A ← A ⊻ (HL)	*1	
		XA, rp'	2	2	XA ← XA ⊻ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ⊻ XA		
Accumulator manipulation	RORC	A	1	1	CY ← A$_0$, A$_3$ ← CY, A$_{n-1}$ ← A$_n$		
	NOT	A	2	2	A ← $\overline{A}$		
Increment/ decrement	INCS	reg	1	1+S	reg ← reg+1		reg=0
		rp1	1	1+S	rp1 ← rp1+1		rp1=00H
		@HL	2	2+S	(HL) ← (HL)+1	*1	(HL)=0
		mem	2	2+S	(mem) ← (mem)+1	*3	(mem)=0
	DECS	reg	1	1+S	reg ← reg–1		reg=FH
		rp'	2	2+S	rp' ← rp'–1		rp'=FFH

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Instruction Group	Mnemonic	Operand	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Comparison	SKE	reg, #n4	2	2+S	Skip if reg=n4		reg=n4
		@HL, #n4	2	2+S	Skip if (HL)=n4	*1	(HL)=n4
		A, @HL	1	1+S	Skip if A=(HL)	*1	A=(HL)
		XA, @HL	2	2+S	Skip if XA=(HL)	*1	XA=(HL)
		A, reg	2	2+S	Skip if A=reg		A=reg
		XA, rp'	2	2+S	Skip if XA=rp'		XA=rp'
Carry flag manipulation	SET1	CY	1	1	CY ← 1		
	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1+S	Skip if CY=1		CY=1
	NOT1	CY	1	1	CY ← $\overline{CY}$		
Memory bit manipulation	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
		fmem.bit	2	2	(fmem.bit) ← 1	*4	
		pmem.@L	2	2	(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) ← 1	*5	
		@H+mem.bit	2	2	(H+mem$_{3-0}$.bit) ← 1	*1	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*3	
		fmem.bit	2	2	(fmem.bit) ← 0	*4	
		pmem.@L	2	2	(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) ← 0	*5	
		@H+mem.bit	2	2	(H+mem$_{3-0}$.bit) ← 0	*1	
	SKT	mem.bit	2	2+S	Skip if(mem.bit)=1	*3	(mem.bit)=1
		fmem.bit	2	2+S	Skip if(fmem.bit)=1	*4	(fmem.bit)=1
		pmem.@L	2	2+S	Skip if(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))=1	*5	(pmem.@L)=1
		@H+mem.bit	2	2+S	Skip if(H+mem$_{3-0}$.bit)=1	*1	(@H+mem.bit)=1
	SKF	mem.bit	2	2+S	Skip if(mem.bit)=0	*3	(mem.bit)=0
		fmem.bit	2	2+S	Skip if(fmem.bit)=0	*4	(fmem.bit)=0
		pmem.@L	2	2+S	Skip if(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))=0	*5	(pmem.@L)=0
		@H+mem.bit	2	2+S	Skip if(H+mem$_{3-0}$.bit)=0	*1	(@H+mem.bit)=0
	SKTCLR	fmem.bit	2	2+S	Skip if(fmem.bit)=1 and clear	*4	(fmem.bit)=1
		pmem.@L	2	2+S	Skip if(pmem$_{7-2}$+L$_{3-2}$.bit (L$_{1-0}$))=1 and clear	*5	(pmem.@L)=1
		@H+mem.bit	2	2+S	Skip if(H+mem$_{3-0}$.bit)=1 and clear	*1	(@H+mem.bit)=1
	AND1	CY, fmem.bit	2	2	CY ← CY ∧ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∧ (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY ← C ∧ (H+mem$_{3-0}$.bit)	*1	
	OR1	CY, fmem.bit	2	2	CY ← CY ∨ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∨ (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY ← CY ∨ (H+mem$_{3-0}$.bit)	*1	
	XOR1	CY, fmem.bit	2	2	CY ← CY ∨̄ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∨̄ (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY ← C ∨̄ (H+mem$_{3-0}$.bit)	*1	

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Instruction Group	Mnemonic	Operand	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Branch	BR[Note 1]	addr	—	—	$PC_{14} \leftarrow 0$, $PC_{13-0} \leftarrow$ addr (Use the assembler to select the most appropriate instruction among the following. • BR !addr • BRCB !caddr • BR $addr)	*6	
		addr1	—	—	$PC_{14-0} \leftarrow$ addr1 (Use the assembler to select the most appropriate instruction among the following. • BRA !addr1 • BR !addr • BRCB !caddr • BR $addr1)	*11	
		!addr	3	3	$PC_{14} \leftarrow 0$, $PC_{13-0} \leftarrow$ addr	*6	
		$addr	1	2	$PC_{14} \leftarrow 0$, $PC_{13-0} \leftarrow$ addr	*7	
		$addr1	1	2	$PC_{14-0} \leftarrow$ addr1		
		PCDE	2	3	$PC_{14} \leftarrow 0$, $PC_{13-0} \leftarrow PC_{13-8}$+DE		
					$PC_{14-0} \leftarrow PC_{14-8}$+DE		
		PCXA	2	3	$PC_{14} \leftarrow 0$, $PC_{13-0} \leftarrow PC_{13-8}$+XA		
					$PC_{14-0} \leftarrow PC_{14-8}$+XA		
		BCDE	2	3	$PC_{14} \leftarrow 0$, $PC_{13-0} \leftarrow$ BCDE[Note 2]	*6	
					$PC_{14-0} \leftarrow$ BCDE[Note 2]	*11	
		BCXA	2	3	$PC_{14} \leftarrow 0$, $PC_{13-0} \leftarrow$ BCXA[Note 2]	*6	
					$PC_{14-0} \leftarrow$ BCXA[Note 2]	*11	
	BRA[Note 1]	!addr	3	3	$PC_{14} \leftarrow 0$, $PC_{13-0} \leftarrow$ addr	*6	
			3	3	$PC_{14-0} \leftarrow$ addr1	*11	
	BRCB[Note 1]	!caddr	2	2	$PC_{14} \leftarrow 0$, $PC_{13-0} \leftarrow PC_{13, 12}$+caddr$_{11-0}$	*8	
					$PC_{14-0} \leftarrow PC_{14, 13, 12}$+caddr$_{11-0}$		

Notes 1. Shaded areas indicate support for Mk II mode only. Other areas indicate support for Mk I mode only.

2. The only following bits are valid in the B register.

For Mk I mode : Low-order 2 bits

For Mk II mode : Low-order 3 bits

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Instruction Group	Mnemonic	Operand	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Subroutine stack control	CALLA[Note]	!addr1	3	3	(SP–5) ← 0, PC_{14-12} (SP–6)(SP–3)(SP–4) ← PC_{11-0} (SP–2) ← X, X, MBE, RBE PC_{14-0} ← addr1, SP ← SP–6	*11	
	CALL[Note]	!addr	3	3	(SP–4)(SP–1)(SP–2) ← PC_{11-0} (SP–3) ← MBE, RBE, $PC_{13, 12}$ PC_{14} ← 0, PC_{13-0} ← addr, SP ← SP–4	*6	
				4	(SP–5) ← 0, PC_{14-12} (SP–6)(SP–3)(SP–4) ← PC_{11-0} (SP–2)← X, X, MBE, RBE PC_{14} ← 0, PC_{13-0} ← addr, SP ← SP–6		
	CALLF[Note]	!faddr	2	2	(SP–4)(SP–1)(SP–2) ← PC_{11-0} (SP–3) ← MBE, RBE, $PC_{13, 12}$ PC_{14} ← 0, PC_{13-0} ← 000+faddr, SP ← SP–4	*9	
				3	(SP–5) ← 0, PC_{14-12} (SP–6)(SP–3)(SP–4) ← PC_{11-0} (SP–2) ← X, X, MBE, RBE PC_{14-0} ← 0000+faddr, SP ← SP–6		
	RET[Note]		1	3	MBE, RBE, $PC_{13, 12}$ ← (SP+1) PC_{11-0} ← (SP)(SP+3)(SP+2) PC_{14} ← 0, SP ← SP+4		
					X, X, MBE, RBE ← (SP+4) 0, PC_{14-12} ← (SP+1) PC_{11-0} ← (SP)(SP+3)(SP+2) SP ← SP+6		
	RETS[Note]		1	3+S	MBE, RBE, $PC_{13, 12}$ ← (SP+1) PC_{11-0} ← (SP)(SP+3)(SP+2) PC_{14} ← 0, SP ← SP+4 then skip unconditionally		Unconditional
					X, X, MBE, RBE ← (SP+4) 0, PC_{14-12} ← (SP+1) PC_{11-0} ← (SP)(SP+3)(SP+2) SP ← SP+6 then skip unconditionally		
	RETI[Note]		1	3	MBE, RBE, $PC_{13, 12}$ ← (SP+1), PC_{14} ← 0 PC_{11-0} ← (SP)(SP+3)(SP+2) PSW ← (SP+4)(SP+5), SP ← SP+6		
					0, PC_{14-12} ← (SP+1) PC_{11-0} ← (SP)(SP+3)(SP+2) PSW ← (SP+4)(SP+5), SP ← SP+6		

Note Shaded areas indicate support for Mk II mode only. Other areas indicate support for Mk I mode only.

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Instruction Group	Mnemonic	Operand	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Subroutine stack control	PUSH	rp	1	1	(SP–1)(SP–2) ← rp, SP ← SP–2		
		BS	2	2	(SP–1) ← MBS, (SP–2) ← RBS, SP ← SP–2		
	POP	rp	1	1	rp ← (SP+1)(SP), SP ← SP+2		
		BS	2	2	MBS ← (SP+1), RBS ← (SP), SP ← SP+2		
Interrupt control	EI		2	2	IME(IPS.3) ← 1		
		IEXXX	2	2	IEXXX ← 1		
	DI		2	2	IME(IPS.3) ← 0		
		IEXXX	2	2	IEXXX ← 0		
I/O	IN[Note 1]	A, PORTn	2	2	A ← PORTn (n=0-7)		
		XA, PORTn	2	2	XA ← PORTn+1, PORTn (n=4, 6)		
	OUT[Note 1]	PORTn, A	2	2	PORTn ← A (n=2-7)		
		PORTn, XA	2	2	PORTn+1, PORTn ← XA (n=4, 6)		
CPU control	HALT		2	2	Set HALT Mode(PCC.2 ← 1)		
	STOP		2	2	Set STOP Mode(PCC.3 ←1)		
	NOP		1	1	No Operation		
Special	SEL	RBn	2	2	RBS ← n (n=0-3)		
		MBn	2	2	MBS ← n (n=0-3, 15)		
	GETI[Note 2, 3]	taddr	1	3	• When using TBR instruction PC13-0 ← (taddr)5-0+(taddr+1), PC14 ← 0	*10	
					• When using TCALL instruction (SP–4)(SP–1)(SP–2) ← PC11-0 (SP–3) ← MBE, RBE, PC13, 12, PC14 ← 0 PC13-0 ← (taddr)5-0+(taddr+1) SP ← SP–4		
					• When using instruction other than TBR or TCALL Execute (taddr)(taddr+1) instructions		Determined by referenced instruction
			1	3	• When using TBR instruction PC13-0 ← (taddr)5-0+(taddr+1), PC14 ← 0	*10	
				4	• When using TCALL instruction (SP–5) ← 0, PC14-12 (SP–6)(SP–3)(SP–4) ← PC11-0 (SP–2) ← X, X, MBE, RBE, PC14 ← 0 PC13-0 ← (taddr)5-0+(taddr+1) SP ← SP–6		
				3	• When using instruction other than TBR or TCALL Execute (taddr)(taddr+1) instructions		Determined by referenced instruction

Notes 1. Before executing the IN or OUT instruction, set MBE to 0 or 1 and set MBS to 15.

2. TBR and TCALL instructions are assembler pseudo-instructions for the GETI instruction's table definitions.

3. Shaded areas indicate support for Mk II mode only. Other areas indicate support for Mk I mode only.

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8. ONE-TIME PROM (PROGRAM MEMORY) WRITE AND VERIFY

The program memory contained in the μPD75P3018A is a 32768 × 8-bit one-time PROM that can be electrically written one time only. The pins listed in the table below are used for this one-time PROM's write/verify operations. Clock input from the X1 pin is used instead of address input as a method for updating addresses.

Pin	Function
V_{PP}	Pin where program voltage is applied during program memory write/verify (usually V_{DD} potential)
X1, X2	Clock input pins for address updating during program memory write/verify. Input the X1 pin's inverted signal to the X2 pin.
MD0-MD3	Operation mode selection pin for program memory write/verify
D0/P40 to D3/P43 (low-order 4 bits) D4/P50 to D7/P53 (high-order 4 bits)	8-bit data I/O pins for program memory write/verify
V_{DD}	Pin where power supply voltage is applied. Applies V_{DD} = 1.8 to 5.5 V in normal operation mode and +6 V for program memory write/verify.

★ **Caution Pins not used for program memory write/verify should be connected to V_{SS} via a resistor individually.**

8.1 Operation Modes for Program Memory Write/Verify

When +6 V is applied to the V_{DD} pin and +12.5 V to the V_{PP} pin, the μPD75P3018A enters the program memory write/verify mode. The following operation modes can be specified by setting pins MD0 to MD3 as shown below.

Operation Mode Specification						Operation Mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Zero-clear program memory address
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	X	H	H	Program inhibit mode

X: L or H

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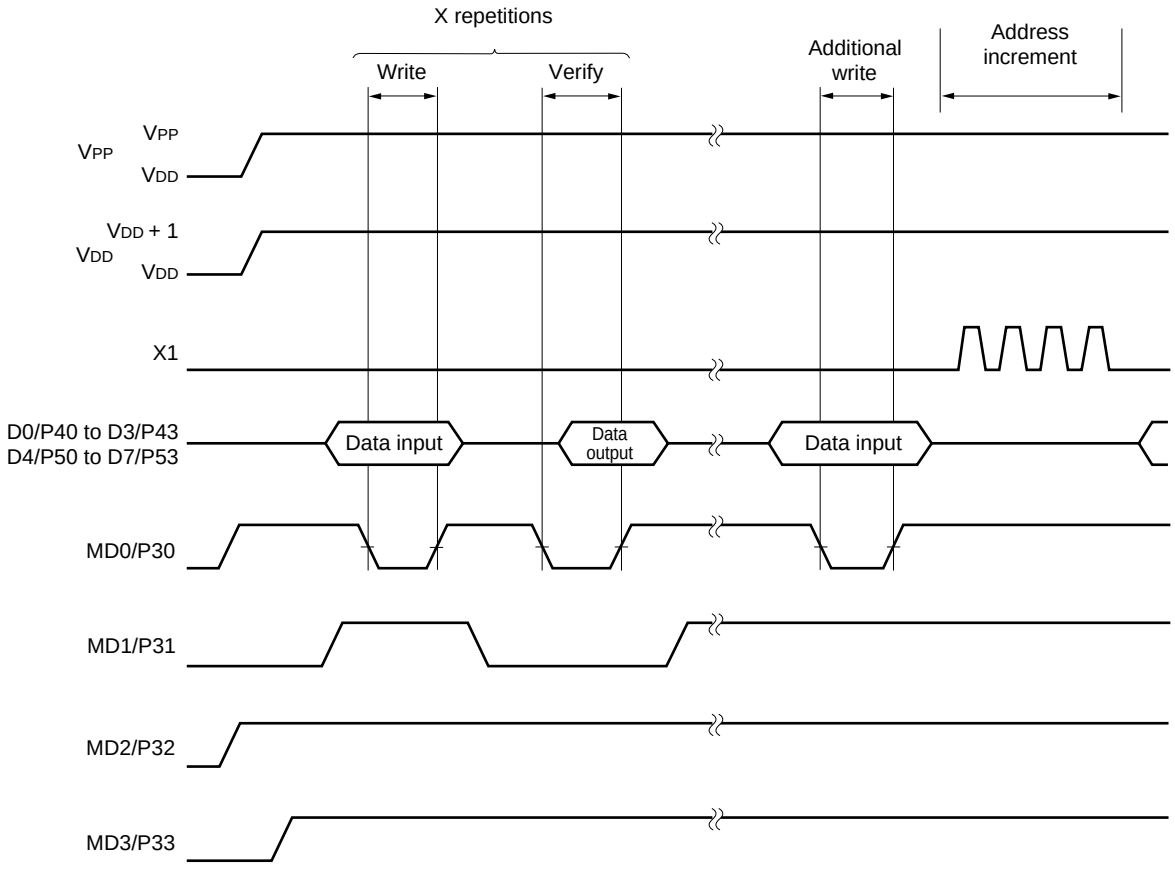
8.2 Program Memory Write Procedure

Program memory can be written at high speed using the following procedure.

(1) Pull unused pins to Vss through resistors. Set the X1 pin low.
(2) Supply 5 V to the V_{DD} and V_{PP} pins.
(3) Wait 10 μs.
(4) Select the zero-clear program memory address mode.
(5) Supply 6 V to the V_{DD} and 12.5 V to the V_{PP} pins.
(6) Write data in the 1 ms write mode.
(7) Select the verify mode. If the data is correct, go to step (8) and if not, repeat steps (6) and (7).
(8) (X : number of write operations from steps (6) and (7)) × 1 ms additional write.
(9) Apply four pulses to the X1 pin to increment the program memory address by one.
(10) Repeat steps (6) to (9) until the end address is reached.
(11) Select the zero-clear program memory address mode.
(12) Return the V_{DD} and V_{PP} pins back to 5 V.
(13) Turn off the power.

The following figure shows steps (2) to (9).



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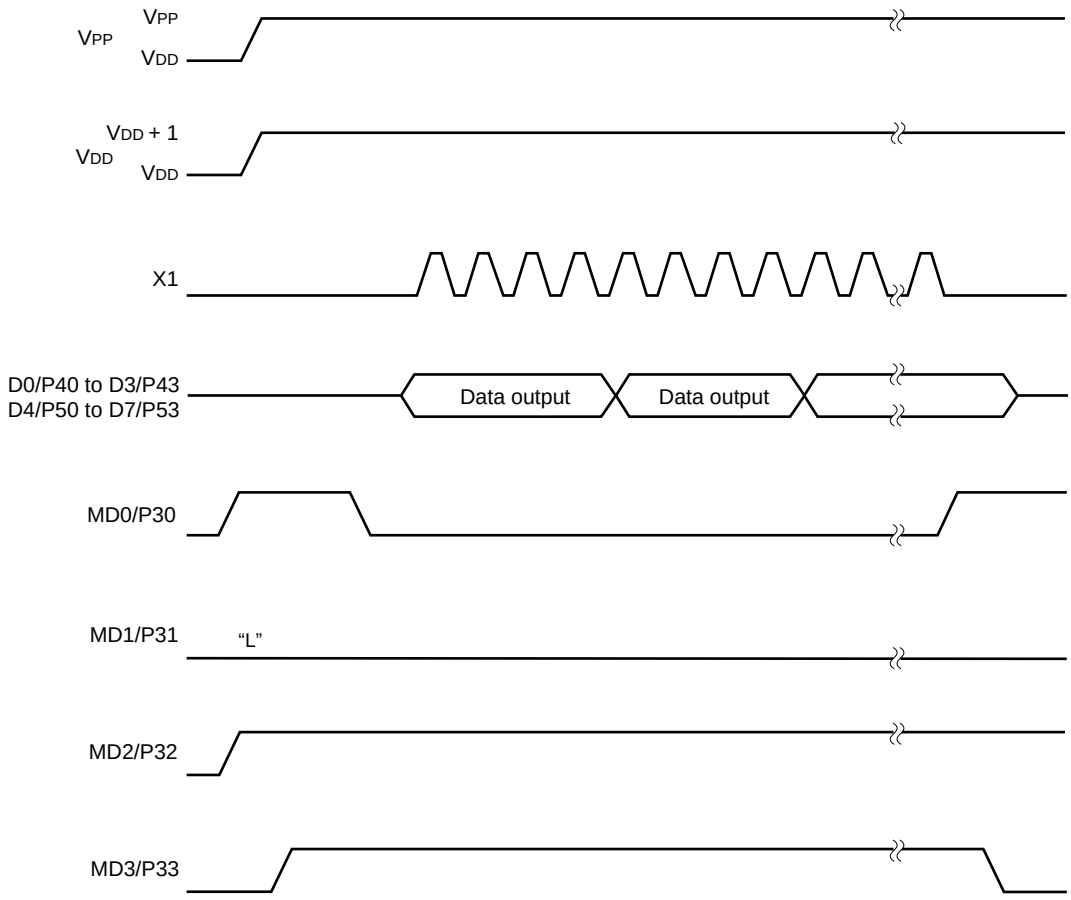
8.3 Program Memory Read Procedure

The μPD75P3018A can read program memory contents using the following procedure.

(1) Pull unused pins to Vss through resistors. Set the X1 pin low.
(2) Supply 5 V to the V_{DD} and V_{PP} pins.
(3) Wait 10 μs.
(4) Select the zero-clear program memory address mode.
(5) Supply 6 V to the V_{DD} and 12.5 V to the V_{PP} pins.
(6) Select the verify mode. Apply four pulses to the X1 pin. Every four clock pulses will output the data stored in one address.
(7) Select the zero-clear program memory address mode.
(8) Return the V_{DD} and V_{PP} pins back to 5 V.
(9) Turn off the power.

The following figure shows steps (2) to (7).



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8.4 One-time PROM Screening

Due to its structure, the one-time PROM cannot be fully tested before shipment by NEC. Therefore, NEC recommends that after the required data is written and the PROM is stored under the temperature and time conditions shown below, the PROM should be verified via a screening.

Storage Temperature	Storage Time
125°C	24 hours

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9. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +7.0	V
PROM supply voltage	V_{PP}		–0.3 to +13.5	V
Input voltage	V_{I1}	Other than ports 4 and 5	–0.3 to V_{DD} + 0.3	V
	V_{I2}	Ports 4 and 5 (During N-ch open drain)	–0.3 to +14	V
Output voltage	V_O		–0.3 to V_{DD} + 0.3	V
High-level output current	I_{OH}	Per pin	–10	mA
		Total of all pins	–30	mA
Low-level output current	I_{OL}	Per pin	30	mA
		Total of all pins	220	mA
Operating ambient temperature	T_A		–40 to +85[Note]	°C
Storage temperature	T_{stg}		–65 to +150	°C

Note To drive LCD in normal mode, T_A = –10 to +85°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Capacitance (T_A = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz			15	pF
Output capacitance	C_{OUT}	Unmeasured pins returned to 0 V			15	pF
I/O capacitance	C_{IO}				15	pF

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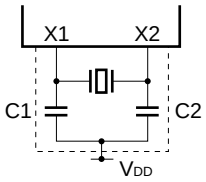
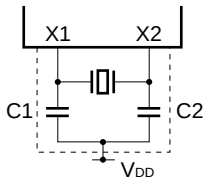
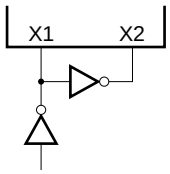
Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1		1.0		6.0Note 2	MHz
		Oscillation stabilization timeNote 3	After V_{DD} has reached MIN. value of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f_X)Note 1		1.0		6.0Note 2	MHz
		Oscillation stabilization timeNote 3	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X)Note 1		1.0		6.0Note 2	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		83.3		500	ns

Notes 1. The oscillation frequency and X1 input frequency shown above indicate characteristics of the oscillator only. For the instruction execution time, refer to **AC Characteristics**.

2. If the oscillation frequency is 4.19 MHz < f_X ≤ 6.0 MHz at 1.8 V ≤ V_{DD} < 2.7 V, do not select processor clock control register (PCC) = 0011. If PCC = 0011, one machine cycle is less than 0.95 μs, falling short of the rated value of 0.95 μs.

3. The oscillation stabilization time is the time required for oscillation to be stabilized after V_{DD} has been applied or STOP mode has been released.

Caution When using the main system clock oscillator, wire the portion enclosed in the broken line in the above figure as follows to prevent adverse influence due to wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with other signal lines.**
- **Do not route the wiring in the vicinity of a line through which a high alternating current flows.**
- **Always keep the ground point of the capacitor of the oscillator at the same potential as V_{DD}.**
- **Do not ground to a power supply pattern through which a high current flows.**
- **Do not extract signals from the oscillator.**

★ **Remark** For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

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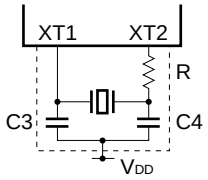
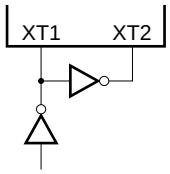
Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 5.5 V		1.0	2	s
						10	
External clock		XT1 input frequency (f_{XT})Note 1		32		100	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. The oscillation frequency and XT1 input frequency shown above indicate characteristics of the oscillator only. For the instruction execution time, refer to **AC Characteristics**.

2. The oscillation stabilization time is the time required for oscillation to be stabilized after V_{DD} has been applied.

Caution When using the subsystem clock oscillator , wire the portion enclosed in the broken line in the above figure as follows to prevent adverse influence due to wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with other signal lines.**
- **Do not route the wiring in the vicinity of a line through which a high alternating current flows.**
- **Always keep the ground point of the capacitor of the oscillator at the same potential as V_{DD}.**
- **Do not ground to a power supply pattern through which a high current flows.**
- **Do not extract signals from the oscillator.**

The subsystem clock oscillator has a low amplification factor to reduce current consumption and is more susceptible to noise than the main system clock oscillator. Therefore, exercise utmost care in wiring the subsystem clock oscillator.

★ **Remark** For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

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DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-level output current	I_{OL}	Per pin				15	mA
		Total of all pins				150	mA
High-level input voltage	V_{IH1}	Ports 2, 3	2.7 V ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0.9V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, 7, $\overline{\text{RESET}}$	2.7 V ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0.9V_{DD}		V_{DD}	V
	V_{IH3}	Ports 4, 5 (N-ch open-drain)	2.7 V ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		13	V
			1.8 V ≤ V_{DD} < 2.7 V	0.9V_{DD}		13	V
	V_{IH4}	X1, XT1		V_{DD} – 0.1		V_{DD}	V
Low-level input voltage	V_{IL1}	Ports 2 to 5	2.7 V ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.1V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, 7, $\overline{\text{RESET}}$	2.7 V ≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.1V_{DD}	V
	V_{IL3}	X1, XT1		0		0.1	V
High-level output voltage	V_{OH}	$\overline{\text{SCK}}$, SO, Ports 2, 3, 6, 7, BP0 to BP7 I_{OH} = –1.0 mA		V_{DD} – 0.5			V
Low-level output voltage	V_{OL1}	$\overline{\text{SCK}}$, SO, Ports 2 to 7, BP0 to BP7	I_{OL} = 15 mA V_{DD} = 4.5 to 5.5 V		0.2	2.0	V
			I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1	N-ch open-drain Pull-up resistor ≥ 1 kΩ			0.2V_{DD}	V
High-level input leakage current	I_{LIH1}	V_{IN} = V_{DD}	Pins other than X1, XT1			3	μA
	I_{LIH2}		X1, XT1			20	μA
	I_{LIH3}	V_{IN} = 13 V	Ports 4, 5 (N-ch open-drain)			20	μA
Low-level input leakage current	I_{LIL1}	V_{IN} = 0 V	Pins other than X1, XT1, Ports 4, 5			–3	μA
	I_{LIL2}		X1, XT1			–20	μA
	I_{LIL3}		Ports 4, 5 (N-ch open-drain) When input instruction is not executed			–3	μA
			Ports 4, 5 (N-ch open-drain). When input instruction is executed			–30	μA
			V_{DD} = 5.0 V		–10	–27	μA
			V_{DD} = 3.0 V		–3	–8	μA
High-level output leakage current	I_{LOH1}	V_{OUT} = V_{DD}	$\overline{\text{SCK}}$, SO/SB0, SB1, Ports 2, 3, 6, 7			3	μA
	I_{LOH2}	V_{OUT} = 13 V	Ports 4, 5 (N-ch open-drain)			20	μA
Low-level output leakage current	I_{LOL}	V_{OUT} = 0 V				–3	μA
Internal pull-up resistor	R_L	V_{IN} = 0 V	Ports 0 to 3, 6, 7 (except P00 pin)	50	100	200	kΩ

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DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}	VAC0 = 0	T_A = –40 to +85°C		2.7		V_{DD}	V
			T_A = –10 to +85°C		2.2		V_{DD}	V
		VAC0 = 1			1.8		V_{DD}	V
VAC current[Note 1]	I_{VAC}	VAC0 = 1, V_{DD} = 2.0 V ±10%				1	4	μA
LCD output voltage deviation[Note 2] (common)	V_{ODC}	I_O = ±1.0 μA	$V_{LCD0} = V_{LCD}$ $V_{LCD1} = V_{LCD} \times 2/3$ $V_{LCD2} = V_{LCD} \times 1/3$		0		±0.2	V
LCD output voltage deviation[Note 2] (segment)	V_{ODS}	I_O = ±0.5 μA	1.8 V ≤ V_{LCD} ≤ V_{DD}		0		±0.2	V
Supply current[Note 3]	I_{DD1}	6.0 MHz[Note 4] crystal oscillation C1 = C2 = 22 pF	V_{DD} = 5.0 V ±10%[Note 5]			3.7	11.0	mA
			V_{DD} = 3.0 V ±10%[Note 6]			0.73	2.2	mA
	I_{DD2}		HALT mode	V_{DD} = 5.0 V ±10%		0.92	2.6	mA
				V_{DD} = 3.0 V ±10%		0.3	0.9	mA
	I_{DD1}	4.19 MHz[Note 4] crystal oscillation C1 = C2 = 22 pF	V_{DD} = 5.0 V ±10%[Note 5]			2.7	8.0	mA
			V_{DD} = 3.0 V ±10%[Note 6]			0.57	1.7	mA
	I_{DD2}		HALT mode	V_{DD} = 5.0 V ±10%		0.90	2.5	mA
				V_{DD} = 3.0 V ±10%		0.28	0.8	mA
	I_{DD3}	32.768 kHz[Note 7] crystal oscillation	Low-voltage mode[Note 8]	V_{DD} = 3.0 V ±10%		42	126	μA
				V_{DD} = 2.0 V ±10%		37	110	μA
				V_{DD} = 3.0 V, T_A = 25°C		42	84	μA
			Low current consumption mode[Note 9]	V_{DD} = 3.0 V ±10%		39	117	μA
				V_{DD} = 3.0 V, T_A = 25°C		39	78	μA
	I_{DD4}		HALT mode	Low-voltage mode[Note 8] V_{DD} = 3.0 V ±10%		8.5	25	μA
				Low-voltage mode[Note 8] V_{DD} = 2.0 V ±10%		5.8	17	μA
				Low-voltage mode[Note 8] V_{DD} = 3.0 V, T_A = 25°C		8.5	17	μA
				Low current consumption mode[Note 9] V_{DD} = 3.0 V ±10%		3.5	12	μA
				Low current consumption mode[Note 9] V_{DD} = 3.0 V, T_A = 25°C		3.5	7	μA
	I_{DD5}	XT1 = 0 V[Note 10] STOP mode	V_{DD} = 5.0 V ±10%			0.05	10	μA
			V_{DD} = 3.0 V ±10%			0.02	5	μA
				T_A = 25°C		0.02	3	μA

Notes 1. Clear VAC0 to 0 in the low current consumption mode and STOP mode. When VAC0 is set to 1, the current increases by about 1 μA.

2. Voltage deviation is the difference between the ideal values (VLCDn ; n = 0, 1, 2) of the segment and common outputs and the output voltage.

3. The current flowing through the internal pull-up resistor is not included.

4. Including the case when the subsystem clock oscillates.

5. When the device operates in high-speed mode with the processor clock control register (PCC) set to 0011.

6. When the device operates in low-speed mode with PCC set to 0000.

7. When the device operates on the subsystem clock, with the system clock control register (SCC) set to 1001 and oscillation of the main system clock stopped.

8. When the sub-oscillation circuit control register (SOS) is set to 0000.

9. When the SOS is set to 0010.

10. When the SOS is set to 00x1, and the feedback resistor of the sub-oscillator is cut (x: don't care).

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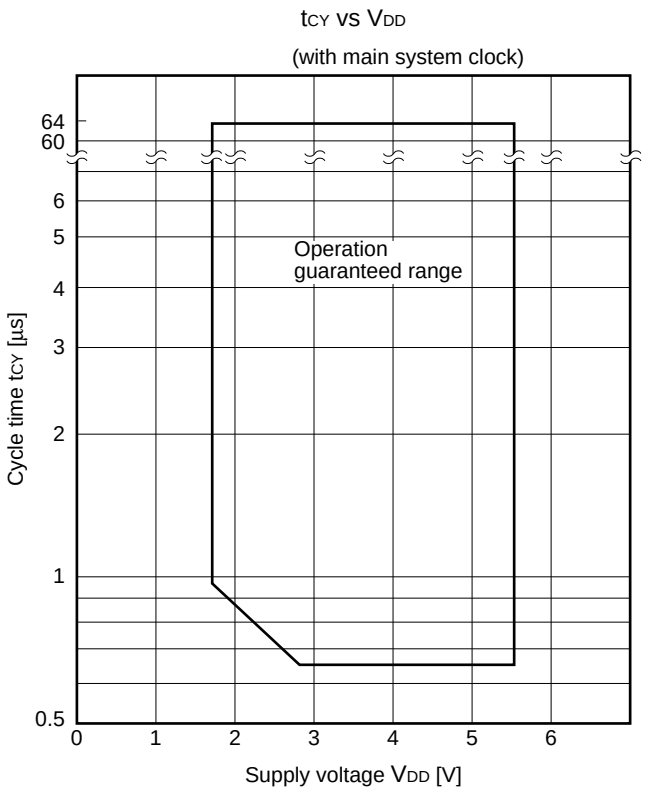
AC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CPU clock cycle time Note 1 (minimum instruction execution time = 1 machine cycle)	t_{CY}	Operation with main system clock	V_{DD} = 2.7 to 5.5 V	0.67		64	μs
				0.95		64	μs
		Operation with subsystem clock		114	122	125	μs
TI0, TI1, TI2 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V		0		1.0	MHz
				0		275	kHz
TI0, TI1, TI2 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V		0.48			μs
				1.8			μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INT0	IM02 = 0	**Note 2**			μs
			IM02 = 1	10			μs
		INT1, 2, 4		10			μs
		KR0-7		10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

Notes 1. The cycle time (minimum instruction execution time) of the CPU clock (Φ) is determined by the oscillation frequency of the connected resonator (and external clock), the system clock control register (SCC), and processor clock control register (PCC).

The figure on the right shows the supply voltage V_{DD} vs. cycle time t_{CY} characteristics when the device operates with the main system clock.

2. $2t_{CY}$ or $128/f_X$ depending on the setting of the interrupt mode register (IM0).



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Serial transfer operation

2-wire and 3-wire serial I/O modes ($\overline{SCK}$ ... internal clock output): (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		1300			ns
				3800			ns
$\overline{SCK}$ high-/low-level width	t_{KL1}, t_{KH1}	V_{DD} = 2.7 to 5.5 V		t_{KCY1}/2–50			ns
				t_{KCY1}/2–150			ns
SI[Note 1] setup time (to $\overline{SCK}$ ↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
				500			ns
SI[Note 1] hold time (from $\overline{SCK}$ ↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
$\overline{SCK}$ ↓ → SO[Note 1] output	t_{KSO1}	R_L = 1 kΩ, [Note 2]	V_{DD} = 2.7 to 5.5 V	0		250	ns
delay time		C_L = 100 pF		0		1000	ns

Notes 1. In 2-wire serial I/O mode, read SB0 or SB1 instead.

2. R_L and C_L respectively indicate the load resistance and load capacitance of the SO output line.

2-wire and 3-wire serial I/O modes ($\overline{SCK}$ ... external clock input): (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCK}$ high-/low-level width	t_{KL2}, t_{KH2}	V_{DD} = 2.7 to 5.5 V		400			ns
				1600			ns
SI[Note 1] setup time (to $\overline{SCK}$ ↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
				150			ns
SI[Note 1] hold time (from $\overline{SCK}$ ↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
$\overline{SCK}$ ↓ → SO[Note 1] output	t_{KSO2}	R_L = 1 kΩ, [Note 2]	V_{DD} = 2.7 to 5.5 V	0		300	ns
delay time		C_L = 100 pF		0		1000	ns

Notes 1. In 2-wire serial I/O mode, read SB0 or SB1 instead.

2. R_L and C_L respectively indicate the load resistance and load capacitance of the SO output line.

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SBI mode ($\overline{SCK}$ ... internal clock output (master)): (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V		1300			ns
				3800			ns
$\overline{SCK}$ high-/low-level width	t_{KL3}, t_{KH3}	V_{DD} = 2.7 to 5.5 V		t_{KCY3}/2–50			ns
				t_{KCY3}/2–150			ns
SB0, 1 setup time (to $\overline{SCK}$ ↑)	t_{SIK3}	V_{DD} = 2.7 to 5.5 V		150			ns
				500			ns
SB0, 1 hold time (from $\overline{SCK}$ ↑)	t_{KSI3}			t_{KCY3}/2			ns
$\overline{SCK}$ ↓ → SB0, 1 output delay time	t_{KSO3}	R_L = 1 kΩ, Note C_L = 100 pF	V_{DD} = 2.7 to 5.5 V	0		250	ns
				0		1000	ns
$\overline{SCK}$ ↑ → SB0, 1 ↓	t_{KSB}			t_{KCY3}			ns
SB0, 1 ↓ → $\overline{SCK}$ ↓	t_{SBK}			t_{KCY3}			ns
SB0, 1 low-level width	t_{SBL}			t_{KCY3}			ns
SB0, 1 high-level width	t_{SBH}			t_{KCY3}			ns

Note R_L and C_L respectively indicate the load resistance and load capacitance of the SB0, 1 output line.

SBI mode ($\overline{SCK}$ ... external clock input (slave)): (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCK}$ high-/low-level width	t_{KL4}, t_{KH4}	V_{DD} = 2.7 to 5.5 V		400			ns
				1600			ns
SB0, 1 setup time (to $\overline{SCK}$ ↑)	t_{SIK4}	V_{DD} = 2.7 to 5.5 V		100			ns
				150			ns
SB0, 1 hold time (from $\overline{SCK}$ ↑)	t_{KSI4}			t_{KCY4}/2			ns
$\overline{SCK}$ ↓ → SB0, 1 output delay time	t_{KSO4}	R_L = 1 kΩ, Note C_L = 100 pF	V_{DD} = 2.7 to 5.5 V	0		300	ns
				0		1000	ns
$\overline{SCK}$ ↑ → SB0, 1 ↓	t_{KSB}			t_{KCY4}			ns
SB0, 1 ↓ → $\overline{SCK}$ ↓	t_{SBK}			t_{KCY4}			ns
SB0, 1 low-level width	t_{SBL}			t_{KCY4}			ns
SB0, 1 high-level width	t_{SBH}			t_{KCY4}			ns

Note R_L and C_L respectively indicate the load resistance and load capacitance of the SB0, 1 output line.

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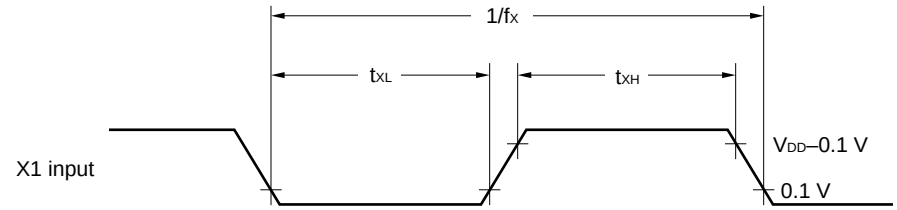
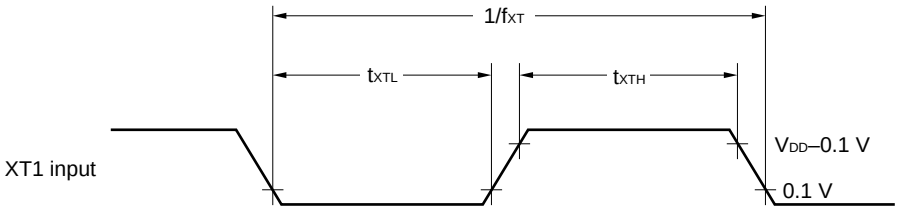
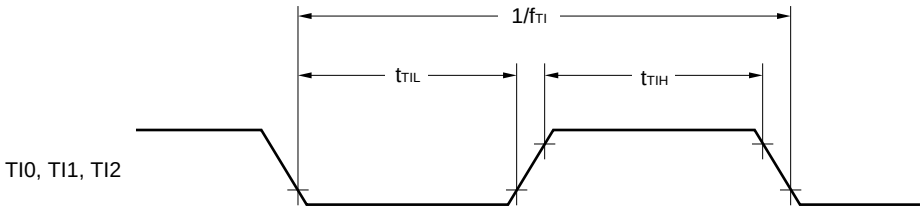
AC Timing Test Points (except X1 and XT1 inputs)

Clock Timing





TI0, TI1, TI2 Timing



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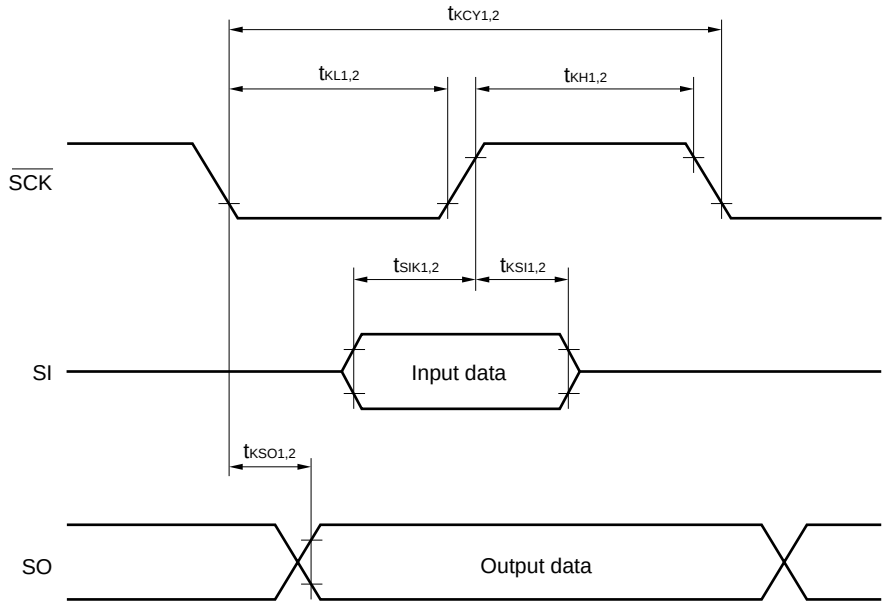
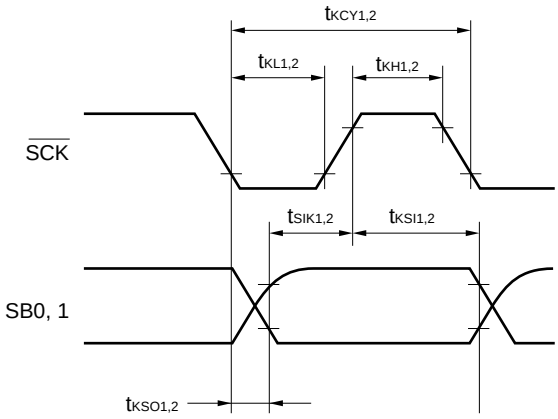
Serial Transfer Timing

3-wire Serial I/O Mode



2-wire Serial I/O Mode



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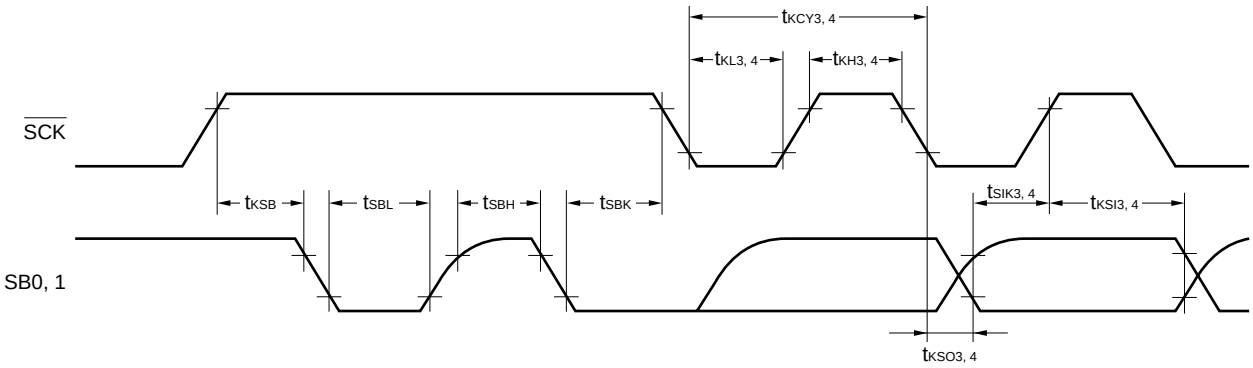
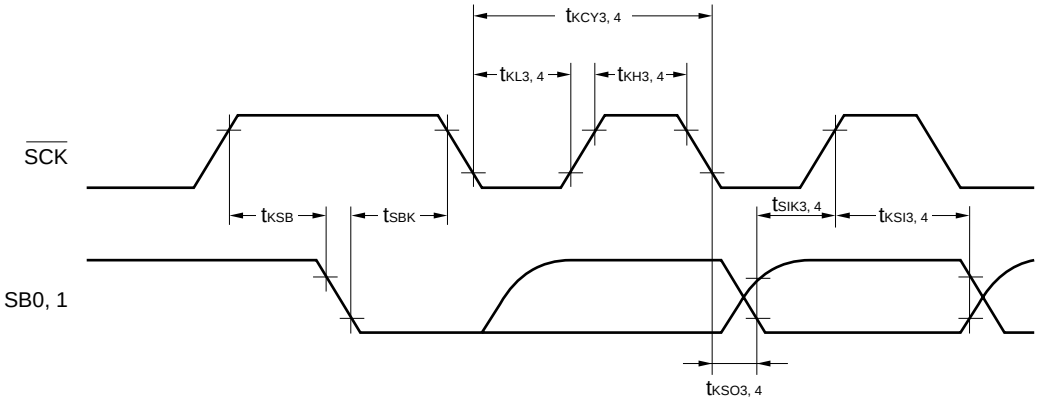
Serial Transfer Timing

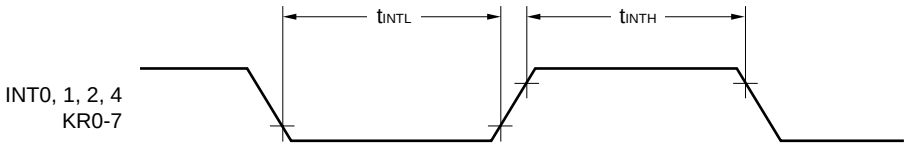
Bus Release Signal Transfer



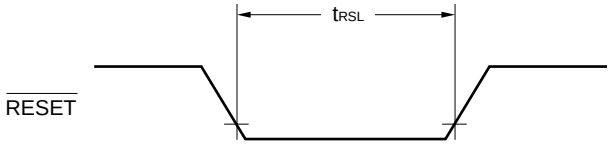
Command Signal Transfer



Interrupt Input Timing



RESET Input Timing



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Data retention characteristics of data memory in STOP mode and at low supply voltage (T_A = –40 to +85°C)

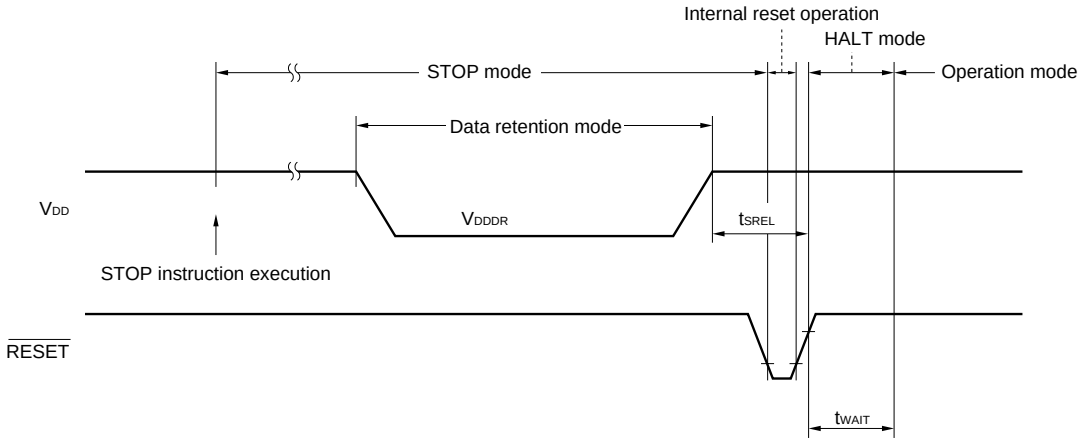
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★ Data retention power supply voltage	V_{DDDR}		1.8		5.5	V
Release signal setup time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note 1]	t_{WAIT}	Released by $\overline{RESET}$		$2^{15}/f_X$		ms
		Released by interrupt request		**Note 2**		ms

Notes 1. The oscillation stabilization wait time is the time during which the CPU stops operating to prevent unstable operation when oscillation is started.

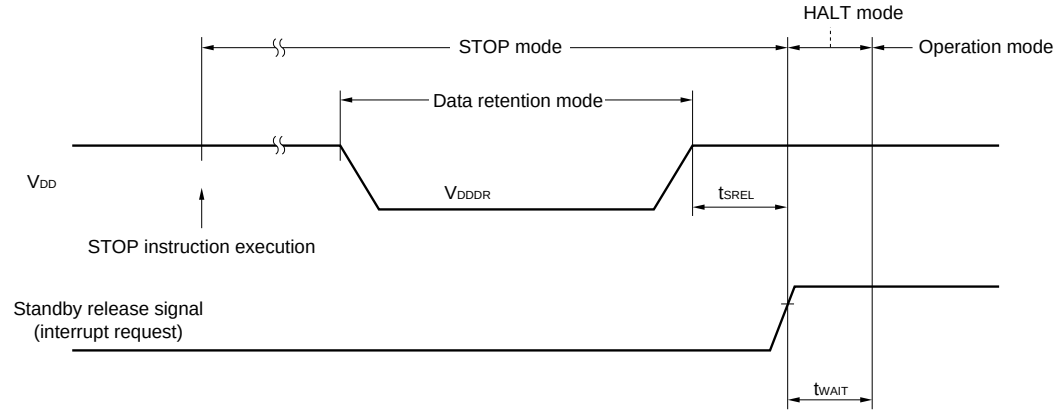
2. Set by the basic interval timer mode register (BTM). (Refer to the table below.)

BTM3	BTM2	BTM1	BTM0	Wait Time	
				f_X = 4.19 MHz	f_X = 6.0 MHz
–	0	0	0	$2^{20}/f_X$ (approx. 250 ms)	$2^{20}/f_X$ (approx. 175 ms)
–	0	1	1	$2^{17}/f_X$ (approx. 31.3 ms)	$2^{17}/f_X$ (approx. 21.8 ms)
–	1	0	1	$2^{15}/f_X$ (approx. 7.81 ms)	$2^{15}/f_X$ (approx. 5.46 ms)
–	1	1	1	$2^{13}/f_X$ (approx. 1.95 ms)	$2^{13}/f_X$ (approx. 1.37 ms)

Data Retention Timing (when STOP mode released by $\overline{RESET}$)



Data Retention Timing (standby release signal: when STOP mode released by interrupt signal)



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DC Programming Characteristics (T_A = 25 ±5°C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	Pins other than X1, X2	0.7V_{DD}		V_{DD}	V
	V_{IH2}	X1, X2	V_{DD} – 0.5		V_{DD}	V
Low-level input voltage	V_{IL1}	Pins other than X1, X2	0		0.3V_{DD}	V
	V_{IL2}	X1, X2	0		0.4	V
Input leakage current	I_{LI}	V_{IN} = V_{IL} or V_{IH}			10	μA
High-level output voltage	V_{OH}	I_{OH} = –1 mA	V_{DD} – 1.0			V
Low-level output voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
V_{DD} supply current	I_{DD}				30	mA
V_{PP} supply current	I_{PP}	MD0 = V_{IL}, MD1 = V_{IH}			30	mA

Cautions 1. Ensure that V_{PP} does not exceed +13.5 V including overshoot.

2. V_{DD} must be applied before V_{PP}, and cut after V_{PP}.

AC Programming Characteristics (T_A = 25 ±5°C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.3 V, V_{SS} = 0 V)

Parameter	Symbol	**Note 1**	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time[Note 2] (to MD0↓)	t_{AS}	t_{AS}		2			μs
MD1 setup time (to MD0↓)	t_{M1S}	t_{OES}		2			μs
Data setup time (to MD0↓)	t_{DS}	t_{DS}		2			μs
Address hold time[Note 2] (from MD0↑)	t_{AH}	t_{AH}		2			μs
Data hold time (from MD0↑)	t_{DH}	t_{DH}		2			μs
MD0↑→Data output float delay time	t_{DF}	t_{DF}		0		130	ns
V_{PP} setup time (to MD3↑)	t_{VPS}	t_{VPS}		2			μs
V_{DD} setup time (to MD3↑)	t_{VDS}	t_{VCS}		2			μs
Initial program pulse width	t_{PW}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{OPW}	t_{OPW}		0.95		21.0	ms
MD0 setup time (to MD1↑)	t_{M0S}	t_{CES}		2			μs
MD0↓→Data output delay time	t_{DV}	t_{DV}	MD0 = MD1 = V_{IL}			1	μs
MD1 hold time (from MD0↑)	t_{M1H}	t_{OEH}	t_{M1H} + t_{M1R} ≥ 50 μs	2			μs
MD1 recovery time (from MD0↓)	t_{M1R}	t_{OR}		2			μs
Program counter reset time	t_{PCR}	—		10			μs
X1 input high-/low-level widths	t_{XH}, t_{XL}	—		0.125			μs
X1 input frequency	f_X	—				4.19	MHz
Initial mode setting time	t_I	—		2			μs
MD3 setup time (to MD1↑)	t_{M3S}	—		2			μs
MD3 hold time (from MD1↓)	t_{M3H}	—		2			μs
MD3 setup time (to MD0↓)	t_{M3SR}	—	Program memory read	2			μs
Data output delay time from address[Note 2]	t_{DAD}	t_{ACC}	Program memory read			2	μs
Data output hold time from address[Note 2]	t_{HAD}	t_{OH}	Program memory read	0		130	μs
MD3 hold time (from MD0↑)	t_{M3HR}	—	Program memory read	2			μs
MD3↓→Data output float delay time	t_{DFR}	—	Program memory read			2	μs

Notes 1. Symbol of corresponding μPD27C256A

2. The internal address signal is incremented by 1 on the 4th rise of the X1 input, and is not connected to a pin.

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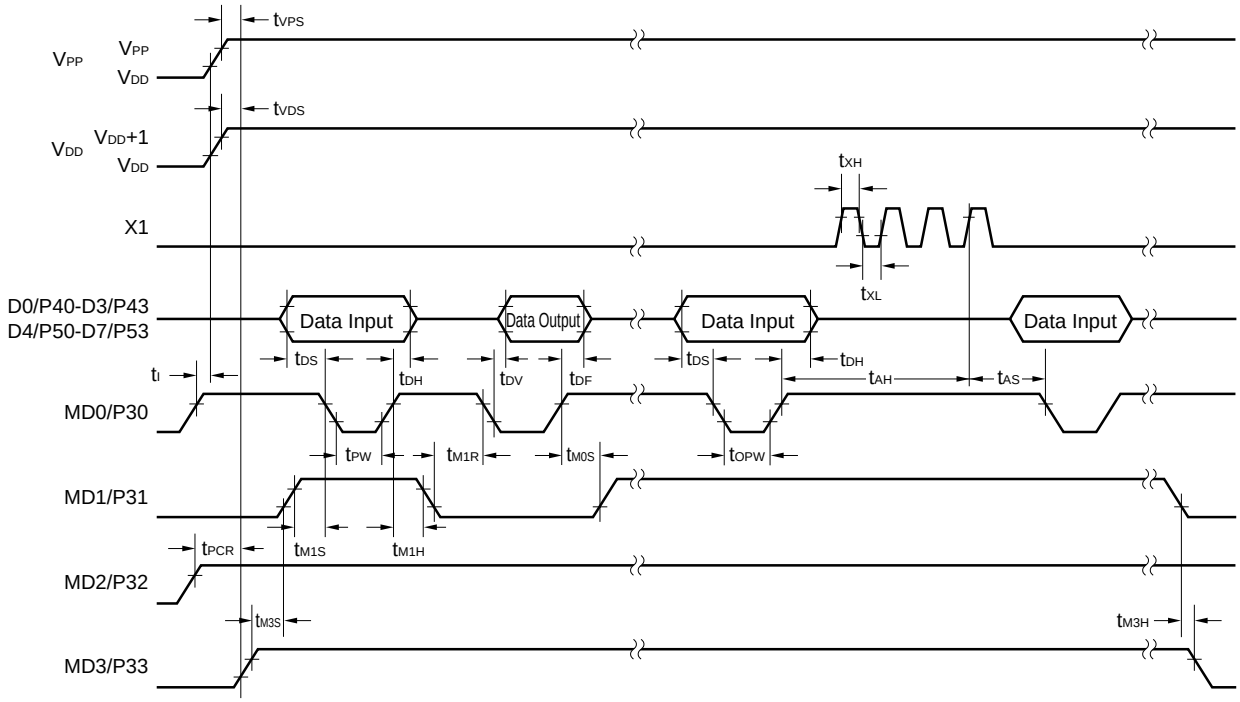
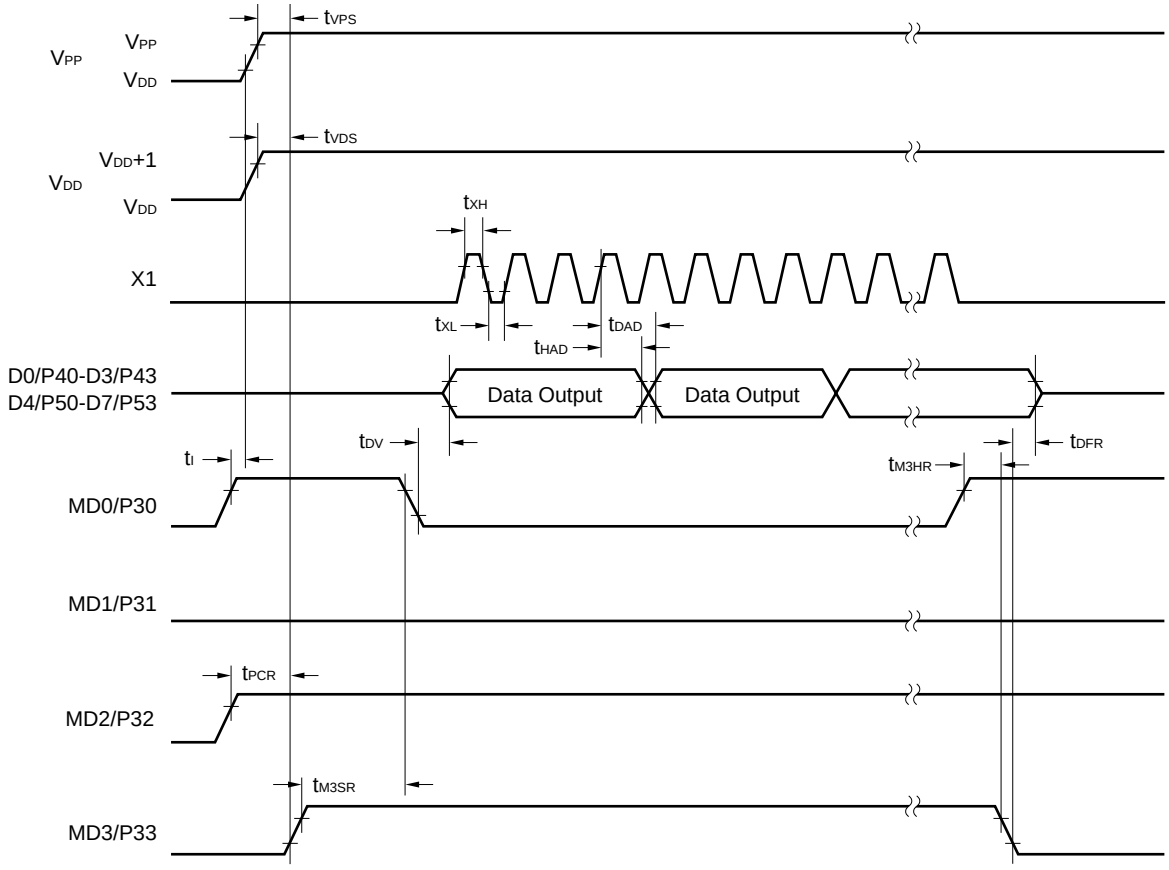
Program Memory Write Timing



Program Memory Read Timing



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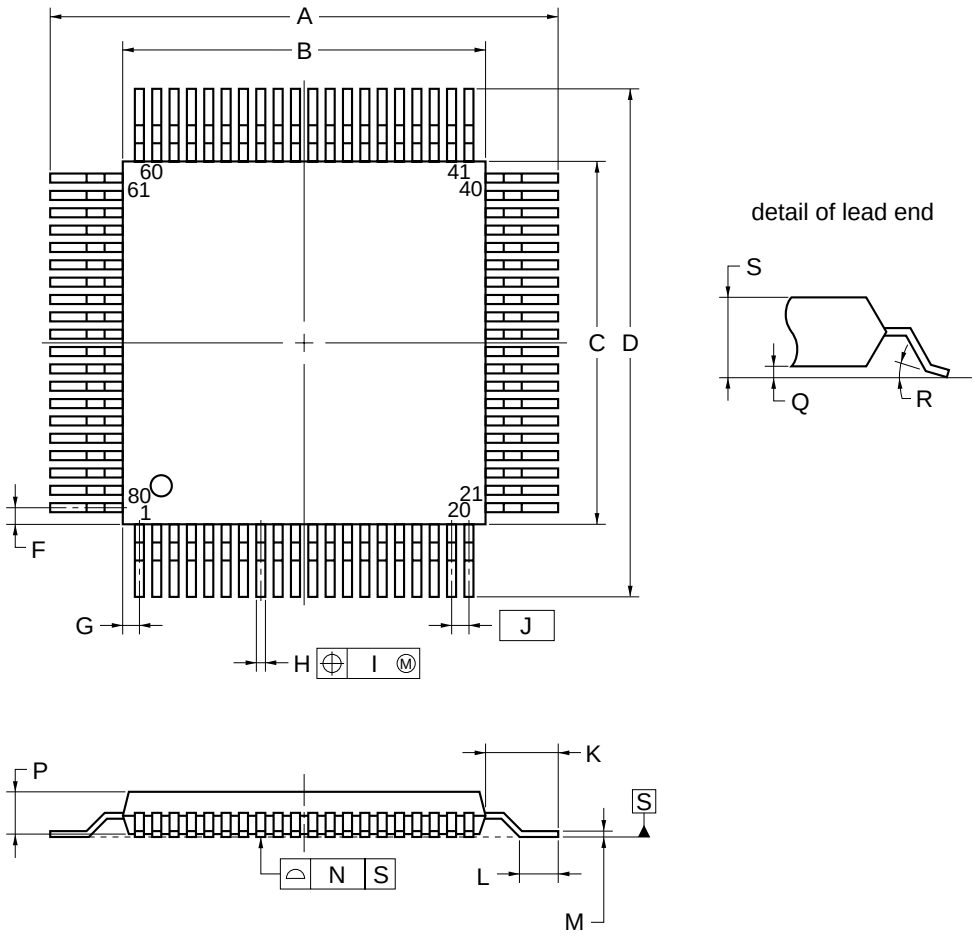
10. PACKAGE DRAWINGS

★80-PIN PLASTIC QFP (14x14)



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.2±0.4
B	14.0±0.2
C	14.0±0.2
D	17.2±0.4
F	0.825
G	0.825
H	0.30±0.10
I	0.13
J	0.65 (T.P.)
K	1.6±0.2
L	0.8±0.2
M	$0.15^{+0.10}_{-0.05}$
N	0.10
P	2.7±0.1
Q	0.1±0.1
R	5°±5°
S	3.0 MAX.

S80GC-65-3B9-6

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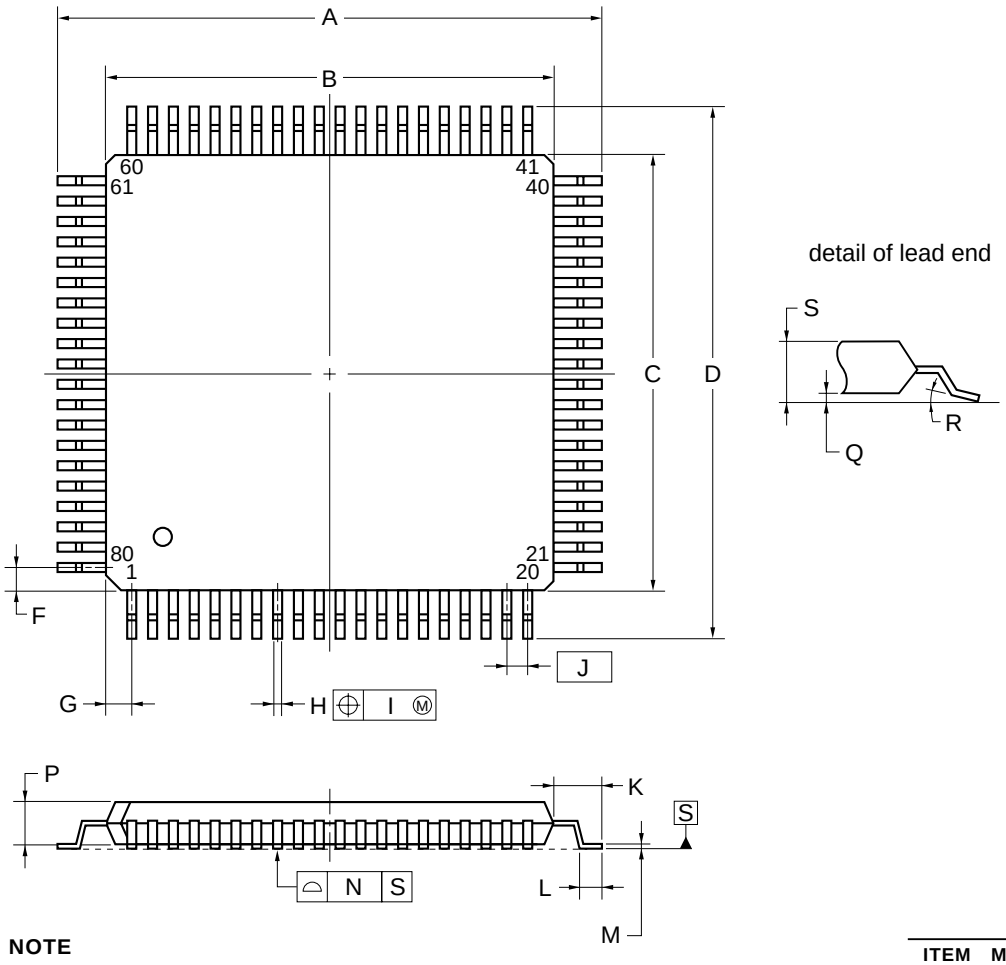
★ 80-PIN PLASTIC QFP (14x14)



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.20±0.20
B	14.00±0.20
C	14.00±0.20
D	17.20±0.20
F	0.825
G	0.825
H	0.32±0.06
I	0.13
J	0.65 (T.P.)
K	1.60±0.20
L	0.80±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	1.40±0.10
Q	0.125±0.075
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.70 MAX.

P80GC-65-8BT-1

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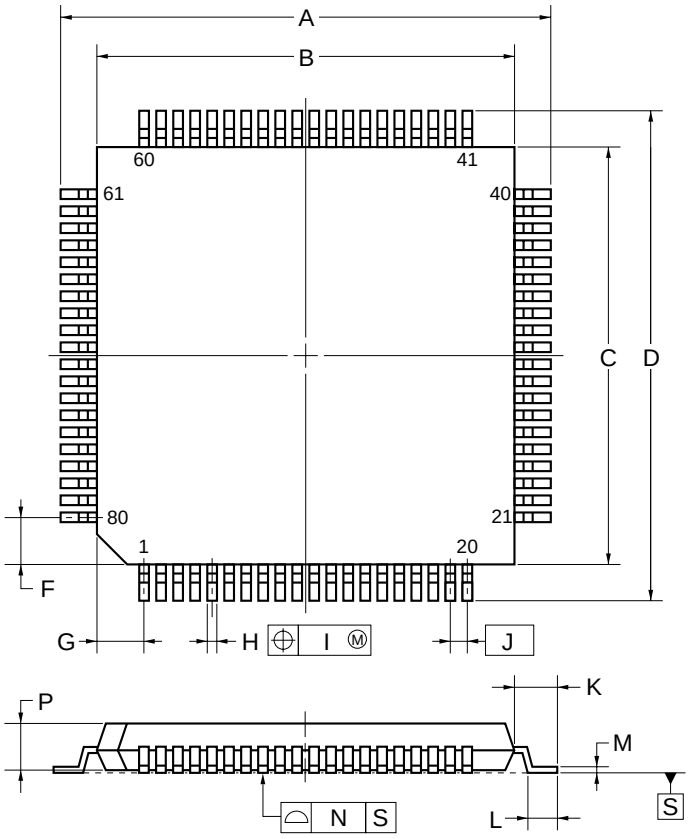
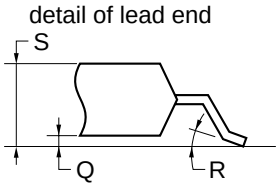
★ 80 PIN PLASTIC TQFP (FINE PITCH) (12x12)





NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	14.00±0.20
B	12.00±0.20
C	12.00±0.20
D	14.00±0.20
F	1.25
G	1.25
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	$0.145^{+0.055}_{-0.045}$
N	0.10
P	1.05±0.07
Q	0.10±0.05
R	5°±5°
S	1.27 MAX.

P80GK-50-BE9-6

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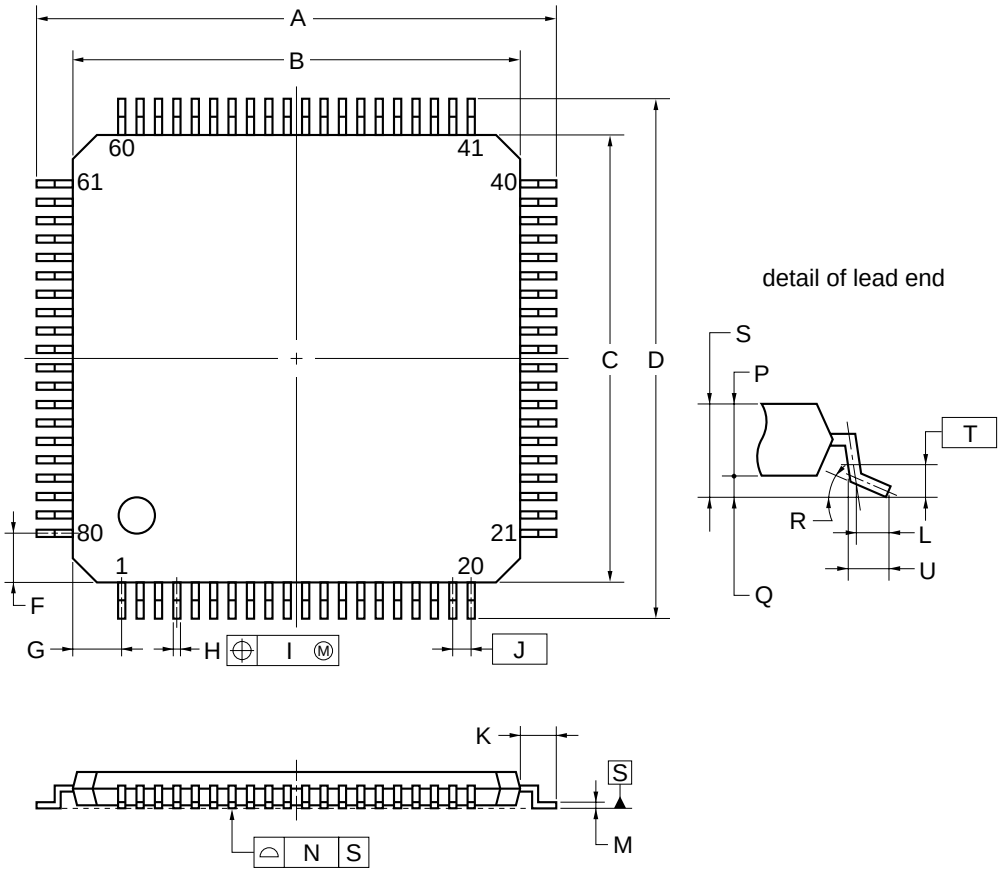
★ 80-PIN PLASTIC TQFP (FINE PITCH) (12x12)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	14.0±0.2
B	12.0±0.2
C	12.0±0.2
D	14.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5
M	0.145±0.05
N	0.08
P	1.0
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.1±0.1
T	0.25
U	0.6±0.15

P80GK-50-9EU-1

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11. RECOMMENDED SOLDERING CONDITIONS

Solder the μPD75P3018A under the following recommended conditions.

For the details on the recommended soldering conditions, refer to Information Document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For the soldering methods and conditions other than those recommended, consult NEC.

Table 11-1. Soldering Conditions of Surface Mount Type (1/2)

(1) μPD75P3018AGC-3B9: 80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Reflow time: 30 seconds or below (210°C or higher), Number of reflow processes: 3 max.	IR35-00-3
VPS	Package peak temperature: 215°C, Reflow time: 40 seconds or below (200°C or higher), Number of reflow processes: 3 max.	VP15-00-3
Wave soldering	Solder temperature: 260°C or below, Flow time: 10 seconds or below, Number of flow processes: 1 Preheating temperature: 120°C or below (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C or below, Time: 3 seconds or below (per side of device)	—

Caution Do not use two or more soldering methods in combination (except the partial heating method).

★ **(2) μPD75P3018AGC-8BT: 80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm)**

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Reflow time: 30 seconds or below (210°C or higher), Number of reflow processes: 2 max.	IR35-00-2
VPS	Package peak temperature: 215°C, Reflow time: 40 seconds or below (200°C or higher), Number of reflow processes: 2 max.	VP15-00-2
Wave soldering	Solder temperature: 260°C or below, Flow time: 10 seconds or below, Number of flow processes: 1 Preheating temperature: 120°C or below (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C or below, Time: 3 seconds or below (per side of device)	—

Caution Do not use two or more soldering methods in combination (except the partial heating method).

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Table 11-1. Soldering Conditions of Surface Mount Type (2/2)

★ **(3) μPD75P3018AGK-BE9: 80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.05 mm)**

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Reflow time: 30 seconds or below (210°C or higher), Number of reflow processes: 3 max., Exposure limit: 7 days[Note] (After that, prebaking is necessary at 125°C for 10 hours)	IR35-107-3
VPS	Package peak temperature: 215°C, Reflow time: 40 seconds or below (200°C or higher), Number of reflow processes: 3 max., Exposure limit: 7 days[Note] (After that, prebaking is necessary at 125°C for 10 hours)	VP15-107-3
Partial heating	Pin temperature: 300°C or below, Time: 3 seconds or below (per side of device)	—

Note The number of days for storage after the dry pack has been opened. The storage conditions are 25°C, 65% RH max.

Caution Do not use two or more soldering methods in combination (except the partial heating method).

★ **(4) μPD75P3018AGK-9EU: 80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.00 mm)**

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Reflow time: 30 seconds or below (210°C or higher), Number of reflow processes: 2 max., Exposure limit: 7 days[Note] (After that, prebaking is necessary at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Reflow time: 40 seconds or below (200°C or higher), Number of reflow processes: 2 max., Exposure limit: 7 days[Note] (After that, prebaking is necessary at 125°C for 10 hours)	VP15-107-2
Partial heating	Pin temperature: 300°C or below, Time: 3 seconds or below (per side of device)	—

Note The number of days for storage after the dry pack has been opened. The storage conditions are 25°C, 65% RH max.

Caution Do not use two or more soldering methods in combination (except the partial heating method).

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APPENDIX A. μPD75316B, 753017A AND 75P3018A FUNCTION LIST

Parameter		μPD75316B	μPD753017A	μPD75P3018A
Program memory		Mask ROM 0000H-3F7FH (16256 × 8 bits)	Mask ROM 0000H-5FFFH (24576 × 8 bits)	One-time PROM 0000H-7FFFH (32768 × 8 bits)
Data memory		000H-3FFH (1024 × 4 bits)		
CPU		75X Standard	75XL CPU	
Instruction execution time	When main system clock is selected	0.95, 1.91, or 15.3 μs (at 4.19 MHz operation)	• 0.95, 1.91, 3.81, or 15.3 μs (at 4.19 MHz operation) • 0.67, 1.33, 2.67, or 10.7 μs (at 6.0 MHz operation)	
	When subsystem clock is selected	122 μs (at 32.768 kHz operation)		
Pin connection	29 to 32	P40 to P43		P40/D0 to P43/D3
	34 to 37	P50 to P53		P50/D4 to P53/D7
	44	P12/INT2	P12/INT2/TI1/TI2	
	47	P21	P21/PTO1	
	48	P22/PCL	P22/PCL/PTO2	
	50 to 53	P30 to P33		P30/MD0 to P33/MD3
	57	IC		V_{PP}
Stack	SBS register	None	SBS.3 = 1; Mk I mode selection SBS.3 = 0; Mk II mode selection	
	Stack area	000H-0FFH	n00H-nFFH (n = 0-3)	
	Subroutine call instruction stack operation	2-byte stack	Mk I mode: 2-byte stack Mk II mode: 3-byte stack	
Instruction	BRA !addr1 CALLA !addr1	Unavailable	Mk I mode: unavailable Mk II mode: available	

	MOVT XA, @BCDE
	MOVT XA, @BCXA
	BR BCDE
	BR BCXA
			Available	

	CALL !addr	3 machine cycles	Mk I mode: 3 machine cycles, Mk II mode: 4 machine cycles	
	CALLF !faddr	2 machine cycles	Mk I mode: 2 machine cycles, Mk II mode: 3 machine cycles	
Mask option		Yes		None
Timer		3 channels: • Basic interval timer : 1 channel • 8-bit timer/event counter : 1 channel • Watch timer: 1 channel	5 channels: • Basic interval timer/watchdog timer: 1 channel • 8-bit timer/event counter: 3 channels (can be used as 16-bit timer/event counter, carrier generator, timer with gate) • Watch timer: 1 channel	

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Parameter		μPD75316B	μPD753017A	μPD75P3018A
Clock output (PCL)		Φ, 524, 262, 65.5 kHz (Main system clock: at 4.19 MHz operation)	• Φ, 524, 262, 65.5 kHz (Main system clock: at 4.19 MHz operation) • Φ, 750, 375, 93.8 kHz (Main system clock: at 6.0 MHz operation)	
BUZ output (BUZ)		2 kHz (Main system clock: at 4.19 MHz operation)	• 2, 4, 32 kHz (Main system clock: at 4.19 MHz operation or subsystem clock: at 32.768 kHz operation) • 2.93, 5.86, 46.9 kHz (Main system clock: at 6.0 MHz operation)	
Serial interface		3 modes are available • 3-wire serial I/O mode ... MSB/LSB can be selected for transfer first bit • 2-wire serial I/O mode • SBI mode		
SOS register	Feedback resistor cut flag (SOS.0)	None	Provided	
	Sub-oscillator current cut flag (SOS.1)	None	Provided	
Register bank selection register (RBS)		None	Yes	
Standby release by INT0		Unavailable	Available	
Interrupt priority selection register (IPS)		None	Yes	
Vectored interrupt		External: 3, Internal: 3	External: 3, Internal: 5	
Supply voltage		V_{DD} = 2.0 to 6.0 V	V_{DD} = 1.8 to 5.5 V	
Operating ambient temperature		T_A = –40 to +85°C		
Package		• 80-pin plastic TQFP (fine pitch) (12 × 12 mm) • 80-pin plastic QFP (14 × 14 mm)		

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APPENDIX B. DEVELOPMENT TOOLS

The following development tools have been provided for system development using the μPD75P3018A. In the 75XL Series, the relocatable assembler common to series is used in combination with the device file of each type.

★

RA75X relocatable assembler	Host machine		Part No. (name)
	OS	Supply medium	
PC-9800 Series	MS-DOS™ (Ver.3.30 to Ver.6.2[Note])	3.5" 2HD	μS5A13RA75X
IBM PC/AT™ or compatible	Refer to **"OS for IBM PCs"**	3.5" 2HC	μS7B13RA75X

★

Device file	Host machine		Part No. (name)
	OS	Supply medium	
PC-9800 Series	MS-DOS (Ver.3.30 to Ver.6.2[Note])	3.5" 2HD	μS5A13DF753017
IBM PC/AT or compatible	Refer to **"OS for IBM PCs"**	3.5" 2HC	μS7B13DF753017

Note Ver. 5.00 or later includes a task swapping function, but this software is not able to use that function.

Remark Operation of the assembler and device file is guaranteed only when using the host machine and OS described above.

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PROM Write Tools

Hardware	PG-1500	This is a PROM programmer that can program single-chip microcontroller with PROM in stand alone mode or under control of host machine when connected with supplied accessory board and optional programmer adapter. It can also program typical PROMs in capacities ranging from 256 K to 4 M bits.			
	PA-75P316BGC	This is a PROM programmer adapter for the μPD75P3018AGC-3B9. It can be used when connected to a PG-1500.			
	PA-75P316BGK	This is a PROM programmer adapter for the μPD75P3018AGK-BE9. It can be used when connected to a PG-1500.			
★	PA-75P3018AGC-8BT	This is a PROM programmer adapter for the μPD75P3018AGC-8BT. It can be used when connected to a PG-1500.			
★	PA-75P3018AGK-9EU	This is a PROM programmer adapter for the μPD75P3018AGK-9EU. It can be used when connected to a PG-1500.			
Software	PG-1500 controller	Connects PG-1500 to host machine with serial and parallel interface and controls PG-1500 on host machine.			
		Host machine			Part No. (name)
			OS	Supply medium	
		PC-9800 Series	MS-DOS (Ver.3.30 to Ver.6.2[Note])	3.5" 2HD	μS5A13PG1500
		IBM PC/AT or compatible	Refer to **"OS for IBM PCs"**	3.5" 2HD	μS7B13PG1500

Note Ver. 5.00 or later includes a task swapping function, but this software is not able to use that function.

Remark Operation of the PG-1500 controller is guaranteed only when using the host machine and OS described above.

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Debugging Tools

In-circuit emulators (IE-75000-R and IE-75001-R) are provided as program debugging tools for the μPD75P3018A.

Various system configurations using these in-circuit emulators are listed below.

Hardware	IE-75000-R[Note 1]	The IE-75000-R is an in-circuit emulator to be used for hardware and software debugging during development of application systems using the 75X or 75XL Series products. For development of the μPD75P3018A, the IE-75000-R is used with optional emulation board (IE-75300-R-EM) and emulation probe (EP-753018GC-R or EP-753018GK-R). Highly efficient debugging can be performed when connected to host machine and PROM programmer. The IE-75000-R includes a connected emulation board (IE-75000-R-EM).			
	IE-75001-R	The IE-75001-R is an in-circuit emulator to be used for hardware and software debugging during development of application systems using the 75X or 75XL Series products. The IE-75001-R is used with optional emulation board (IE-75300-R-EM) and emulation probe (EP-753018GC-R or EP-753018GK-R). Highly efficient debugging can be performed when connected to host machine and PROM programmer.			
	IE-75300-R-EM	This is an emulation board for evaluating application systems using the μPD75P3018A. It is used in combination with the IE-75000-R or IE-75001-R.			
	EP-753018GC-R	This is an emulation probe for the μPD75P3018AGC. When being used, it is connected with the IE-75000-R or IE-75001-R and the IE-75300-R-EM.			
	EV-9200GC-80	It includes a 80-pin conversion socket (EV-9200GC-80) to facilitate connections with target system.			
	EP-753018GK-R	This is an emulation probe for the μPD75P3018AGK. When being used, it is connected with the IE-75000-R or IE-75001-R and the IE-75300-R-EM.			
	TGK-080SDW[Note 2]	It includes a 80-pin conversion adapter (TGK-080SDW) to facilitate connections with target system.			
Software	IE control program	This program can control the IE-75000-R or IE-75001-R on a host machine when connected to the IE-75000-R or IE-75001-R via an RS-232-C or Centronics interface.			
		Host machine			Part No. (name)
			OS	Supply medium	
		PC-9800 Series	MS-DOS (Ver.3.30 to Ver.6.2[Note 3])	3.5" 2HD	μS5A13IE75X
				5" 2HD	μS5A10IE75X
		IBM PC/AT or compatible	Refer to **"OS for IBM PCs"**	3.5" 2HC	μS7B13IE75X
				5" 2HC	μS7B10IE75X

Notes 1. This is a maintenance product.

★ **2.** This is a product of TOKYO ELETECH CORPORATION.

For further information, contact: Daimaru Kogyo, Ltd.

Tokyo Electronics Department (TEL +81-3-3820-7112)

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3. Ver. 5.00 or later includes a task swapping function, but this software is not able to use that function.

Remark Operation of the IE control program is guaranteed only when using the host machine and OS described above.

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OS for IBM PCs

The following operating systems for the IBM PC are supported.

OS	Version
PC DOS™	Ver.5.02 to Ver.6.3 J6.1/V to J6.3/V
MS-DOS	Ver.5.0 to Ver.6.22 5.0/V to 6.2/V
IBM DOS™	J5.02/V

Caution Ver. 5.0 or later includes a task swapping function, but this software is not able to use that function.

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★ APPENDIX C. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Device Related Documents

Document Name	Document No.	
	Japanese	English
μPD753012A, 753016A, 753017A Data Sheet	U11662J	U11662E
μPD75P3018A Data Sheet	U11917J	U11917E (This document)
μPD753017 User's Manual	U11282J	U11282E
μPD753017 Instruction Table	IEM-5598	—
75XL Series Selection Guide	U10453J	U10453E

Development Tool Related Documents

Document Name			Document No.	
			Japanese	English
Hardware	IE-75000-R/IE-75001-R User's Manual		EEU-846	EEU-1416
	IE-75300-R-EM User's Manual		U11354J	U11354E
	EP-753017GC/GK-R User's Manual		EEU-967	EEU-1495
	PG-1500 User's Manual		U11940E	U11940E
Software	RA75X Assembler Package	Operation	U12622J	U12622E
	User's Manual	Language	U12385J	U12385E
	PG-1500 Controller User's Manual	PC-9800 Series (MS-DOS) base	EEU-704	EEU-1291
		IBM PC Series (PC DOS) base	EEU-5008	U10540E

Other Related Documents

Document Name	Document No.	
	Japanese	English
SEMICONDUCTOR SELECTION GUIDE Products & Package (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices Electrostatic Discharge (ESD)	C11892J	C11892E
Guide to Microcontroller-Related Products by Third Parties	U11416J	—

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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