

# BIPOLAR ANALOG INTEGRATED CIRCUIT

# $\mu$ PC4570

## DUAL ULTRA LOW-NOISE, WIDEBAND, OPERATIONAL AMPLIFIER

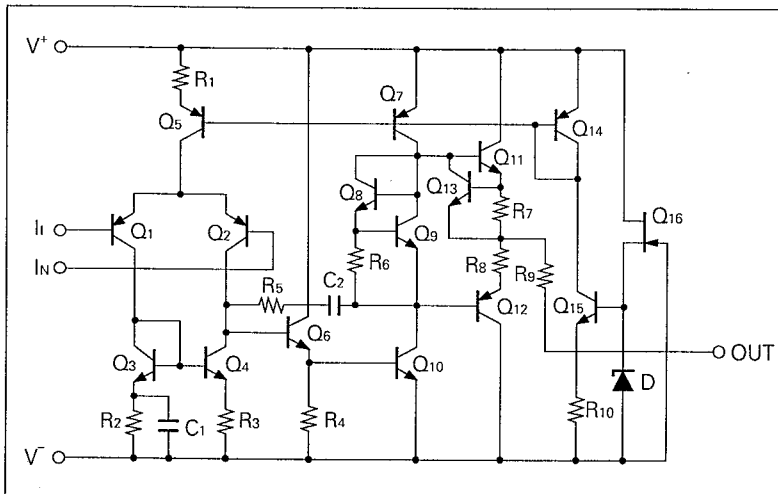
### DESCRIPTION

The  $\mu$ PC4570 is an ultra low-noise, wideband high slew-rate, dual operational amplifier. Input equivalent noise is three times better than the conventional 4558 type op-amps. The gain bandwidth products and the slew-rate are seven times better than 4558. In spite of fast AC performance, the  $\mu$ PC4570 is extremely stable under voltage-follower circuit conditions. Supply current is also improved compared with conventional wideband op-amps. The  $\mu$ PC4570 is an excellent choice for pre-amplifiers and active filters in audio, instrumentation, and communication circuits.

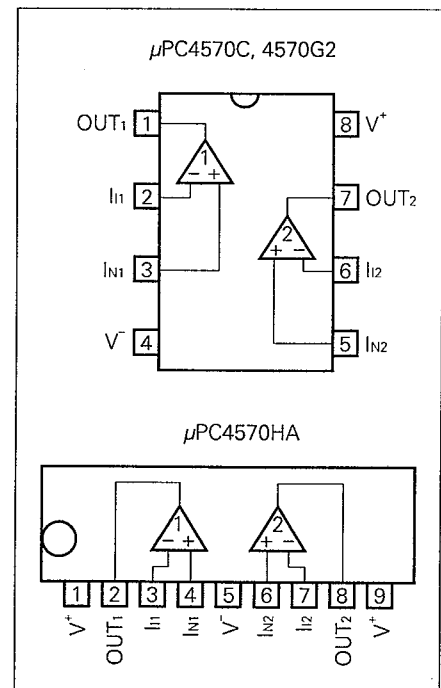
### FEATURES

- Ultra low noise :  $e_n = 4.5 \text{ nV}/\sqrt{\text{Hz}}$
- High slew rate:  $7 \text{ V}/\mu\text{s}$
- High gain bandwidth product:  
GBW = 15 MHz at 100 kHz
- Internal frequency compensation

### EQUIVALENT CIRCUIT (1/2 Circuit)



### CONNECTION DIAGRAM (Top View)



### ORDERING INFORMATION

PART NUMBER	PACKAGE	QUALITY GRADE
$\mu$ PC4570C	8 PIN PLASTIC DIP (300 mil)	Standard
$\mu$ PC4570G2	8 PIN PLASTIC SOP (225 mil)	Standard
$\mu$ PC4570HA	9 PIN SLIM SIP	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

**ABSOLUTE MAXIMUM RATINGS (T<sub>a</sub> = 25 °C)**

PARAMETER		SYMBOL	μPC4570	UNIT
Voltage between V <sup>+</sup> and V <sup>-</sup> (Note 1)		V <sup>+</sup> -V <sup>-</sup>	-0.3 to +36	V
Differential Input Voltage		V <sub>ID</sub>	±30	V
Input Voltage (Note 2)		V <sub>I</sub>	V <sup>-</sup> -0.3 to V <sup>+</sup> +0.3	V
Output Voltage (Note 3)		V <sub>O</sub>	V <sup>-</sup> -0.3 to V <sup>+</sup> +0.3	V
Power Dissipation	C Package (Note 4)	P <sub>T</sub>	350	mW
	G2 Package (Note 5)		440	mW
	HA Package (Note 4)		350	mW
Output Short Circuit Duration (Note 6)			10	sec
Operating Temperature Range		T <sub>opt</sub>	-20 to +80	°C
Storage Temperature Range		T <sub>stg</sub>	-55 to +125	°C

**Note 1.** Reverse connection of supply voltage can cause destruction.

**Note 2.** The input voltage should be allowed to input without damage or destruction. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The normal operation will establish when the both inputs are within the Common Mode Input Voltage Range of electrical characteristics.

**Note 3.** This specification is the voltage which should be allowed to supply to the output terminal from external without damage or destructive. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The output voltage of normal operation will be the Output Voltage Swing of electrical characteristics.

**Note 4.** Thermal derating factor is -5.0 mW / °C when ambient temperature is higher than 55 °C.

**Note 5.** Thermal derating factor is -4.4 mW / °C when ambient temperature is higher than 25 °C.

**Note 6.** Pay careful attention to the total power dissipation not to exceed the absolute maximum ratings, Note 4 and Note 5.

**RECOMMENDED OPERATING CONDITIONS**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V <sup>±</sup>	±4		±16	V
Output Current	I <sub>o</sub>			±10	mA
Source Resistance	R <sub>s</sub>			50	kΩ
Capacitive Load (A <sub>v</sub> = +1)	C <sub>L</sub>			100	pF

**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C, V<sup>±</sup> = ±15 V)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Offset Voltage	V <sub>io</sub>		±0.3	±5	mV	R <sub>s</sub> ≤ 50 Ω
* Input Offset Current (Note7)	I <sub>io</sub>		±10	±100	nA	
* Input Bias Current (Note7)	I <sub>b</sub>		100	400	nA	
Large Signal Voltage Gain	A <sub>v</sub>	30	300		V/mV	R <sub>L</sub> ≥ 2 kΩ, V <sub>o</sub> = ±10 V
Supply Current	I <sub>cc</sub>		5	8	mA	I <sub>o</sub> = 0 A, Both Amplifiers
Common Mode Rejection Ratio	CMR	80	100		dB	
Supply Voltage Rejection Ratio	SVR	80	100		dB	
Output Voltage Swing	V <sub>om</sub>	±12	±13.4		V	R <sub>L</sub> ≥ 10 kΩ
Output Voltage Swing	V <sub>om</sub>	±10	±12.8		V	R <sub>L</sub> ≥ 2 kΩ
Common Mode Input Voltage Range	V <sub>icm</sub>	±12	±14		V	
Slew Rate	SR	5	7		V/μs	R <sub>L</sub> ≥ 2 kΩ
Gain Bandwidth Product	GBW	10	15		MHz	f <sub>o</sub> = kHz
Unity Gain Frequency	f <sub>unity</sub>		7		MHz	open loop
Phase Margin	φ <sub>unity</sub>		50		degree	open loop
Total Harmonic Distortion	THD		0.002		%	V <sub>o</sub> = 3 V <sub>r.m.s.</sub> , f = 20 Hz to 20 kHz (Fig. 1)
* Input Equivalent Noise Voltage	V <sub>n</sub>		0.9		μV <sub>r.m.s.</sub>	RIAA (Fig. 2)
Input Equivalent Noise Voltage	V <sub>n</sub>		0.53	0.65	μV <sub>r.m.s.</sub>	FLAT + JIS A, R <sub>s</sub> = 100 Ω (Fig. 3)
Input Equivalent Noise Voltage Density	e <sub>n</sub>		5.5		nV/√Hz	f <sub>o</sub> = 10 Hz, R <sub>s</sub> = 100 Ω
Input Equivalent Noise Voltage Density	e <sub>n</sub>		4.5		nV/√Hz	f <sub>o</sub> = 1 kHz, R <sub>s</sub> = 100 Ω
Input Equivalent Noise Voltage Density	i <sub>n</sub>		0.7		pA/√Hz	f <sub>o</sub> = 1 kHz
Channel Separation			120		dB	f = 20 Hz to 20 kHz

**Note 7.** Input bias currents flow out from IC. Because each currents are base current of PNP-transistor on input stage.

**Note 8.** For asterisk items, those spec was applied to the production lots mode after Jun. '87 by the effect of input PNP Tr's h<sub>fe</sub> rise. Before spec is following.

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Offset Current (Note7)	I <sub>io</sub>		±10	±200	nA	
Input Bias Current (Note7)	I <sub>b</sub>		500	1000	nA	
Input Equivalent Noise Voltage	V <sub>n</sub>		1.2		μV <sub>r.m.s.</sub>	RIAA (Fig. 2)

MEASUREMENT CIRCUIT

Fig. 1 Total Harmonic Distortion Measurement Circuit

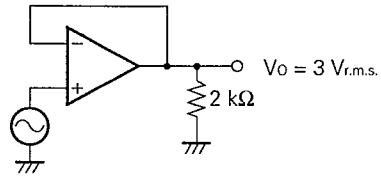


Fig. 2 Noise Measurement Circuit (RIAA)

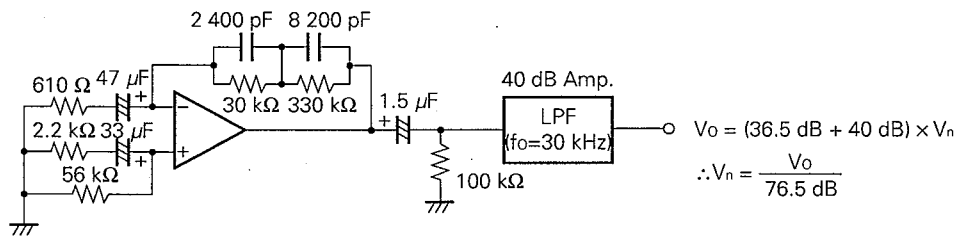
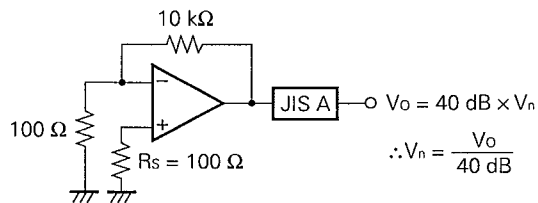
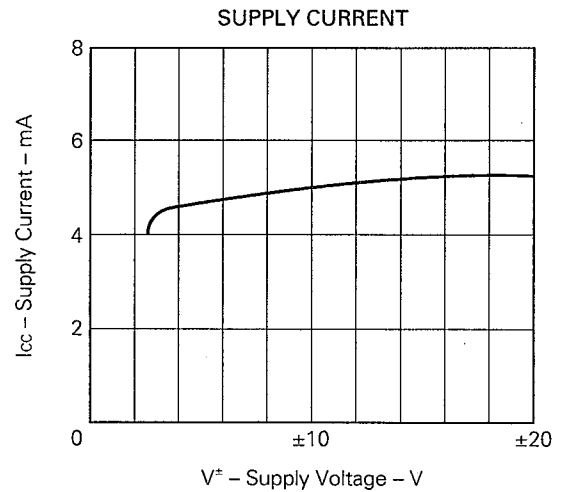
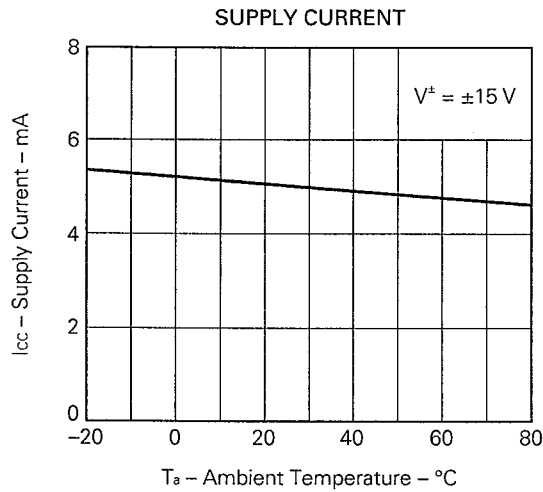
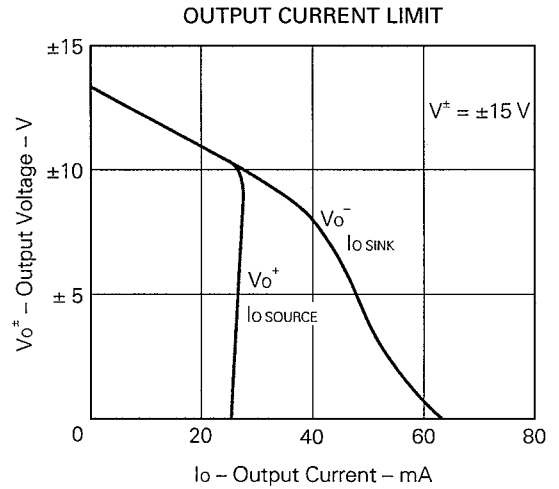
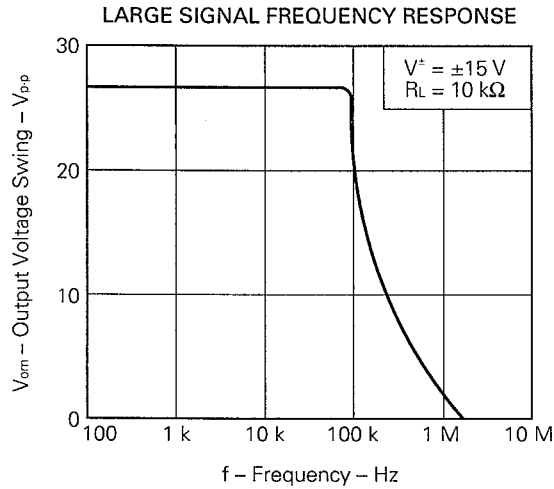
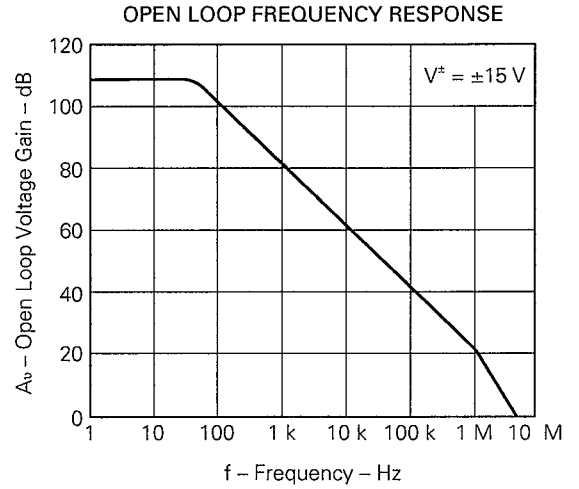
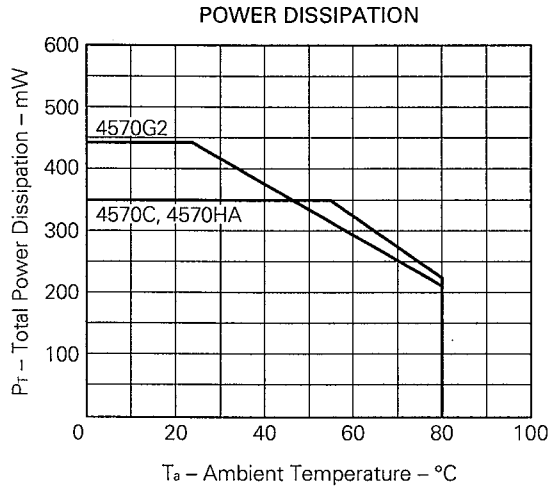
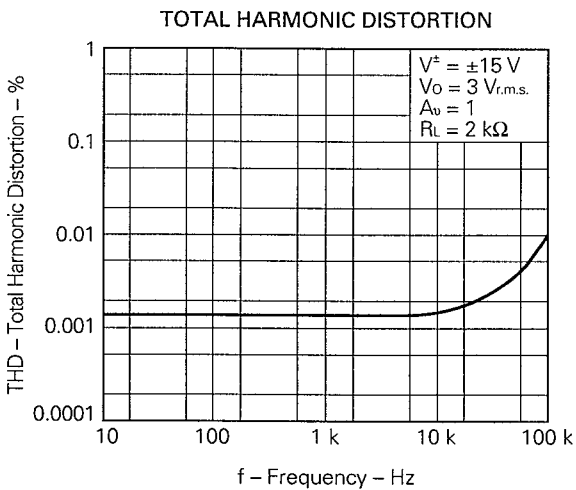
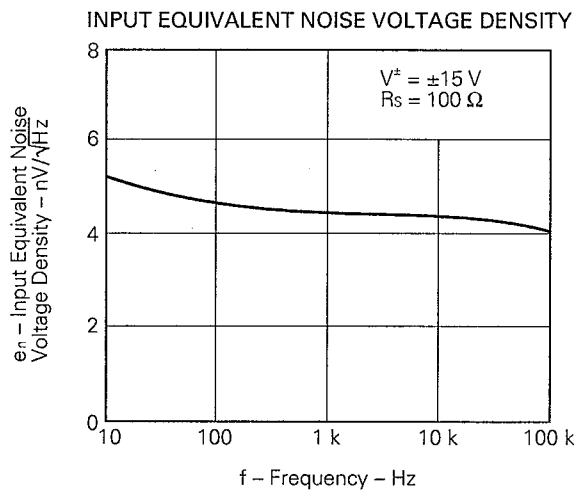
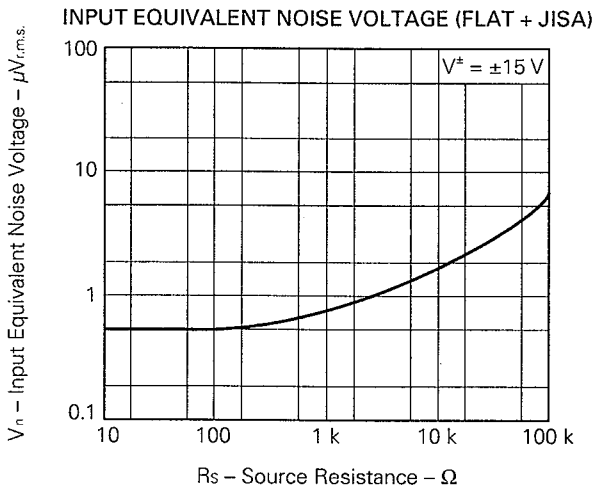
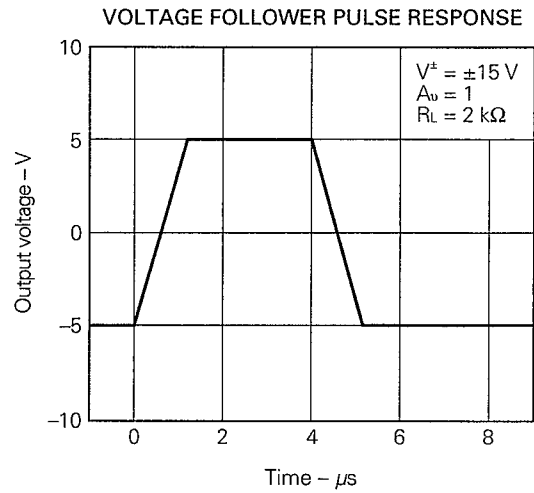
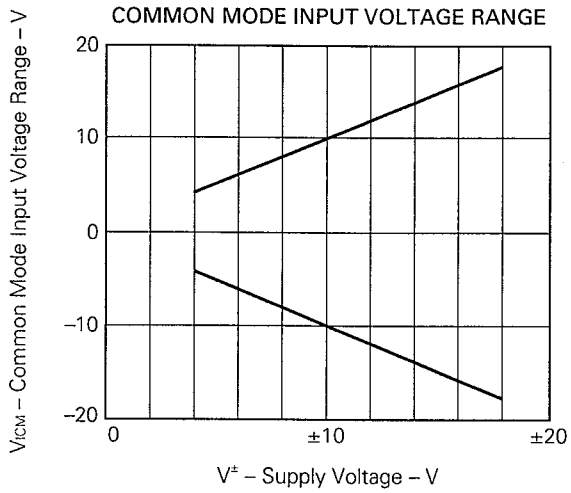


Fig. 3 Noise Measurement Circuit (FLAT + JIS A)

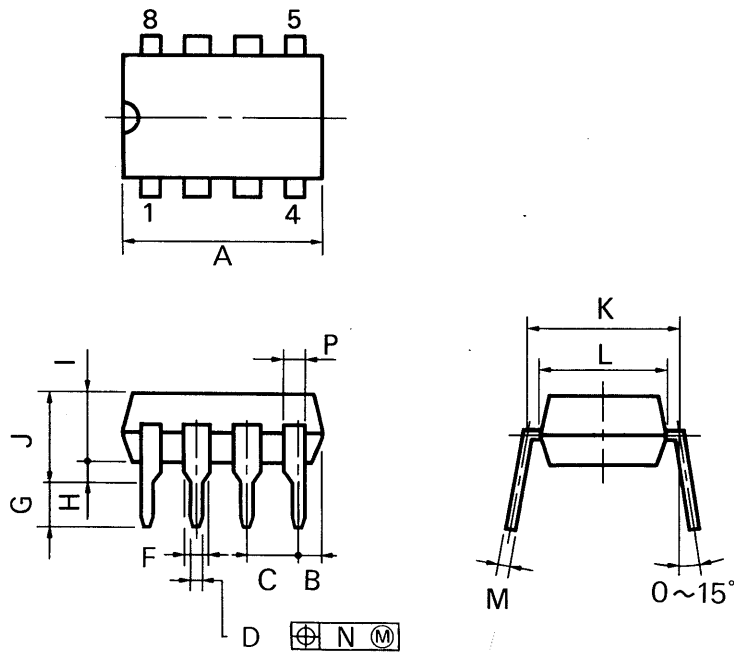


TYPICAL PERFORMANCE CHARACTERISTICS ( $T_a = 25^\circ\text{C}$ , TYP.)





8PIN PLASTIC DIP (300 mil)



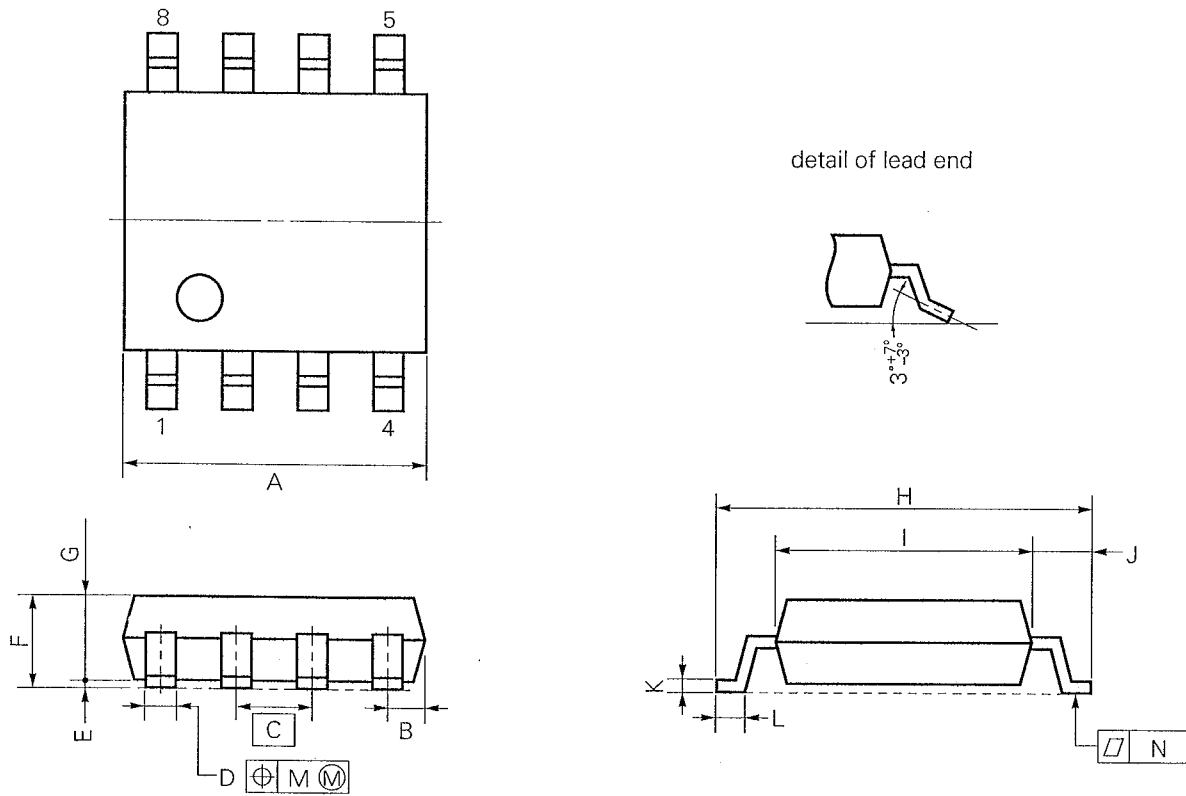
P8C-100-300B,C

NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	10.16 MAX.	0.400 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 <sup>±0.10</sup>	0.020 <sup>+0.004</sup> <sub>-0.005</sub>
F	1.4 MIN.	0.055 MIN.
G	3.2 <sup>±0.3</sup>	0.126 <sup>±0.012</sup>
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	0.25 <sup>+0.10</sup> <sub>-0.05</sub>	0.010 <sup>+0.004</sup> <sub>-0.005</sub>
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.

8 PIN PLASTIC SOP (225 mil)



**NOTE**

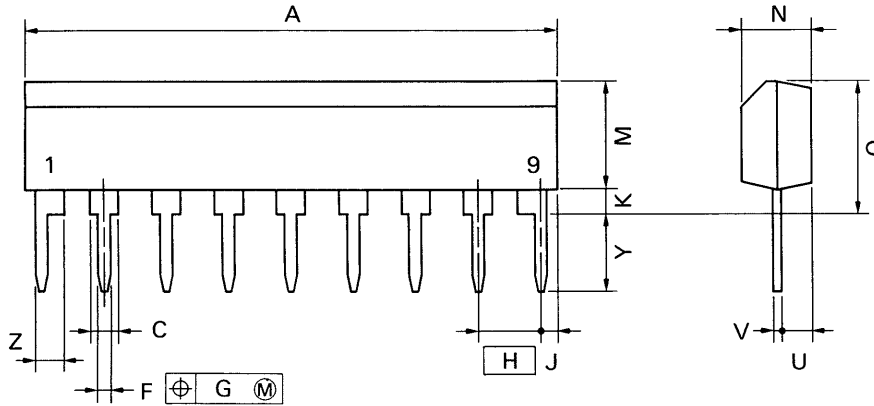
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S8GM-50-225B-2

ITEM	MILLIMETERS	INCHES
A	5.37 MAX.	0.212 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 <sup>+0.10</sup> <sub>-0.05</sub>	0.016 <sup>+0.004</sup> <sub>-0.003</sub>
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071 MAX.
G	1.49	0.059
H	6.5±0.3	0.256±0.012
I	4.4	0.173
J	1.1	0.043
K	0.15 <sup>+0.10</sup> <sub>-0.05</sub>	0.006 <sup>+0.004</sup> <sub>-0.002</sub>
L	0.6±0.2	0.024 <sup>+0.008</sup> <sub>-0.009</sub>
M	0.12	0.005
N	0.15	0.006



9 PIN PLASTIC SLIM SIP



**NOTE**

Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

P9HA-254B

ITEM	MILLIMETERS	INCHES
A	22.86 MAX.	0.9 MAX.
C	1.1 MIN.	0.043 MIN.
F	0.5 <sup>±0.1</sup>	0.02 <sup>±0.008</sup>
G	0.25	0.01
H	2.54	0.1
J	1.27 MAX.	0.05 MAX.
K	0.51 MIN.	0.02 MIN.
M	5.08 MAX.	0.2 MAX.
N	2.8 <sup>±0.2</sup>	0.11 <sup>±0.008</sup>
Q	5.75 MAX.	0.227 MAX.
U	1.5 MAX.	0.059 MAX.
V	0.25 <sup>±0.010</sup>	0.01 <sup>±0.003</sup>
Y	3.2 <sup>±0.5</sup>	0.126 <sup>±0.02</sup>
Z	1.1 MIN.	0.043 MIN.

**RECOMMENDED SOLDERING CONDITIONS**

The following conditions (see table below) must be met when soldering this product.  
Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

**TYPES OF SURFACE MOUNT DEVICE**

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

[μPC4570G2]

Soldering method	Soldering conditions	Recommended condition symbol
Infrared ray reflow	Peak package's surface temperature: 230 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 1, Exposure limit*: None	IR30-00-1
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 1, Exposure limit*: None	VP15-00-1
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below Number of flow process: 1, Exposure limit*: None	WS15-00-1
Partial heating method	Terminal temperature: 300 °C or below, Flow time: 10 seconds or below, Exposure limit*: None	

\*: Exposure limit before soldering after dry-pack package is opened.  
Storage conditions: 25 °C and relative humidity at 65 % or less.

**Note:** Do not apply more than a single process at once, except for "Partial heating method."

**TYPES OF THROUGH HOLE DEVICE**

[μPC4570C, μPC4570HA]

Soldering method	Soldering conditions	Recommended condition symbol
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below	

[MEMO]

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Application examples recommended by NEC Corporation.

Standard: Computer, Office equipment, Communication equipment, Test and Measurement equipment, Machine tools, Industrial robots, Audio and Visual equipment, Other consumer products, etc.

Special: Automotive and Transportation equipment, Traffic control systems, Antidisaster systems, Anticrime systems, etc.

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